Performance Enhancement of Electrically Doped Tunnel Field Effect Transistor by Incorporating SiGe Material in the Source

Submitted in partial fulfillment of the requirements for the degree of

Master of Technology in VLSI Design

by

Arun Kumar Sharma

(Roll no: 2016PEV5093)

Under the guidance of

Dr. Chitrakant Sahu

Assistant Professor

Electronics and Communication Engineering

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY,

JAIPUR 302017

Aug, 2019

APPROVAL SHEET

This thesis entitled **"Performance Enhancement of Electrically Doped Tunnel Field Effect Transistor by Incorporating SiGe Material in the Source"** submitted by **Mr. Arun Kumar Sharma (2016PEV5093)** is approved for partial fulfillment of the requirements for the degree of ***Master of Technology in Electronics and Communication Engineering.***

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This is to certify that the thesis entitled, **"Performance Enhancement of Electrically Doped Tunnel Field Effect Transistor by Incorporating SiGe Material in the Source"** submitted by **Arun Kumar Sharma** (**2016PEV5093**) is the work completed under my supervision and guidance, hence approved for submission in partial fulfillment for the award of degree of Master Of Technology in **VLSI DESIGN** to the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur

To the best of my knowledge, the matter embodied in the thesis has not been submitted elsewhere to any other university /institute for the award of any other degree.

Place: Jaipur

Date:

Dr. Chitrakant Sahu
Assistant Professor
Deptt. of E.C.E
MNIT, Jaipur

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(Arun Kumar Sharma)

ABBREVIATIONS

BTBT	Band-to-Band Tunneling
CB	Conduction Band
CG	Control-Gate
D	Drain
JLT	Junctionless Transistor
MOSFET	Metal-Oxide-Field Effect Transistor
PG-1	Polarity-Gate-1
PG-2	Polarity-Gate-2
PVT	Process-Voltage-Temperature
RDF	Random Dopant Fluctuation
S	Source
SCE	Short Channel Effect
SS	Subthreshold Swing
TFET	Tunnel Field Effect Transistor
VB	Valence Band
DIBL	Drain Induced Barrier Lowering

LIST OF SYMBOLS

V_{TH}	Threshold voltage
V_{DD}	Supply voltage
I_{ON}	ON-state current
I_{OFF}	OFF-state current
C_G	Gate capacitance
k	Boltzmann constant
m	Body coefficient
C_{DM}	Bulk depletion capacitance
C_{OX}	Oxide capacitance
I_{DS}	Drain to source current
V_{GS}	Gate to source voltage
I_{leak}	Leakage current
T_{SI}	Thickness of silicon flim
T_{OX}	Thickness of oxide flim
L_{CG}	Control Gate length
$S_{GAP,S}$	Source side spacer thickness
$S_{GAP,D}$	Drain side spacer thickness
V_{CG}	Control gate voltage
V_{PG-1}	Polarity gate-1 voltage

V_{PG-2} Polarity gate-2 voltage

f_T Cut-off frequency

f_{max} Maximum frequency of oscillation

C_{gd} Gate to drain Capacitance

c_{gs} Gate to source Capacitance

g_m Transconductance

g_{ds} Output Transconductance

ABSTRACT

Nowaday's the system on a chip (SoC) products are designed to broaden a multitudinous range of functionality on a single die like digital, analog and mixed-signal characteristic, and so forth. Transistor density in SoC is increasing rapidly to achieve limitless functional capability on a single die. Therefore, the semiconductor companies are continuously facing the challenge of transistor scaling to increment in the packaging density and integration density. CMOS scaling technology emerged as very essential for nano and microelectronic devices. This results in an enhancement in static power consumption, reduction gate control ability, and increase in SCEs. Conventional MOSFETs are not suitable nano and micro-electronics region. Therefore, non-conventional devices like as Tunnel Field Effect Transistor, JL-Field Effect Transistor, Schottky Field Effect Transistor, and variants of these devices are developed to achieve the current requirements of ITRS. Tunnel FETs are getting wide attention due to its high I_{on}/I_{off} ratio, scalable SS, and very low power dissipation. This thesis reports a new design of electrically doped Tunnel FET (ED-TFET) by using $Si_{1-x}Ge_x$ (x= .5) in the source region. Recently, Si-based ED-TFET with both charge plasma and polarity control concept have been explored. Si-based ED-TFET shows excellent electro-static channel control with low thermal budget and ease of processing. The proposed device uses the electrically doped source & drain regions, which allows dynamic configuration. The 2-D simulations have been carried out for showing the promising switching behavior of the device. The proposed changes in our device are helpful to get steeper band tunneling at the source/channel side. This provides the maximum rate of generation of tunneling charge carriers and it resolves the issues off low ON-state current. Hence, On current is increased by one order of magnitude as compared to the Si-Based ED-TFET. In SiGe-Based device RF performances are improved because gate electrode is underlapped. In the proposed device, Transconductance is also increased approximately one order of magnitude, which further increases cut off frequency (f_T) as well as maximum frequency of oscillation f_{max}. Moreover, ambipolar effect is suppressed in proposed device because of lightly doped drain.

TABLE OF CONTENTS

	Approval	I
	Certificate	II
	Acknowledgements	III
	Abbreviations	IV
	List of Symbols	V
	Abstract	VI
	List of figures	XI
	List of Tables	XIII
Chapter-1	Introduction	1
1.1	Introduction	1
1.1.1	Scaling of Threshold Voltage	2
1.1.2	Scaling Requirement for Slow Supply Voltage (V_{DD})	3
1.2	Probable method to resolve the Power Consumption issues	6
1.3	Introduction of the Tunnel FET	7
1.3.1	TFET structure and working	7
1.3.2	The potential merits of TFETs over conventional MOSFETs	8
1.4	Thesis Organization	8
Chapter-2	Proposed SiGe-based ED-Tunnel FET	10
2.1	Introduction	11
2.2	Device Structure and Specification Parameters	11
2.2.1	Device Structure	11
2.2.2	Simulation Specification and Model	13

2.3 Simulation output & Discussion 14

2.3.1 Carrier Concentration and Energy Band Diagram 14

2.3.2 Transfer Characteristics with different Ge Compositions 14

2.3.3 Suppression of ambipolar effect 16

2.4 Summary 17

Chapter-3 Dc Characterstics and Performance Analysis of Proposed ED-TFET 18

3.1 Introduction 18

3.2 Device Structure and specification Parameters 18

3.2.1 Device Structure 18

3.2.2 Simulation Specification and Models 19

3.3 Simulated output and Discussion 19

3.3.1 Transfer Characteristics Comparison of Conventional, ED-TFET and SiGe-Based ED-TFET 19

3.3.2 Output Characteristics for traditional & SiGe-Based TFET 20

3.3.3 Effect of Supply Voltage and Polarity gate Bias Scaling on Proposed SiGe-Based TFET 21

3.4 Summary 24

Chapter-4 Analog and RF Performance Analysis 25

4.1 Introduction 26

4.2 Device structure and Simulation specification 26

4.2.1 Device Structure 26

4.2.2 Simulation Specification 26

4.3 Simulation Output & Discussion 26

4.3.1 Analysis of Transconductance (g_m) and Output Transconductance (g_{ds}) 26

4.3.2 Comparative Analysis of gate to drain capacitance and gate to source capacitance 28

4.3.3 Variation in f_T and f_{max} 28

4.4 Summary 32

Chapter-5 Conclusion and Future Work 33

5.1 Conclusion 33

5.2 Future Work 33

References 35

List of Figures

1.1	Scaling Curve of V_{DD} & V_{th} v/s Technology Generations	2
1.2	Thermionic emission mechanism where carriers travel from source to drain over the potential barrier	3
1.3	I_{DS}-V_{GS} graph of MOSFET	4
1.4	Flow of dynamic and static CMOS power	4
1.5	Processor chip power trend, with increment in heat sink size.	6
1.6	TFET , as n-i-p diode	7
1.7	TFET energy level diagram diagram of (a) in OFF-state (b) in ON-state for n-type Tunnel FET, & (c) ON-state for p-type TFET	7
2.1	Cross-sectional view of conventional TFET	11
2.2	Cross-sectional view of ED- TFET	12
2.3	Cross-sectional view of proposed SiGe-based ED- TFET	12
2.4	E (electron) & h (hole) concentration of SiGe-Based n-type TFET	15
2.5	Energy Band Diagram of SiGe Based n-type TFET	15
2.6	Transfer Characteristics curve of SiGe-based n-type TFET At variable SiGecomposition	16
2.7	In ambipolar state Energy Band Curve of n-type TFET	16
3.1	I_D $-V_{GS}$ curve of conventional and Si and SiGe-based n-type TFET at V_{DS} = 1.0 V	19
3.2	I_D $-$ V_{GS} curve of conventional and SiGe -Based p-type TFET for V_{DS} = 1.0 V	20
3.3	Output characteristics of conventional TFET for different Control-Gate (CG) voltages.	21
3.4	Output characteristics of n-type SiGe-Based TFET for different Control-Gate (CG) voltages.	21
3.5	I_D– V_{CG} characteristics of n-type ED-TFET at different V_{DS}.	22
3.6	Effect of PG bias on transfer characteristics	23

3.7 Effect of PG bias on energy band diagram 23
4.1 Variation in Transconductance (g_m) 27
4.2 Variation in output Transconductance (g_{ds}) 27
4.3 Variance in C_{gd} with V_{GS} in n-type TFET 29
4.4 Variance in C_{gs} with V_{GS} in n-type TFET 30
4.5 Variation In Total Capacitance (c_{total}) in n-type TFETs 30
4.6 Variation in f_T With V_{GS} in n-type TFET 31
4.7 Variation in f_{max} V_{GS} in n-type TFET 31

List of Tables

2.1 Biasing condition to PG-1 and PG-2 for configure the ED-TFET and proposed ED-TFET 14

2.2 Simulation specification for Si & SiGe-based ED-TFETs. 14

4.1 Indicates the summarized output result for comparative analysis. 33

Chapter 1

Introduction

1.1 Introduction

According to Dennard's scaling law, constant electric field must be maintained inside the device and doping of source (S) & drain (D) region must be increased by factor of *K* [1]. In addition, other dimensions and voltage also scaled by 1/k.

As technology is shifting towards nanometer region, Tunnel Field-Effect Transistors are getting wide attention as the semiconductor devices. It is necessary to know how Tunnel FETs are beneficial as semiconductor switches; Also, In depth study about the limitations of traditional MOSFETs is needed. Hence, this work begin with the scaling of conventional MOSFET and it's pros and cons.

Dennard's scaling rule did not follow longer for conventional MOSFETs scaling, because threshold voltage never follows Dennard's scaling rule. As we can see in Fig. 1.1, when scale technology went node 1 micrometer to 65-nanometer node, voltage (V_{DD}) reduced to approximate 77% of its initial value while the threshold voltage (V_{th}) decrease approximate half of its initial value. Because of that gate overdrive voltage also reduces downwards [2].

When gate overdrive voltage reduces, we get a reduction in ON-state current as consequence MOSFET performances also decreases such as I_{on}/I_{off} ratio, dynamic speeds (C_gV_{DD}/I_{on}), for more drive voltages there are two methods.

1. Threshold voltage should be scale.
2. Scaling of the slow supply voltage (V_{DD}).

Above mentioned both possible solution and their effects will be discuss in sequence.

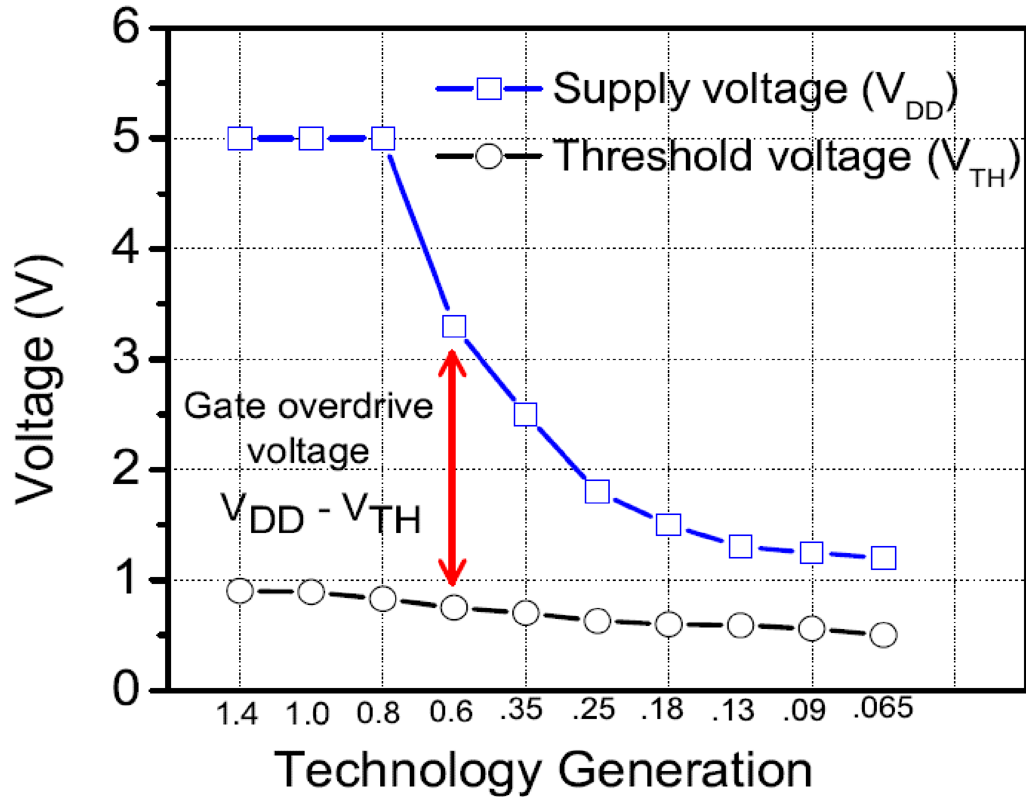

Fig. 1.1: Scaling Curve of V_{DD} & V_{th} v/s Technology Generations [1].

1.1.1 Scaling of threshold voltage

As we know in MOSFET, carrier flows from source to drain. Thermionic emission process causes the movement of carrier from source to drain and help carriers to cross potential barrier. Thermionic emission limits SS by 60mv/dec.

SS is limited to $KT/q_{mV,}$ which is mention in below equation 1.1.

$$SS = \frac{dV_G}{dlogI_D} = \ln(10)\frac{mkT}{q} \qquad 1.1$$

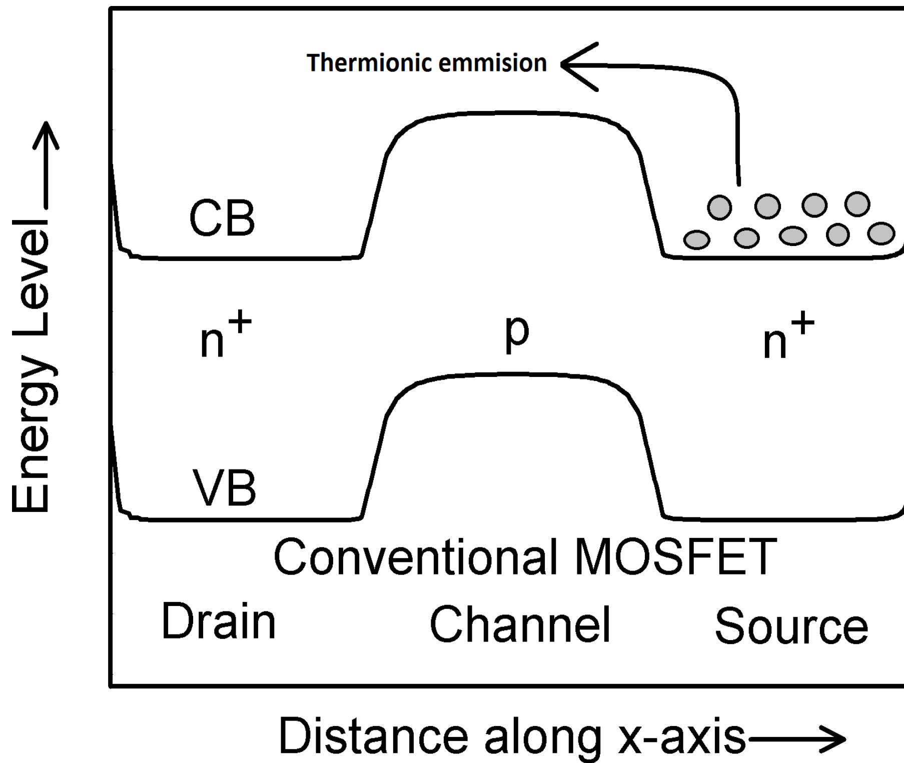

Fig. 1.2: Thermionic emission mechanism where carriers travel from source to drain over the potential barrier. [2]

M = body effect coefficient

T = temperature

K = Boltzmann constant

At room temperature, the thermal constant is 60 mV/dec for MOSFETs [3].

1.1.2 Scaling Requirement for Slow Supply Voltage (V_{DD})

When scale down supply voltage the MOSFET performances will degrade like I_{on}/I_{off} ratio and dynamic speed, so slow scaling of supply voltage is desirable to maintain these performances of MOSFET. Power consumption increases drastically if supply voltage is not scaled down. This is due to direct dependence of power supply (V_{DD}) voltage on both dynamic and static power consumption. MOSFET power is shown in Fig 1.2 showing that static power consumption has become a more significant problem than dynamic power consumption.

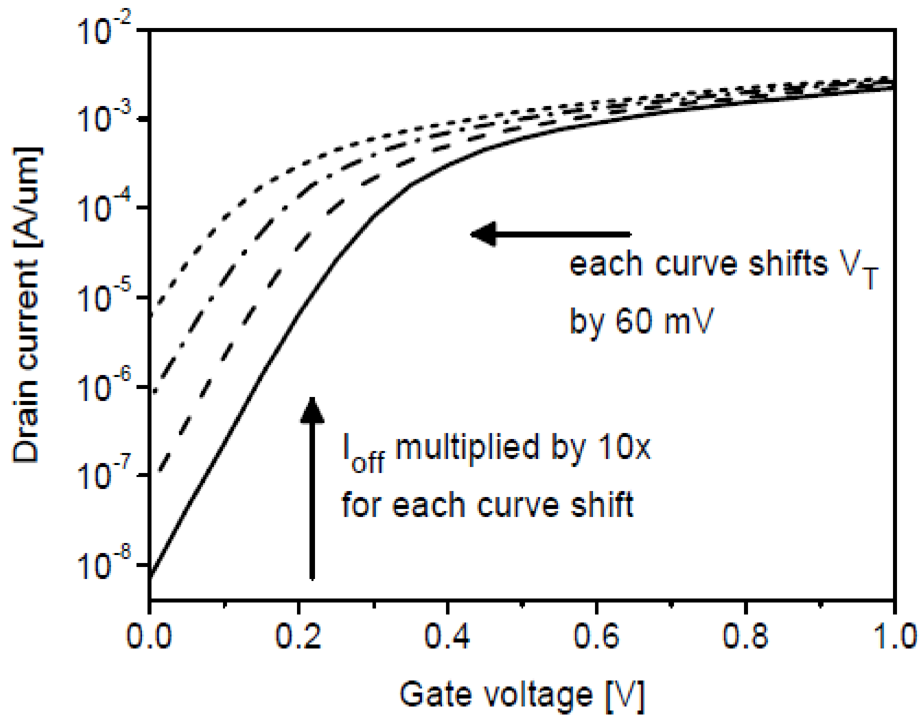

Fig. 1.3: I_{DS}-V_{GS} graph of MOSFET [4]

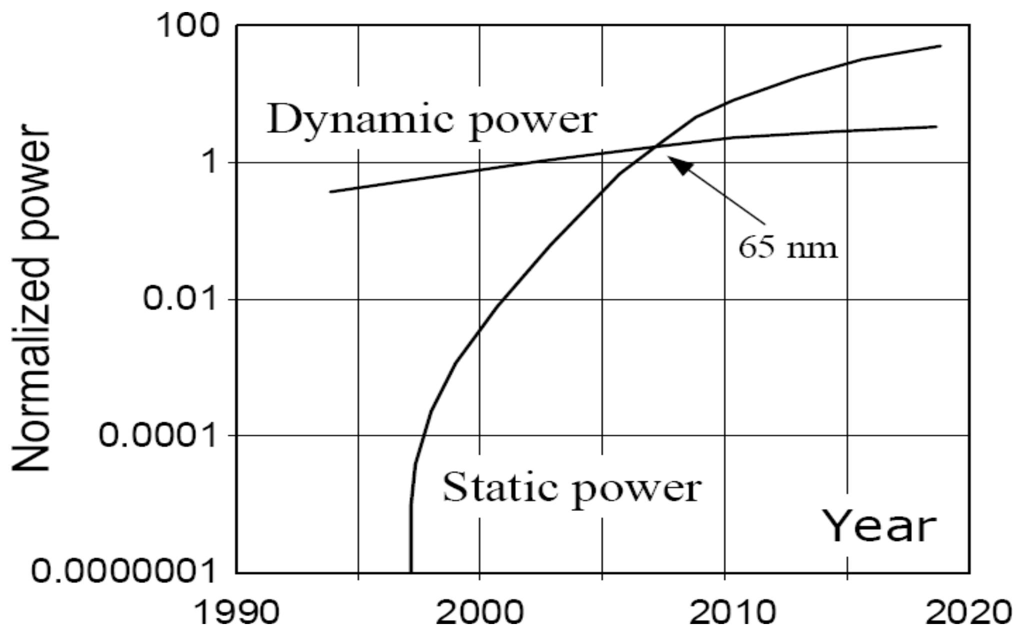

Fig. 1.4: Flow of dynamic and static CMOS power [5]

$$P_{Dynamic} = fC_L V_{DD}^2 \quad (1.2)$$

Where f = frequency

C_L = switched capacitive load

$$P_{Static} = I_{leak} V_{DD} \quad (1.3)$$

I_{leak} = leakage currents in OFF-state condition

Why is power dissipation such a problem? There are some reasons for which circuits should use less power, some of which will be discussed here. First, we can see in a global scale. We use our computers; electronic instrument our electronic gadgets and we want less power consumption for good environment and can say to it is less expensive to use less electricity.

Second, in Fig 1.5, we can see that to cope with increasing power density, the heat sink must grow in volume. This is also has the limit because everybody want small size or same size instrument if the size of our instrument will increase like computer, phone and other electronic instrument that will be inconvenient for everyone.

1.2 Probable Methods for resolving Power Consumption issues

In MOSFET subthreshold swing is limited to 60mv/dec so we required a new current phenomenon where SS can be further reduce. So it is required another current transport mechanism where we can get desirable SS. To change the current transport mechanism, many researcher studied and found that transistor size are becoming less day by day. The distance between different transistor region are reduced like source to drain. In semi-classical current transport mechanism carries have to travel over the potential barrier because the source to drain barrier were so thick. Now the barrier is reduced so carriers will find very thin barriers now electron can travel through thin barriers so research found idea and turn this phenomenon to advantage. According to this electron can tunnel from thin barrier and it is known as band-to-band tunneling. This mechanism showed its suitability for same from last decade. In general this is quantum tunneling mechanism, where electron travels via thin barrier instead of potential barrier. TFETs are based on BTBT process.

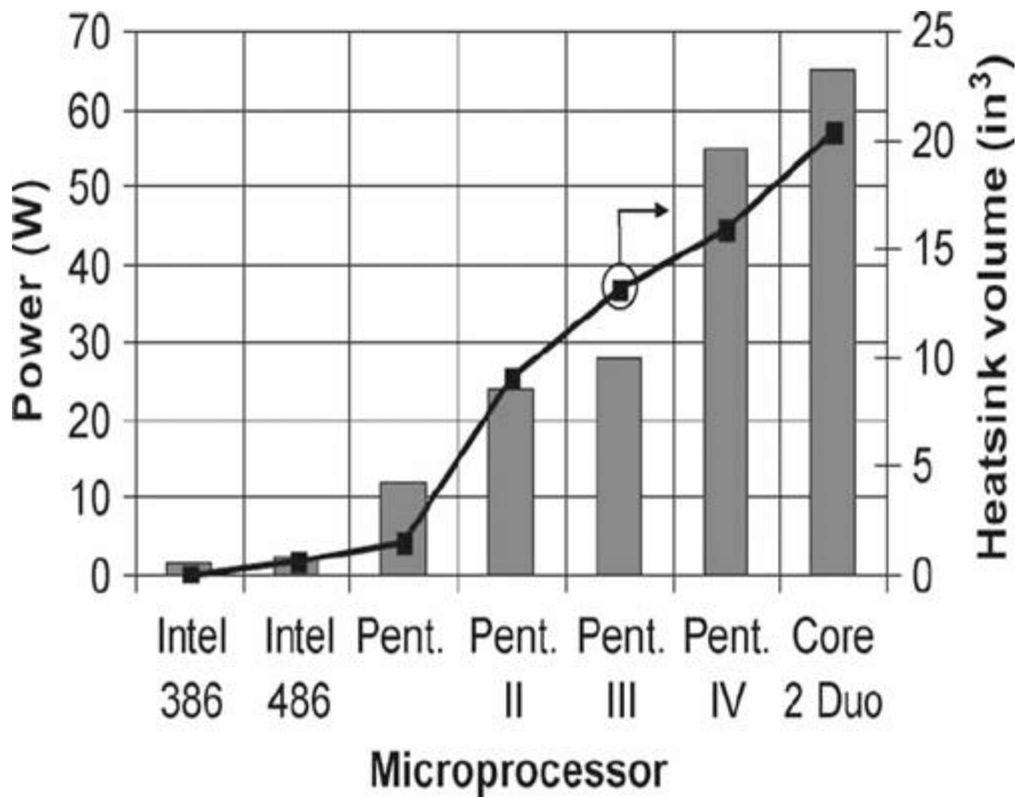

Fig. 1.5: Processor chip power trend, with increment in heat sink size. [6]

1.3 Introduction: The Tunnel FET

TFETs are good substitution of MOSFETs. TFETs are very useful as low power application because in TFETs in ON-state very strong current flow through thin barrier while in OFF-state very low leakage current flow through thick barrier. This OFF-state current is very small than that of conventional MOSFET. So, when the device is off, TFET offers a high barrier for source to drain electron flow. On the other hand when it is on, TFET offers very low potential gradient for source to drain electrons flow. Therefore, very good or scalable subthreshold swing can be achieved in TFET.

1.3.1 TFET structure and working

TFETs are gated P-I-N diodes that means in TFETs three region created. P stands for p-type that region referred to source, I stands for intrinsic that region referred to gate and n (N-type) given to drain region in N-type TFET. Or we can say TFTES are gated P-N diodes. Diode should be reversed biased to make the device on and for making Tunnel FET operation to compatible with MOSFET same voltage applied to the gate the terminal of the device. Reverse biased P-I-N structure results in tunneling. Application of positive voltage to both

drain and gate terminals of NMOS, it starts conduction. The cross-section of P-I-N TFET is illustrated in Fig.1.6.

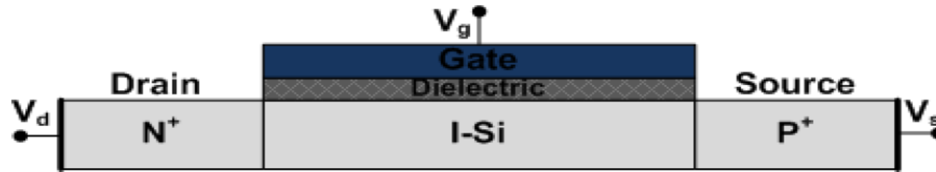

Fig. 1.6: TFET , as n-i-p diode . [7]

In a p-type TFET source and drain are n+ and p+ doped, respectively. All Tunnel FETs reported in this work, have a metal gate with a work function of 4.5eV.

From Fig.1.7 (a),(b) and (c) and Fig 1.6 (a) it is can be said that in OFF-state condition the band diagram are horizontal with the body of TFET only leakage current flow from source to drain which is also very less because TFETs are having less tunneling barrier width in off condition.

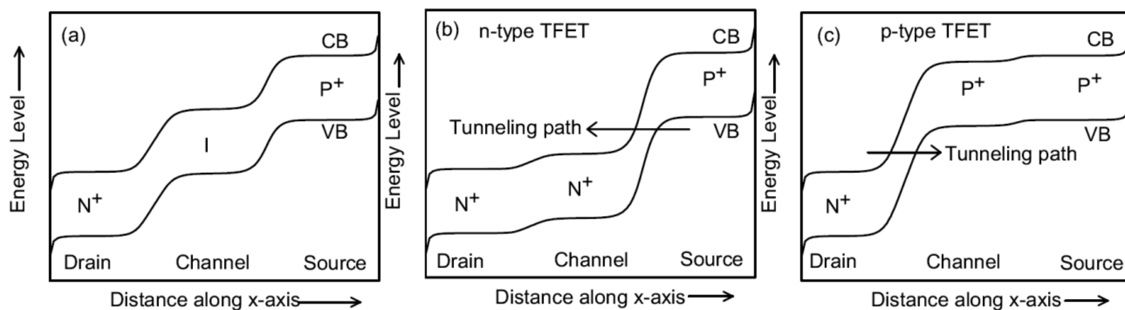

Fig. 1.7: TFET energy level diagram of (a) in OFF-state (b) in ON-state for n-type Tunnel FET, & (c) ON-state for p-type TFET [8]

From Fig 1.7 (b) we can see that in ON-state positive voltage is applied to the gate of TFET. Due to application of positive gate voltage, the intrinsic region conduction band (CB) and valence band (VB) are aligned to that of source region. Hence, carrier tunnels from VB of source region to CB of intrinsic region. This produces band tunneling, due to this tunneling width becomes narrow. Hence, large current flows from the device.

Fig. 1.7 (c) shows the ON-state CB diagram for P-type TFET. For P-type Tunnel FET, application of negative voltage to gate results in misalignment of CB and VB of intrinsic

region to that of source region. Due to this electron tunnel CB of source region to the valence band of the intrinsic region in this way current phenomenon takes place.

1.3.2 The potential merits of TFETs over conventional MOSFETs

1. TFETs having good SS that is scalable.

2. TFET can be used at low supply voltage so can be used as low power devices.

3. TFETs are not suffered from short channel effects.

1.4 Thesis Organization

Chapter 1 Introduction

This chapter briefly states technology trend with scaling. And what is the limitation with conventional MOSFET. And why we need another device. And we discussed about what is limitation with scaling of V_{th} and SS and to overcome with same and brief introduction about TFETS.

Chapter 2 Proposed SiGe-Based ED-TFET

This chapter gives the basics of proposed structure of SiGe-based Tunnel FET. The proposed SiGe-Based Tunnel FET named as Performance Enhancement of Electrically Doped TFET by incorporating SiGe material in source that can be configured into n-type and p-type TFET. Also discussed about electron and hole concentration of proposed device. There is detail about how device become a n-type or P-type by just applying polarity. We also discuss Energy band diagram of the device.

Chapter 3 DC Characteristics and Performance analysis of proposed SiGe-Based ED- TFET

This chapter shows the simulation of DC performance of the Proposed SiGe based new TFET. Also, impact of supply voltage scaling on drain current have been discussed. Furthermore, the impact of polarity gate biasing on drain current and energy band diagram have been discussed.

Chapter 4 Analog and RF Performance analysis

Chapter 4 shows simulation of Proposed TFET for analyzing analog/RF performance. The important analog/RF figures of merits (FOM) cut-off frequency ($f_T = g_m/2\Omega C_T$), source-to-gate capacitance (C_{gs}) and source-to-drain capacitance (C_{gd}) of the device.

Chapter 5: Result and Scope for Future Work

This chapter resolves the dissertation work by showing the conclusion & future work expected. In this chapter given the brief detail about all simulated results. In last section brief about the future works that can be done on the proposed device.

Chapter 2

Proposed SiGe Based ED-Tunnel FET

2.1 Introduction

Presently technology is transferring to sub 20 nano meter gate length regime, CMOS devices are scaled down some as result additional constraints come into picture. The main constraints with traditional MOSFETs are: subthreshold swing (SS) must be constrained to 60 mV/decade at room temperature and supply voltage scaling, that doesn't scale inside the same way as CMOS era scales anticipated by using global generation road maps for semiconductors ITRS [9]. Also, power intake in modern chip area technology has been improved and affects the performance of electronics circuit. Subsequently, broadly, research is focused to the investigation of modern MOSFET architectures. These architecture includes silicon nanowire, JLT, Schottky barrier, and Tunnel FETs. Among all the numerous probable devices, TFETs are fascinating notable interest for their low leakages, low energy intake, and good Subthreshold swing [10,11,12,13,14].

The overall performance metrics, random variability of different technological parameters along with (V_{TH}), I_{ON} /I_{OFF} ratio and high Subthreshold Swing, and other problems with Si-TFET are discussed. For efficient BTBT in TFET, abrupt p-n junction are required. The generation of abrupt junctions results in excessive-temperature which will increase the thermal price range requirements [12]. To report these troubles noted for TFETs and to make it a much less prone to RDF, a new tool has already been explored. This is named as an Electrically Doped Si-based TFET (ED-TFET). The doping can be achieved using polarized gate method.

The ED-TFET, involves the recently introduced doping less JLT concept [15]. Where in lightly doped silicon at some stage in the source, channel and drain region had been employed. In [16], the formation of source, channel, and drain area is carried out by using gate & contacts by metal of different works functions to create carrier concentration but in Electrically Doped -Tunnel FET, the identical metals are used for both polarities. In addition to this gate and carrier concentration in source & drain areas are brought out via polarity biasing concept. Subsequently, a combination of both procedures make ED-TFET less liable to Random dopant Fluctuations, decreases thermal

finances, fabrication complexity & significant decrement in leakage current. This is because it does not require ions implantation & thermal annealing. ON-state current is decreased in Si-based Tunnel FET but other performance parameters of the Si-based ED-Tunnel FET device are similar to TFET. ON-state current of ED-TFET is less than conventional TFET by one order of magnitude. Hence, for increasing the ON-state current of ED-TFET a new device has been reported using $Si_{1-x}Ge_x$ in source region. Where X= 50%, which shows germanium is used 50% and Si is also 50%. The simulation results show increment in ON-state current by one order of magnitude. Also, the reported device maintains the benefits of dynamically configurable PVT insensitive ED-TFET device.

2.2 Devices Structure & Specification Parameter

2.2.1 Device Structure

The structural view of conventional TFET, Si-based ED-TFET and the proposed SiGe-based ED-TFET device are shown in Fig. 2.1, 2.2, 2.3, respectively. In proposed design, P^+ and N^+ source and drain regions are created through proper biasing to PG-1 and PG-2 as depicted in Fig. 2.2 like ED-TFET. This leads to dynamic device configuration. While ON-OFF switching of TFET is controlled through Control Gate (CG). Table 2.1 depicts a proper biasing voltage for PG-1and PG-2 for configuring the Si-based and SiGe-Based TFET.

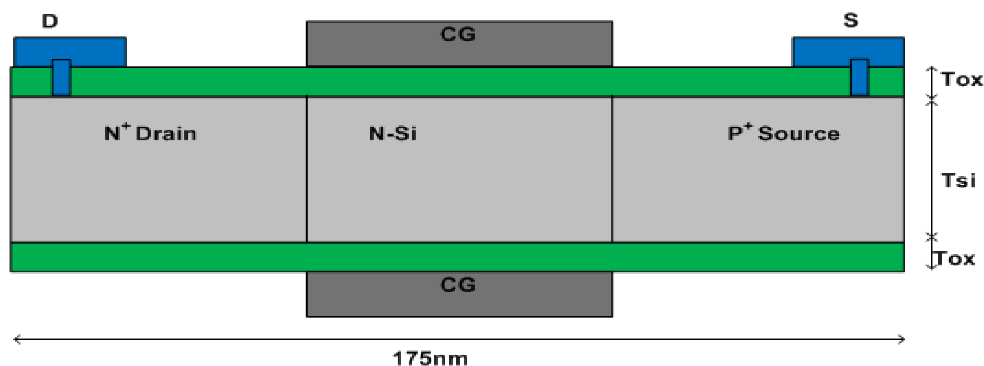

Fig. 2.1: Cross-sectional View of Conventional TFET

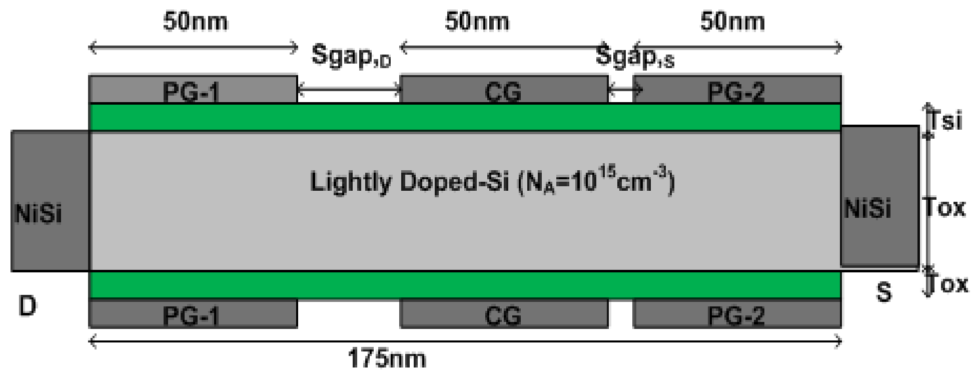

Fig. 2.2: Cross-sectional View of ED-TFET

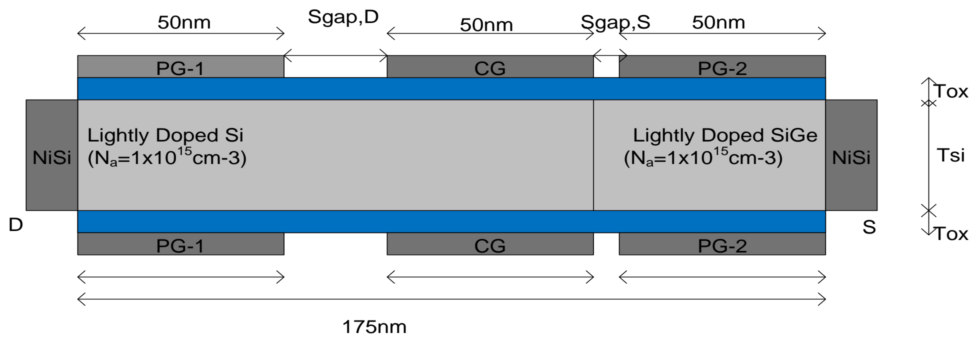

Fig. 2.3: Cross-sectional View of SiGe-Based ED-Tunnel FET

Table 2.3: Biasing condition to Polarity gate -1 and Polarity gate -2 for configure the Si-based and Sige-Based TFETs.

Contact	TFET	
	n-type	p-type
Polarity Gate-1	+1.2 Volt	-1.2 Volt
Polarity Gate-2	-1.2 Volt	+1.2 Volt

2.2.2 Simulation Model & Parameters

Table 2.1: Simulation specification for Si & SiGe based ED-TFETs.

Specification	Value.
Drain Doping (N_D)	5x E18cm^{-3}
Source Doping (N_A)	1 x E20cm^{-3}
Channel doping	1 x E17cm^{-3}
Lightly doped Silicon	1 x E15cm^{-3}
Lightly doped SiGe	1 x E15cm^{-3}
Work function of CG, PG-1,&PG-2	4.5 eV
Silicon film ThicknessT_{SI}	10 nanometer
Effective gate oxide thickness (T_{OX})	0.8 nanometer
L_{CG}, L_{PG-1}, and L_{PG-2}	50 nanometer
Spacer Thickness at drain side ($S_{GAP,D}$)	20 nanometer
Spacer thickness at source side ($S_{GAP,S}$)	5 nanometer

Fig. 2.2 indicates the cross-section of the electrically doped Si-based Tunnel FET. Simulation specifications are taken into consideration as identical to traditional TFET with doping concentration. In Si-based Tunnel FET, P^+ supply and N^+ drain areas are formed by use of the polarity gate concept [17,18]. We have kept spacer thickness between CG and PG-2 5 nm while between CG and PG-1 it is kept 20 nanometer.

Fig. 2.3 shows cross-section of the new Proposed SiGe-based ED-TFET. The simulation parameters are the same as ED-TDET except for that source region. In the source region, lightly doped $Si_{1-x}Ge_x$ (x = .5) is used instead of Si. 2D device simulator, Atlas Silvaco V5.19.20 is used to perform the simulations [19] for simulating both conventional TFET & the SiGe-based proposed ED-TFET.

To achieve tunneling, non-local Band to Band Tunneling model (BTBT) is used [19]. Wentzel Kramer Brillouin approximation, Electron-Hole wave vector is also enabled because SiNi (Silicon Nickel Silicide) contacts are used for drain and source. Hence, UST model is included in the structure. TAT model is also used, and Newton method is included.

2.3 Results and Discussion

2.3.1 Carrier Concentration and Energy Band diagram

Fig 2.4 shows SiGe-based ED-TFET the OFF-state & ON-state carrier concentrations diagram. The concentration of electrons in the intrinsic region is less and almost equal to conventional TFET. Only there is fall down in concentration diagram below source and drain contact because of NiSi contacts. When we applied positive gate voltage V_{CG} = 1.2 V at common gate (CG), the electron concentration becomes almost equal to the conduction region (n^+) concentration, which is 10^{-19} $cm^{-3.}$ Hence, our proposed approach make sure that there is reverse p-n junction where the tunneling of carriers occurs through of p^+ region to CB of intrinsic region.

In addition to analyzing tunneling mechanism in proposed TFET Fig 2.5 shows OFF-state and ON-state energy band diagrams. It is evident that in OFF- state tunneling of carriers is very less from VB of the p^+ region to CB of intrinsic region. This is because of higher energy barrier tunneling width at common gate and PG-2.

When applied biasing voltage at common gate V_{CG} = 1.2 v and at PG-1 = 1.2 V and at PG-2 = 1.2 V CB & VB of intrinsic region get aligned with CB & VB of n^+ region. This phenomenon reduces the barrier tunneling width at p^+ and intrinsic side, which cause carrier flow from source to intrinsic region and can say that device is on and high drive current flow. For both band diagram and carrier concentration diagram in off condition $V_{PG\text{-}1}$ = 1.2 V, and V_{PG-2} = -1.2 V and V_{CG}= 0 V and for ON-state condition (V_{CG}= 1.2 V).

2.3.2 Transfer Characteristics with different Ge Compositions

Fig 2.6 shows the ON-State current and OFF-State current of proposed device when varying the SiGe composition in source region. It shows that the increase of Ge (germanium) composition also increases the ON-State current but also increase the OFF-State current, which is leakage current. This current is not desirable. Hence we find x = 0.5 is a suitable composition where we can get good I_{on} and $I_{off..}$

Fig. 2.7 shows the impact of drain doping which is no doped (lightly doped) concentration on the tunneling barrier. When applied negative gate voltage V_{gs}= -1.0 and V_{ds} = 0.5 V it can be seen that ED-TFET and Proposed SiGe-based TFET have more barrier width as compared traditional TFET which reduce ambipolar current to flow when the gate is at negative bias.

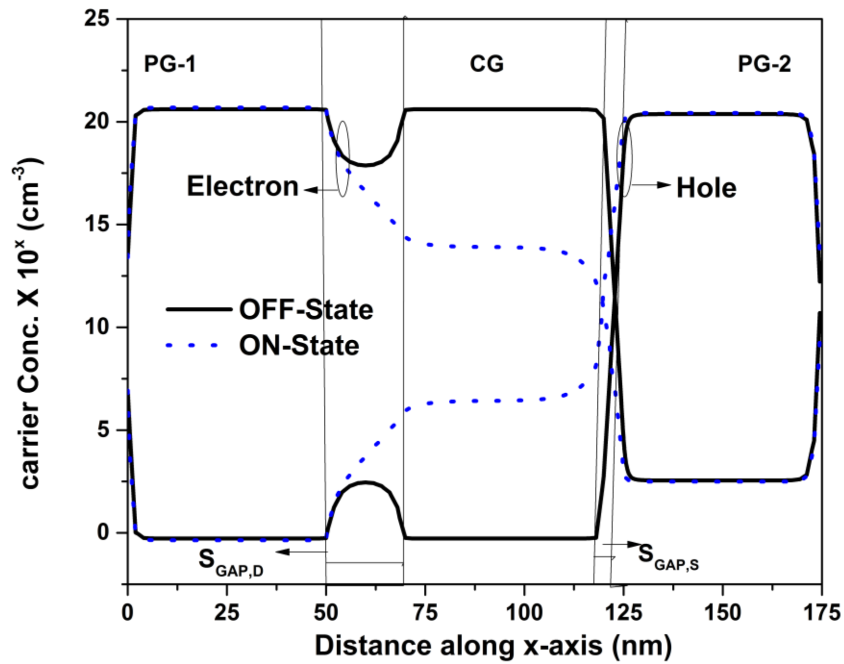

Fig. 2.4: E (electron) & h (hole) concentration of SiGe-based n-type TFET

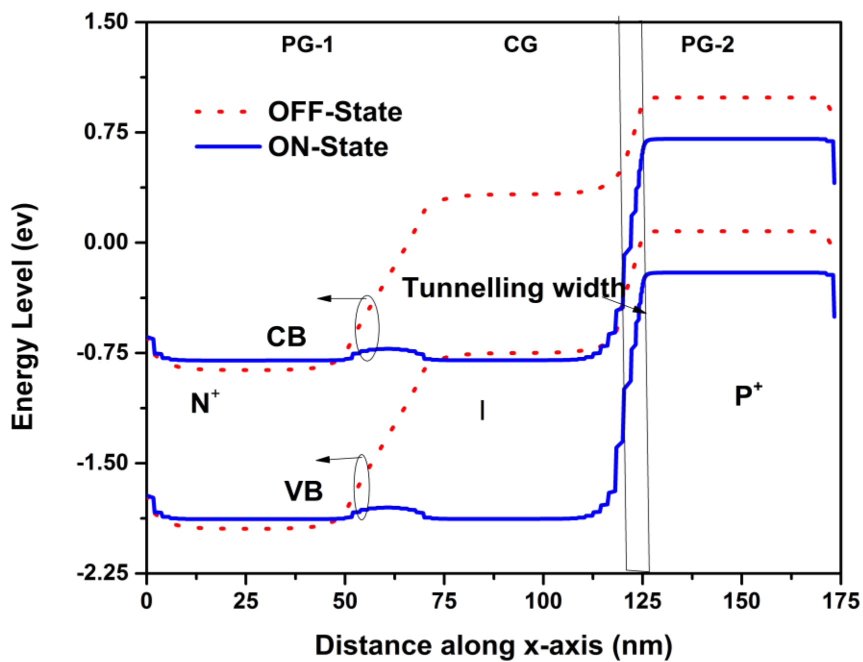

Fig. 2.5: Energy Band Diagram of SiGe-based n-type TFET

2.3.3 Suppression of Ambipolar Effect

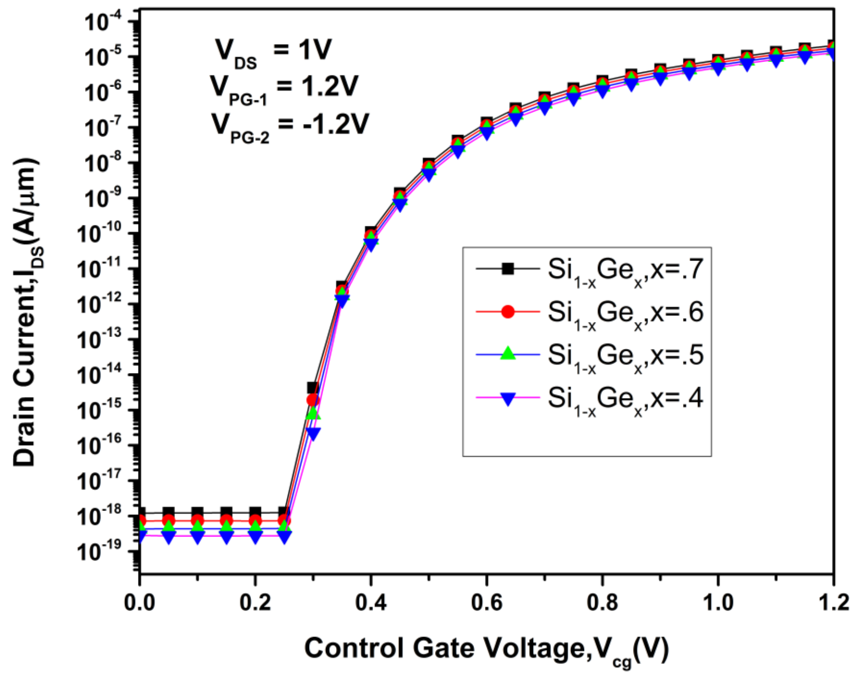

Fig 2.6: Transfer Characteristic curve of SiGe-based n-type TFET at variable SiGe Composition

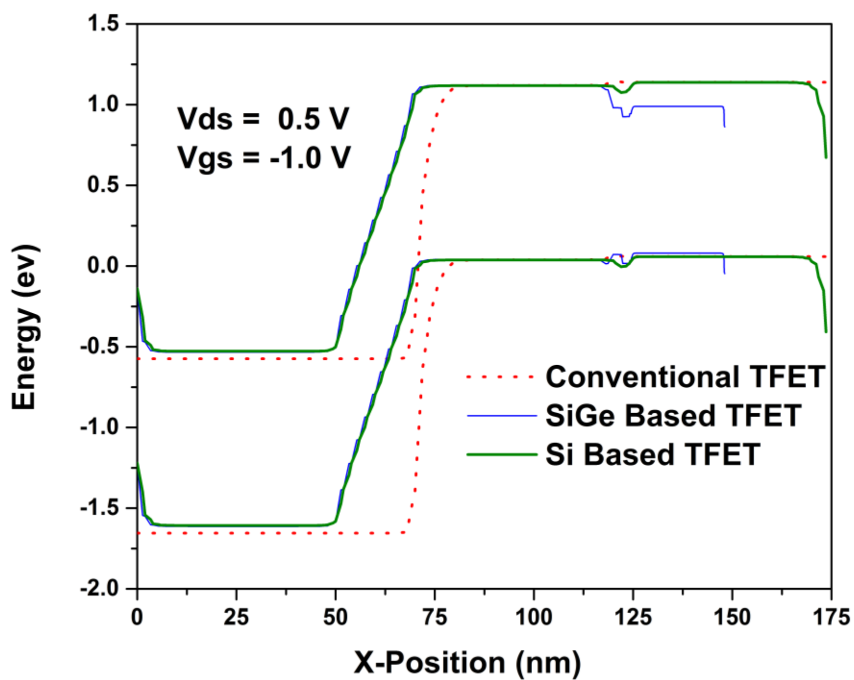

Fig. 2.7: In Ambipolar State Energy Band Curve of TFET

2.4 Summary

In this chapter concept of SiGe-based ED-TFET is affirmed the usage of 2D TCAD simulations. The P^+ is triggered using SiGe composition, and N^+ is induced on lightly doped si film through polarity gate biasing. Conduction mechanism in Proposed SiGe-based TFET is managed using tunneling barrier width that same as conventional TFET. Chapter 2 reports that the lower energy bandgap material used for source region could increase ON-state current therefore proposed consequences may also provide incentives & guidelines for in further studies.

Chapter 3

Dc Characteristics and Performance Analysis of Proposed ED-TFET

3.1 Introduction

Considering potential merits of Electrically Doped -TFET, a new SiGe- Based doping less dynamically configurable Tunnel FET has been introduced. In doping less FET (DL-FET) source /drain areas were made with metal work function engineering, known as charge plasma [20-22]. It shows good improvement over SCEs and RDF. In this device, doping less $Si_{1-x}Ge_x$ is used in source region. Where x = 0.5 while in drain and channel lightly doped Si is used. Creation of drain channel source is accomplished by applying proper biasing at polarity gates (that is electrically-doped) yield P^+ and N^+ source and drain for this reason the Tunnel FET turns into dynamically configurable to exchange among n- and p-type TFETs. These features resolve the requirements of abrupt junction doping, high thermal budget and ion-implantation process for device fabrication. Junction less and doing less mechanisms in the new device yield simpler fabrication method and good electrostatic controls over the channel [23, 24].

ON-state current of Si-based ED-Tunnel FET is one order of magnitude less than traditional TFET. So to increase ON-state current of ED-TFET introduced a new device using Si_{1-x} Ge_x in source region. Where X= 50% which shows germanium is used 50% and Si is also 50%. The simulation results show approximate one order of magnitude increment in ON-state current.

3.2 Devices Structures and specification Parameter

3.2.1 Device Structure

Fig. 2.1, Fig. 2.2 and 2.3 shows cross-section of Traditional Tunnel FET, Si-based ED-Tunnel FET and new proposed SiGe-Based ED-Tunnel FET. In proposed SiGe-based TFET, the $P^{+,}$ and N^+ Source/Drain areas are create via choosing suitable biasing, just like PG-1 & PG-2 as demonstrated in Fig. 2.1(c), like ED-TFET, which permits dynamic configurations of device. While the control-Gate is used to switch the TFET OFF to ON-state & vice versa. Table 2.1 suggests the proper biasing corresponded to the Polarity Gate-1 and the Polarity Gate-2 to configure ED-Tunnel FET.

3.2.2 Simulation specifications and Models

All the specifications and models are described in table 2.2 and section 2.2.2 in chapter 2.

3.3 Simulated output and Discussion

3.3.1 Transfer Characteristics Comparison of Conventional, ED-TFET, and SiGe-based ED-TFET

Fig. 3.1 display the $I_d - V_{GS}$ characteristics of n-type traditional and ED-TFETs and Proposed SiGe-Based ED-TFET, it can been seen that, all TFETs are following almost same trend with slightly different OFF and ON-state currents. The OFF-state current in the new device is more than Si-based TFET (order of 10^{-18} A/μm). Also, the ON-state current is increased by almost one order of magnitude. Hence, there is a trade-off between ON & OFF-state current. This takes place due to lower bandgap material is utilized in the source (50%) similarly, to make p-type device we have reversed the polarity of PG-1, PG-2, and CG and we get symmetric I_d-V_{gs} characteristics as shown in Fig. 3.2.

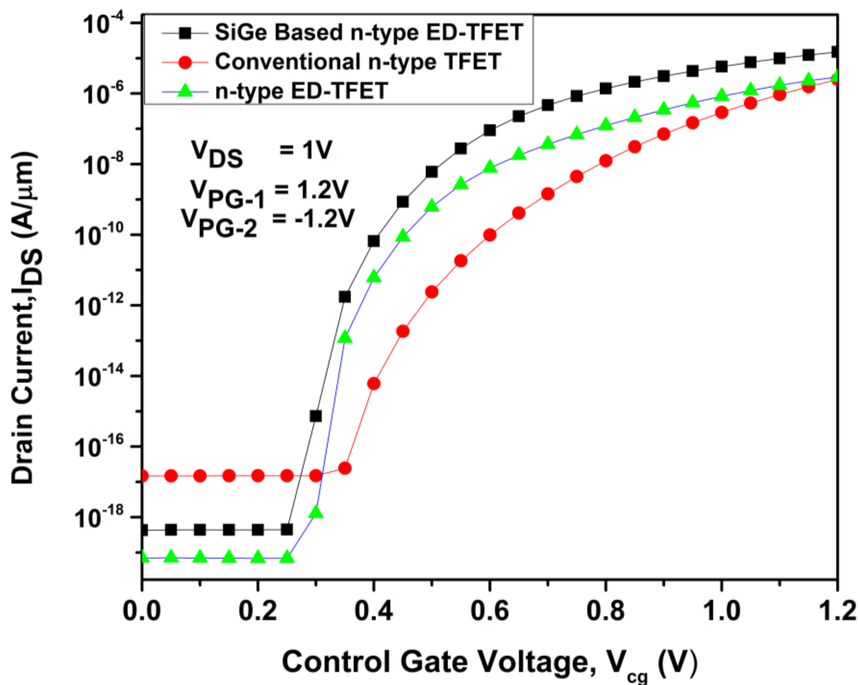

Fig. 3.1: $I_D - V_{GS}$ curve of conventional and Si and SiGe-based n-type TFET at V_{DS} = 1.0 V

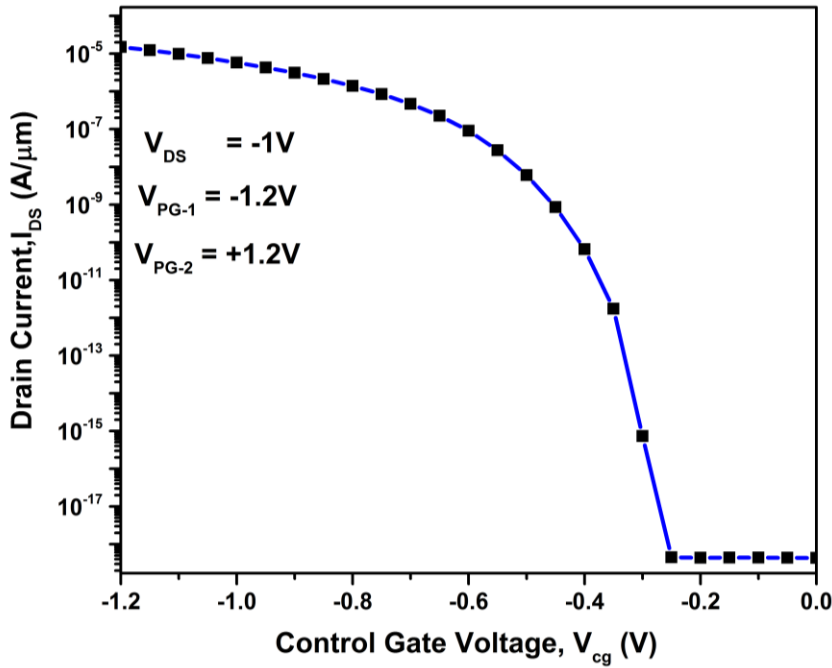

Fig. 3.2: $I_D - V_{GS}$ curve of conventional and SiGe-Based p-type TFET at $V_{DS} = 1.0$

3.3.2 Output Characteristics for Conventional & SiGe-Based TFET

Fig. 3.3 and Fig 3.4 state the output characteristics of conventional TFET and SiGe-based ED-TFET for different common gate voltage. When Tunnel FET enter in triode region more numbers of carriers tunnel and established a exponentional relation with drain current as drain to source voltage is increased. This happens because of drain induced barrier lowering. Good saturation current is achieved because tunneling width is now not dependent too much on drain to source voltage.. Also, to keep up good ON state current & steep SS at room temperature energy barrier width must be less and carrier should tunnel maximum as common gate voltages vary.

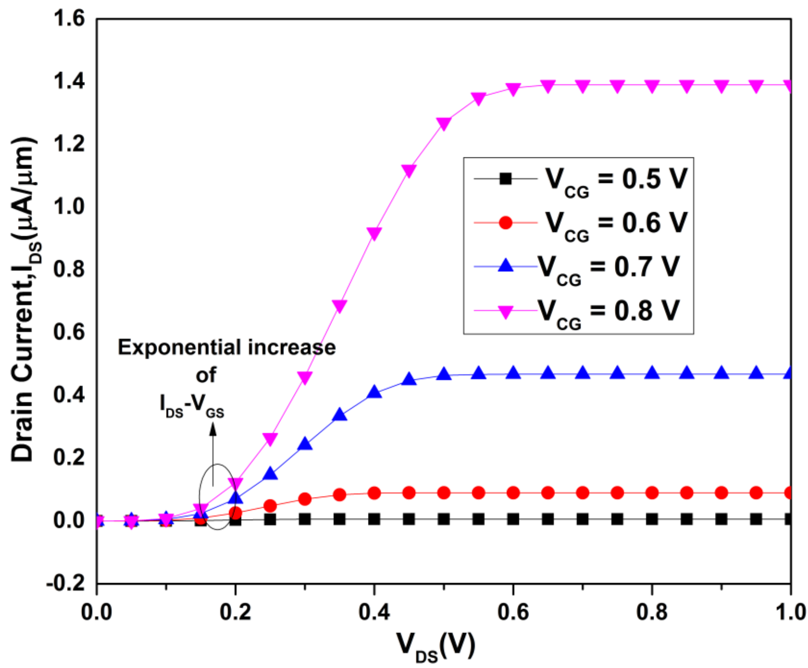

Fig. 3.3: Output characteristics of conventional TFET for different ControlGate (CG) voltages.

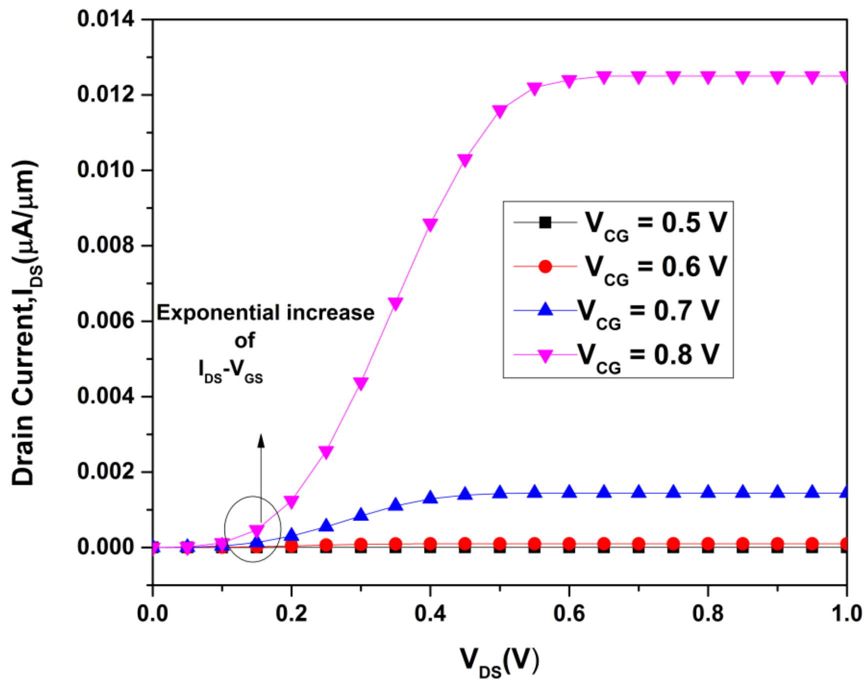

Fig. 3.4: Output characteristics n-type SiGe-based TFET when CG vary.

3.3.3 Effect of Supply Voltage and Polarity gate Biasing Scaling on Proposed SiGe-Based TFET

Fig. 3.5 shows the supply voltage & PG biasing dependence on TFET performances. When Supply voltage (V_{DS}) varies from the 0.5V to 0.3 V, I_{ON} decreases approximate 88%. This current reduces because of reduction in lateral direction electric field. Whereas it has less effect on the leakage current that is almost insignificant.

Fig 3.6 and 3.7 shows the effect of PG biasing on transfer characteristics of OFF-state band diagram of SiGe-Based TFET. It is evident from Figure 3.6 that increase in PG biasing increases the OFF-state current. This is due to less number of accumulation carries, results in decrement in carrier concentration and that lower the bends edges in drain region that permit more carriers to flow from drain to channel side results in higher off state or leakage current.

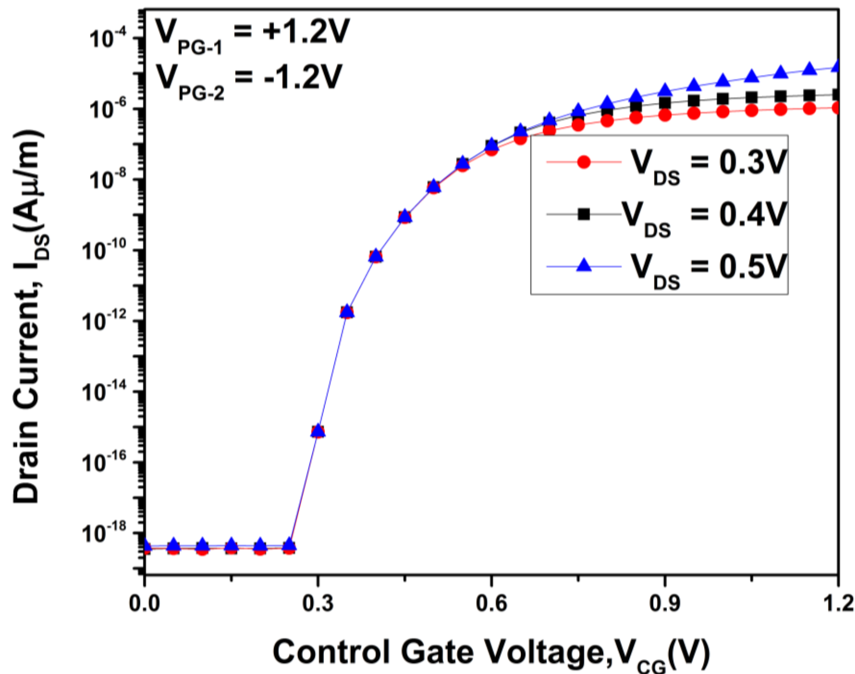

Fig. 3.5: I_D– V_{CG} curve of n-type SiGe-TFET at differents V_{DS}.

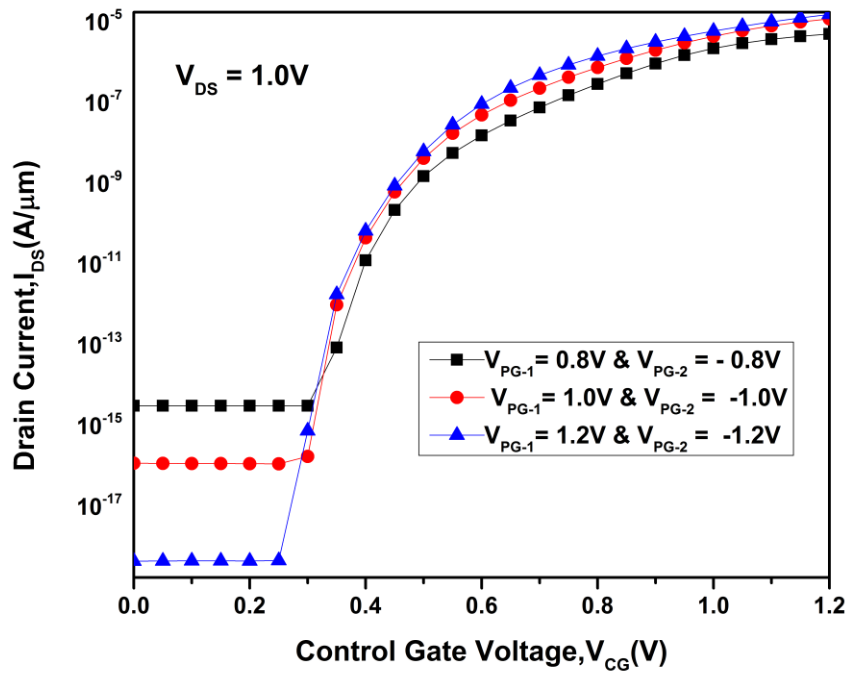

Fig. 3.6: Effect of PG bias on transfer characteristics.

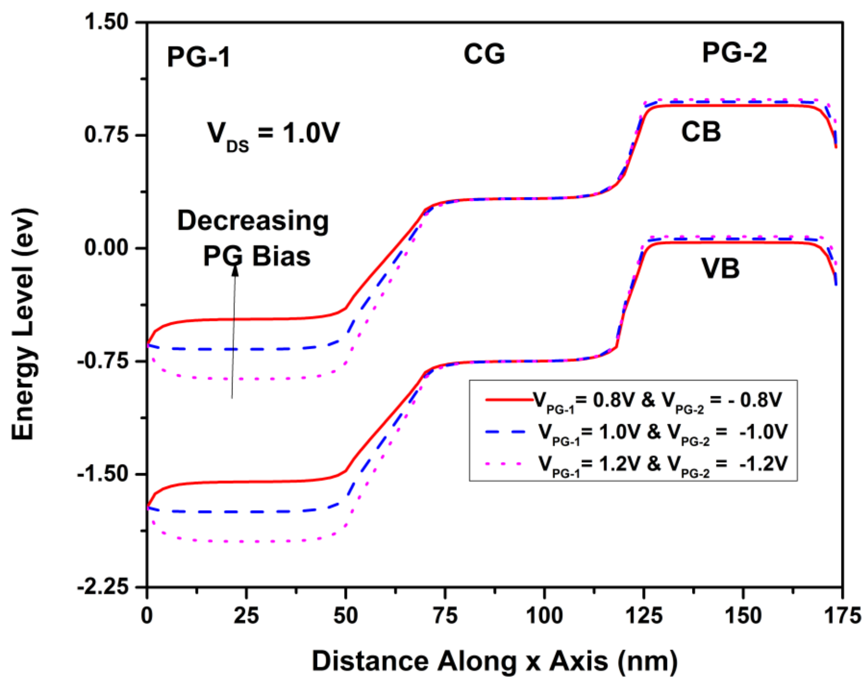

Fig. 3.7: Effect of PG bias on the energy band diagram.

3.4 Summary

SiGe-based TFET has designed and simulated with the help of 2-D TCAD silvaco tool. The result shows that both ON-state and OFF-state currents are increased. Hence, there is a trade-off between ON-state and OFF-state currents. This is acceptable because OFF-state current has less significant effect on device performances. Results, also shows the impact of supply voltage scaling and PG biasing scaling. It can be concluded that the same device can be used either p-type or n-type TFET by just changing the polarity of PG-1 and PG-2. Therefore, proposed results and concept may provide guidelines and initiative for further research.

Chapter 4

Analog and RF Performance Analysis

4.1 Introduction

Power intake in modern chip Engineering has been improved and notably deteriorate the electronics circuit functioning. Subsequently, high-quality attention has been devoted to advanced Metal Oxide Semiconductor FET architectures, which includes silicon nanowire & junction less Schottky barrier, and TFET. Amongst the numerous possible device, TFET is getting notable interest for their low leakage current, low energy intake, and steep Subthreshold swing [25-27]. Other problem with Si-based ED-TFET is overall performance metrics, random variability of different technological parameters along with V_{TH}, I_{ON} /I_{OFF} ratio & high SS, and so on. For efficient BTBT in TFETs, abrupt p-n junctions is required. This sudden junction results in excessive temperature that dramatically will increase the thermal price range requirements. To report these troubles noted for TFETs and to make it a much less prone to RDF, a new tool has been explored already. The device named as an Electrically Doped Si-based TFET. The electrically doping can be achieved using PG concept.

The Si-based Tunnel FET also involves the doping less or JLTconcept that has these days been introduced. In JLTs lightly dope Si at some stage in the source, channel, & drain regions had been employed. Creation of source, channel, and drain area is carried out by using gate & contacts by metal of different works functions to create carrier concentration. But in Electrically Doped -Tunnel FET, identical metals are used for both polarities in addition to gates and carrier concentration in source & drain areas is brought out via applying polarity bias. Subsequently, a combination of both procedures make ED-TFET less liable to Random Dopant Fluctuations, decrease thermal finances, fabrication complexity & significant decrement in leakage current. Ions implantation & thermal annealing are not required; hence it is possible.

In addition to have the above mentioned benefit and to overcome mentione above drawbacks, a new device is proposed named as Performance Enhancement of Electrically Doped Tunnel Field Effect Transistor by incorporating SiGe material in the source. In this chapter, the RF performance of proposed SiGe-Based Electrically Doped Tunnel Field Effect

Transistor has been analyzed. The comparative analysis of transconductance (g_m), output transconductance (g_{ds}), the gate to drain capacitances (C_{gd}) the gate to source capacitances (C_{gs}), cut off frequency (f_T) and maximum operating frequency (f_{max}) have been done. Figure of merit have been compared with conventional TFETs, Electrically Doped TFETs and proposed SiGe-Based Electrically Doped TFETs.

4.2 Devices structure and Simulation specification and models

4.2.1 Device Structure

The device structures are the same as to mention in chapter 2. Which are shown in Fig. 2.1, 2.2 and 2.3

4.2.2 Simulation Specification

The device specification and models are the same as mentioned in chapter 2 because structure of device is same that is described in section 2.2 and in table 2.2.

4.3 Simulation outputs & Discussion

4.3.1 Analysis of Transconductance (g_m) & Output Transconductance (g_{ds})

Fig 4.1 and 4.2 shows the transconductance (g_m) and output transconductance (g_{ds}). Change in the drain current with respect to the gate to source voltage is known as transconductance or in other words, we can say that capacity of the device to change input voltage in to output current as mention in below expression:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \qquad (4.1)$$

Electrostatic doping PG-1 in source region provides higher transconductance. In the case of Si-based Tunnel Field Effect Transistor and SiGe-Based TFET possess higher transconductance in comparison with Conventional TFET.

Consequently, SiGe-based Proposed Tunnel FET and ED-TFET has higher sensitivity for converting gate voltage into drain current. Convert of the drain to source voltage (V_{ds}) in to drain current (I_{ds}) is known as output transconductance (g_{ds}) or in other words, g_{ds} inverse of output resistance. g_{ds} is higher in the case of our proposed device.

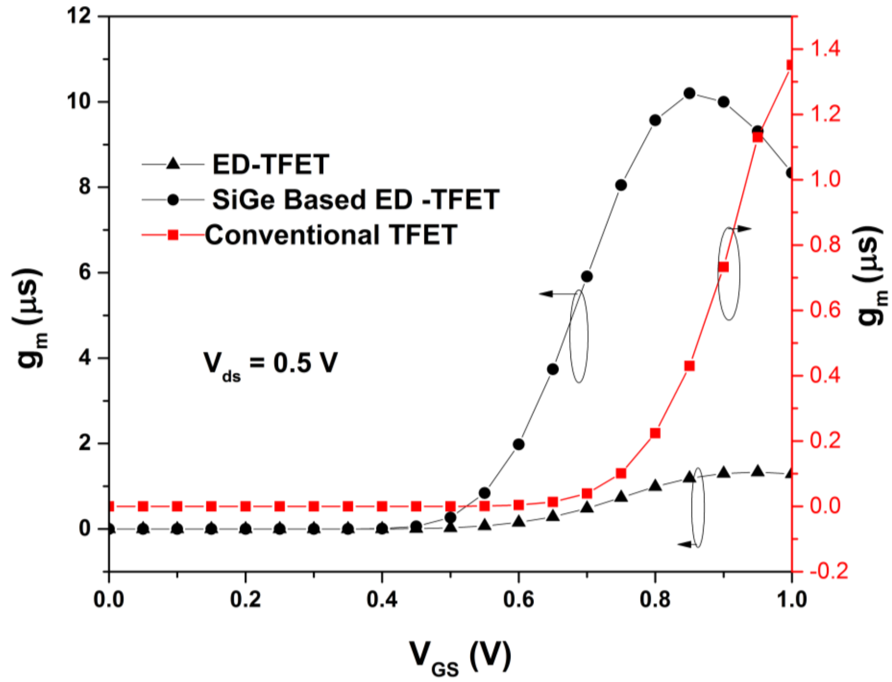

Fig.4.1: Variation in Transconductance (g_m)

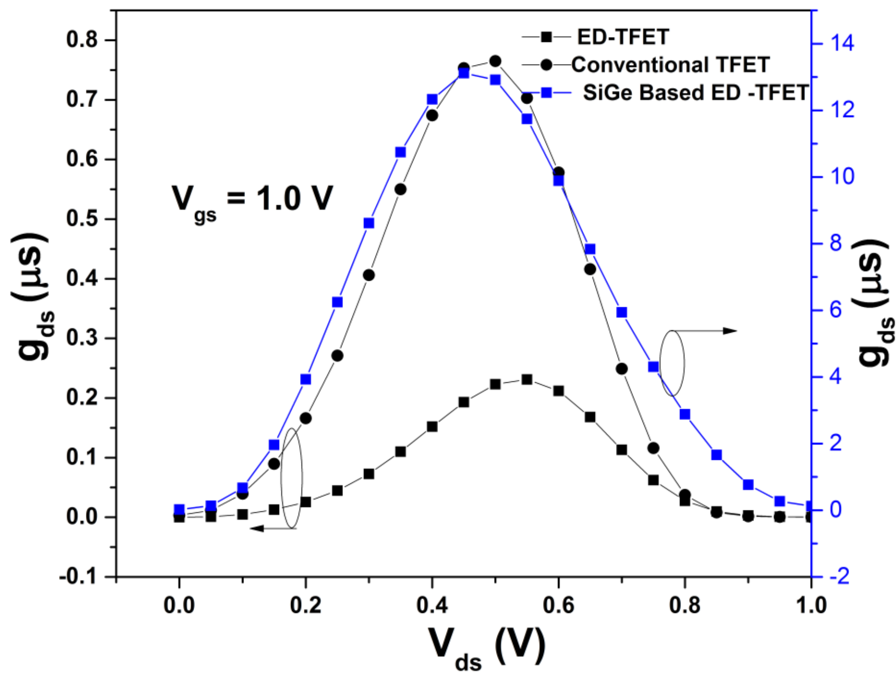

Fig. 4.2: Variation in output Transconductance (g_{ds})

4.3.2 Comparative Analysis of gate to drain capacitance (C_{gd}) and gate to source Capacitance (C_{gs})

Fig. 4.3 and 4.4 shows the Gate to source capacitances (C_{gs}) and gate to drain capacitances (C_{gd}) respectively. Electrical performance can be affected by parasitic capacitances at the circuit level. When the frequency is low the effect of parasitic capacitances is very low, but when we talk about higher frequency it plays a very important role at high frequencies the circuit makes a loop between output and input this caused circuit oscillates, and distortion occurs in the signal, so reduction in these capacitances is required. In this context, the gate to drain capacitances (C_{gd}) has more impact in operating frequency.

Lightly doped/ undoped drain region are selected therefore depletion region is wider and capacitance is inversely proportional to depletion width. And drain to gate capacitance decrease, which causes frequency increase as we can see in equation 4.2 and 4.3. In addition, the drain is underlapped between gate electrode; this also decreases drain to gate capacitances. Gate to source capacitances (C_{gs}) has very less effect in frequency because it is negligible as compared to C_{gd}. As shown in Fig. 4.5 we have shown changes in overall capacitances. Fig 4.5 shows small increment in C_{total} due to $C_{gs.}$

4.3.3 Variation in f_T and f_{max}

Other RF parameter Cut-off frequency (f_T) and a maximum frequency of oscillation (f_{max}) are important to determine of the high-frequencies performance of the devices. The cut-off frequency f_T is basically operating frequency of the device at short circuit when current gain decreases to unity it referred to as operating frequency. Cut-off frequency (f_T) formulated as:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (4.2)$$

$$f_{max} = \frac{f_T}{\sqrt{4R_g(g_{ds}+2\pi f_T C_{gd})}} \qquad (4.3)$$

In Fig 4.6, we can see that when the V_{gs} increases gradually the cut-off frequency increases because of transconductance increase and reaches to a maximum value further, it decrease for because then C_{gd} also increases and there is reduction in the mobility.

Transconductance g_m is high for SiGe-Based TFET due to Ge (germanium) in the source region, and C_{gd} is lower due to the underlapping of gate electrode. Both reason collectively increases the cut-off frequency of proposed SiGe-based Tunnel field-effect transistor as compare to conventional TFET and Si-based electrically doped TFET. The maximum cut-off frequency f_{max} also depends on the gate to drain capacitances and transconductance and f_T as equation (4.3) dictated. So f_{max} follow almost same graphs cut-off frequency. SiGe-Based TFET has to produce higher frequency than other two comparative structures, and it is about 15.2 GHz..

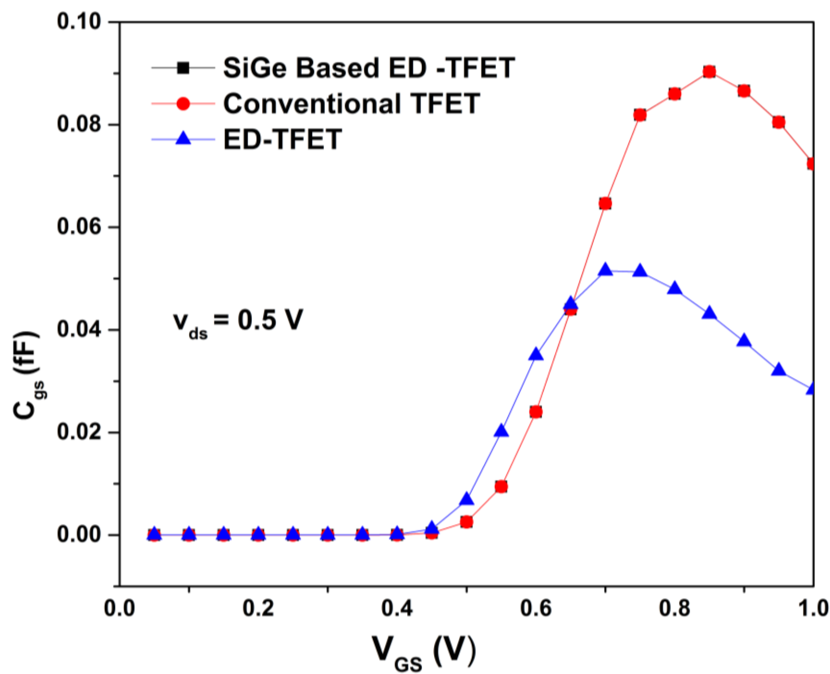

Fig. 4.3: Variance in C_{gs} with V_{GS} n-type TFETs

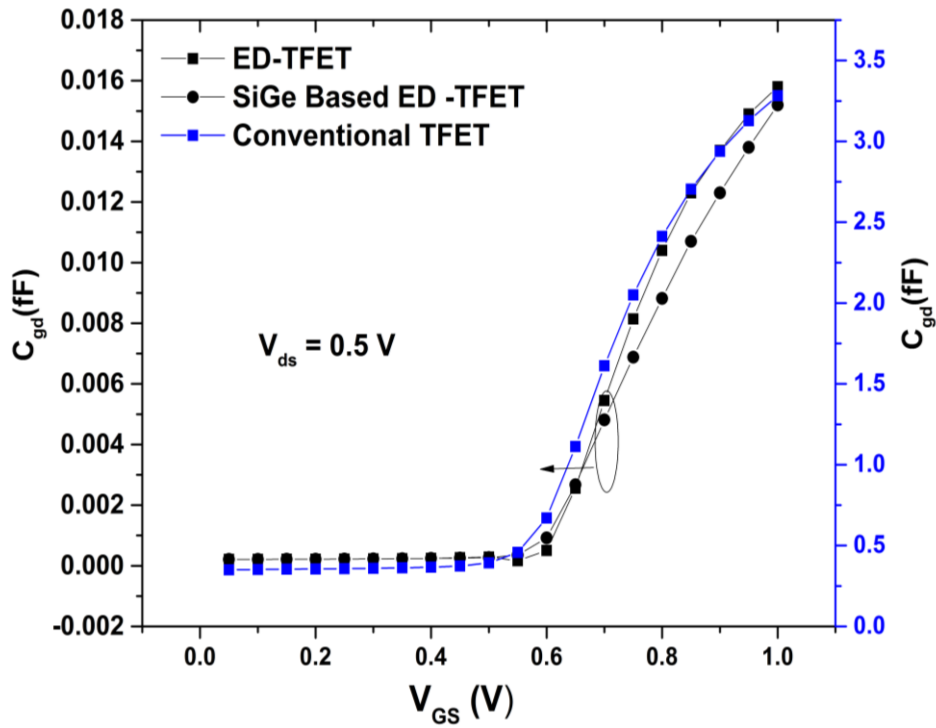

Figure 4.4: Variance in c_{gd} with V_{GS} in n-type TFET

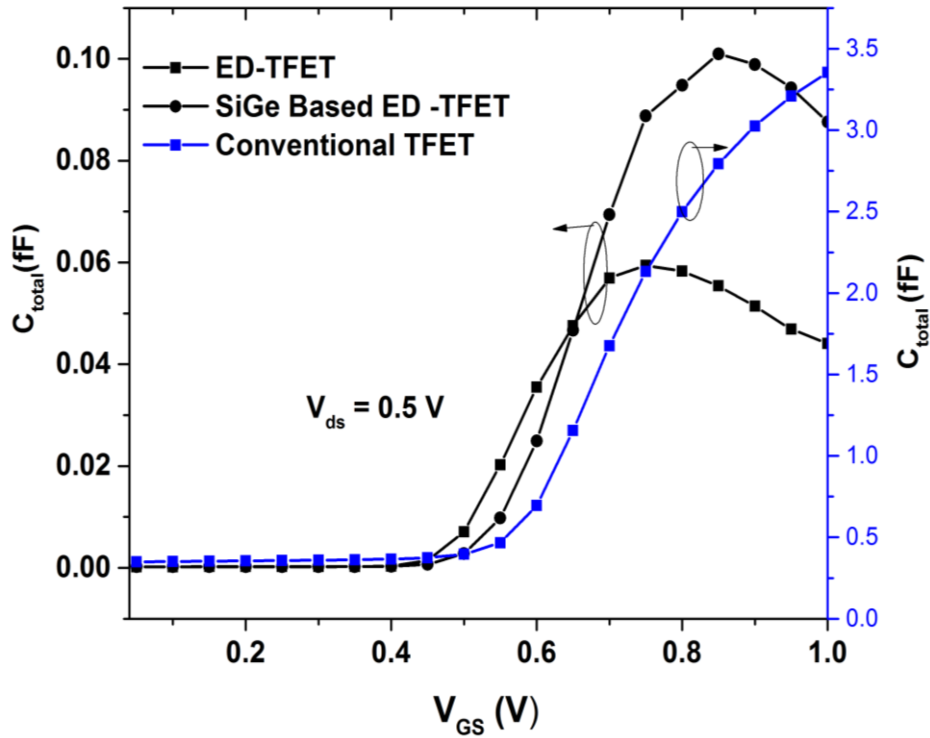

Fig. 4.5: Variation in Total Capacitance (c_{total}) in n-type TFETs

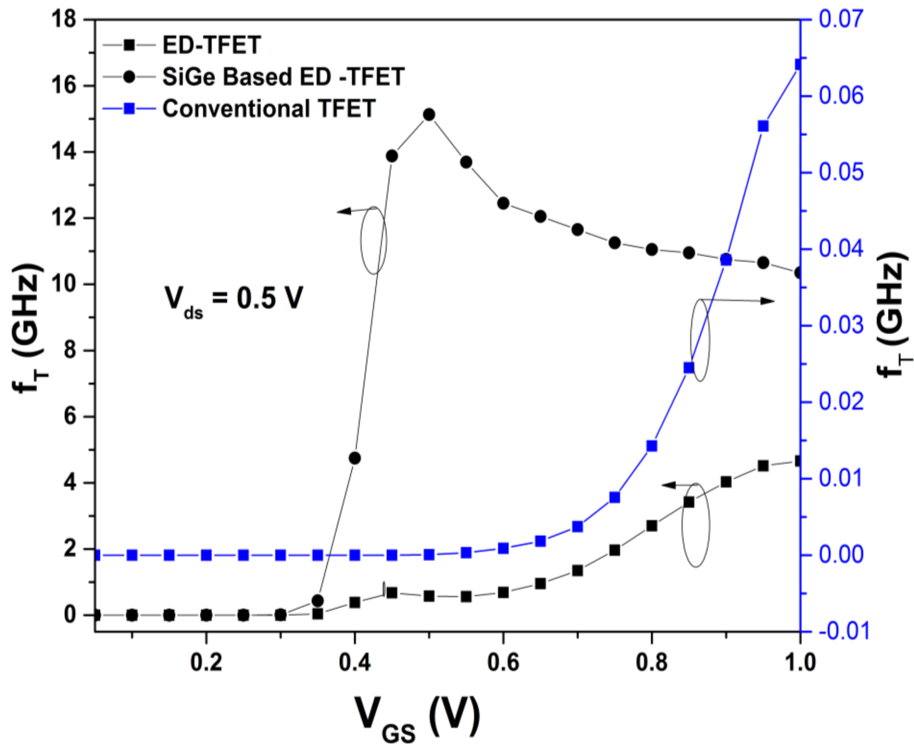

Fig. 4.6: Variation in f_T with V_{GS} in n-type TFETs.

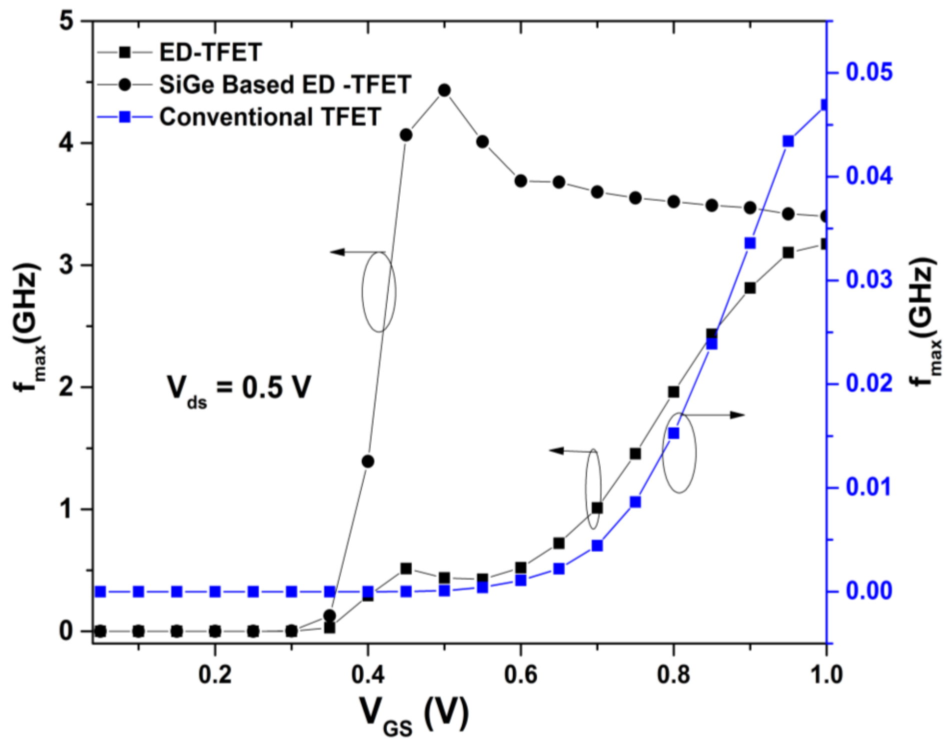

Fig. 4.7: Variation in f_{max} with V_{GS} in n-type TFETs

4.4 Summary

In SiGe-based device gate electrode is underlapped, that improves the RF performances. In proposed, SiGe-based device transconductance is also increased approximate one order of magnitude, which increases Cut-Off Frequency (f_T) & the maximum frequency of oscillation (f_{max}). Moreover in proposed device drain is lightly doped which suppress the bipolar effect. Fig 4.6 and 4.7 show the variance in cut-off frequency (f_T) as a function of gate to source voltage (V_{gs}) where we can see an increment in frequency, which is mainly due to increased transconductance and reduced gate to drain capacitances (C_{gd}). The result is summarised and reported in Table 4.1.

Table 4.1 Indicates the summarized output result for comparative analysis.

Parameter	Unit	Conventional TFET	ED-TFET	SiGe based ED-TFET
I_{on}	µm	8.52×10^{-6}	2.52×10^{-6}	2.7×10^{-5}
I_{off}	µm	1.48×10^{-17}	9.02×10^{-19}	6.02×10^{-19}
SS	mv/dec	30	14	15.10
C_{gs}	fF	.086	.047	.086
C_{gd}	fF	2.41	.0104	.009
g_m	µS	.22	.98	9.5
f_T	GHz	.14	2.70	16.1
f_{max}	GHz	.015	1.96	04.56

Chapter 5

Conclusion and Future Work

5.1 Conclusion

A detailed studied of SiGe-Based ED-TFET has been done in this thesis. We studied and analysis how doping less or lightly doped TFET can be configured as dynamically for n-type or p-type TFET and analyzed its basic fundamental operations. In addition to this, simulated outputs shows that the proposed SiGe-Based ED-TFETs, can be configured as n-type/p-type TFETs by changing polarity of bias. Also, in proposed SiGe-Based ED-TFET leakage current is so less in order of 10^{-18} A/μm, that makes this device suitable for low power application. Moreover, in the proposed device, the loss of small ON-state current of Silicon-based ED-TFET has been eliminated. In proposed SiGe Based ED-TFET ON-state current has been increased by one order of magnitude using $Si_{1-x}Ge_x$ (x= .5) in source Region.

The proposed device uses the electrically doped source & drain region for carrier concentration, which allows dynamic configuration. The promising switching behavior of proposed 2-D device simulations has been observed. The Proposed Changes in our device is helpful to achieve steeper band tunneling at source/channel side. This is due to that maximum tunneling generation rate of charge carriers. Proposed devices also overcome the issues off low ON-state current. Thus, ON current is increased by as compared with that of the Si-based ED-TFET because in proposed device narrow band gap matrail Ge is used in source region. In SiGe-Based device gate electrode is underlapped, which improves the RF performance. It also minimizes C_{gd} and increase cut-off frequency (f_T) and the maximum frequency of oscillation f_{max}.. Moreover, in proposed device drain is no doped which suppress the ambipolar effect.

5.2 Future Work

- Spice model development can be done on proposed device.

- Circuit integration of proposed structure.

- Detailed analog/RF performance analysis of proposed device.
- Noise analysis.

REFERENCES

[1] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, “Design of Ion-Implanted MOSFETs with Very Small Physical Dimensions,“ IEEE J. Solid-State Circuits, vol. SC-9, no. 5, pp. 256-268, Oct.1974.

[2] P. Packan, Short Course, IEDM 2007.

[3] International Technology Roadmaps for Semiconductor, ITRS, 2012

[4] Y. Taur and T. Ning, Fundamentals of modern VLSI devices, Cambridge University Press, New York, NY, 1998.

[5] P. Nilsson, Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS, IEEE Int. Conf. on Electronics, Circuits and Systems, 2006, pp. 656-659.

[6] Meyerson, IBM, Semiconductor Conference, January 2004.

[7] A. Lahgere, Thesis on Design and Analysis of Electrically Configurable Dopingless Field-EffectTransistors June.2015.

[8] Katirine boucart A thesis on “Simulation of Double-Gate Silicon Tunnel FETs with a High-k Gate Dielectric”

[9] International Technology Roadmaps for Semiconductor, ITRS, 2012

[10] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, ”Tunneling Field-effect Transistors (TFETs) with Subthreshold Swing (SS) Less Than 60 mV/dec,” IEEE Electron Device Letts., vol.28, no.8, pp.743-745, Aug. 2007.

[11] K.Boucart and A.M.Ionescu,” Double Gate Tunnel FET with High-k Gate Dielectric,” IEEE Trans. Electron Devices, vol.54, no.7 pp. 1725-1733, Jul. 2007.

[12] P. F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel and W.Hansch, ”Complementary Tunneling Transistor for Low Power Application,” Sold-state Electronics, vol.48 no.12, pp.2281- 2286, Dec 2004.

[13] K. K. Bhuwalka, J. Schulze and I. Eisele, ”Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering,. IEEE Trans. Electron Devices, vol. 52, no. 5, pp. 909-917, 2005.

[14] S.Saurabh and M.J. Kumar, ”Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor,”

Japanese Journal of Appl. Phys., vol. 48, pt. 1, no. . Article no.064503, June 2009.

[15] A. S. Verhulst, W. G. Vandenberghe, K. Maex, S. De Gendt, M. M. Heyns and G. Groeseneken," Complementary Silicon-Based Hetero-structure Tunnel-FETs With High Tunnel Rates," IEEE Electron Device Lett., vol.29, no.12, pp.1398-1401, Dec. 2008.

[16] T. Krishnamohan, D. Kim, C. D. Nguyen, C. Jungemann, Y. Nishi and K. C. Saraswat, "High-mobility Low Band-to-band Tunneling Strained-germanium Double-gate Heterostructure FETs: Simulations," IEEE Trans. Electron Devices, vol.53, no.5, pp.1000-1009, May 2006.

[17] M.-H. Chiang, J.-N. Lin, K. Kim, and C.-T. Chuang, "Random dopant fluctuation in limited-width FinFET technologies," IEEE Tran. Electron Devices, vol.54, no.8, pp. 2055-2060, Aug 2007.

[18] Y.; Zhang and M.; Tabib-Azar, "Tunnel field-effect transistor with two gated intrinsic regions," AIP Advances 4, 077109 (2014).

[19]Silvaco,Version 5.19.20.R. (2014) [Online]. Available: http://www.silvaco.com.

[20] Sahu, C.; Singh, J., "Charge-Plasma Based Process Variation Immune Junctionless Transistor," Electron Device Letters, IEEE, vol.35, no.3, pp.411,413, March 2014.

[21] Silvaco,Version 5.19.20.R. (2014) [Online]. Available: http://www.silvaco.com.

[22] International Technology Roadmaps for Semiconductor, ITRS, 2012.

[23] M. Alam, K. Kang, B. C. Paul, and K. Roy, "Reliability- and process variation-aware design of VLSI circuits," in Proc. 14th IPFA, Bangalore, India, 2007.

[24] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, “Tunneling Field-effect Transistors (TFETs) with Subthreshold Swing (SS) Less Than 60 mV/dec,“ IEEE Electron Device Letts., vol.28, no.8, pp.743-745, Aug. 2007.

[25] Seabaugh, “Low-Voltage Tunnel Transistors for Beyond CMOS Logic,“ Proce. of the IEEE, vol.98, no.12, pp.2095-110, Dec.2010.

[26] Ionescu A,“Tunnel field-effect transistors as energy effcient electronic switches“Nature Publishing, vol. 479, pp329-337, Nov.2011.

[27] De Marchi, M. “Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs,“ Electron Devices Meeting, 2012 IEEE International, vol., no., pp.8.4.1,8.4.4, 10-13 Dec. 2012.

[28] De Marchi, M.et al, “Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs,“ Electron Device Letters, IEEE, vol.35, no.8, pp.880,882, Aug. 2014.

[29] Chitrakant Sahu, Avinash Lahgere, Jawar Singh,“A Dynamically Configurable Silicon Nanowire Field Effect Transistor based on Electrically Doped Source/Drain,“ arXiv:1412.4975 [cond-mat.mes-hall].

[30] Kumar, M.J.; Janardhanan, S., “Doping-Less Tunnel Field Effect Transistor: Design and Investigation,“ Electron Devices, IEEE Transactions on, vol.60, no.10, pp.3285,3290, Oct. 2013.

[31] Ghosh, B.; Akram, M.W., “Junctionless Tunnel Field Effect Transistor,“ Electron Device Letters, IEEE, vol.34, no.5, pp.584,586, May 2013.

[32] Silvaco,Version 5.19.20.R.(2014) http://www.silvaco.com.

[33] Parihar, M.S.; Kranti, A., “Volume accumulated double gate junctionless MOSFETs for low power logic technology applications,“ Quality Electronic Design (ISQED), 2014 15th International Symposium on, vol., no., pp.335,340, 3-5 March 2014.

[34] D. Soni, D. Sharm, S. Yadav, M. Aslam, N. Sharma, Performance improvement of doped TFET by using plasma formation concept, Superlattices and Microstructures (2017), doi: 10.1016/j.spmi.2017.10.012.