Design and Implementation of Ohmic Metal Contact RF MEMS Switch

By

Manishkumar Patel

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Under the supervision of

Dr. D. Boolchandani

Professor, Dept. of ECE

MNIT, Jaipur

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Dr. S. Ali Akbar,
Head, Project Management & Business Development &
Chairman, International Science & Technology Affairs Group

No: PMBD\S\Trg\MNITJ\2017
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This is to certify that **MR. MANISHKUMAR PATEL, ID No. 2015PEV5082, M. Tech. (VLSI Design)** student of your Institute has completed his project work at this Institute during **2nd August, 2016 to 30th December, 2016.** His project was on ***"DESIGN AND SIMULATION OF OHMIC METAL CONTACT RF MEMS SWITCH"***

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पिलानी–333031, (राजस्थान)/Pilani-333031, (Rajasthan)

Fax: 01596-242393, 242294; email: saakbar@ceeri.ernet.in Ph: 01596-245287(O) 252646, 252244 (O)

QUALCOMM India Private Limited

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DLF Centre, 3rd Floor,
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www.QUALCOMM.com

INTERN CERTIFICATE

This is to certify that Manish Kumar Patel worked as an Interim Engineering Intern at Qualcomm from 9th Jan'17 to 30th June'17.

Manish Kumar Patel's performance during the internship was satisfactory.

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18th June 2017

Date

Pooja Joshi

Director Staffing

Other offices:
Mumbai: Unit no. 1102, Platina Building, G Block 11th Floor, Plot # C-59, Bandra Kurla Complex, Mumbai, India 400051 India. Tel: +91-22-67041400; Fax: +91-22-6704150
Hyderabad: 5th Floor, Bldg # 8 Mindspace, Hitec City, Madhapur, Hyderabad, 500 081, Andhra Pradesh, India. Tel: 91-40-3011-0000; Fax: 91-40-3011-0001
Bangalore: Plot no. 125-127, EPIP IInd Phase, Whitefield, Bangalore, Karnataka 560 066, India. Tel: 91-80-3984-1800; Fax: 91-80-3984-2001

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Manishkumar Patel
(2015PEV5082)

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Manishkumar Patel

Abstract

The advancement in the field of Micro-fabrication has revolutionized the field of RFMEMS (Radio Frequency-Micro Electromechanical System). With the advancement in RF MEMS, the miniaturization of communication devices has reached new horizon of technology. The advantages like small size, low power consumption, high Isolation, low Insertion loss has drawn the attention of many commercial as well as research institutions towards RF MEMS Switches. The RF MEMS Switches can be used in handheld communication devices, Satellite communication, defense RADAR systems, etc. Here the presented thesis is focused on the Ohmic Metal contact RF-MEMS Switches among many MEMS Switch configurations. The various designs of SPST, SPDT, SP4T has Designed and simulated. Moreover, T-Type and C-Type switches have also been implemented for the use as basic building blocks in redundancy system matrix. The C-Type switch has been developed using least number of hanging structure and the possibilities for T-Type switches has been discussed.

The second part of the thesis is dedicated to the work carried out at the Qualcomm Ind. Pvt. Ltd., Bangalore. Being a part of the CPUSS DV (CPU Sub-system Design Verification) team, the work is focused on the verification of some specific features of CPUSS. Over here, the brief explanation of the memory hierarchy and problems due to shared memory in a multiprocessor system is given. However, the verification plan is not discussed over here.

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PART-A
1 INTRODUCTION

This Chapter starts with the brief introduction of Electromagnetic Radio Frequency parameters and the role of MEMS Technology in Radio Frequency Engineering. Next subchapter explains the working principle of RF MEMS Switches. In a subsequent part, comparison and applications of MEMS Switches are shown.

1.1 PROLOGUE

Before moving towards the thesis content it is necessary to get familiar with the basic technical parameters and terminologies related to RF MEMS Switches. Here we will discuss the parameters related to mechanical analysis and S-parameters for the better understanding of RF analysis. Then we will have a brief glimpse of micromachined transmission lines.

Pull-In Voltage

Many electrostatic sensors and actuators involve at least one deformable by springs. An important design for such sensors and actuators is to determine the amount of static displacement under a certain bias voltage.

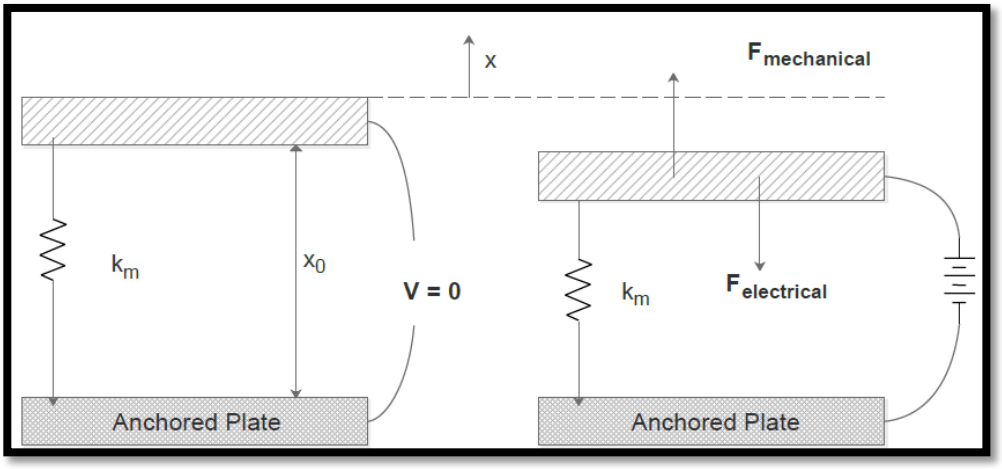

FIGURE1 SCHEMATIC OF ELECTROSTATIC CAPACITIVE PLATES.

A parallel plate capacitor with one movable plate supported by a mechanical spring is diagramed in Figure 1. When the voltage is applied, an electrostatic force $\mathbf{F_{electric}}$ will be developed. The magnitude of $\mathbf{F_{electric}}$ when the movable plate is at its starting position is given by

$$Felectric = \frac{1}{2}\frac{\epsilon A}{d}V^2 = \frac{1}{2}\frac{CV^2}{d}$$

This force will tend to decrease the gap, which gives rise to displacement and mechanical restoring force. Under static equilibrium, the mechanical restoring force has equal magnitude but opposite direction as the electrostatic force. The spatial gradient of the electric force is defined as an *electrical spring constant*,

$$k_e = \left|\frac{\partial F_{electric}}{\partial d}\right| = \left|-\frac{CV^2}{d^2}\right| = \frac{CV^2}{d^2}$$

The effective spring constant of a structure is the mechanical spring constant minus the electrical spring constant. The magnitude of the mechanical restoring force is,

$$F_{mechanical} = -k_m x$$

Equating the magnitudes of $\mathbf{F_{mechanical}}$ and $\mathbf{F_{electrical}}$, at x and rearranging terms, we obtain

$$-x = \frac{F_{mechanical}}{K_m} = \frac{F_{electrical}}{K_m} = \frac{C(x)V^2}{2(x_0 + x)K_m}$$

Where $\mathbf{x_0}$ is the initial gap between two plates and **x** is the displacement under the effect of non-zero external bias. The equilibrium distance between two capacitor plates can be calculated by solving the quadratic equation above with respect to **x**. Now at a particular bias voltage, the electrostatic and mechanical restoring force balance each other. Moreover, the magnitude of the electric force constant equals the mechanical force constant. The spring in such condition exhibits extreme softness. The bias voltage that invokes such condition called the *pull-in voltage*, or **Vp**. If the bias voltage is further increased beyond **Vp**, the equilibrium solution disappears. In reality, the electrostatic force will continue to grow while the mechanical restoring force, increasing only linearly, is unable to catch up with it again. The two plates will be pulled against each other rapidly until they made a contact, at which point the mechanical contact force will finally balance the electric one. These conditions are called pull in or snap in. At the pull-in voltage, the magnitude of the electrical force and the mechanical balance force are the same. By equating two forces and rearrange terms, we obtain,

$$V^2 = \frac{-2k_m x(x + x_0)^2}{\epsilon A} = \frac{-2k_m x(x + x_0)}{C}$$

The value of **x** is negative when the spacing between two electrodes decreases. In addition, the gradients of these two curves at the intersection point are identical, namely,

$$|K_e| = |K_m|$$

The expression for the electric force constant,

$$k_e = \frac{CV^2}{d^2}$$

Can be rewritten by plugging in the expression for $\mathbf{V^2}$. This procedure results in a new expression for the electric force constant,

$$k_e = \frac{CV^2}{(x + x_0)^2} = \frac{-2k_m x}{(x + x_0)}$$

The only solution for **x** under which Equation can be satisfied is

$$x = -\frac{x_0}{3}$$

The above equation states that the relative displacement of the parallel plate from its rest position is exactly one-third of the original spacing at the critical pull-in voltage. The critical displacement is true irrespective of the mechanical force constant and the actual pull-in voltage. Consequently, the pull-in voltage is found to be

$$V_p = \sqrt{\frac{4{x_0}^2 k_m}{9C}}$$

In the practical scenario, the pull-in voltage and threshold distance will deviate from the calculation obtained using the idealized case. There are two sources of deviation. First, the fringing capacitive field will alter the linearity of the electrostatic force expression. Second, the restoring force provided by the mechanical springs will differ from that predicted by linear model if the displacement is large. Understanding the pull-in effect and mathematical tools for estimating the pull-in effects have been advanced steadily *[9].*

S-Parameters

First of all, let's start with the phenomenon behind s-parameter before we jump into the mathematics. The s-parameters define low RF energy travels through the multiport network. With the help of s-parameters, we can simply replace the properties of the complicated network with a black box. For an RF signal that incident on one port, some sectional part of an incident energy get reflected back and some of the part enters into the port and travels through the network and exists from one more port with or without having amplification or attenuation. The left of the incident RF power is lost as in form of heat or in form of electromagnetic radiation.

The s-parameters of N port network consists N^2 s-parameters coefficients. The each of the N s-parameters represents possible inputs and output paths. S-parameters are a complex quantity used so it is having magnitude and phase. We refer another magnitude only as we don't consider the change in phase by an amplifier or attenuator. We only worry about the noise or loss. S-parameters are defined for a given frequency and are a relation of a system frequency for the network which is non-ideal.

$$(S_{11})$$

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

$$\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix}$$

The basic representation of s-parameters is in the formal matrix, in which a number of rows and which represent the ports. For the s-parameters Sij in the matrix, the j subscript stands for the port that where the input power is incident (the input port) and I stands for the output port. For example, S11 represents the ratio of the amplitude of the signal that is getting reflected from the port 1 to the power which is incident on the port 1. If we take a close look parameters positioned on diagonal represents the reflection coefficients as they represent what happened on a single port. The parameters other than diagonal elements are reflected as transmission coefficients as they represent what happens at one port if power is incident on another port.

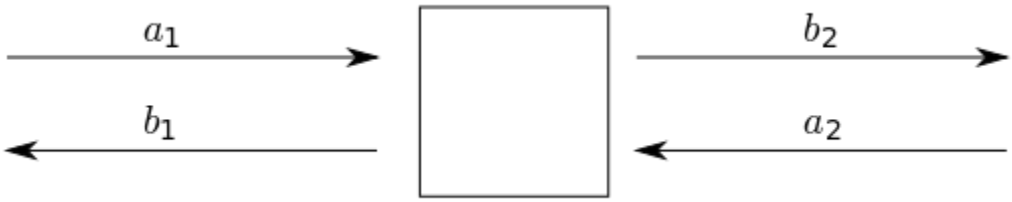

FIGURE 1 SCHEMATIC OF TWO PORT NETWORK

To represents the complex network blocks; most commonly two-port network s-parameters matrix is used in that case; the relation between incident power and reflected power is shown as below by using s-parameters matrix.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

By simplifying the matrix we get,

$$b_1 = S_{11}a_1 + S_{12}a_2\,; \qquad and \qquad b_2 = S_{21}a_1 + S_{22}a_2.$$

Each equation over here represents the relation between the reflected and incident power at each network ports of s-parameters.

If we consider a1 as the incident power wave at port 1, it may exit from the network by port 2 (b2) or from port 1 (b1) itself.

Now if port 2 of the network is terminating at system impedance (Z0) then by maximum power transfer theorem b2 will be totally absorbed making a2 equals to zero. Therefore, if we consider incident voltage waves as a1=v1+ and a2=v2+ and further consideration of b1=v1- and b2=v2-.

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+} \quad and \quad S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+}$$

In the same every port 1 is terminated in the system impedance then eventually a1 parameters becomes zero giving

$$S_{12} = \frac{b_1}{a_2} = \frac{V_1^-}{V_2^+} \quad and \quad S_{22} = \frac{b_2}{a_2} = \frac{V_2^-}{V_2^+}.$$

S-parameters at two-port network can be described in more generic manner as following

S_{11} Is the input port voltage reflection coefficient

S_{12}Is the reverse voltage gain

S_{21} Is the forward voltage gain

S_{22} Is the output port voltage reflection coefficient.

Smith charts are used to plot the diagonal parameters that are input and output reflection coefficient. Transmission coefficient is usually not plotted on the Smith chart.

Insertion Loss: Insertion loss measures the amount of energy that is lost as the signal arrives at the receiving end of the cabling link. The insertion loss measurement quantifies the effect of the resistance the cabling link offers to the transmission of the electrical signals.

Isolation: Isolation is the insertion loss in the open path of a switch or between two ports on a passive device.

Return Loss: Return loss is the loss of power in the signal returned/reflected by a discontinuity in a transmission line or optical fiber. This discontinuity can be a mismatch with the terminating load or with a device inserted in the line.

1.2 Overview of MEMS and RF MEMS

The MEMS stands for Micro-Electromechanical System. It refers to the collection of sensors and actuators which sense the change in the environment and have the ability to react to change in that environment with the use of control circuits *[2].* The IC technology is the starting point for discussing the history of MEMS. The transistor, an electronics switching device invented in 1947 at AT&T Bell Laboratories, unleashed a revolution in communication and computing. In 1971, then the

State-of-the-Art Intel 4004 chip was constructed of only 2250 transistors. The density of transistor integration has increased by two fold every 12 to 18 months then after following Moore's law *[1].* In the beginning of the 1990's, MEMS emerged with the aid of the development of Integrated Circuits fabrication process, where sensors. Actuators and control circuits are fabricated on the same silicon substrate. With the support of government and industry more financial support comes into the picture and as a result, remarkable progress has been achieved in MEMS *[9]*. Efforts of all sectors summed up and presented in the commercialization of some less integrated MEMS devices such as micro-accelerometers, head of a inject printer, micromirrors for projection. By the end of 1990's most of the

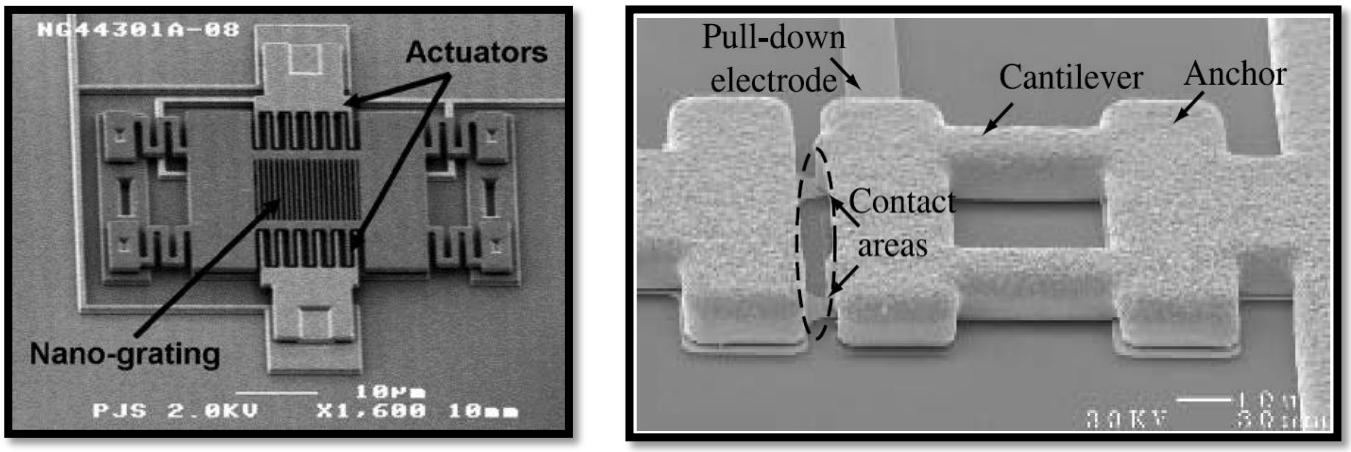

FIGURE 2 (A) MEMS ACCELEROMETER (B) RF MEMS RADANT SWITCH

MEMS devices having various sensing and actuating mechanism were fabricated using silicon bulk micromachining, surface micromachining, and LIGA *[8]*. Sometimes many microdevices can also be fabricated using semiconductor processing technology or stereo lithography. Stereolithography is a low-cost LIGA for fabricating high aspect ratio MEMS devices in UV curable semiconducting polymers.

Among the diverse areas of engineering and science, MEMS have also become popular in Microwave and millimeter wave systems. The recent drastic change in personal communication handheld devices has created new requirements for the miniaturization of devices. To serve this need, RF MEMS comes into the picture. The RF MEMS deals with the designs as well as fabrication of MEMS for RF integrated circuits. The role of MEMS devices in RF MEMS is to develop actuation or adjustment of a separate RF devices or components. The concept of MEMS switches was introduced back in 1980's for low frequencies but remained a topic of curiosity for a long time *[3]*. They were the essential devices that used a micromechanical movement to achieve short circuit and an open circuit for the transmission lines. Later in 1990-91, with the impactful support of Defense Advance Research Project Agency, Dr. Larry Larson at the Hughes Research Labs located in Malibu, California developed the first MEMS switch for the purpose of Microseven application *[3]*. This switch showed extremely good

performance up to 50GHz which was run better than what had been demonstrated with devices. The initial results demonstrated by Larson were so outstanding that they get the attention of serval companies and labs. By the time of 1995, Rockwell Science Centre and Texas Instrument; both had implemented their own outstanding RF MEMS switch. The Rockwell Switch was a useful to metal constant type switch other than that Texas Instrument switch was developed using capacitive contact switch *[3]*. By the end of the 1990s, due to its commercial and defense potential, RF MEMS had seen an amazing growth.

The reason behind that was while the there was a tremendous advance in GaAs HEMT devices and in silicon CMOS transistor; there was a barely an advance in semiconductor switching diodes. Clearly, a radical new technology was needed for low loss applications, which was achieved with RF MEMS. RF MEMS research focuses on four major areas *[7]*. (a) RF MEMS Switches, varactors and inductors (b) Micromechanical Transmission Line (c) FBAR and filters (d) RF Micromechanical resonators. This thesis solely concentrates on RF MEMS Switches.

1.3 Working Principle of RF Switches

One can distinguish the phenomenon of RF MEMS switch it two ports; one is the actuation section (mechanical port) and the other is electrical section. The actuation part of the switch requires external force for the mechanical movement which can be obtained by using different phenomenon based designs such as electrostatics, magnetostatic, piezoelectric or thermal design.

The movement of the switch can be vertical or horizontal based on the length of the design. Till now different concept based switches like electrostatic type; thermal type and magnetostatic type switches have been demonstrated with a wide range of frequency of 0.1 to 100 GHz. With higher reliability up to 60 billion cycles and different wafer scale manufacturing techniques. Considering the electrical part, a MEMS switch can be implemented either in series or in parallel configuration and other than that it can be distinguished as per the kind of contact it has like as metal to metal or capacitive switch that leads to the total number of combinations of 32 (2*2*2*4) different kind of MEMS switches using different contact circuit and actuation mechanism implementation *[6]*.

The Basic Working principle is simple. The Transmission Line is interrupted. The Interruption is made to obtain the OFF state of the switch that is an input port and output ports are isolated to each other. Interruption can be of any kind like the capacitive coupling of the input port to the ground or physical open circuited contact between the input port and an output port. According to the

phenomenon used for the interruption, the switches are classified as capacitive switches or ohmic switches *[6]*. For toggling the state (ON state to OFF state/OFF state to ON state), the actuation part of a switch is made to move. The movement can be accomplished by one of four actuation mechanism mentioned above. Electrostatic actuation is the most prevalent technique in use today due to its virtually zero power consumption, small electrode size, thin layers used, Comes with short switching time compared to others, the achievable contact force of 50-200 mN and with the possibilities of bias times having higher resistivity. In many of the RF switches; the actuation voltage is high up to 30-80V in which case, a CMOS up converter circuit is used for the actuation voltage

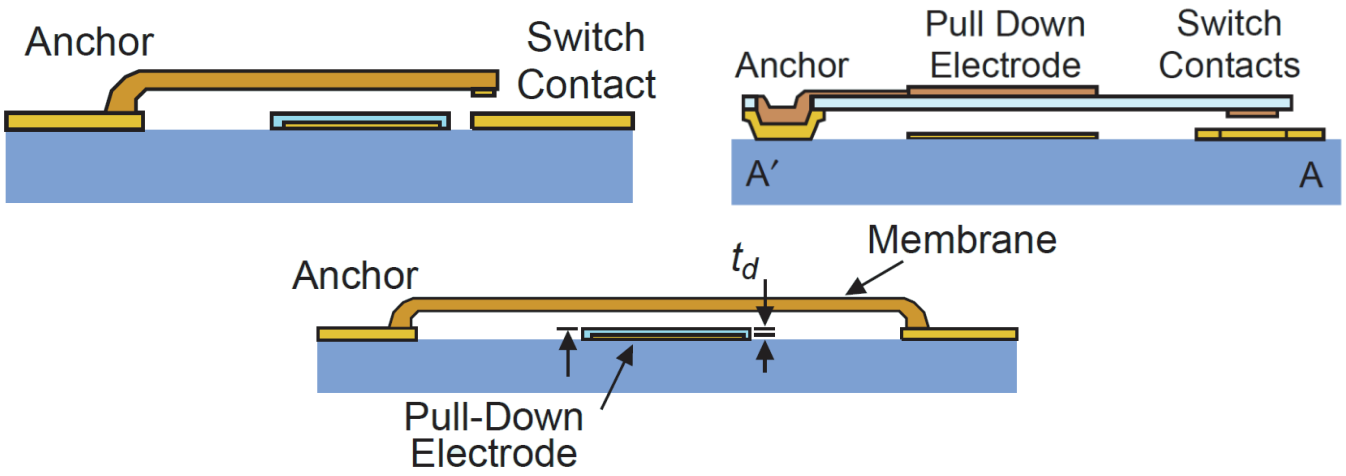

FIGURE 3 RF MEMS SWITCH CONFIGURATIONS

As shown in figure 3(a) and figure 3(b) an actuation part is placed in series with the electrical part and the contact formed is ohmic contact hence termed as Ohmic Series Off-line switch and Ohmic Series In-line switch respectively. In figure 3(c), we can see that the actuation part is placed in shunt with the electrical part and contact made is also capacitive hence called Shunt Capacitive Switch. Furthermore, according to the number input and output port, the Switches are termed as accordingly. Likewise, a switch having a single input and two outputs termed as SPDT (Single Pole- Double Throw).

1.4 COMPARISON OF RF SWITCHES

The commonly used RF switches in the microwave industry are mechanical switches which include coaxial and waveguide and semiconductor switches which include p-i-n diode and FET. By virtue of its designs, mechanical switches have benefits of low insertion loss, large all style isolation and high power handling capability and are highly linear *[3]*. Moreover, they are heavy, bulky and slow in switching compare to that, semiconductor switches a faster switching speed are smaller in size and

weight but have lower performance in insertion loss, dc power consumption isolation, intermodulation and power handling capabilities.

Whereas MEMS switch ensures the combine advantages properties of both semiconductor switches and mechanical switches. MEMS switch unhouses the good RF properties and low power consumption of mechanical switches. For attenuation purpose, most MEMS switch uses electrostatic phenomenon which results in near zero power consumption as there is no current flow in the switch. Other than that, MEMS switches use air gaps in isolation state result in higher isolation. Adding to that it has very low intermodulation products.

TABLE 1 COMPARISON OF RF SWITCHES

	FET	p-i-n Diode	Mechanical	MEMS
FOM (10^{-15}s)	270	110	0.073	2.5
dc Power	~0	10mW	~	~
Isolation	Low	Medium	High	High
Size (mm^2)	Small	Small	Large	Small

Table 1 gives the comparison among MEMS RF switch and other RF switches including FET, pin diode and a mechanical switch. There are some disadvantages with RF MEMS switch. One of them was lifetime but later on, it has been addressed nowadays with researchers indicating; life cycles of millions in number. As MEMS switch cannot withstand with high power operations it restricts its usage to few watts. Increasing their power handling capabilities will allow their usage in satellite communication. The other concern with MEMS switches was packaging as more number of moving and mechanical parts were involved in the design. Conventional techniques for packaging overshadows the capabilities of MEMS structure.

1.5 APPLICATION OF MEMS SWITCHES

The major two areas where RF MEMS switches can gain the potential amount of attentions are spacecraft application and mobile communication *[7]*.

The spacecraft applications demand highest switching performance and MEMS RF switch can be the best choice for the same, in wireless communication mobile devices demands low-cost designs which can be served by RF MEMS technology. In the following session, our focus will be on RF MEMS switches and switch Matrices for satellite application.

MEMS switches have replaced the SP2T and SP3T switches, which were used in dual-band, and triple-band cell phones. Those switches were implemented using semiconductor technology. The advantage of using MEMS technology, in this case, is an RF-performance improvement, which would, in turn, reduce dc power consumption. A commercial MESFET provided about 0.9 dB insertion loss which by itself consuming about 19% of generated RF power. In principle, a MEMS switch is providing 0.2 dB insertion loss which reduces the power loss to 4.5%. This improvement is a worthwhile engineering objective *[7]*. Figure 4 shows the use of MEMS SP8T, SP16T switches in the handheld wireless communication device.

Satellite communication systems also rely on switch matrices to provide system redundancy and to enhance the satellite capacity by providing full and flexible interconnectivity between the received and transmitted signals. The switch matrix provides the flexibility to independently direct the subchannels to the desired downlink beam. One of the most common use cases of switch matrices is to provide system redundancy to the satellite payloads *[13]*.

The switch matrices help to provide redundancy in the case of failure of any receivers or high power amplifier. In the case of failure of any of the component in the payload, switch matrices will reroute the incoming signals to the spaced components placed in the system and assures the full functionality of the payload system We will discuss further of Switch Matrices in Chapter 5.

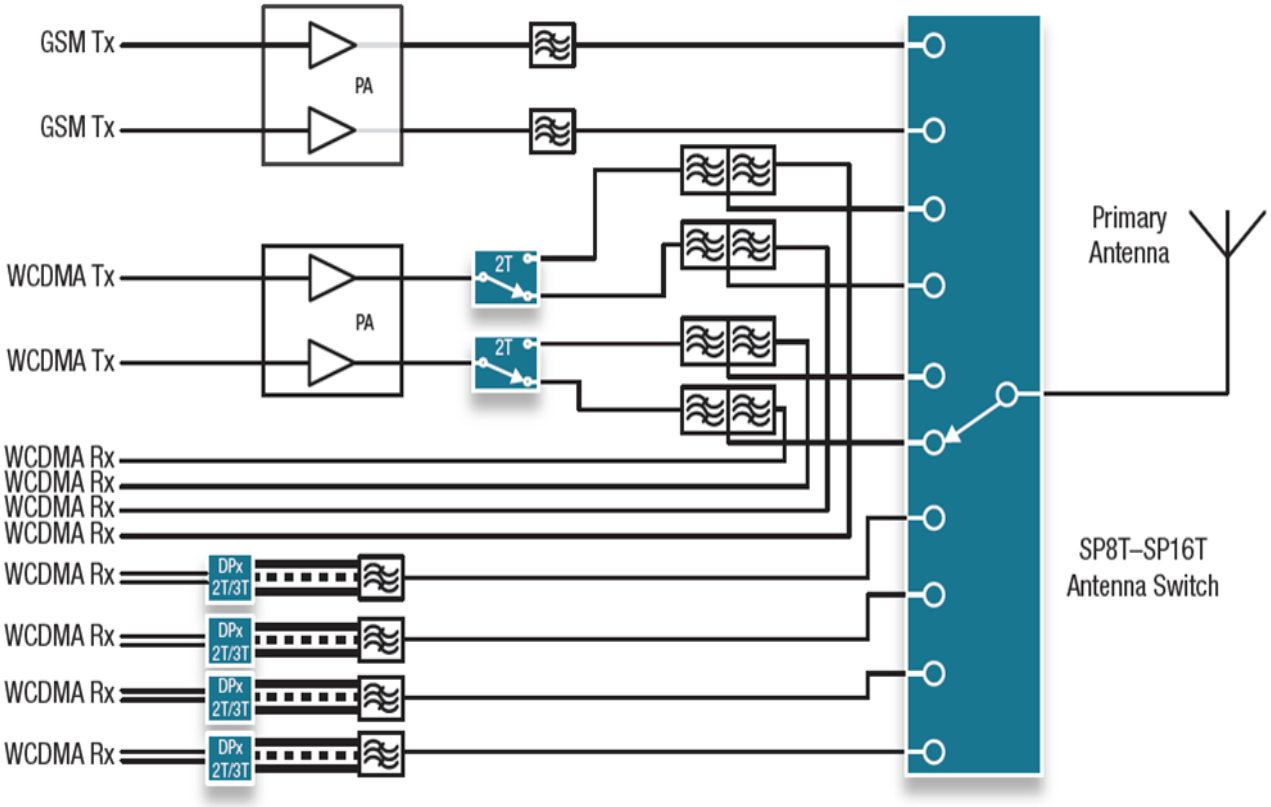

FIGURE 4 APPLICATION OF RF MEMS SWITCH IN MOBILE COMMUNICATION

2 CHALLENGES FOR MEMS SWITCHES

Considering Reliability a key factor for enabling use of MEMS Switch in Space Application, the presented chapter focuses on the Reliability Issues for the MEMS Switches. And same is summarized in the next subchapter.

2.1 RELIABILITY ISSUE

one of the most common use cases of switch matrices is to provide system redundancy to the satellite payloads. The switch matrices help to provide redundancy in the case of failure of any receivers or high power amplifier. In the case of failure of any of the component in the payload, switch matrices will reroute the incoming signals to the spaced components placed in the system and assures the full functionality of the payload system.

2.1.1 DIELECTRIC CHARGING

The dielectric charging constitutes a major problem that still inhibits the commercial application of RF MEMS capacitive switches. The effect arises from the presence of the dielectric film, which limits the displacement of the suspended electrode and determines the device pull-down state capacitance. Macroscopically, the dielectric charging is manifested through the shift or/and narrowing of the pull-in and pull-out voltages window thus leading to stiction hence the device failure. The first qualitative characterization of dielectric charging within capacitive membrane switches and the impact of high actuation voltage upon switch lifetime were presented by C. Goldsmith et al. (Goldsmith et al. 2001) who reported that the dependence of a number of cycles to failure on the peak actuation voltage follows an exponential relationship *[11]*. The reliability of low-power capacitive switches is dominated by stiction between the dielectric layer and the metal layer due to the large contact of the switch. The major stiction component is due to the charge injection and charge trapping in the dielectric layer. The Phenomenon is simple. Whenever we apply a DC Voltage level to the actuation electrode for the actuation purpose, some of the charged particles trapped in the dielectric layer above the actuation electrode which is supposed to provide isolation between actuator and actuation electrode. The charge carriers can be trapped in any of three trapping areas. These include (i) The interface traps between Metal and Dielectric Layer, (ii) the bulk of Dielectric layer (iii) Surface of the dielectric layer. The Dielectric charging causes drift in C-V Curves and Pull-in, Pull-out voltages. With the increment in trapped charge carrier, it eventually results in Stiction of an actuator to the bottom electrode. Figure 5 shows the drift in C-V curves due to dielectric charging.

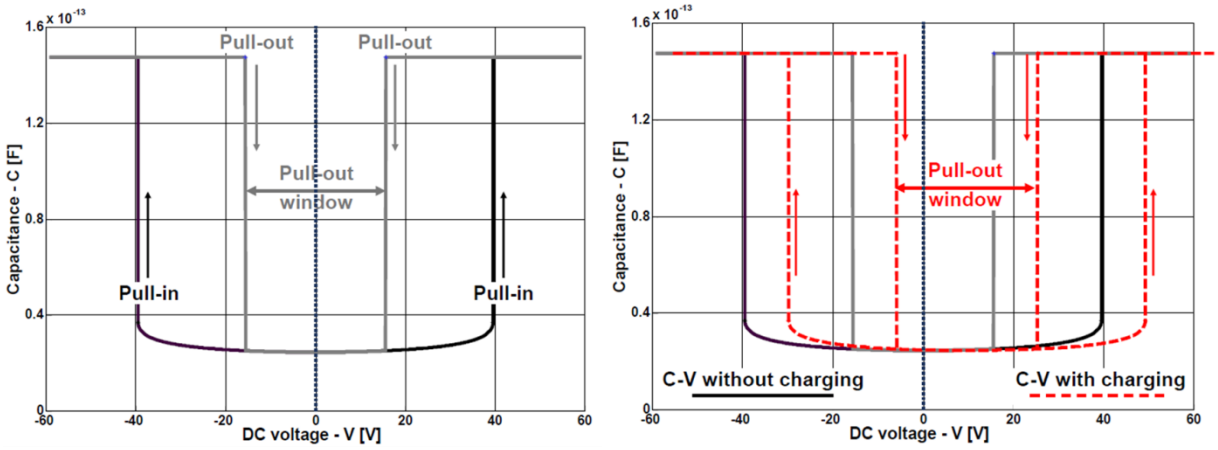

FIGURE 5 CV CHARACTERISTIC OF RF MEMS SWITCHES AND DIELECTRIC CHARGING EFFECT

The solution to the dielectric is as follows. (A) Use of Different Dielectric Materials. (B) Use of Bipolar actuation instead of unipolar actuation. Starting from the dielectric material choice; as silicon dioxide arrears lower trap density compare to the SiN, the use of SiO2 as a dielectric layer slows down the role of dielectric charging. The trap density of PECVD silicon dioxide is much lesser than the PECVD silicon nitride. The disadvantage of using SiO2 is it offers lower down state capacitance which results in poor insertion loss.

Another technique to slow down the role of dielectric charging is to use bipolar voltage signals for the purpose of actuation in capacitive plates is proportional to V2. So which any amplitude sign of biasing voltage, the electrostatic force will be attractive always use of bipolar actuation voltage signals will remove/ inject charge carriers at every switching. The removal and injection of charge carrier are not identical. So it will eventually result into net charge trapping. But though it enhances the performance of the switch in a vast manner.

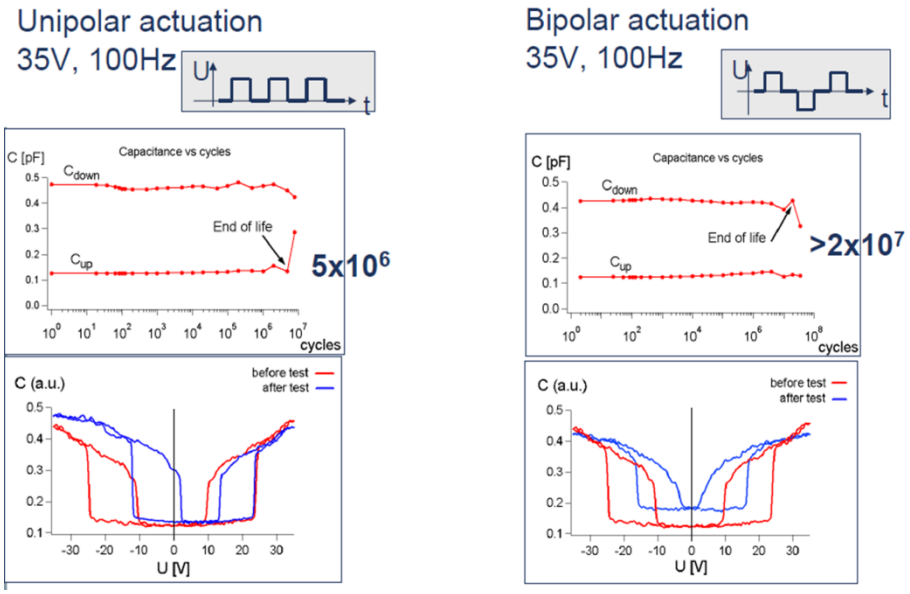

FIGURE 6 EFFECT OF UNIPOLAR AND BIPOLAR ACTUATION VOLTAGES IN DIELECTRIC CHARGING

2.1.2 NANO-SCALE HEATING

As many conceptual phenomena like detonation, current flow healthier at the contact are involved in metal to metal control, understanding the failure of metal contact switch is a tough task. Adding to that many more issues being reported like adhesion, material transport, melting thermally induced explosions related to boiling at metal contact and increasing contact resistance and heating at contact points *[13]*. We will extend one discussion further. The significant amount of contact resistance is due to roughness at the surface. As two metal surfaces come into the contact the contact is not idle. Only the higher points of the rough surface touch each other. Due to that the contact areas reduces significantly and give rise in contact resistance significant component of contact resistance is caused by the roughness of the contacting surfaces as shown in Figure 7.

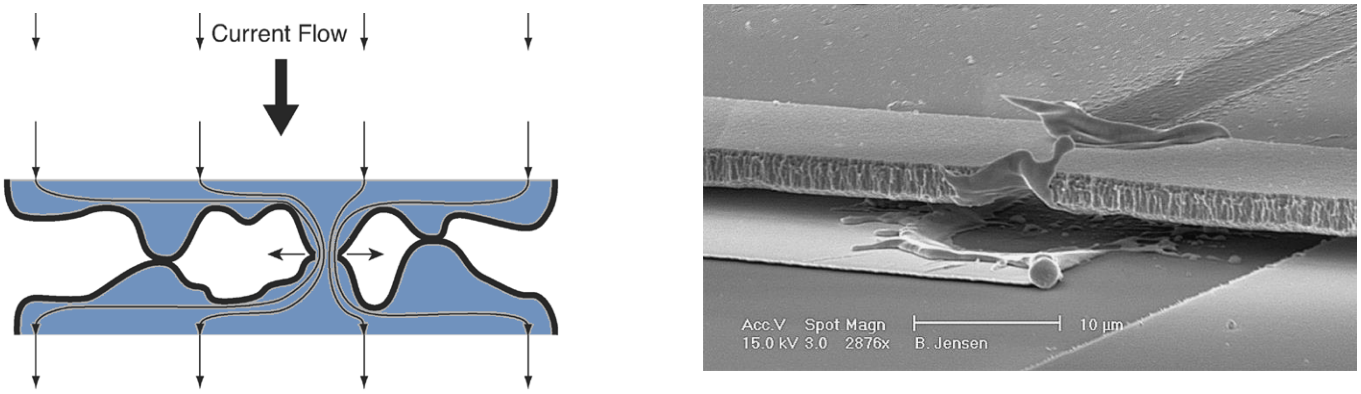

FIGURE 7 EFFECT OF NANO SCALE HEATING AND MELTING OF A METAL CONTACT

As a result of that, the effect on areas is a sum of finite elements at small asperities. The decrease in contact area forces higher current to pass from small asperities. This eventually results in a rise in the temperature at the contact point as the resistance is also increased *[32]*. These concepts of the rise in temperature of the contact point known as nanoscale heating which sometimes causes the melting of a contact point.

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2.1.3 Curl-up of Cantilever due to residue stress

The successful fabrication and reliable operation of micro- structures strongly depend on the sufficiently rigorous understanding of their length-scale dependent and process- dependent mechanical properties. For example, as a popular material for the fabrication of microstructures, polysilicon is typically deposited by low- pressure chemical vapor deposition (LPCVD). The vapor deposition causes either high compressive or tensile residual stress gradients, depending on the deposition process. The existence of residual stress (gradients) causes the change of equilibrium configuration and shifts of the resonant frequency of the microstructures. Residual stress/ strain become a parameter of fundamental importance in micro- structure, thin film, surface micromachining and improving the reliability of micro-devices *[20]*. Tremendous effort has been infused to develop the measurement methods for the built -in residual stress/strain in microstructures. In most of the electrostatic switch designs, the switch is in the form of a miniaturized cantilever beam as shown in Figure 8. When external DC voltage is applied across the driving electrode pair, the actuating electrode is pulled down due to generated electrostatic force. Many times to curled up cantilever the pull-in voltage is dominated by the air gap between two electrodes. The air gap is decided the thickness of the sacrificial layer. One can reduce the height of sacrificial layer to reduce the air gap. This results in lower pull-in voltage. It is the downside of this is poor isolation in all state as the air gap is reduced.

As seen from the figure 9, the residual stress causes the bending of a cantilever beam in an upward direction.

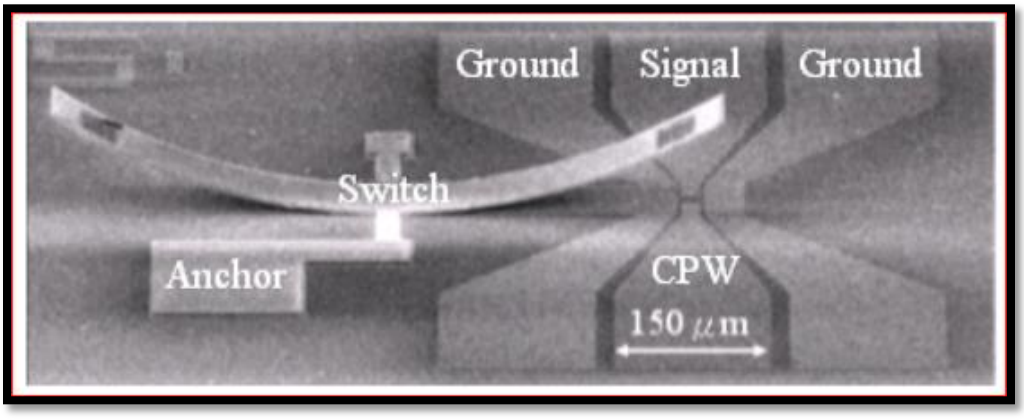


Figure 8 Curled up Cantilever Beam due to stress Gradient

This prompts the change in the predicted pull-in voltage. The altered pull-in voltage can be much higher than the predicted one. The higher pull-in voltage is not desirable as the higher value of the pull-in voltage enhances the possibilities of dielectric charging. As stated by *[22]*, every 5-7 V increase in pull-in voltage degrades the life cycles of a switch by ten times. There are some models has been demonstrated to determine the pull-in voltage and the curvature under the influence of the residual stress. Though the care must be taken to control the residual stress by means of the fabrication process or by the effective geometry of an actuator.

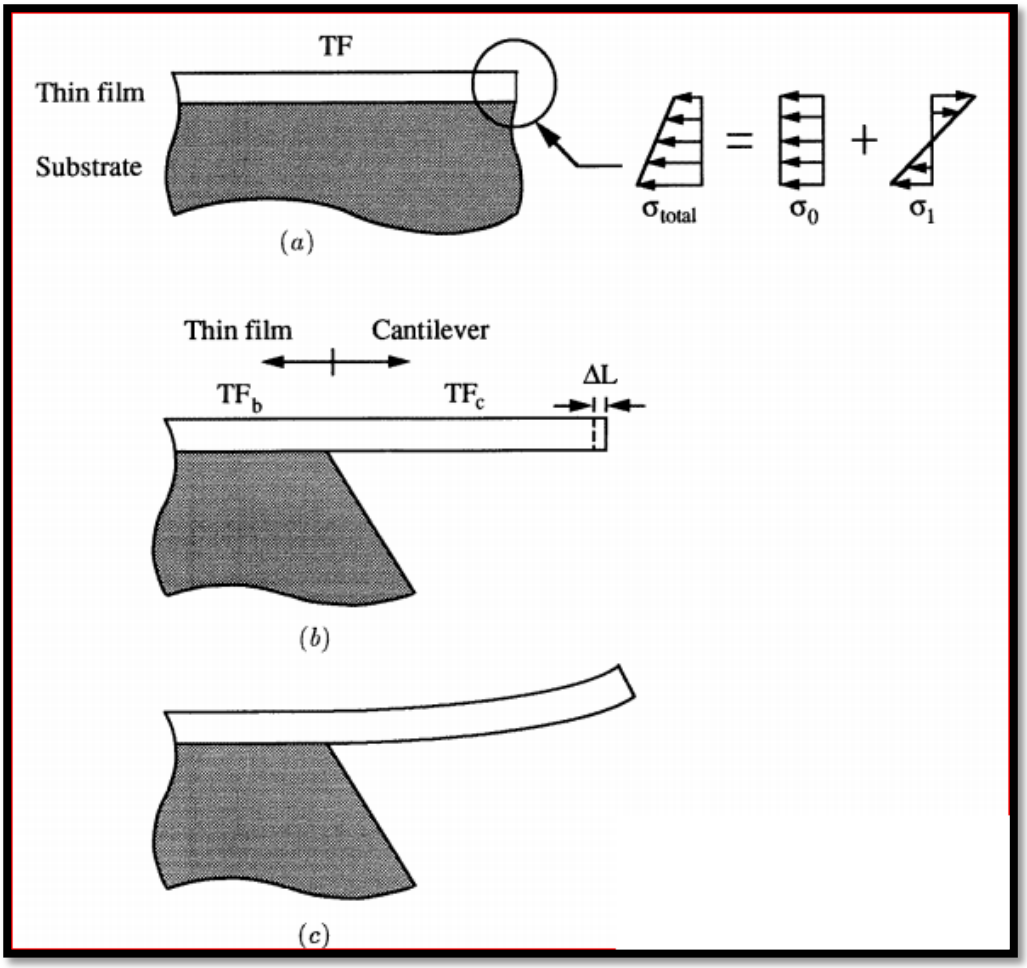


FIGURE 9 SCHEMATIC OF RESIDUAL STRESS AND STRESS GRADIENT

Figure 9 shows the stress profile that causes the curvature in the cantilever beam. As shown in Figure 9(a), the thin film is under the influence of two different stress components before release, (a) General mean stress (b) Gradient stress. The first component of stress prompts the change in the length of a cantilever beam where as other is responsible for the curvature of a cantilever. The

presented thesis solely focuses on the curvature issue in the cantilever based actuator designs. The remedy for the problem is shown as the effective geometry of a cantilever beam.

2.2 SUMMARY

With the development in the RF MEMS Switches across the globe, the research also carried in the field of possibilities of deploying RF MEMS Switches in space application. The key issue to be concerned was the reliability. In August 2005, the project titled ENDORFINS (Enabling Deployment Of RF MEMS technology IN Space telecommunication) was started. The objective of the project was to perform an in-depth assessment of the reliability and related failure modes of RF-MEMS, in view of their deployment in space and improve this reliability (for switches) through processing optimization. As the conclusion of the project, they listed out 18 possible failure modes which were theoretically expected. The table shows the summary of the listed Failure Modes.

TABLE 2 FAILURE MODE EFFECT ANALYSIS

Index	Mechanism	Defect	Failure Mode	Possible Cause
1	Dielectric Charging of the Insulator in capacitive switch	Stiction to the bottom electrode. Not permanent (Charges Flow away when charging cause is taken away)	Drift in CV Curves drift in Pull-in and Pull-out voltages, Dead Devices	Electric field charge injection
				Air-Gap Breakdown
				Electron Emission
				Radiation
2	Micro welding (ohmic switches and capacitive Switches with contact metal on dielectric)	Stiction	Dead Devices, Drift in Contact Resistance, anomalous switching behavior (temporary stiction)	Soft metals coming into contact (cold welding)
				High current through metal-metal contacts (often at asperities) (hot welding)
				ESD
3	T- induced elastic deformation of the bridge	Non-Permanent deformation of the bridge(is restored when T-source is removed) Possibly stiction if large deformation	Shift of electrical parameters(pull-in/pull-out V,capacitance,Contact resistance); Change of mechanical properties	Different Thermal Expansion Coefficients
				Environmental Temperature
				Power RF signal induced
				Temperature
				Non-Uniform temperature repartition
4	Plastic	Permanent	Shift of electrical	Creep

	deformation of the bridge	deformation of the bridge(is restored when T-source is removed) Possibly stiction if large deformation	parameters(pull-in/pull-out V, capacitance, Contact resistance); Change of mechanical properties	Thermally induced changes in material properties (for T > Tc)
5	Structural short (electrical and non-electrical connections)	Particles, shorted metals, contamination, remains of sacrificial layer, Stuck Bridge	Change in Electrical parameter; Dead device	Contamination; Particles; remaining sacrificial layer material
				Wear Particles
				Fracture
				Lorenz Forces
				Shocks
6	Capillary forces	Stiction	Dead Device.	Presence of Humidity (Package leaks, Incorrect release step)
7	Fusing	opens, roughness increase	Dead Device.	High RF Power Pulses, ESD
8	Fracture	Broken Bridges and Hings	Dead Device.	Fatigue
				Brittle Materials + shock
				High local stresses + shock
9	Dielectric Breakdown of the insulator	Possibly Stiction	Short between bridge and actuation electrode.	ESD
				Excessive charging of insulator
10	Corrosion	Dendrites formation, oxidation, changes in color	Degradation of electrical and mechanical properties; shorts.	Presence of water or other fluid (Chemical reaction), enhanced by bias
				Corrosive gasses induced chemical reaction (Ex. Oxidation)
11	Wear; Friction; Fretting Corrosion	Surface modifications, Particles(Debris), Stiction	Shorts, Opens, Shift in electrical parameters.	Sliding Rough Surface in contact
12	Creep	Deformation in Bridge in time	Electrical and Mechanical parameter shifts.	High metal stress and high temperatures creep sensitive metals.
13	Equivalent DC Voltage	Self-biasing Stiction	Anomalous Switching behavior, Changes in electrical parameters.	High RF inducing spontaneous collapsing or stiction of mobile part
14	Lorenz Forces	Self-biasing Stiction	Anomalous Switching behavior, Changes in electrical parameters.	High RF power in two adjacent lines
				External magnetic field
15	Whisker Formation	Bumps in metal, holes in insulator on the top of the metal layers	Anomalous down capacitance or a contact resistance possible increase of charging sensitivity.	High Compressive stress in metal resulting in grain extensions, might be enhanced by T-step

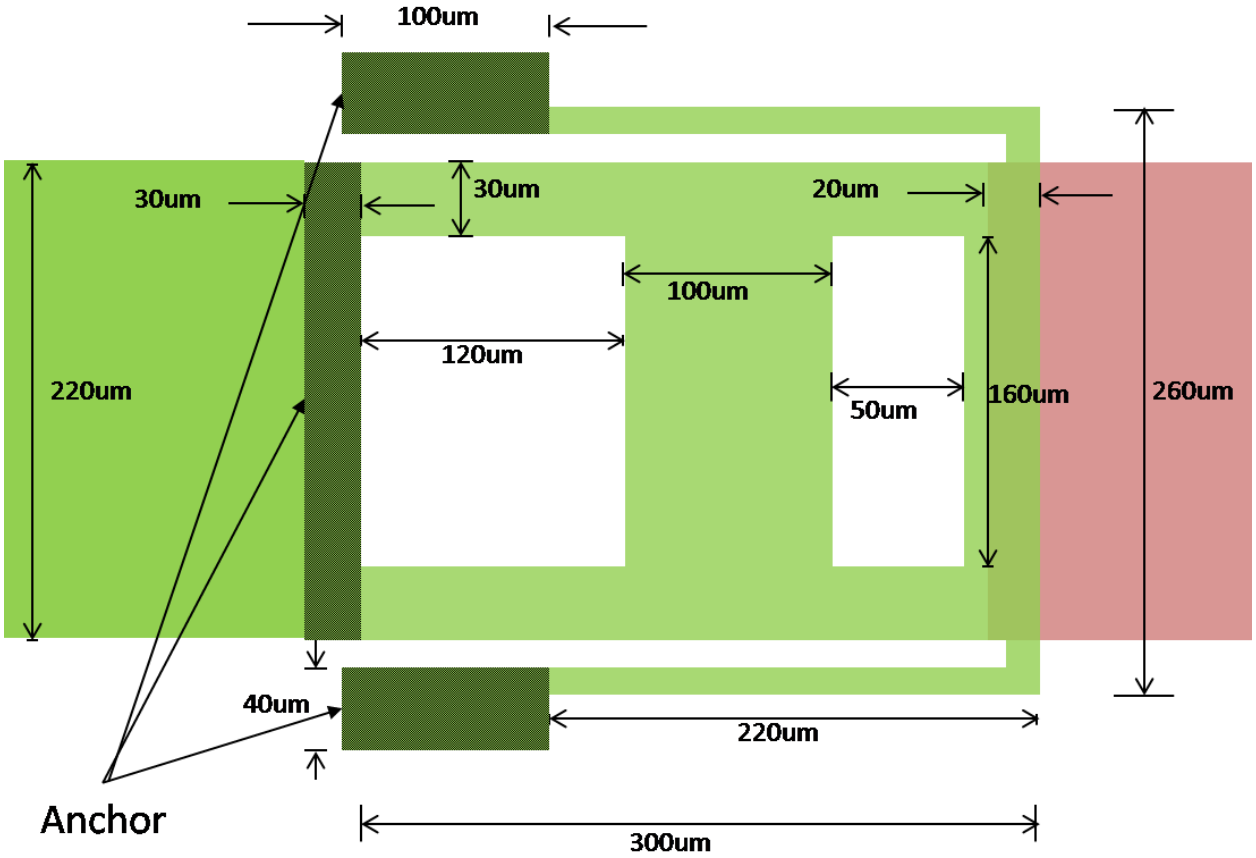
16	Fatigue	Broken Bridges and Hings, Cracks, microcracks, deformation of bridge	Electrical and Mechanical parameter shifts; Dead Device.	Local stresses variations due to the motion of parts (intended or due to vibrations and thermal cycles). Enhanced probability if cracks are present of the surface is rough.
17	Electromigration	Cracks, Opens, thickness changes (mass transport) in metal lines	The increase of resistance, opens, shorts.	High current density in metal lines enhanced by too thin and/or narrow lines and steps.
18	Van der Waals Forces	Station	Dead Devices.	Large very smooth and flat surfaces in close contact.

3 Design of an Actuator

The Chapter accounts proposed design starting with the geometry of proposed design. Following chapters comprises of Mechanical analysis of an actuator and RF Analysis of designed SPST, SPDT and SP4T Switches. The Presented chapter aimed at Switch Matrices. Starting with the working principle and application of the Switch matrices, the chapter includes design of T-Type and C-Type Switch matrices and their simulated response.

3.1 Design of an Actuator

As discussed in Chapter 2.1, reliability is the main concern for the potential use of the RF MEMS Switches. Here the proposed design of an actuator is illustrated. The design was proposed with the concern of a curvature issue of a cantilever beam due to residual stress. The proposed design is tethered based. The tip (free end) of a cantilever beam connected with tethers and anchored to the base. In such a way we can somehow control the uplifting of a free end of a cantilever beam. Figure 10 shows the top view and cross-sectional view of a proposed design of an actuator.



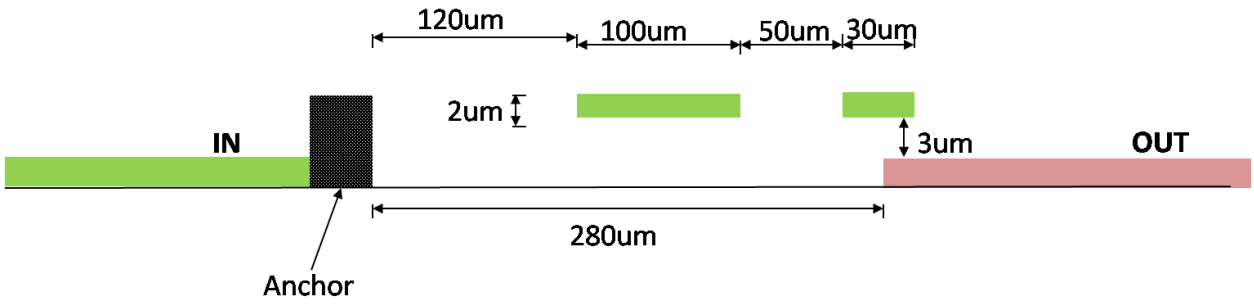


FIGURE 10 DIMENSIONS OF AN ACTUATOR

The width of an actuator is kept 220um to match the characteristic impedance of 50Ohm as per the coplanar waveguide standards. The design parameters are listed in Table. Here an actuator is designed with two open windows. The reason for that is, an open window effectively reduces the mass of a hanging structure. This enhances the speed of vertical movement which results in enhanced switching speed. The pull-in voltage also decreases with the reduction in overall mass. The open near the anchor (160*120 um^2) is made for a specific set of purposes. Inherently it reduces the overall mass of a structure. Prior to that, it decreases the effective mechanical spring constant of the cantilever beam. As shown in the Equation, the pull-in voltage will decrease with a decrease in the mechanical spring constant. The mechanical spring constant of a cantilever beam is directly proportional to the width of the structure. By making an open window at the anchor end, we are reducing the effective width of a cantilever.

TABLE 3 DIMENSIONS OF AN ACTUATOR

Design Parameter	**Value**
Cantilever Width	220 um
Cantilever Length	300 um
Tether Width	10 um
Tether Length	220 um
Tether Anchor Area	40*100 um^2
Window(#1,#2) Width	160 um
Window #1 Length	120 um
Window #2 Length	50 um
Separation between Windows	100 um

++Area of an Actuation Pad	280*120 um^2
Air Gap	3 um
Overlap Area	220*20 um^2
Thickness of a Cantilever Beam	2 um

The area of an anchor for the tether is kept somewhat large(40*100 um^2). It is to ensure the enough stiction force even after the release of a hanging structure. The overlap area between hanging actuator and underneath transmission line is 20*220 um^2. The overlap area is the key factor for controlling the Isolation. Larger the overlap is, the large will be the value of capacitance. The larger value of capacitance boosts the capacitive coupling in Off State and decreases the RF Performance (in particular Isolation). On another hand, smaller contact area will limit the transfer of a power from an actuator to underneath transmission line in ohmic metal contact switch. So the Overlap area is one of the key design parameters. There will be a trade-off between Isolation and Insertion Loss with respect Overlap area. Another key parameter is Air Gap. The air gap is the amount of distance by which the free end of an actuator and the underneath transmission line are separated. The higher will be the gap, the better will be the Isolation in Off state. But the higher value of Air gap also reflects the value of pull-in voltage. The pull-in voltage increases with increase in the Air gap. This is not desirable. The higher value of pull-in voltage, in turn, boosts the possibilities of dielectric charging as discussed earlier. So there is also a tradeoff between the better Isolation and desired value of a pull-in voltage regarding the Air gap.

3.2 Mechanical Analysis

The mechanical of an actuator is carried out to determine the pull-in voltage and the fundamental resonating frequency of a structure. As discussed earlier, the pull-in voltage is a one

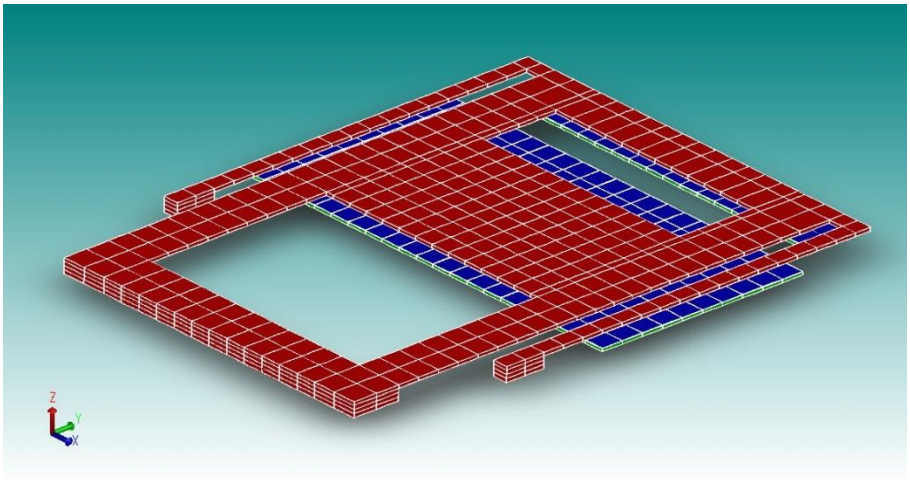


Figure 11 3-D View of an ACTUATOR

the key parameter determining the mechanical performance of a Switch. Adding to that, the fundamental resonating frequency shows the switching speed of a switch as it is the measure of how fast an actuator can move in a vertical direction. The mechanical analysis was carried by FEA Tool (Finite Element Analysis) CoventorWare. Figure 13 shows the 3D structure of the proposed design implemented in CoventorWare. The part in red color is proposed actuator design.

For the test setup, an assembly of the conductive layer and the dielectric layer is formed to serve the purpose of an actuation and sensing. The part in green color is a conductor with the thickness of 1.4 um. And the part in blue color is a dielectric layer with the thickness of 0.6 um. The area of an actuation pad is kept 120*280 um^2. The analysis shows the fundamental resonating frequency of the structure to be kHz. The actuation voltage versus deflection in cantilever beam is shown in the figure. For an air gap of 3um, the pull-in voltage found to be V. The rapid decrement in the air gap is seen after the height of air gap decreased to 0um. This simulated result supports the analytical result derived in Eq. The result is shown for the optimized design structure.

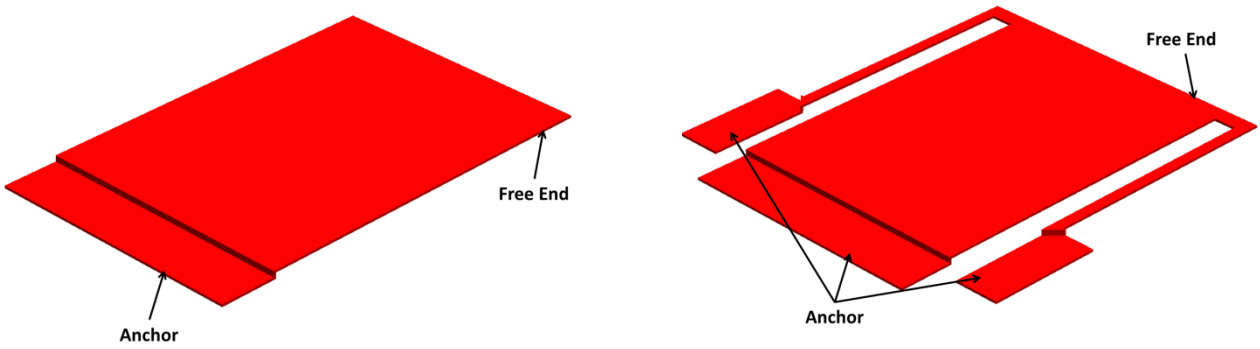


FIGURE 12 SIMPLE CANTILEVER AND TETHERED CANTILEVER

The optimization approach is as followed. As explained in the earlier chapter, the cantilever beam tends to curved up due to stress gradient generated during the fabrication process. The simple logic to restrict the curvature is to tie the free end of a cantilever beam to anchor support plane. A material used for a beam is Gold. The properties of the Gold material are shown in the Table. In spite of having almost same conductivity and thermal properties, the Gold is chosen over Copper due to its higher skin depth.

TABLE 4 PROPERTY OF GOLD

Density	1.93E-14 (kg/um^3)

TCE Integral Form	1.41E-05 (1/K)
Thermal Conductivity	2.97E+08 (pW/um K)
Specific Heat	1.287E+14 (pJ/kg K)
Electrical Conductivity	4.40E+13 (pS/um)

As shown in the figure 13 the free end is tethered and anchored to the support plane. The pull-in voltage of the tethered beam is shown in figure 13.

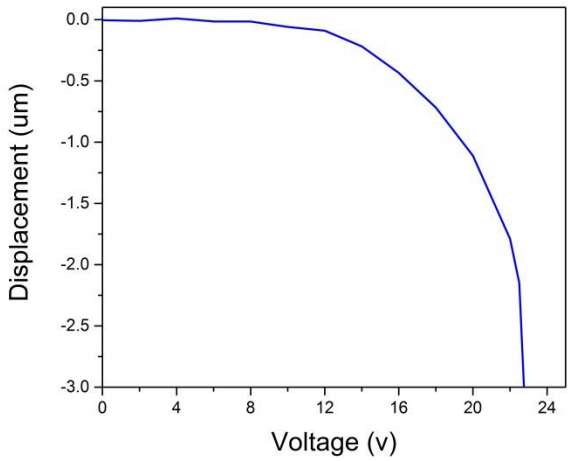
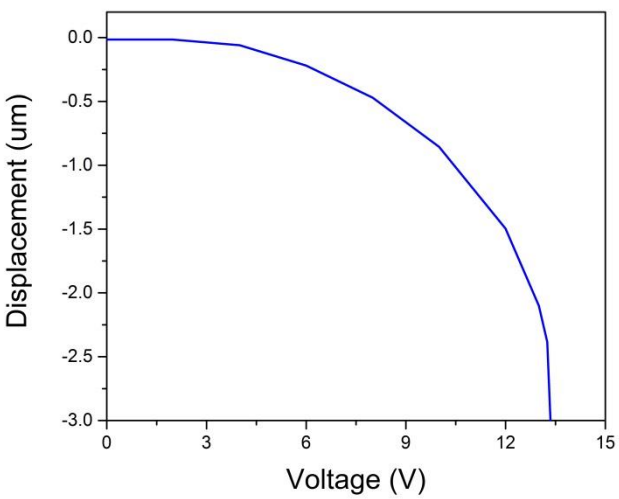
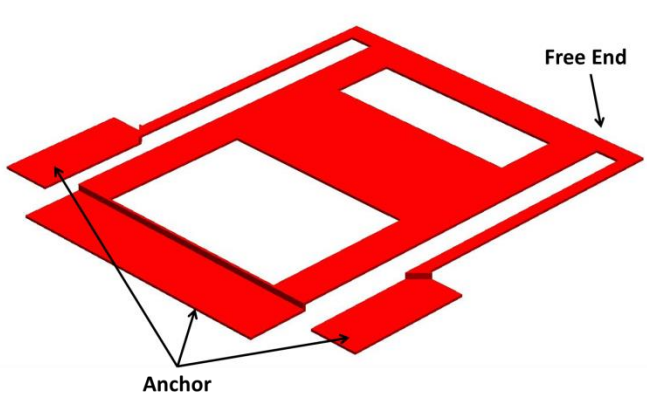


FIGURE 13 PULL-IN VOLTAGE WITHOUT WINDOWS

Pull-in voltage for the tethered beam is calculated using FEA Tool (CoventorWare). The simulation results show the pull-in voltage in the range of 22.5-22.75 V. This is quite higher than the accepted range. A Higher value of pull-in voltage affects the life cycles of the device as discussed earlier. To diminish the pull-in voltage two window openings are formed in the beam. The window at a free end effectively reduces the overall mass of the beam. Whereas the second window at the anchor

FIGURE 14 PULL-IN VOLTAGE WITH WINDOWS





end effectively reduces the spring constant of a beam. The separation between the windows is managed such a way that, the window openings do not overlap the area of an actuation pad. The geometry is shown in figure 14. The pull-in voltage for the new design is found to be 13.25-13.35 V.

3.3 RF Analysis

The RF (Radio Frequency) analysis of the proposed design is carried out to evaluate the RF performance. For an FEA RF analysis HFSS, 15.0(High-Frequency Structure Simulator) software tool was used. Basic switch design for the RF analysis comprising the proposed actuator is shown in the figure. Here the actuator is clubbed with the input transmission line. And the underneath transmission line serves the purpose of the output transmission line for the basic structure. The

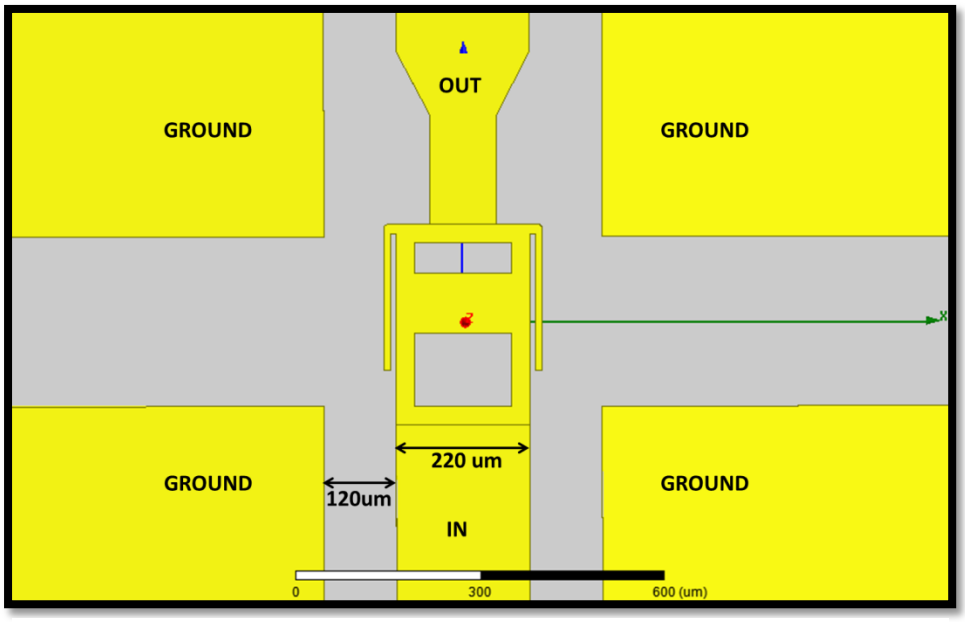


Figure 15 RF Analysis Setup

Coplanar Waveguide is formed around the basic switch configuration. The separation between the central conductor and ground planes is set to 120um. This is in order to match the impedance of coplanar waveguide with the characteristic impedance of transmission line that is 50ohm. The whole 120um/220um/120um coplanar waveguide configuration is formed using Gold. The thickness of all the parts of Gold is kept 2um. The metal assembly is formed on the 1um thick Silicon dioxide (SiO_2) layer. Here Silicon dioxide layer serves as a dielectric layer to diminish the parasitic effects. Above described assembly is formed on the top of the Silicon substrate of 275um thick (Standard thickness of 2inch wafer). The underneath transmission line is tapered in shape as can be

seen from the figure. The reason for that is discussed in next subsection. Teflon connector is also modeled at the input and output port of the switch. The connector is modeled by placing the cylindrical perfect conductor in the center of a hollow Teflon cylinder. Using the basic configuration of the switch shown in Figure, the varieties of switch configurations are designed including SPST (Single Pole Single Throw), SPDT (Single Pole Double Throw) and SP4T (Single Pole Four Throw). In the presented design, the ON state and OFF state is achieved by the short-circuiting and open circuiting the metal contact respectively hence called Ohmic metal contact series switch.

3.3.1 SPST

As the name suggests SPST is the simplest kind of configuration among the present Switches. The structure is consisting of two ports. Any one of them can be used to the incident the RF power. The switch has simply two working modes (a) On State in which two port are short-circuited and (b) Off State in which two ports are open circuited. The geometry of the switch is shown in Figure 16.

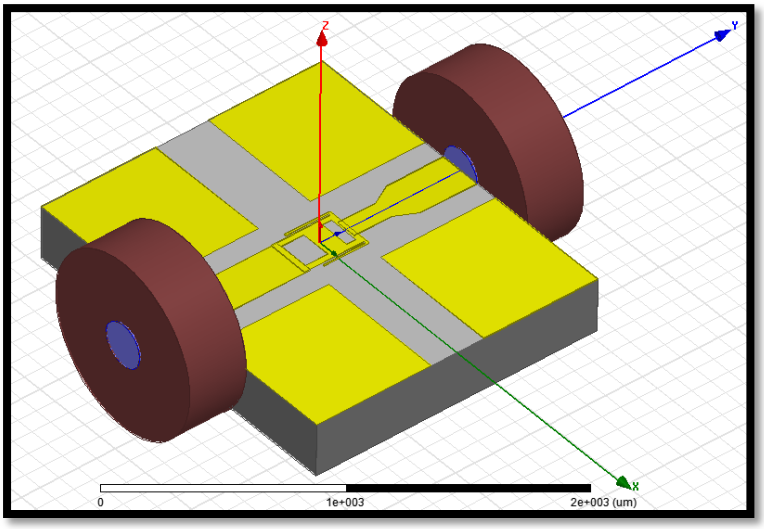


FIGURE 16 SPST CONFIGURATION

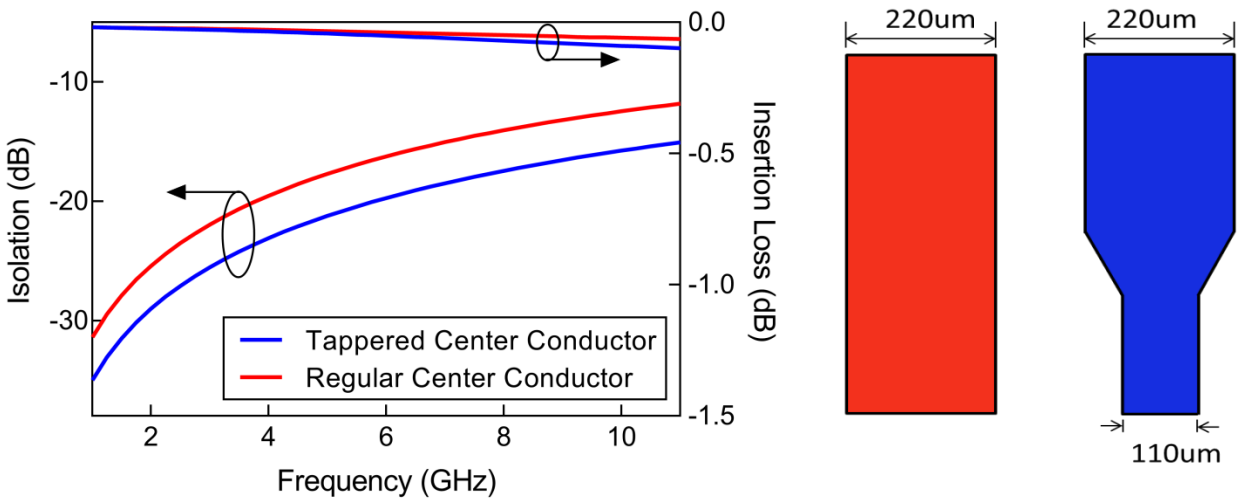


FIGURE 17 RF RESPONSE FOR TAPERED AND RECTANGULAR CENTRAL CONDUCTOR

As Shown in figure 17, the underneath transmission line has the tapered shape rather than conventional rectangular shape. The reason behind that is simple. The tapered shape at the tip of an underneath transmission line effectively reduces the overlap area. The reduction in overlap area reduces the Off state capacitance. Thus the performance in Isolation is achieved. In figure 17, the Insertion Loss and Isolation loss plotted for the SPST with both the shape of an underneath transmission line. The comparison shows the ~3.5dB enhancement in Isolation. The design demonstrates the Insertion loss of -0.0413 dB and Isolation of -21.607 dB at 4.75GHz. The same design exhibits the Insertion loss of -0.0824 dB and Isolation of -15.712 dB at 10GHz.In all the following structures the same configuration is used resulted during the optimization process.

3.3.2 SPDT

The SPDT configuration is the somewhat modified version of the SPST switch. Comparing to SPST switch it has two output port rather than one in SPST. The input RF signal can be routed to the any of the paths among two available paths. The SPDT switch is made of two hanging structures (Actuators).

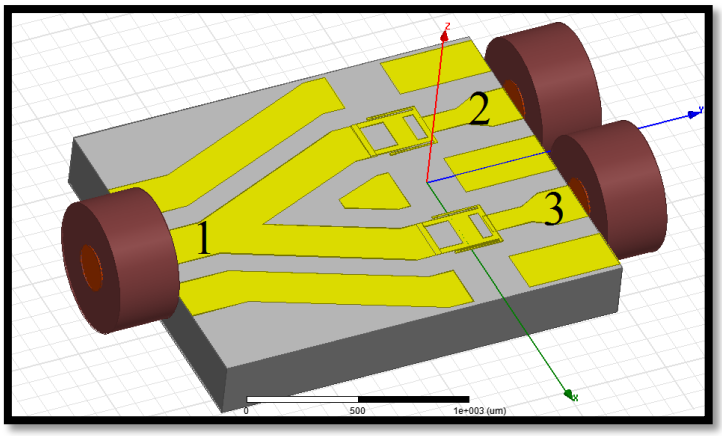


FIGURE 18 SPDT CONFIGURATION

The configuration of the SPDT switch is shown in Figure 18. The separation between two output transmission lines is kept 480um. The RF response of the SPDT is shown in figure 19. In the response, the port 1 and port 2 are short-circuited (Insertion Loss) whereas port 1 and port 2 are open circuited (Isolation).

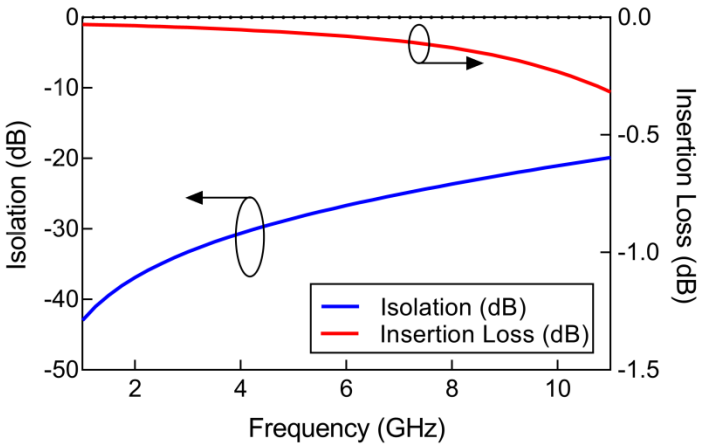


FIGURE 19 RF RESPONSE OF SPDT

Here the response for the toggled mode (port 1 and port 2 are open circuited and port 1 and port 3 are short-circuited) will be same as the geometry of the switch is completely symmetric respect to both output ports. The design demonstrates the Insertion loss of -0.0682dB and Isolation of -29.0495 dB at 4.75GHz. The same design exhibits the Insertion loss of -0.2829 dB and Isolation of -21.152 dB at 10GHz.

3.3.3 SP4T

The SP4T is more complex structure than the above-explained devices. In return, it offers the more flexibility in operating states. As the name suggests, SP4T configuration comprises of one input port and four output ports. For the shake of symmetricity, the configuration is designed in a pentagon shape, where each of five transmission lines (one input and four outputs) are separated to each other by 72°. The configuration of the SP4T switch is shown in figure 20.

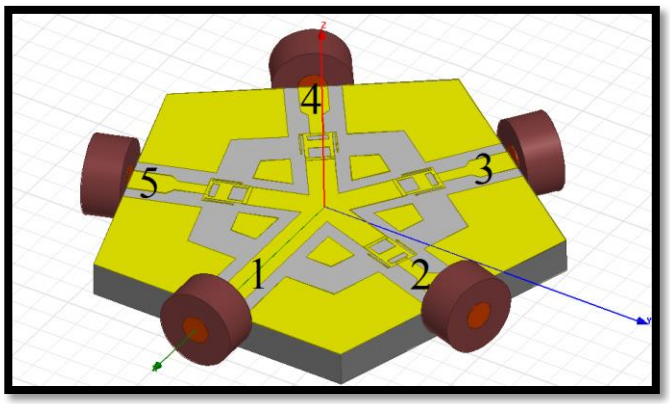


FIGURE 20 SP4T CONFIGURATION

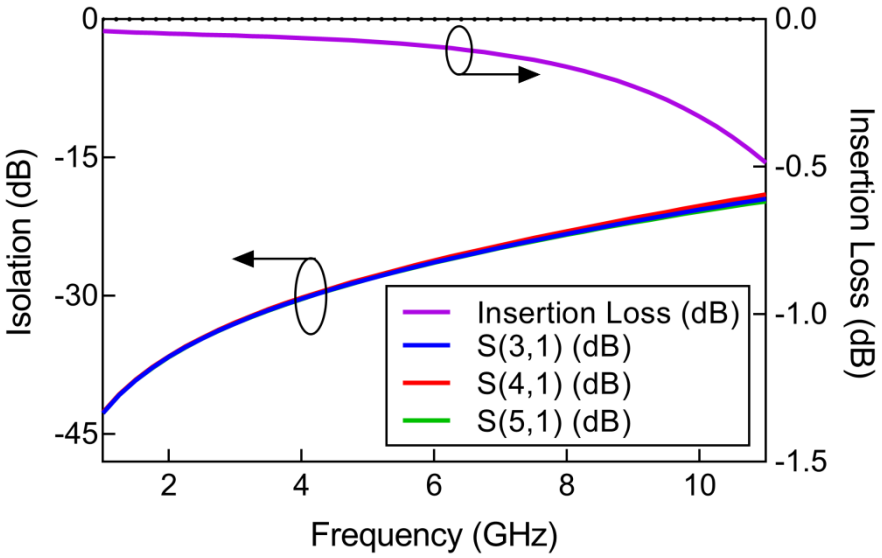


FIGURE 21 RF RESPONSE OF SP4T

The SP4T switch is made of four hanging structures (Actuators). Here it can be seen that with an increase in the flexibility of the operation, the number of the hanging structures are also increased in the configuration. A Higher number of hanging structures prompts the issue of reliability. The degradation in the Insertion loss can also be noticed with increase in the number of hanging structures from SPST to SP4T.The RF response for the SP4T configuration is shown in Figure 21. Here port 1 and port 2 are short-circuited. Port 1 is considered as an input port of the switch configuration. All other ports than the port 2 are isolated from the input port one. Due to the symmetricity in the structure, the Isolation between different ports and port 1 is found to be almost identical. The design demonstrates the Insertion loss of -0.0838 dB and Isolation of -28.873 dB at 4.75GHz. The same design exhibits the Insertion loss of -0.3586 dB and Isolation of -20.829 dB at 10GHz.

3.4 SWITCH MATRIX

The Presented sub-chapter aimed at Switch Matrices. Starting with the working principle and application of the Switch matrices, the chapter includes the design of T-Type and C-Type Switch matrices and their simulated response.

3.4.1 WORKING PRINCIPLE AND APPLICATION

Working Principle

In satellite payloads; switch matrices are formed by integrating hundreds of switch to serve the purpose of providing system redundancy in case of failure. For implementing switch matrices, C-type, R-type, and T-type switches are basic building blocks. Satellite communication systems also rely on switch matrices to provide system redundancy and to enhance the satellite capacity by providing full and flexible interconnectivity between the received and transmitted signals. Switches can be seen as a Combination of interconnected Switches which are made to provide more flexible connections. The structure is a kind of multiport configuration with different operating states according to the active conducting path. As mentioned above, the three basic building blocks of the switch matrices differ each other by means of their operating states. Each type of switch provides a different combination of conducting paths. Let's have a brief overview of such building blocks.

C-Type

The C-Type of the switch can be viewed as the 2 X 2 matrix. It is a four port structure having two operating states. The schematic of the C-Type switch is shown in Figure 22. In State, I, Ports 1 and 2 and Ports 3 and 4 are connected. In State II, Ports 1 and 4 and Ports 2 and 3 are connected. Due to its working operating states, the C-Type switches often termed as 'Transfer Switch'. The C-Type switch is the basic one among the switches used for switch matrices. Hence it requires more number of switches to build redundancy switch matrices.

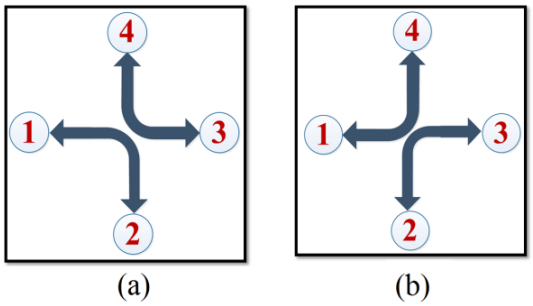


FIGURE 22 MODES OF C-TYPE

R-Type

The R-type switch has three different operational states, as shown in Figure 23. In State I, R-type switch offers one more operating state compare to the C type switch. This addition the

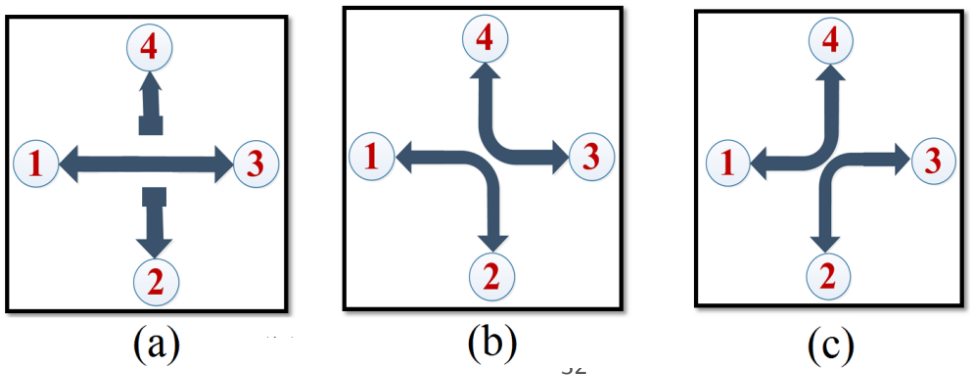


FIGURE 23 MODES OF R-TYPE

operating state adds up the flexibility and simpler network topology. In the additional state, R-type switch offers a connection between port i and iii. Other ports ii and iv are remained isolated during this state.

T-Type

The T-type switch is the evolved version of the C-type or R-type switch. It alters three operating states with six different conducting paths. Due to the increased number of the path, it provides more flexibility and higher simplicity in the network topology. In an additional operating state other that C-type and R-type ports (i) and (iii) are connected and the ports (ii) and (iv) are

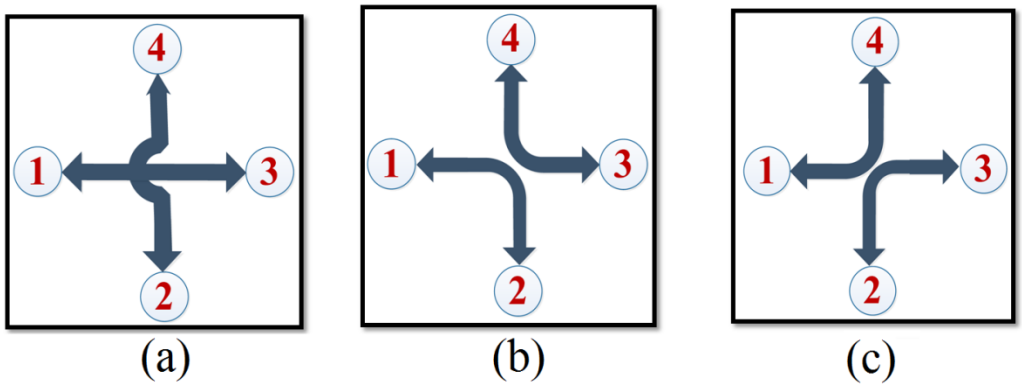


FIGURE 24 MODES OF T-TYPE

connected with this addition the T-type offers great simplicity in remaining switch matrices.

Applications

The above-mentioned Switch Types are widely used in the Switch Matrices as building blocks. Switch matrices are widely used to provide system redundancy in satellite payloads. The more flexible the configuration is, the less dense the switches will be to implement the switch matrices. The higher operating states also provide simply in the topology to form a redundancy matrices. Let's consider a topology where 5 amplifiers are connected in 5 different RF power lines. Now assume a scenario where any of the amplifiers start malfunctioning or faces permanent failure. In such case(s), the redundancy switch matrices are used. The switch matrices re-route RF signal for hassle free functioning. Implementation of such switch matrix with two spare amplifiers using a C-Type switch is shown in Figure 25.

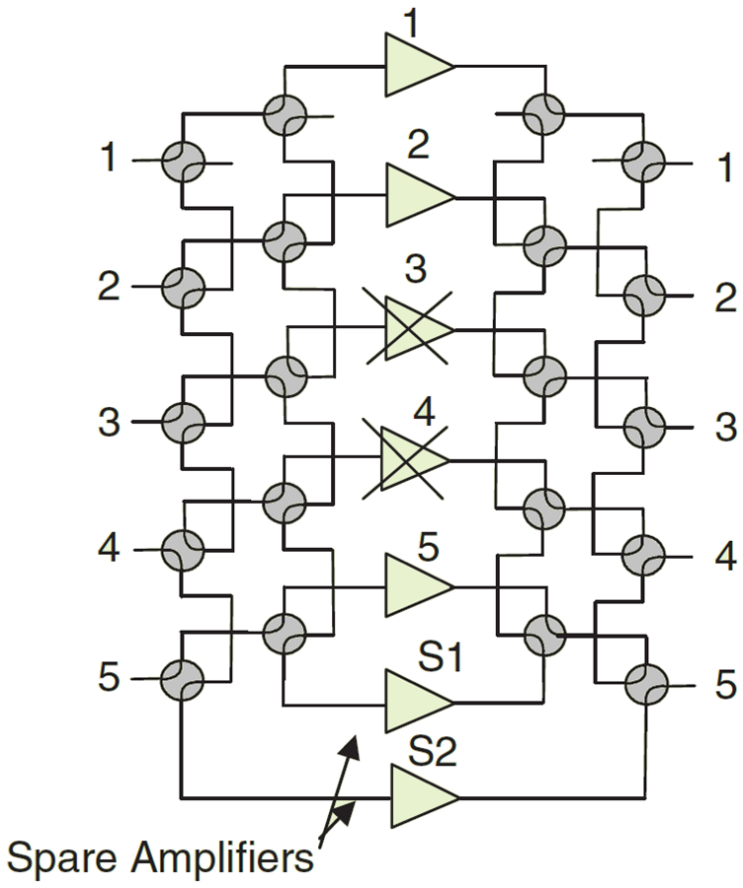


FIGURE 25 REDUNDANT MATRIX USING C-TYPE

As shown in figure 25, the switch matrix consist of seven amplifiers with two of them is spare-amplifiers. As the transfer switch provides two operating states it requires 20 such switches to form a redundancy matrix for the given topology. The higher number of switches leads to the dense and complex implementation. Moreover, as stated before, the switch is consisting of two parts: (a) Mechanical part and (b) Electrical part. The mechanical part comprises an actuator. The actuator is most probably the hanging structure in the configuration. The higher number of hanging structures eventually reduces the reliability as the chance of failure increases with that. So the key design consideration is to use as less hanging structures as one can. The problem will be solved if we use a different kind of switch configuration that provides more flexible connectivity than the C-Type switch. This will eventually reduce the density of switches and the complexity of the topology. Here in Figure 26, we have implemented the redundancy matrices with the same topology using T-Type switches. It can be seen that the same topology is implemented using 10 T-Type switches. The reason for that is comprehensive, as T-Type Switch provide one extra cross conducting state. It makes implementation simpler and less dense. Here S1 and S2 represent the spare amplifiers.

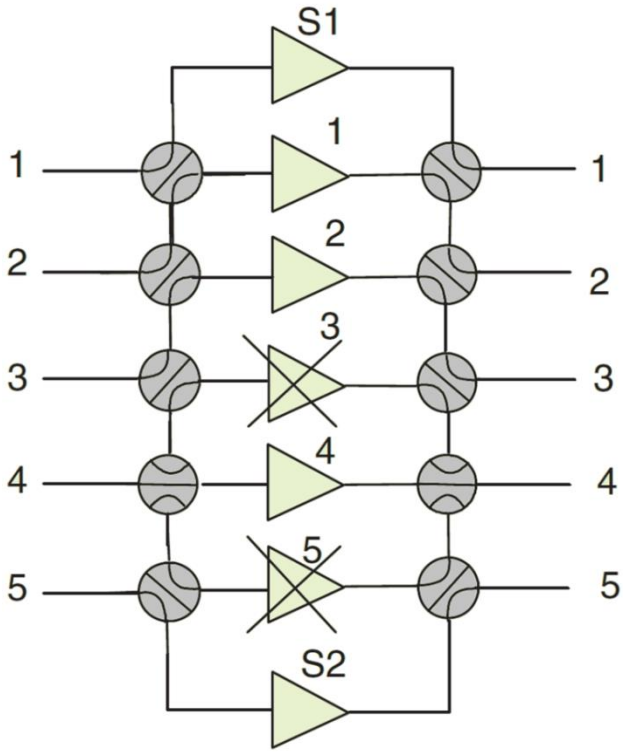


FIGURE 26 REDUNDANT MATRIX USING T-TYPE

3.4.2 T- TYPE

As explained above T-Type switches gives more flexible operating states comparing to the C-Type and R-Type. The major difference b/n all these three switch configurations is the number of conducting paths. The C-Type and R-Type offer four and five conducting paths respectively. Whereas the T-Type configuration offers the maximum number of conducting paths that are six! A Higher number of conducting path requires more area for the obvious reason. Moreover, the hanging structures also increase with the number of conducting path as a part of the actuation mechanism. This is a price you pay in T-Type switches in return of flexibility of conducting path.

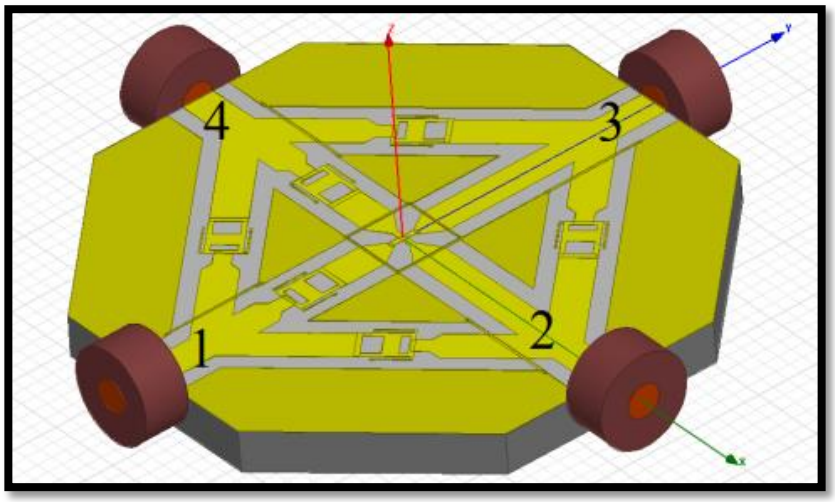


FIGURE 27 T-TYPE USING 6 SWITCHES

Here a T-Type switch proposed using the basic tethered based actuator is shown in figure 27. The first design is proposed using six actuators. The RF response for the states shown in figure 28.

It is noticed from the response that the Isolation response for state II is non-uniform. This is because of the de-symmetricity of the structure. The proposed design is made using only 6 hanging structure instead of 8 in [REF]. The RF response of the structure is not predictable as it depends on the number of distributed electrical parameters having the different values according to the geometry of the structure. The symmetricity costs in the number of hanging structures in the design. The same design is implemented in a symmetric manner with two additional actuators as shown in figure 29.

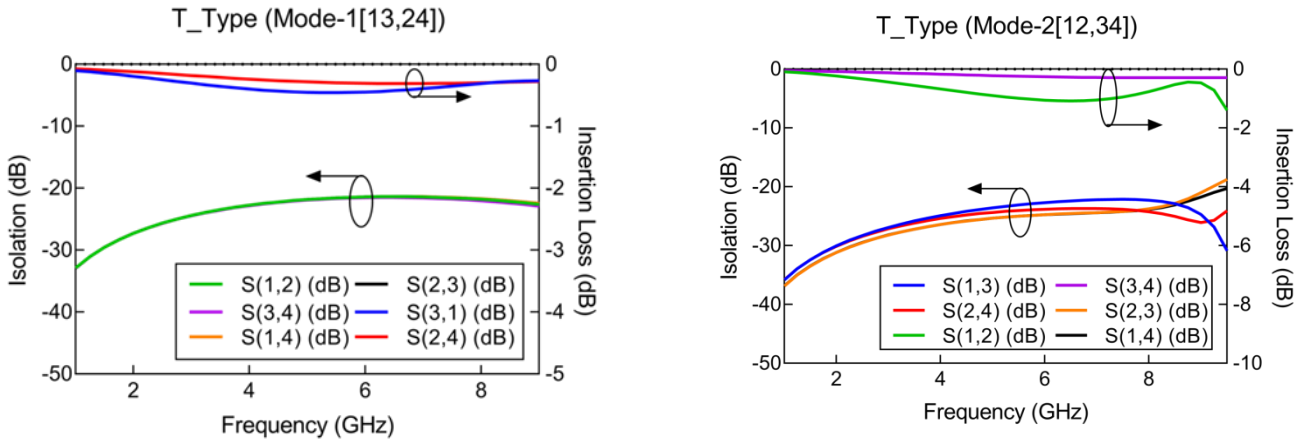


FIGURE 28 RF RESPONSE OF T-TYPE

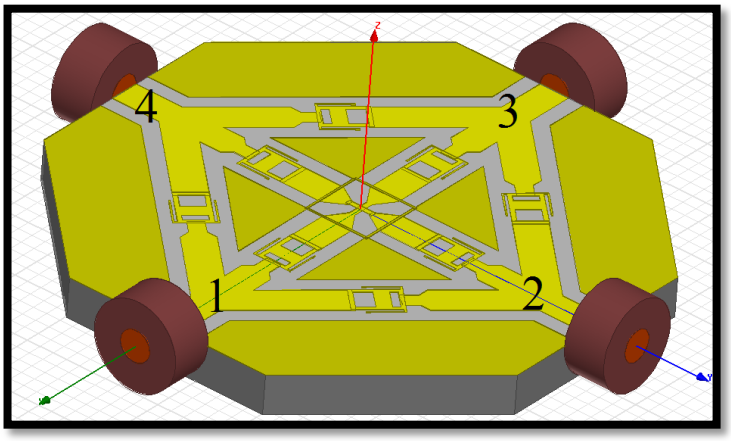


FIGURE 29 T-TYPE USING 8 SWITCH

Due to geometrical operating symmetry, the RF response for the operating states, I and III are identical as per the simulated results of new design. The RF response is shown in figure 30. There are some points to be observed in an RF response.

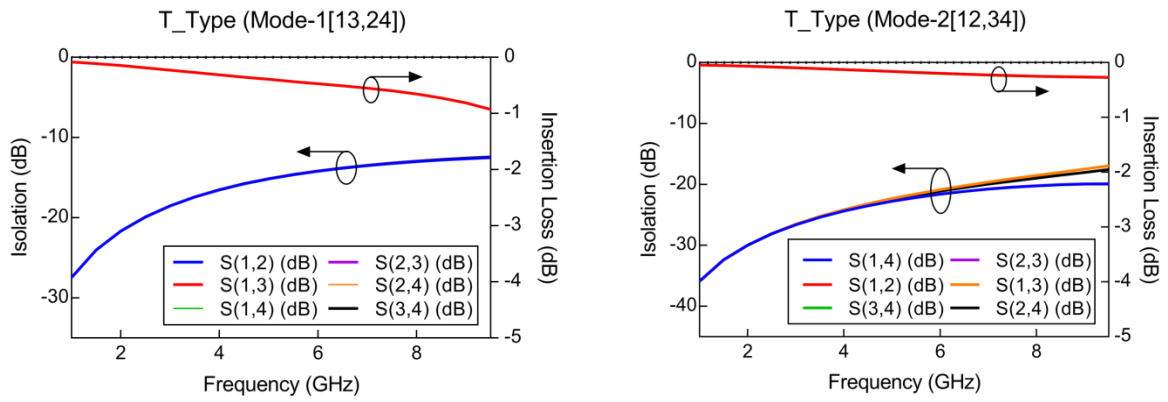


FIGURE 30 RF RESPONSE OF T-TYPE

As we can see that, Isolation performance is poorer than of a de-symmetric structure. The increased number of actuators (hanging structures) not only cost in terms of reliability. It causes a physical nonuniformity in the conducting path. Such non-uniformities boost the fringing fields at the edges of the structure. That eventually results in poor isolation. Another observation can be made in insertion loss. The symmetric structure offers the poor insertion performance in the state I comparing to the de-symmetric structure. The reason can be given as below. A conducting path of state I in the asymmetric structure comprises of only one ohmic contact switch as can be seen from the figure 30. Whereas in a symmetric structure, the conducting paths in the state I are comprises of two ohmic contacts (actuators in down state) in series. An increased number of series ohmic contacts raise the series resistance. The effect of increased resistance is reflected in Insertion performance loss in the symmetric structure. In numbers, the symmetric structure offers the Insertion loss of -0.96dB and Isolation of -12.26dB in the state I at 9GHz. On another side, the de-symmetric structure offers the Insertion loss of -0.18dB and Isolation of -21.23 dB at 9GHz.

3.4.3 C-TYPE

The C-Type switch offers the four different conducting paths during the operation. At a time, a port is connected to only single other port in an operating state. The behavior of the operating states displays the toggling property of the C-Type Switch. Use of such property is excellently demonstrated in by means of geometry.

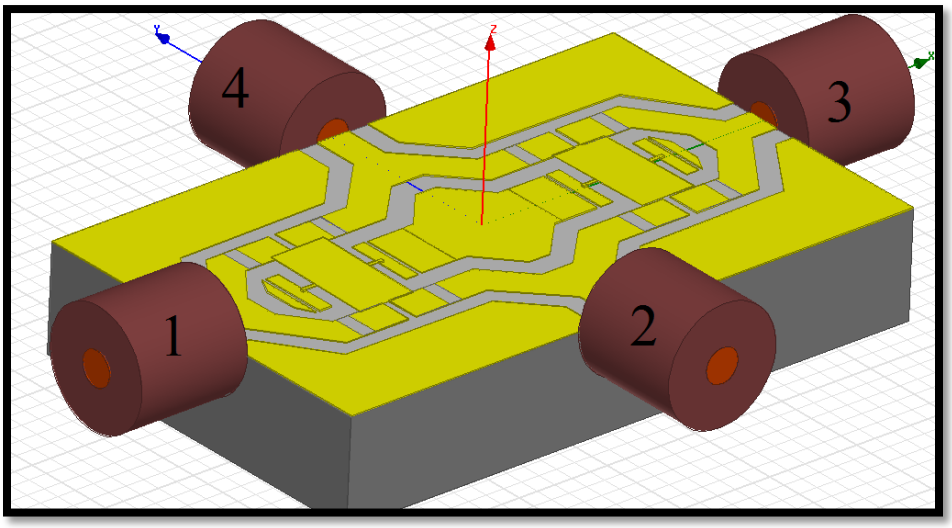


FIGURE 31 C-TYPE SWITCH

The SPDT switch demonstrated in consists only one hanging structure. The toggling between the conducting paths is performed using the torsional bridge. Continuing with the further modification the C-Type switch is implemented as shown in figure 31. The implemented C-Type switch consists of two torsional bridges. The use of least number of hanging structure in the implementation pushes the reliability to a higher extent. The RF response for the C-Type switch is shown in figure 32.

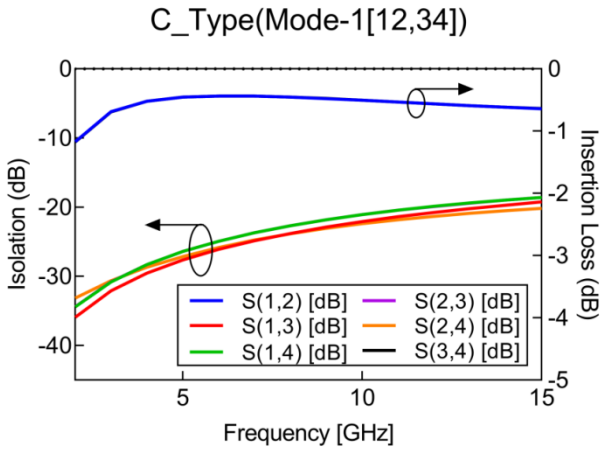


FIGURE 32 RF RESPONSE OF C-TYPE

The response of state II is identical to the response of state III due to geometrical symmetricity of conducting path in both the modes. The structure offers the isolation of -20.06dB and insertion of

-0.62dB in the state I at 15GHz. The least number of the hanging structure is the key fascinating design concept for the proposed C-Type switch.

4FABRICATION OF A DESIGN

The chapter describes the development procedure for the proposed design. Explanation starts from the mask making navigating to the process steps for the fabrication.

4.1 5 MASK PROCESS

The Fabrication of the all the ohmic switches(SPST, SPDT,SP4T,T-Type asymmetric) is planned in such a way that a common process flow can be followed for all the configurations. The fabrication process involves the 5 mask lithography. All switch configurations are divided into five parts: (i) Actuation Pad, (ii) Actuation Pad Window, (iii) Underneath Transmission line, (iv) Sacrificial Layer(Spacer) and (v) Transmission line and Actuator. Starting with the Silicon wafer the first step is to thermally grow an oxide layer of 1um on the surface to diminish the parasitic effect. Then the deposition and patterning of actuation pads are carried out. The deposition of 0.6um polysilicon layer is done by LPCVD process. The diffusion is carried out for the doping purpose to increase the conductivity. After the sheet resistivity measurement of the polysilicon layer, the patterning of is carried out by lithography and etching (RIE). The lithography is done using mask#1 for actuation pad.

After the actuation pad formation, the next step is to cover actuation pad and lines with Silicon dioxide for isolation purpose and make windows at actuation pads for the external electrical connections. These pads are supposed to be used for probing purpose during electrical measurements. The layer of 0.4um thick silicon dioxide is fabricated by PECVD process. After that, the patterning process is carried out by lithography using mask#2 followed by RIE of a silicon dioxide. The role of mask#2 is to pattern windows on isolation layer for the external electrical connections.

After pad windows, the next step is to fabricate underneath transmission lines. All the transmission lines are fabricated using Gold. For gold deposition, electroplating technique is used. For electroplating, a thin layer of Cr/Au (20/70 nm) is deposited first by DC sputtering for the purpose of the seed layer. The lithography process is carried out using mask#3. Following to that electroplating is carried out to deposit 2um thick gold (Au) layer.

After that, deposition and patterning of the spacer are done. The spacer is used as a sacrificial layer. For spacer, HIPR material is used. Sacrificial layers are key aspects in the fabrication of hanging structures. After the deposition and patterning of the spacer, the layer for the hanging structure is deposited. And after that, the spacer material is removed. For the present process, 3 um thick layer of the spacer is deposited. The sacrificial layer serves as a base for the cantilever beam. The patterning of the sacrificial layer is done by mask#4.

After the patterning of the spacer, the deposition of remaining structure is carried out. The remaining last structures are hanging bridge with ground planes and transmission lines. All mentioned structures are meant to be made by gold. The deposition of the gold layer is done by an electroplating process. The thickness of the gold layer is kept 2um. Patterning of a gold layer is done using mask#5. As discussed till now, 5 masks are developed for all the configurations to serve the specific purpose. Some improvements are carried out during mask designing process. That includes sorting of ground planes and making bumps underneath the transmission lines at contact point for the desirable contact asperities. The graphical representation of fabrication flow is shown in figure 33. The summary of a process step is shown in Table.

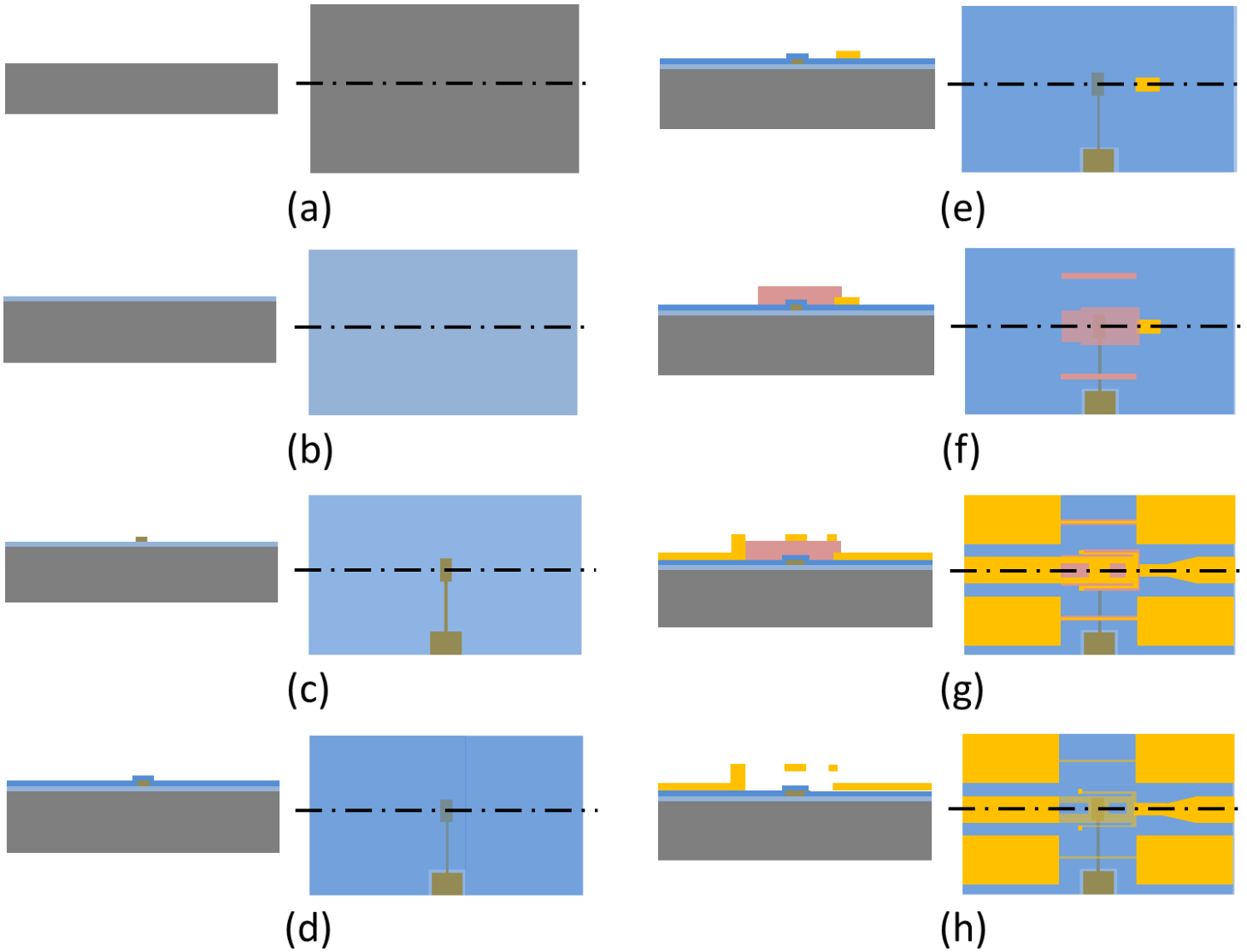


FIGURE 33 SCHEMATIC OF FABRICATION FLOW

TABLE 5FABRICATION PROCESS STEPS

Process Index	Description
A	Cleaning of 2'' Silicon Wafer
B	Growth of an Oxide Layer
C	Deposition and Patterning of Actuation Electrode(*Mask#1*)
D	Oxide Layer Deposition and Patterning for Actuation Pad Window (*Mask#2*)
E	Deposition and Patterning of Underneath Transmission Line (*Mask#3)*
F	Deposition and Patterning of Sacrificial Layer *(Mask#4)*
G	Deposition and Patterning of bridge, Cantilever, Ground Plane *(Mask#5)*
H	Removal of Sacrificial Layer

Masks are made for all four configurations (SPST, SPDT, SP4T, and T-Type). For a comparison purpose among the various improvements mask for all versions are made. By saying versions it means for every switch configuration four masks are made. Two for with and without tethered cantilever beam. And another two for tapered and rectangular shape central conductor. With all possible combinations total four (2 X 2) versions of masks are made for each switch configurations. With the addition to that, for SPST and SPDT mask for microstrip configuration is also made. Cut in the ground planes surrounding the switch configurations to realize the microstrip configurations. This is done for all four configurations of SPST and SPDT switches. Thus we have total eight configurations for both the switches. It is practically impossible to implement the uniform and complete process steps during fabrication throughout the area of a wafer. So for a safe side, we implement the wafer in an iterative manner were same structure is repeated several times on the same wafer. Summary of a number of devices is shown in Table.

TABLE 6 SUMMARY OF MASKS

Switch	Number of Configurations	Iterations	Total
SPST	8	4	32

SPDT	8	4	32
SP4T	4	5	20
T-Type	4	5	20
Total	24	-	**104**

Next consecutive set of Figure 34 shows the designed MASKS for all Four Switches.

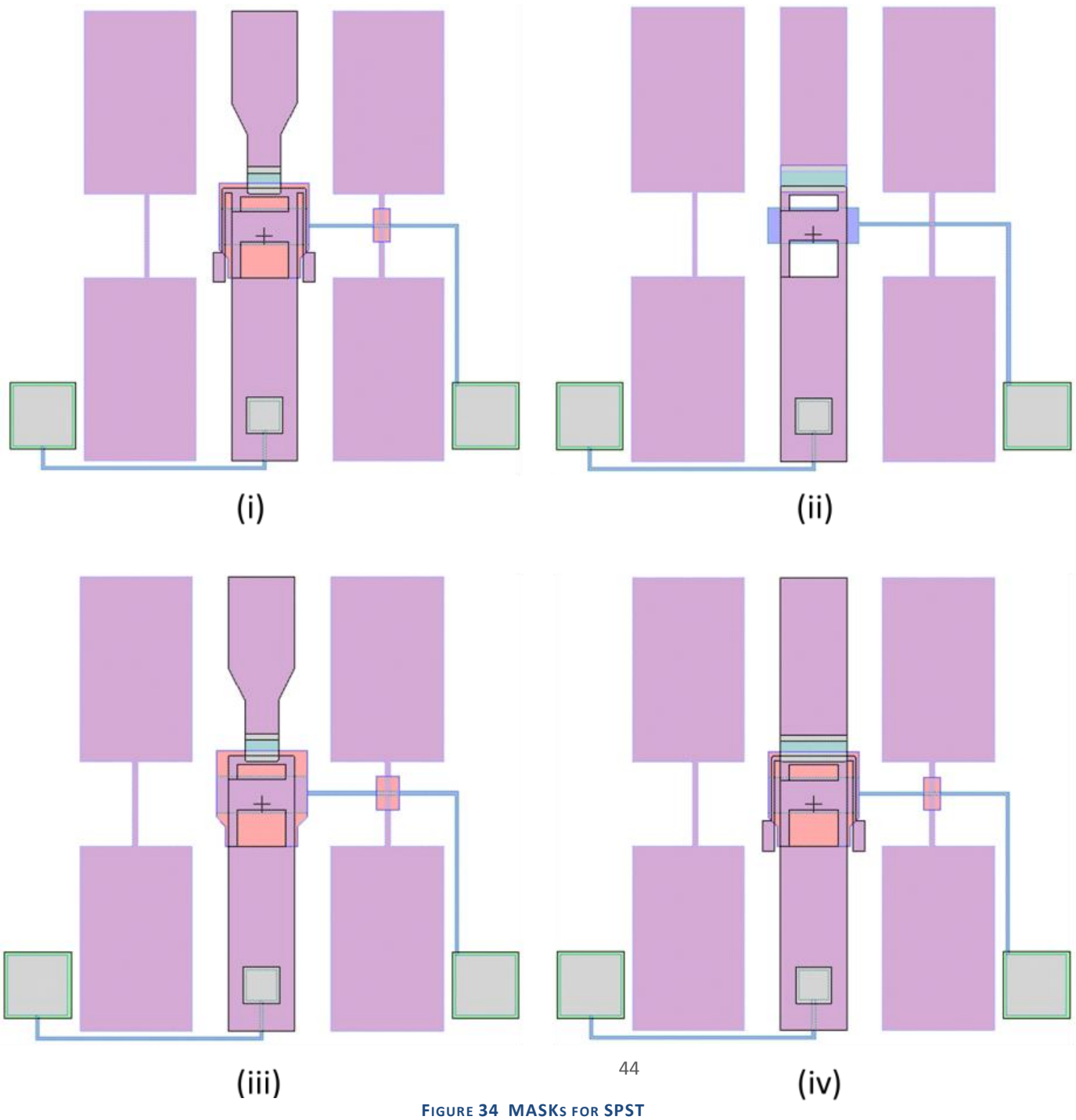


FIGURE 34 MASKS FOR SPST

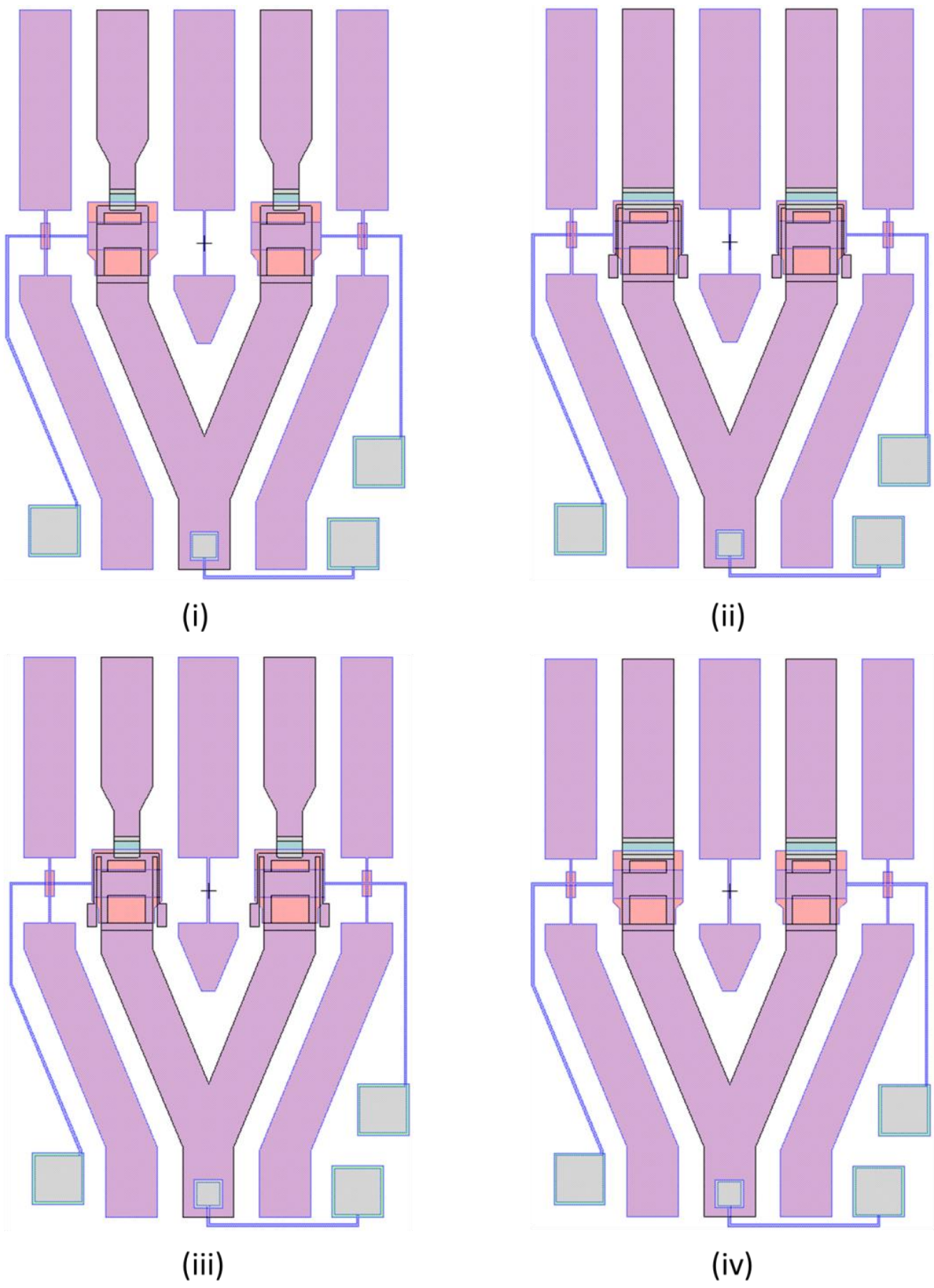


FIGURE 35 MASKS FOR SPDT

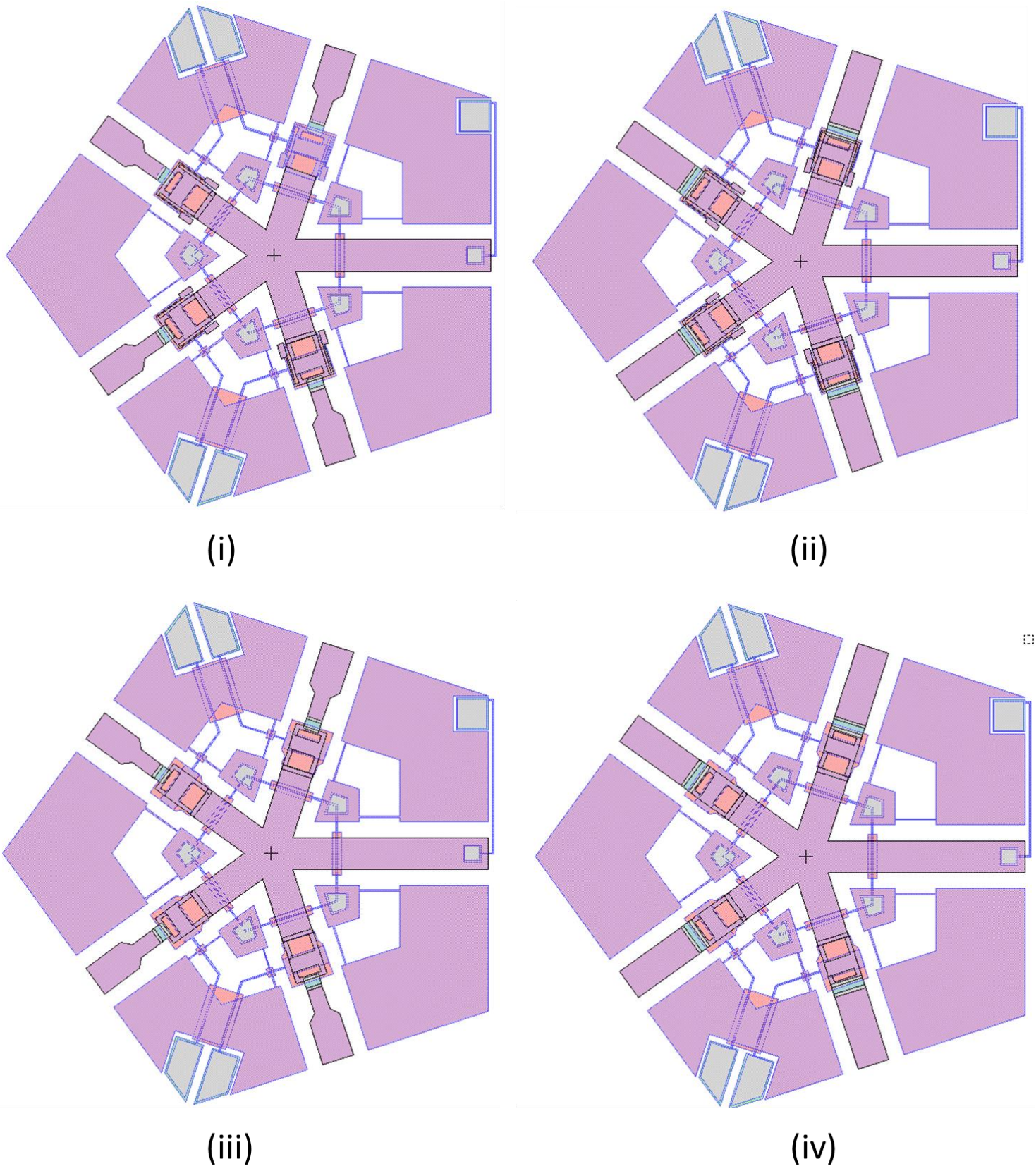


FIGURE 36 MASKS FOR SP4T

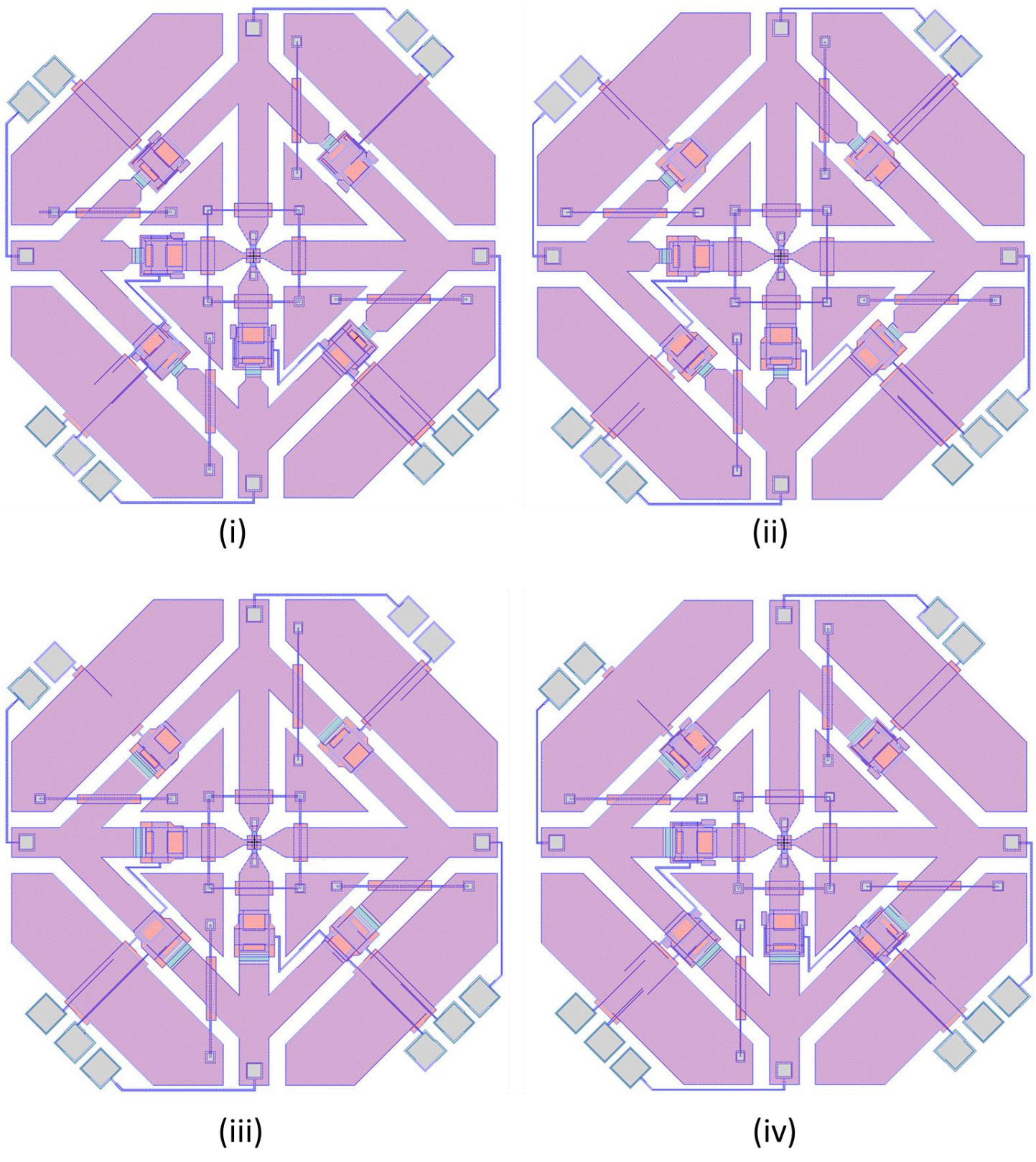


FIGURE 37 MASKS FOR T-TYPE

4.2 Fabrication Process

As explained in the previous chapter, the fabrication process involves five mask lithography processes. During the fabrication, many of the microfabrication processes are followed. The brief introduction of the key processes like wafer cleaning, thermal oxidation, UV-lithography Electroplating, PECVD(Plasma Enhanced Chemical Vapor Deposition), LPCVD(Low-Pressure Chemical Vapor Deposition), RIE(Reactive Ion Etching), Sputtering is given here.

4.2.1 Wafer Cleaning

Fabrication of device is carried out in a clean room where air has been filtered of particle contamination, temperature, humidity, vibrations and electrical disturbances are under stringent control. Smoke, dust, bacteria, and cells are micrometers in size, and their presence will destroy the functionality of a microfabricated device so in order to avoid these interruptions from these contaminations it is necessary to do these steps in the clean room. Cleanroom provides only passive cleaning but the wafers are to actively clean before every critical step. Contamination comes in different forms like particles, organics, native oxides. The various process of Wafer Cleaning are:

- Degreasing
- RCA cleaning
- Piranha Cleaning
- HF dip

4.2.2 Thermal Oxidation

Oxidation is a very important step in both microsystem and microelectronics. It includes thermal oxidation, plasma enhanced chemical vapor deposition (PECVD), and electrochemical anodization. Among these processes, thermal oxidation is the most important for silicon devices. These processes are used to form thin films such as thermal oxidation of electrical or insulation media, metal films for electrical (ohmic) and junctions, dielectric layer.

Thermal oxidation of silicon: Silicon dioxide is used as an electric insulator as well as for etching masks for silicon and sacrificial layers in surface micromachining. The simple and expensive way to produce SiO2 over the silicon substrate is by the thermal oxidation. The schematic cross section of

resistance- heated furnace is given below in figure 38. This can be done in two ways either wet or dry oxidation. The chemical reactions involved in this process are as follows:

I. Dry oxidation:

It is used for thinner oxides and oxides of high quality.

Si (solid) + O2 (gas)→ SiO2 (solid)

II. Wet oxidation

It is used for thicker oxides because the growth rate is higher.

Si (solid) + $2H_2O$(steam) → SiO_2(solid) + $2H_2$ (gas)

The figure 38 shows the schematic of the thermal oxidation process.

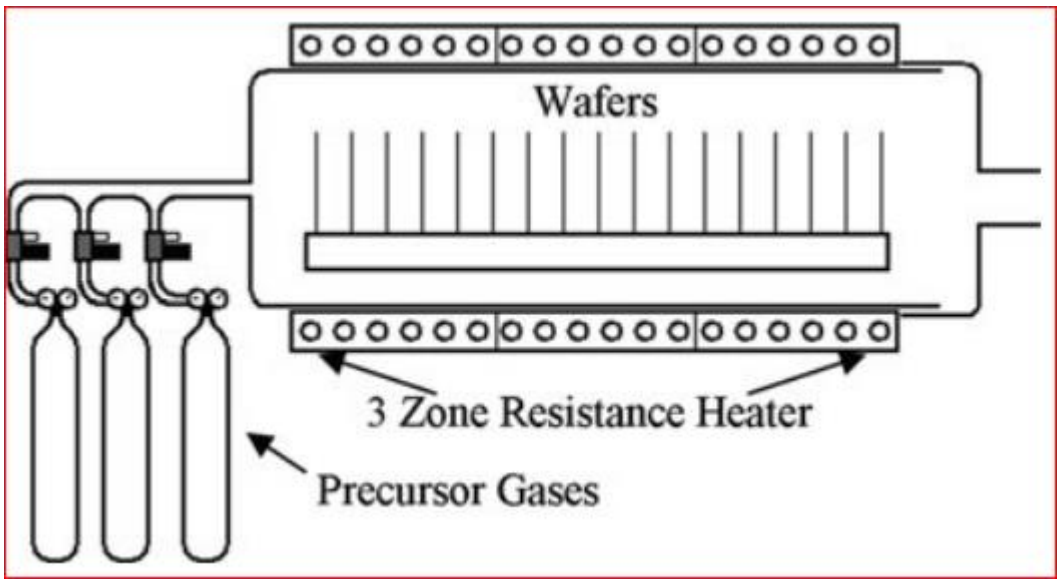


FIGURE 38 SCHEMATIC OF THERMAL OXIDATION (PHOTO COURTESY '36)

4.2.3 UV-LITHOGRAPHY

The concepts underlying photolithography are quite simple. The process uses a patterned mask comprised of transparent and opaque regions. Using an optical projection system, this pattern is illuminated onto a photosensitive film called a photoresist. When light strikes the photoresist, it causes a chemical change to take place within the photoresist film which in turn changes the ability of the photoresist to be dissolved by various solvents. This allows specific areas of the photoresist layer to be removed, which uncovers (exposes) the underlying substrate surface for further processing. The real advantage of the photolithographic process is that it can be performed over large areas at a very high resolution *[35]*. The photolithographic process contains four main components (photomask, optical projection system, photoresist, and substrate) and can be described by a five-step process.

I. Deposit photoresist
II. Expose photoresist
III. Develop photoresist
IV. Transfer pattern
V. Remove photoresist

These steps are illustrated in9.3 with each component and processing step labeled.

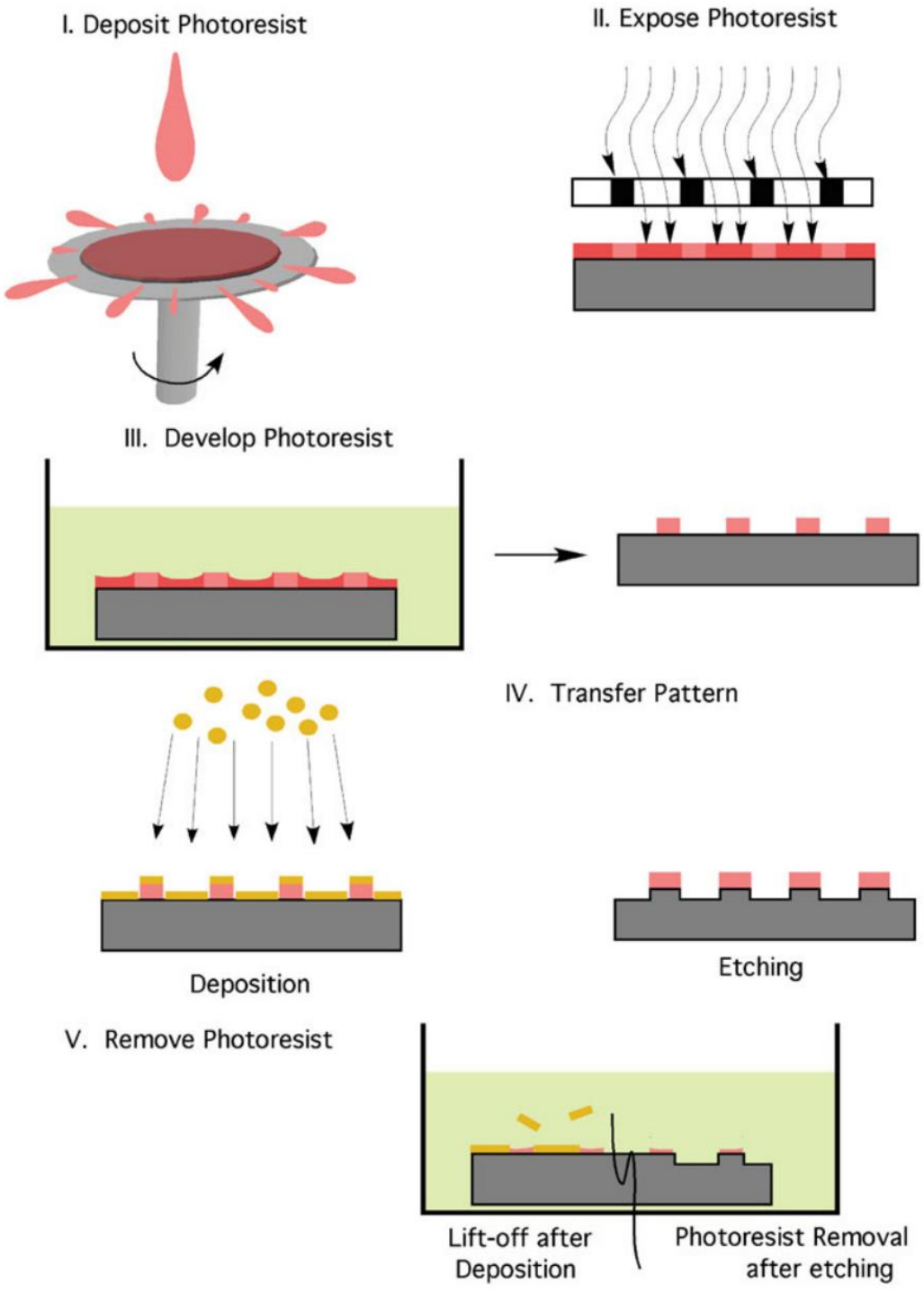


FIGURE 39 SCHEMATIC OF UV LITHOGRAPHY (PHOTO COURTESY '36)

4.2 SEM OF IMPLEMENTED SAMPLE

Here in this section SEM images of implemented samples been shown. As can be seen from the figure 40 the SPDT switch has been implemented. This version of SPDT is tethered based having rectangular shape ground conductor. As shown in figure 40, ‘A’ represents actuation pad, ’B’ is a central conductor, ‘C’ represents Ground Conductor.

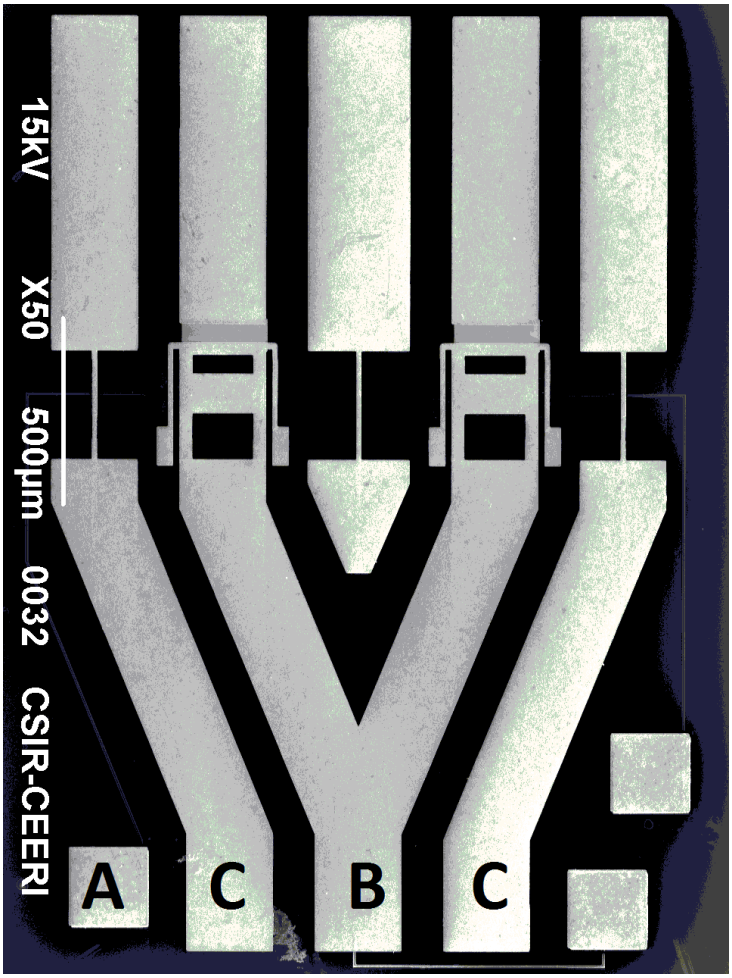


FIGURE 40 SEM OF SPDT

Other than that as shown in figure 41 the T-Type Switch has been implemented. Shown version of T –Type Switch is without tether having tapered shape ground conductor.As shown in figure 41, ‘C’ represents actuation pad, ’B’ is a central conductor, ‘A’ represents Ground Conductor.

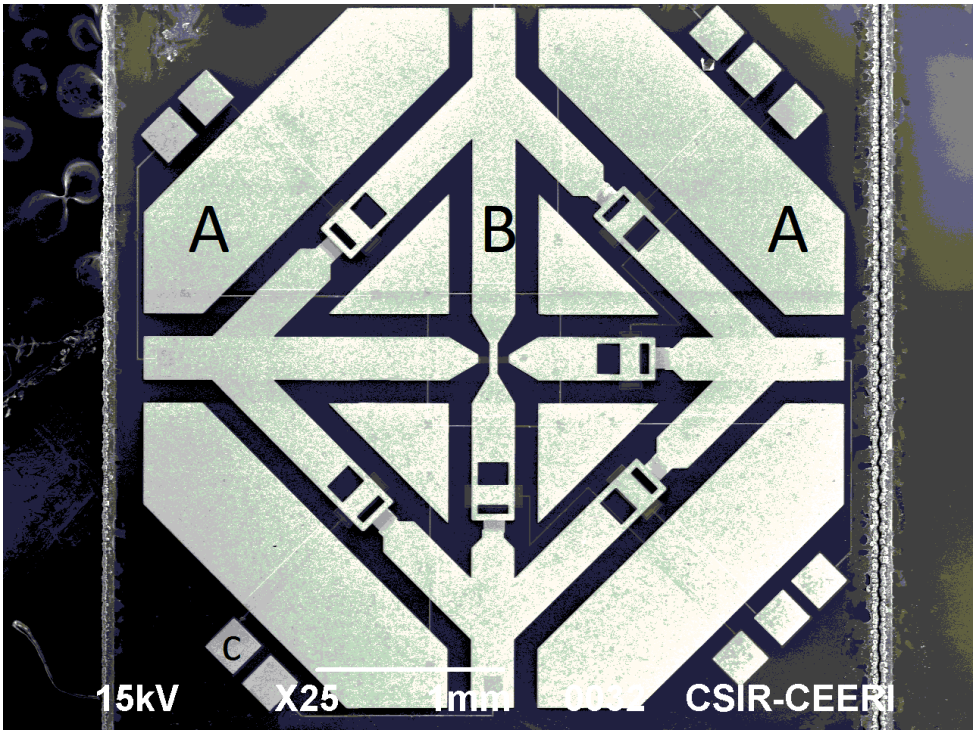


FIGURE 41 SEM OF T-TYPE SWITCH

5 Conclusion and Future Work

The designing and fabrication process for a different kind of Switch structure is carried out. The Simulated results of SPST, SPDT, SP4T and T-Type switch shows an excellent performance over C-Band(4-8GHz). RF Response for SPST shows an Isolation of -15.712dB and Insertion Loss of -0.0824dB at 10GHz. RF Response for the T-Type switch in mode I shows Isolation of -0.18dB and Insertion Loss of -21.23dB at 9GHz for asymmetric structure. The improvement in actuator design to prevent curvature in the hanging cantilever beam doesn't alter the pull-in voltage response much. The pull-in voltage found to be 13.25-13.35 V which is fairly within the acceptable range. The C-Type switch is also implemented using basic Capacitive SPDT Switch. The RF response of a C-Type switch shows the Insertion loss of -0.62dB and Isolation of -20.06dB @15GHz.

In the future work, implementation of the T-Type switch using least number of hanging structures can be proposed. As shown in C-Type implementation, the T-Type switch can also be implemented using 3 hanging structures. Moreover, characterization can also be done of implemented switches. Switches can also be implemented using Copper (Cu) to verify the performance over switches made of Gold (Au).

PART-B
6INTERNSHIP WORK AT QUALCOMM

The chapter is dedicated to the overview of the carried at Qualcomm during the period of JAN'2017 to JUNE'2017. Over where work was focused on the verification of the CPU subsystem.

As a part of internship work, a verification of CPU subsystem was allotted. For the same understanding of Memory hierarchy and Coherency were developed. This chapter is dedicated to the understanding of the memory hierarchy in computer architecture and explanation of coherency management is provided at the end. The implementation of proposed has not been shown as a part of this chapter.

6.1 MEMORY HIERARCHY

From the very early days, computers programmers would want the unlimited and the fast memory. Due to different tradeoffs in memory technology, an economical solution to that requirement is memory hierarchy. Memory hierarchy takes advantages of locality while taking into account all those trade-offs in the cost-performance of memory technology. The principle of locality deals with the fact that most of the all programs do not access entire data memory or a code memory uniformly. There will always some locality be incorporate with time and space *[37]*. Locality in time is termed as temporal locality and locality in space is termed as spatial locality. The trade-off in memory technology concludes that faster memories are costly and larger and smaller memories are slower. This trade-off pushes the idea of hierarchical memory for the implementation. Figure 42 shows the multilevel hierarchical implementation of memory including typical sizes and speeds of access. As fast memories are larger and expensive, the memory hierarchy is implemented in serval different levels for smaller, faster and comparatively more expensive than the lower level. The main objective of such implementation to provide a memory which is as fast as the fastest memory and as cheap as the cheapest memory *[38]*. Not every time but in most of the cases, the data stored in the higher level is the subset of the data stored in the lower level. Such property is termed as inclusion property. Here lower level is considered as main memory in the case of cache and further considered as disk memory in the case of virtual memory.

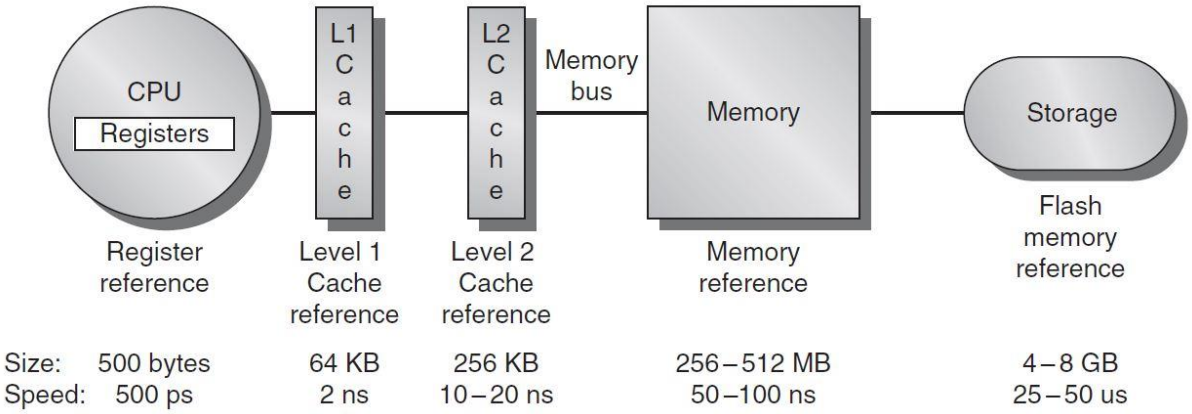


FIGURE 42 MEMORY HIERARCHY IN MOBILE DEVICE (PHOTO COURTESY '37)

TABLE 7 COMPARISON OF MEMORY

Memory technology	Typical access time	$ per GiB in 2012
SRAM semiconductor memory	0.5–2.5 ns	$500–$1000
DRAM semiconductor memory	50–70 ns	$10–$20
Flash semiconductor memory	5,000–50,000 ns	$0.75–$1.00
Magnetic disk	5,000,000–20,000,000 ns	$0.05–$0.10

As shown in figure 42, we can see that as we go away from the processor, the memory in the lower level becomes slower and larger. The table shows the comparison of different memory in terms of access time and cost is shown.

The need of the memory hierarchy has increased following to the advancement in the processor. In Figure 43 shows the performance of the single processor with an access time of the main memory over the years. It clearly states that memory requests are much higher in improved processors than the average access time of the memory. In recent high-end processors which are using multiple cores are having more bandwidth requirements than what has shown in the graph for the single core processors.

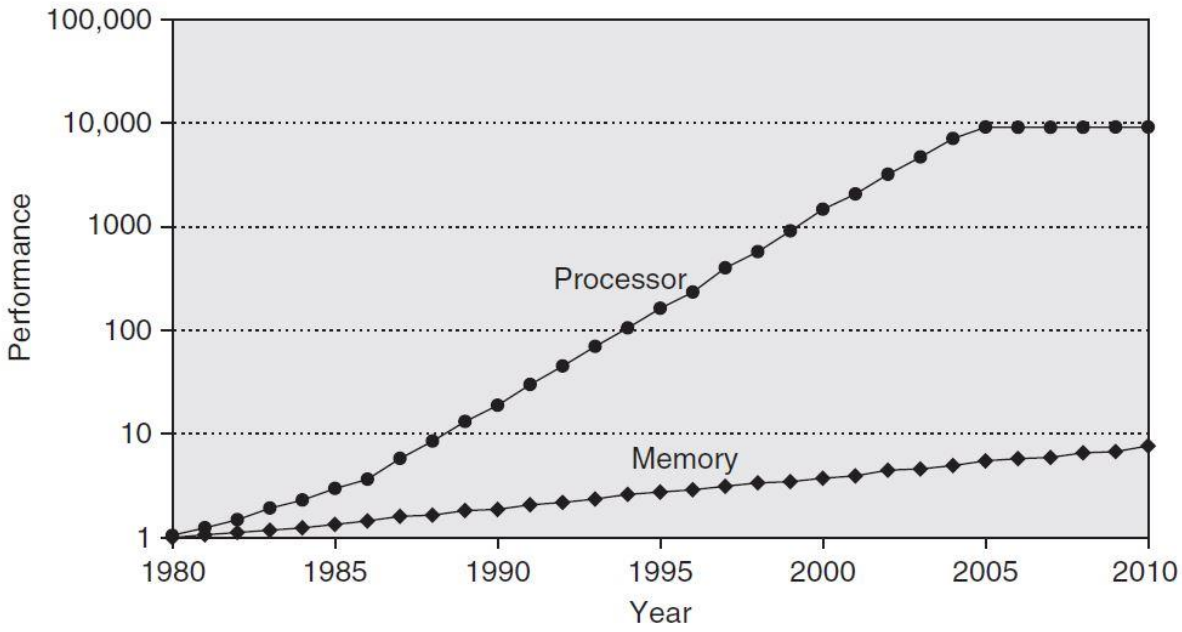


FIGURE 43 PERFORMANCE COMPARISON OF MEMORY AND PROCESSOR (PHOTO COURTESY 37)

Coming back to the principle of locality we will discuss the couple of localities that can be found in memory access. Temporal locality or the locality in time states that if a memory block is accessed,

then it is very likely that it will be accessed again in short period of time. Other than that there is a spatial locality. Spatial locality or the locality in space states that if some memory block is accessed then it is very likely that memory blocks in its neighborhood will be referenced again.

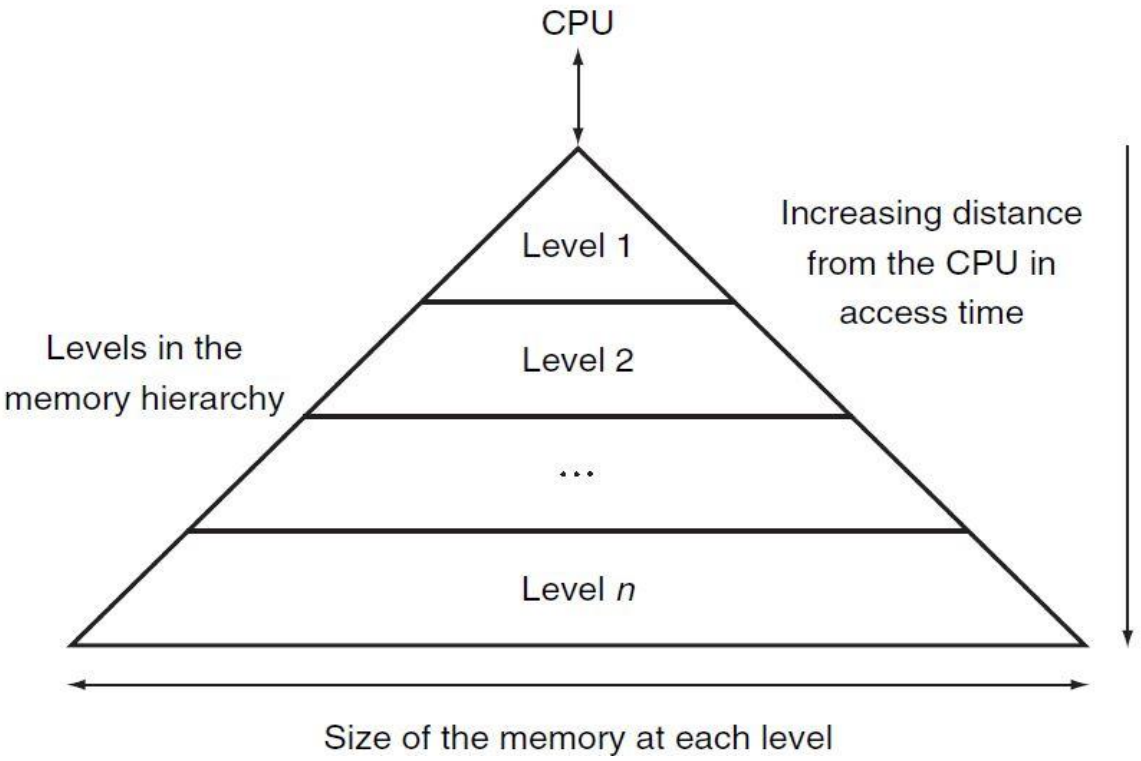


FIGURE 44 LEVEL OF MEMORY HIERARCHY (PHOTO COURTESY 37)

Any program exhibits both the mentioned localities. Temporal locality, the tendency of reusing the data block in near future and the Spatial locality, the tendency of the data that is near to the accessed block. Memory hierarchy takes advantages of both, temporal locality and the spatial locality as it keeps the recently used data as well as the data blocks nearer to the accessed data block near to the processor means in the higher level of memory blocks.

6.2 BASICS OF CACHE

As discussed in memory hierarchy implementation, based on the principle of locality some data in

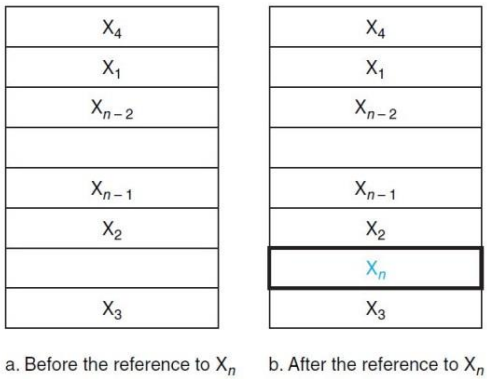


FIGURE 45 MEMORY BLOCKS

computing kept nearer to the processor. Thus increasing the performance by virtue of faster memory access rate. The memory hierarchy levels coming between the processor and main memory is termed as a cache. The basic meaning of word cache is a safe place for hiding or storing the things. The cache was first introduced as a part of research in computer architecture in the 1960s, and same flow carried away to the production computers by end of the same decade. Nowadays every general purpose computer which is built application ranging from servers to the low power embedded processor equipped with the cache. In the following section, the discussion starts with the simple cache having single word requests from the processor and the blocks also consist of a single word. As shown in figure 45, the memory block is having all the address values referenced before the memory request of an element which is not present in the cache. In this scenario access of the memory reference results in miss access. And thus the access of the address routed to the main memory and content of that memory address is brought into the cache. The important thing to notice down is how a processor will come to know that there no content available for the requested reference address? The answer lies in the implementation of the cache. If the particular memory address is mapped to the exact location of the cache than in straightforward manner one can determine the absence of the data. This method allocating the address locations directly to the particular block of the cache is called direct mapping of cache. Direct mapping of the cache is the simplest kind of mapping among all the mapping implementations. For example, almost all direct-mapped caches use this mapping to find a block:

(Block address) modulo (Number of blocks in the cache)

The calculation of block address is easy as the number of blocks in the cache is a power of 2. For example, if there are 16 blocks in the cache than lower four bits of the address are considered as block address. Same can be seen from the figure 45. To understand the following section properly some terms should be defined related to the cache.

Cache block – This indicates the basic unit of cache memory. The size of this basic unit can be anything varying from the bytes to the word.

Cache line – Cache line is referred as the group of cache blocks. This is different from the Raw of a cache.

Cache set – Cache set is referred as the number of row in the cache block. A number of a row in the cache determined by the layout of the cache whether it is a set associative cache or a direct mapped cache or a fully associative cache.

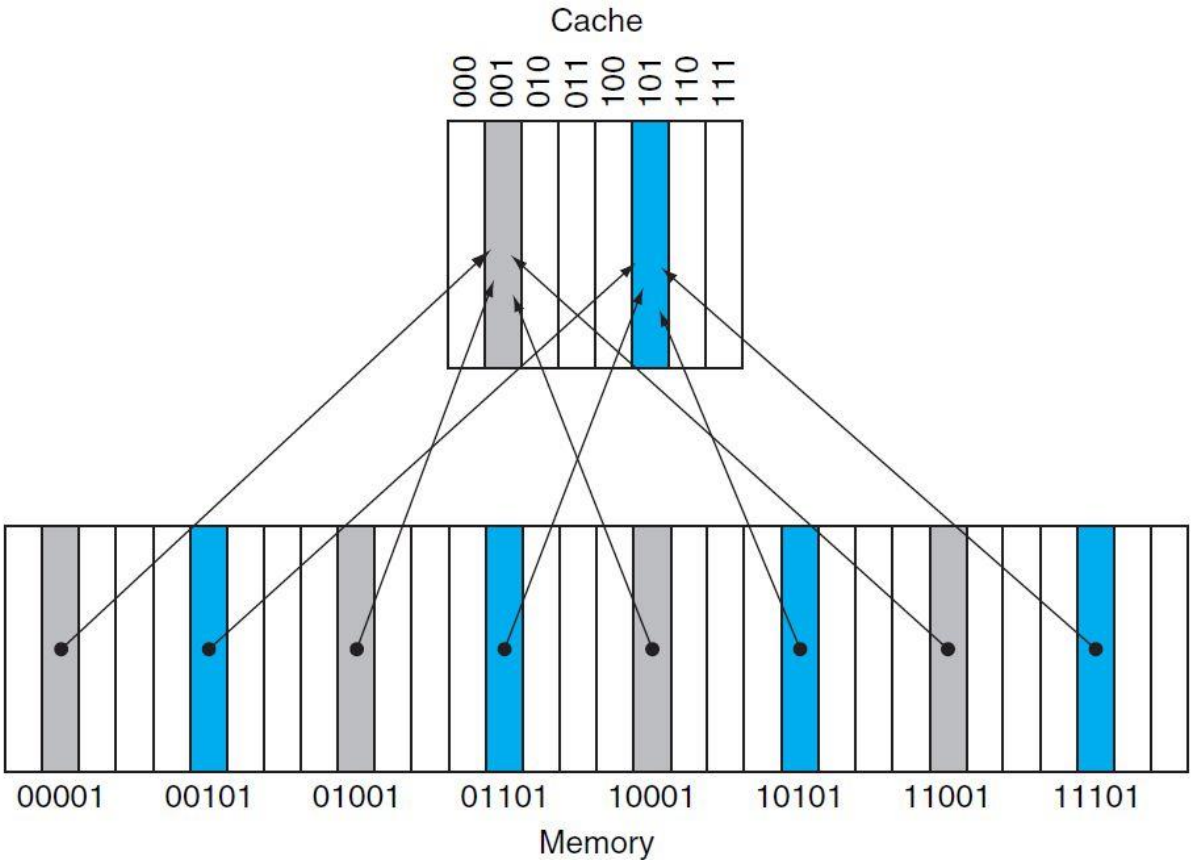


FIGURE 46 DIRECT MAPPING OF CACHE IN MEMORY (PHOTO COURTESY '38)

Tag - Tag can be considered as the unique ID within the same block. As many addresses are mapped to the same block, the value of tag differentiates between them.

Valid bit – A valid bit associated with each cache determines whether the data in the cache line is valid or not.

Basic access to cache:

Locating data in the cache

For the requested access of address, one can determine whether the content of that memory location is present in the cache or not. For the same one can follow the below given procedure.

1. Go for the set in which the requested address is residing by using set index.
2. Now go for the particular block in the given set, compare the tag of the address with the tag present at that location to determine the presence of block. If the address is matched at that location than one should go for the validation of the same.
3. Check for the valid bit in the block was the content was found to be present. If the valid bit is one that one can conclude that the data is present in the cache. Otherwise, it is not.
If the data at that address is in the cache, then we use the block offset from that address to find the data within the cache block where the data was found.

Divisions of the address for cache use.

All the information needed to locate the address in the cache can be decoded from the address itself. As shown in above, address contains the dedicated bits for the block offset, set index and the tag value. The block offset bits determine the number of address locations in a single block. For example, three dedicated bits for block offset concludes that there are 8 addresses in the single block entry. The next group of bits is dedicated for the set index which determines how many sets are there in the cache. Same as block offset it determines the number of sets in the cache. The remaining bits are used as tag bits to determine the presence of the address.

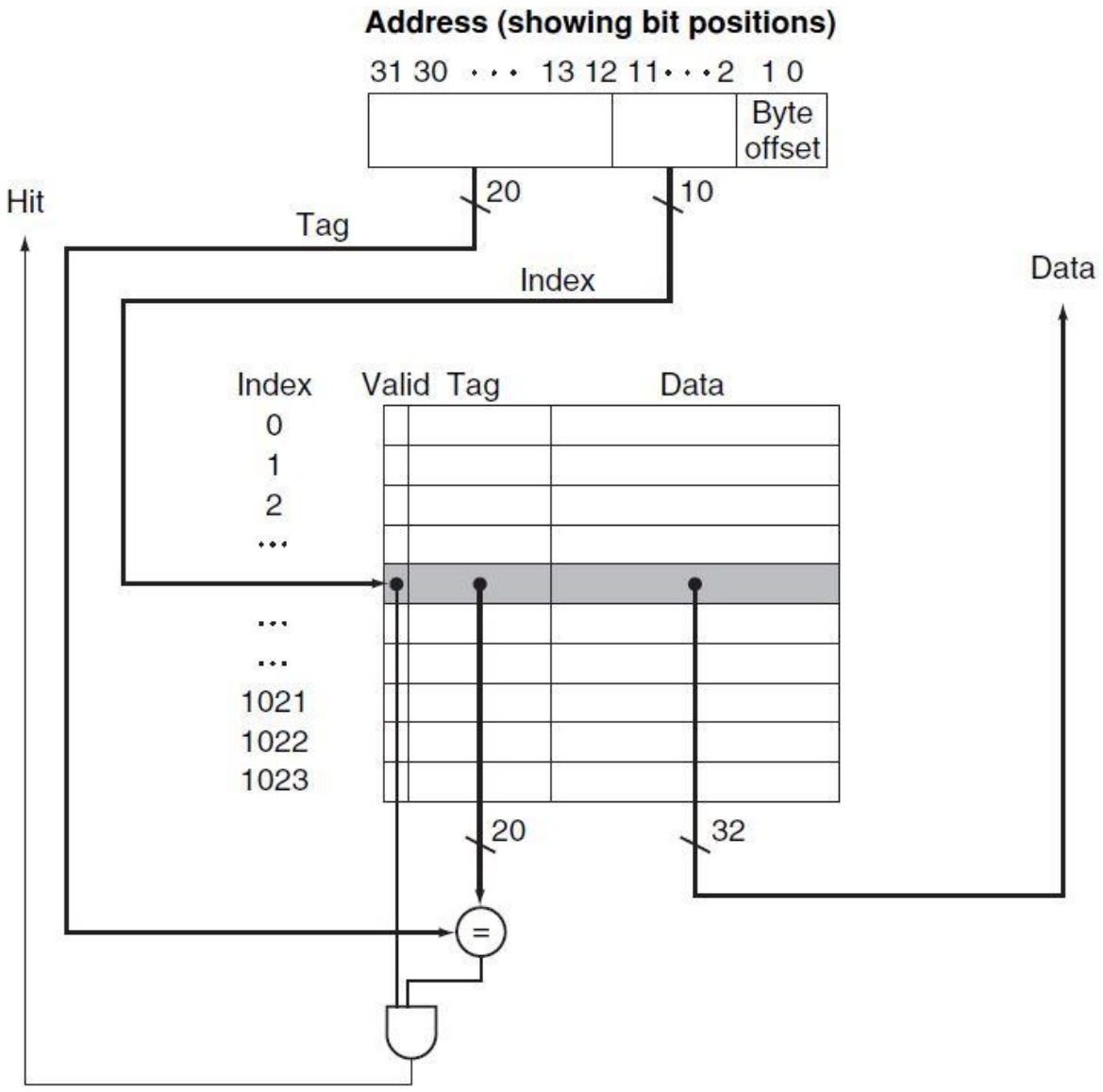


FIGURE 47 CACHE BASIC ACCESS (PHOTO COURTESY '38)

6.2.1 LOADING DATA INTO THE CACHE

When one particular address requested and not found in the cache than the cache miss happens. In that case, the content of the main memory is loaded into the respective locations in the cache block. To serve the principle of spatial locality, the entire cache block is loaded with the content of the address range of the block size. The starting address of the block size is determined by zeroing all the block offset bits of the requested address. The end address is determined by writing 1s to all the block offset

bits. The range of this address is exactly the same as the size of the cache block. In the direct mapping of address in the cache, the addresses are written on the pre-decided block, where the requested block is directly mapped. Whereas in associative cache mapping, the decision needs to be made to load the content of the address among the possible ways of implementation. In this case, if none of the location is free of all ways of cache than the eviction of the cache block is made. Eviction can be based on different algorithms known as LRU(least recently used) or can be random.

Apart from this, there are policies for writing data into the cache whenever changes occurred in the data locations. Major used policies are Write through and Write back

Write Though: Write through is a content storage mechanism when the cache memory is incorporated as a part of the memory hierarchy. In write through method, data is written back to the main memory as well as in the cache whenever any change made in the data. Due to this, it is promised that the main memory will not have any stale data at any point of time. The risk of data loss is reduced highly as the main memory contents are updated at the same time. But for every change in particular address location, whole cache block needs to be written back in the main memory. This slows down the operation. The security of the data is achieved by manipulating the latency of access. This method is implemented in the application areas where the data loss cannot be tolerated such as medical and banking areas. In other areas where a large amount of data is being dealt with, another method than writing through is implemented.

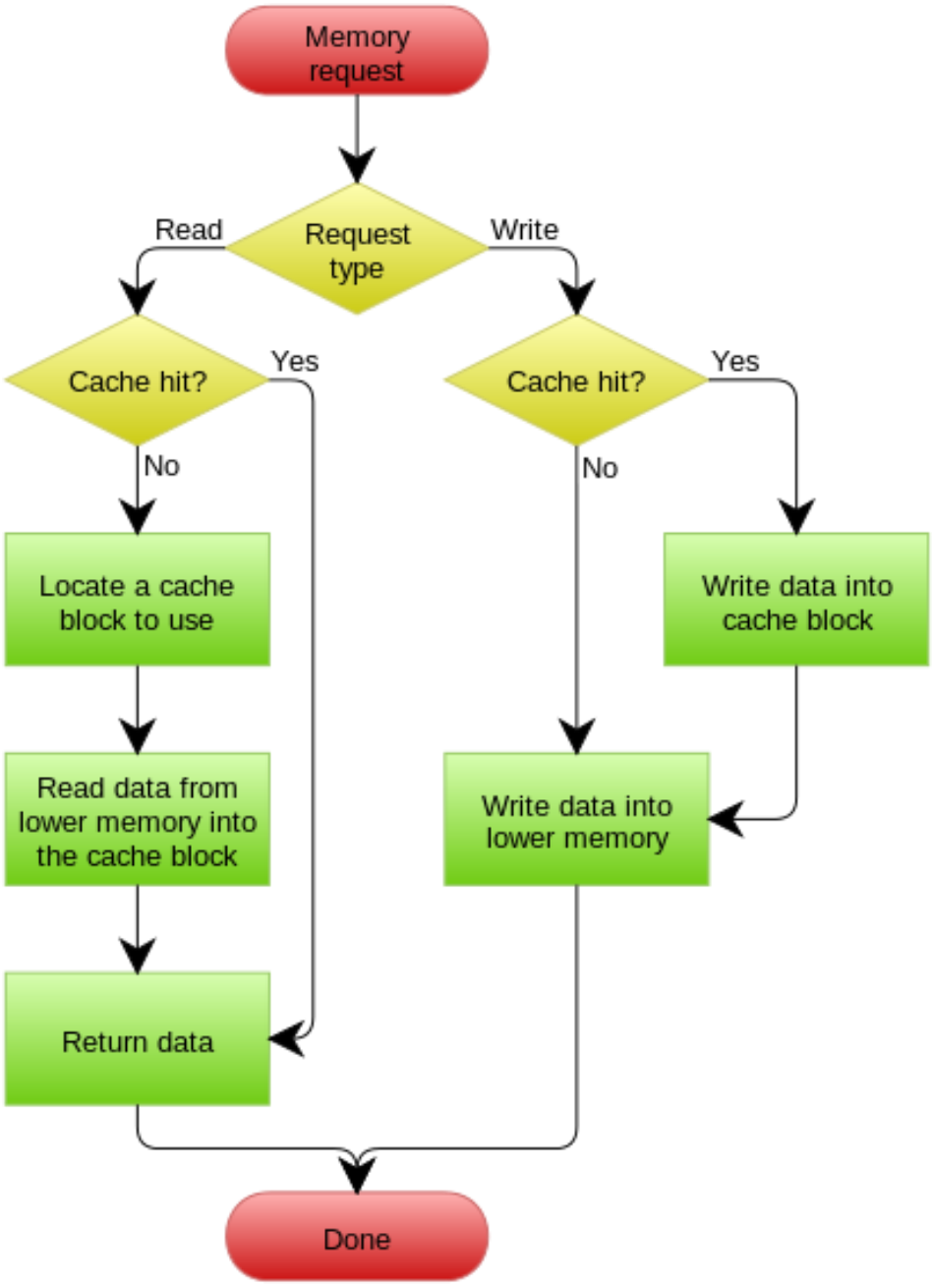


FIGURE 48 WRITE THROUGH TOPOLOGY(PHOTO COURTESY '39)

Write Back: Write back is a storage method in which whenever the data is changed in the location that is written to the cache block only. The data is written back to the main memory after specifics time interval or based on some conditions to be met. When data is updated in the cache block then that data is considered as the fresh data whereas the data on the same location in memory is called stale data.

Due to a lesser number of main memory access in the write through method, it is found to be faster than the write through method. This method can be implemented where the loss of data can be tolerated as this the con in such implementation.

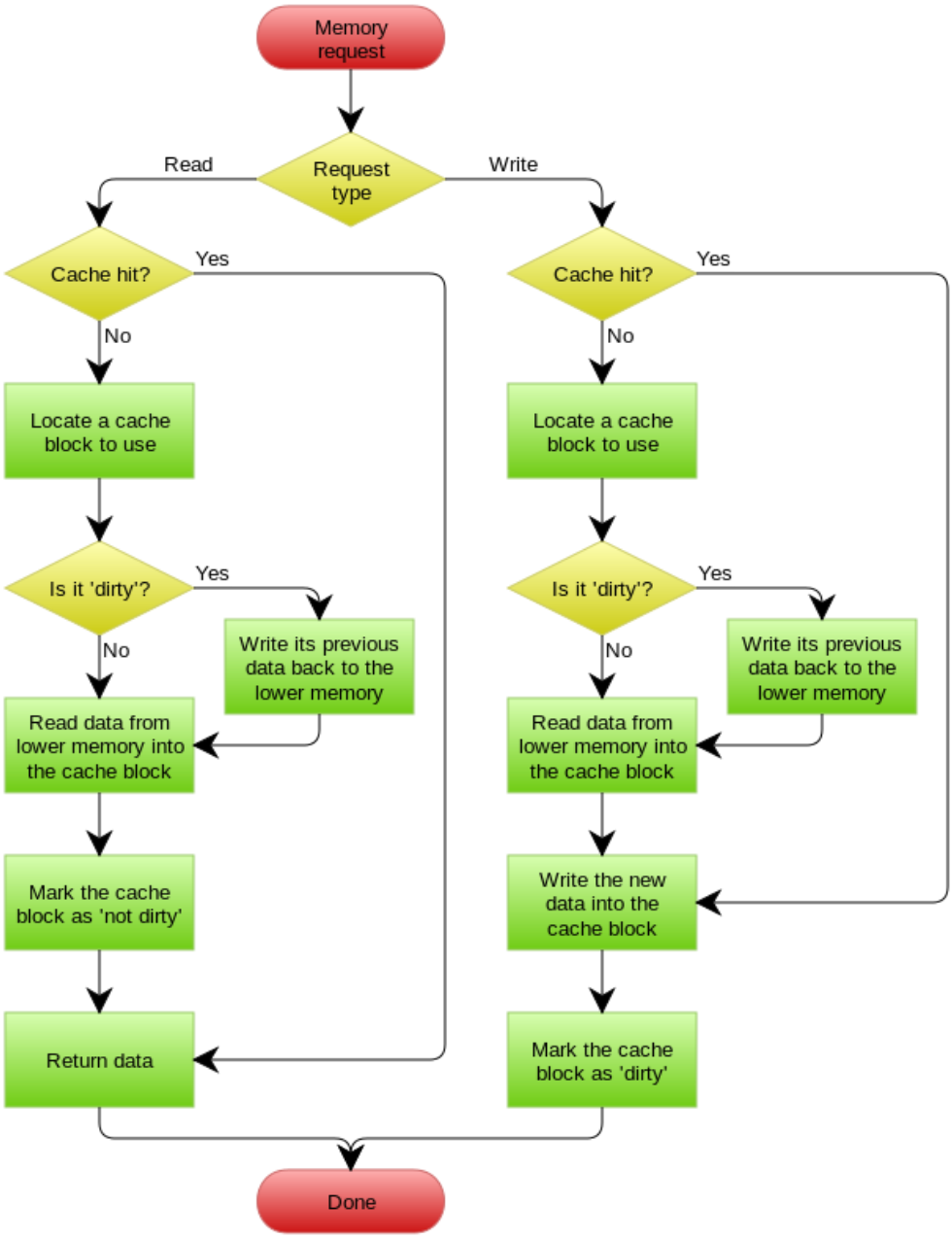


FIGURE 49 WRITE BACK TOPOLOGY (PHOTO COURTESY '39)

6.3 Coherency Protocols

In computer architecture, to overcome the need of the higher computing leads to the multiprocessing system. These multiple processing units share the same main memory among all the elements. The problem of incoherent data arises when the processing element only maintain the data in the local cache. For example, consider the case shown in figure #50 below. Here let suppose both the processing elements are working on the same address. Both are updating the data independent of each other. Now from the main memory point of view, the data is incoherent as both processing elements were locally updating the data. Cache coherent protocols are supposed to deal with such scenario and are keeping track of the data to maintain the coherent view of the data.

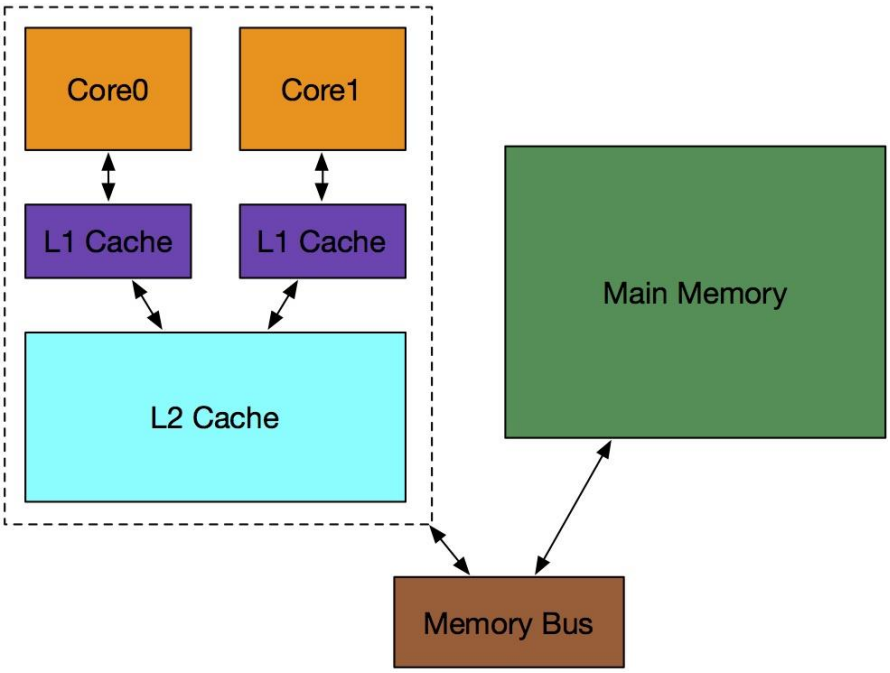


Figure 50 Shared Memory Hierarchy

To deal with the cache coherency many of the algorithms been implemented. To understand the algorithms properly we need to have a look at the basic terminology of cache states.

Write Invalidate: when a write operation is observed to a location that a cache has a copy of, the cache controller invalidates its own copy of the snooped memory location.

Write Update: when a write operation is observed to a location that a cache has a copy of, the cache controller updates its own copy of the snooped memory location with the new data.

MODIFIED (M) - Cache line has been modified. It is different from main memory and is the only cached copy.

OWNED (O) - Cache line is dirty and is possibly in more than one cache. A cache line in the Owned state holds the most recent, correct copy of the data. Only one core can hold the data in the Owned state. Other cores can hold the data in the Shared state.

EXCLUSIVE (E) - Cache line is the same as main memory and is the only cached copy.

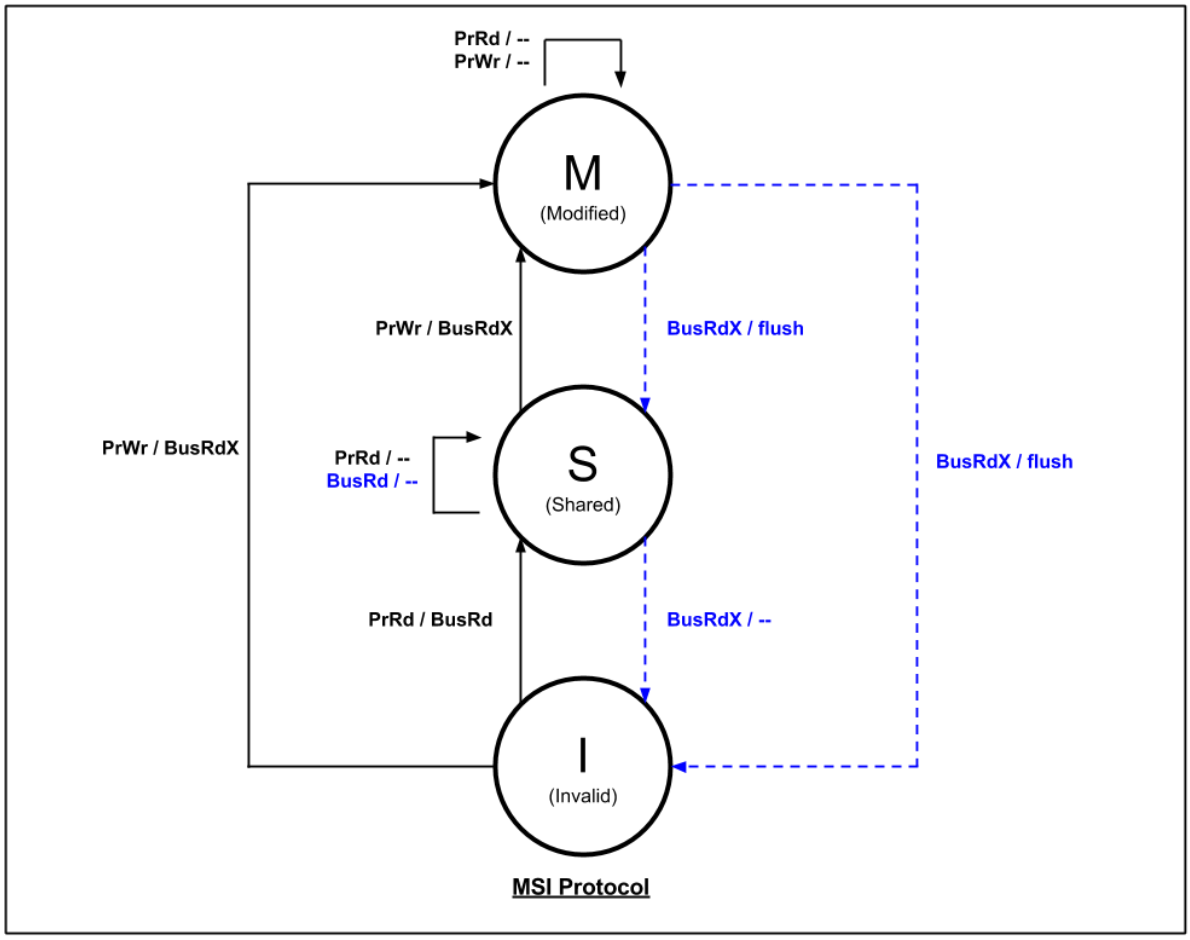


FIGURE 51 MSI PROTOCOL

SHARED (S) - Same as the main memory but copies might exist in other caches.

INVALID (I) - Line data is not valid as in simple cache

Let's move to the basic protocols to manage data coherency in the cache. In the following part of the session, we will be discussing three widely used coherence protocols in detail. There many different types of protocols like MSI, MESI, MOSI, MOESI, etc.

6.3.1 MSI

As the name suggests in MSI protocol we have three different states of the cache block corresponding to the each letter of the protocol Modified (M), Shared (S), Invalid (I). The in-depth operation of the MSI protocol is shown in the Flowchart shown in figure 51. MSI protocol is the most common protocol for cache coherency.

Consider the following scenario for an example. When request read is generated to the cache for the block in the M or S states than the cache supplies the data to the request as it is having the requested data. But if block in the case where the block is not in the cache than some points supposed to be verified before loading data from the main memory. It must ensure that the data is not in the M state in any other cache. This can be done by different methods according to the different caching architecture. Likewise, bus-based architecture invokes the snooping for the read request in which data read request is broadcast to the all of the caches. Some of the architecture has a directory to serve the same purpose in which the information of the last data updated is being kept. If another cache block is in M state than it must be written back in the main memory. When a write request arrives for the cache block in M state than the data must be modified locally. If the block is in S state where the write request is made then the block should notify other blocks of the S state to evict that block as the data is going to be changed by another client. This invalidation request in the write operation is also made using snooping or directory-based method explained earlier. If the block is in I state prior to the write request than the cache must notify the other block having state S or M to evict the block. If the block is in M state then the cache must update the main memory or serve the requesting cache.

6.3.2 MESI

In MESI protocol there are four different states of the cache line are defined. These are Modified (M), Exclusive (E), Shared (S), Invalidate (I). The MESI protocol is mostly based on the invalidation-based cache coherence protocol. This is one of the best commonly used a protocol which can be implemented in write back caches. The write back phenomenon saves a lot of bandwidth as it demands a lesser number of bus transactions. The MESI protocol is also known as the Illinois protocol as it was developed at the University of Illinois. As main memory transactions are less in this protocol, it significantly improves the performance. Figure 52 shows the algorithm for the MESI algorithm.

6.3.3 MOESI

There are five different states are defined in the MOESI protocol. These states are Modified (M), Owned (O), Exclusive (E), Shared (S), Invalid (I). MOESI protocol is the most evolved protocol among cache coherent protocols. It comprises of all the possible states of all other protocols. Advancement in MOESI protocol from the MESI protocol is the owned state. In this owned state a cache can provide the data if it is in the M state prior to writing back to the main memory. This saves extra time and improves the latency. Figure 53 shows the algorithm for the MESI algorithm.

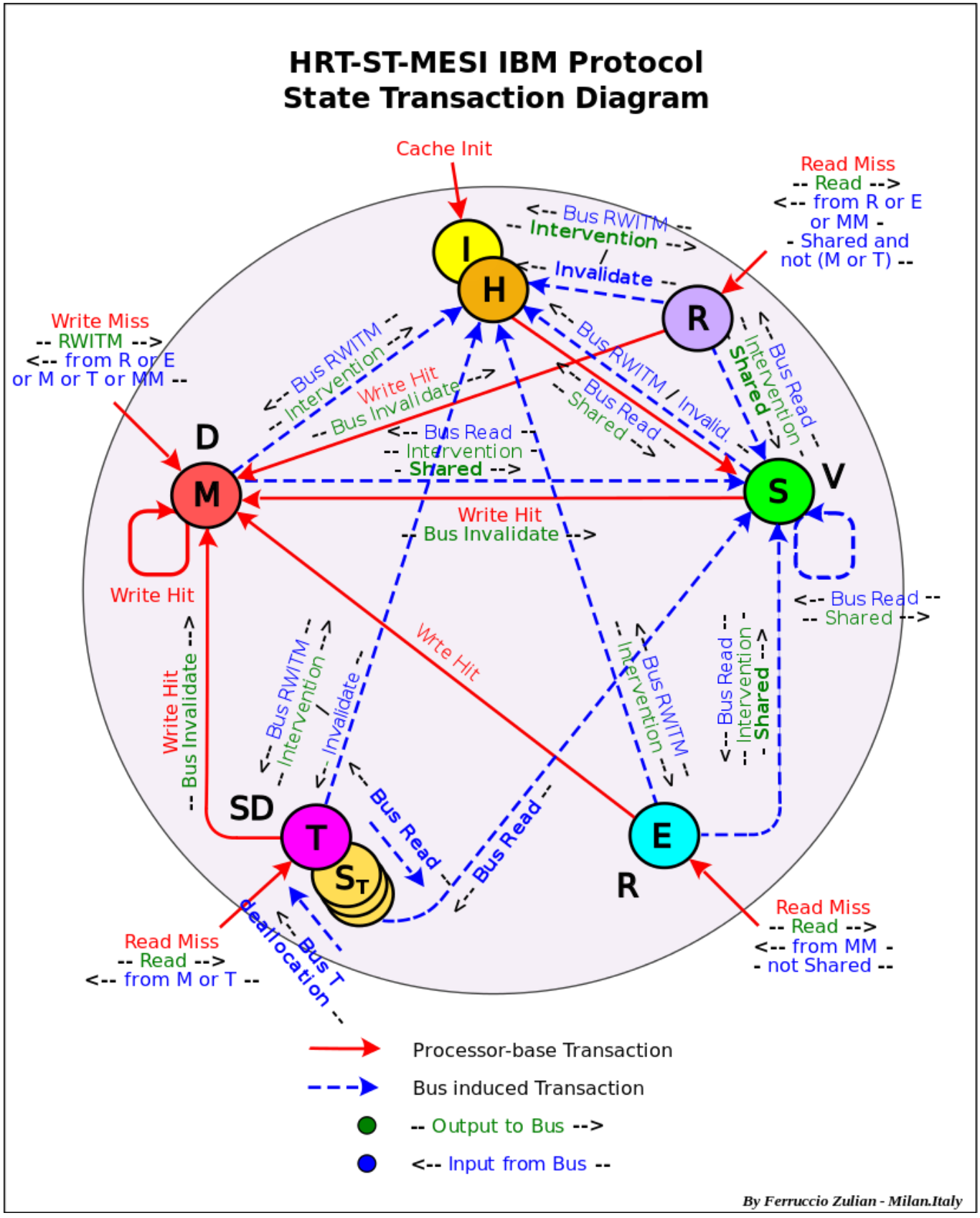


FIGURE 52 MESI PROTOCOL (PHOTO COURTESY '39)

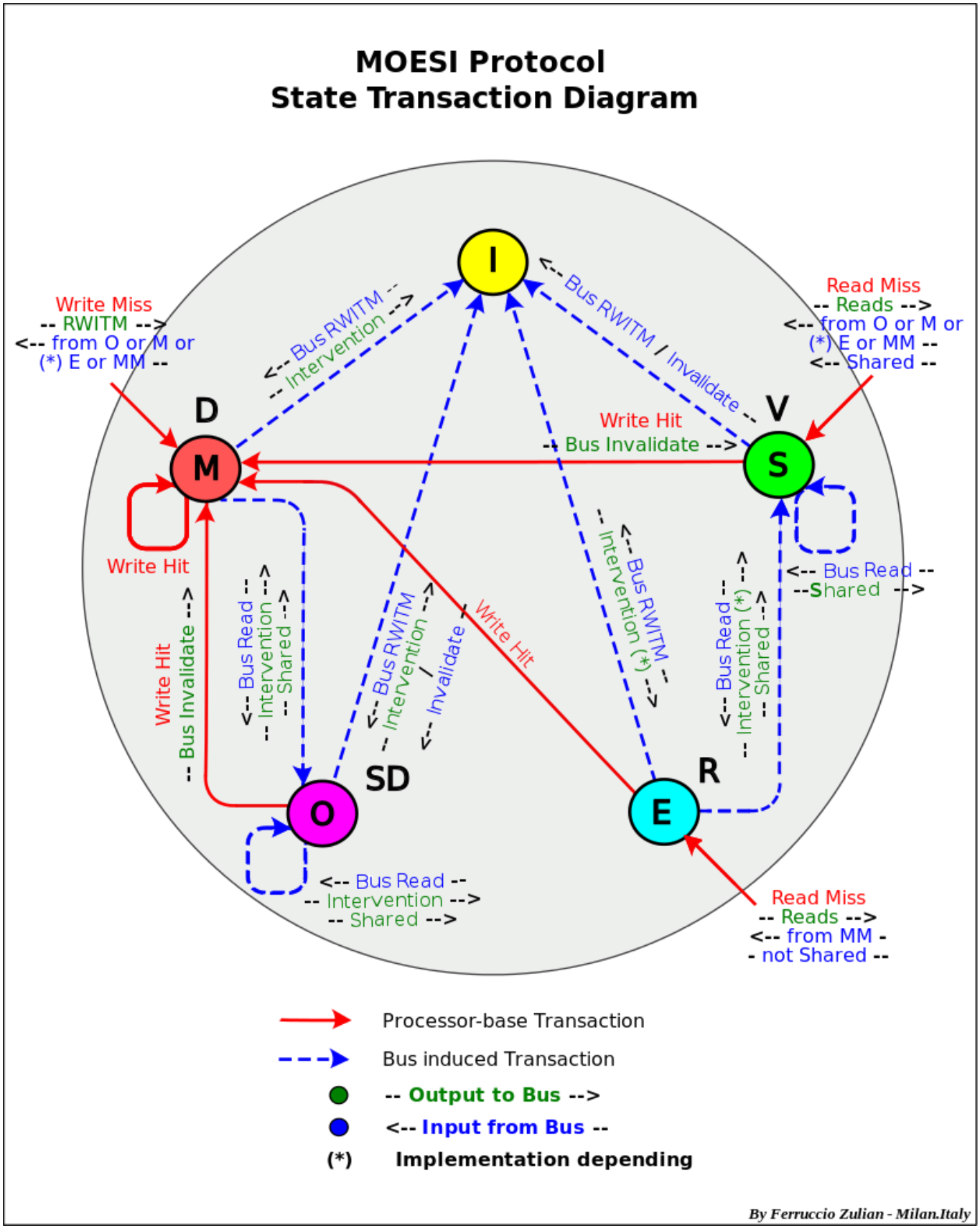


FIGURE 53 MOESI PROTOCOL (PHOTO COURTESY '39)

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