DESIGN AND PERFORMANCE ANALYSIS OF CNFET-BASED CURRENT CONVEYOR FOR ANALOG SIGNAL PROCESSING APPLICATIONS

Ph.D. Thesis

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Design and Performance Analysis of CNFET-based Current Conveyor for Analog Signal Processing Applications

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Dedicated

To

My Beloved and Inspiring Parents

Shrimati Shyama Tripathi

&

Shri Swatantra Kumar Tripathi

DECLARATION

I, Shailendra Kumar Tripathi, declare that the thesis titled, **"Design and Performance Analysis of CNFET-based Current Conveyor for Analog Signal Processing Applications"** and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this university.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this university or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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CERTIFICATE

This is to certify that the thesis entitled, **"Design and Performance Analysis of CNFET-based Current Conveyor for Analog Signal Processing Applications"** being submitted by Shailendra Kumar Tripathi (ID No. 2013REC9547) is a bonafide research work carried out under my supervision and guidance in fulfillment of the requirement for the award of the degree of **Doctor of Philosophy** in the Department of Electronics & Communication Engineering, Malaviya National Institute of Technology, Jaipur, India. The matter embodied in this thesis is original and has not been submitted to any other University or Institute for the award of any other degree.

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ABSTRACT

The processing of real-world signals using analog techniques is more accessible than digital. Analog signals in nature have all measurable physical quantities like force, speed, temperature, sound, light, acceleration *etc.* The ultimate reason for the processing of real-world signals is to extract valuable information from them. This information normally exists in the form of frequency, phase, signal amplitude or timing relations with other variables. Current conveyor turned out to be a very versatile device, having a vast variety of applications in analog signal processing, communication systems, and many front-end building blocks. This research work deals with the realization of the Carbon nanotube field effect transistor (CNFET)-based inverting current conveyor. It also includes the performance analysis of CNFET current conveyor by varying the CNT parameter such as diameter, pitch, and the number of tubes.

CNFET shows enormous potential as an alternative to Silicon MOSFET for building high performance and low power VLSI circuits. Carbon nanotubes (CNTs) with their superior transport properties, exceptional thermal conductivities, and high current capability expelled to be a potential alternative device to the bulk CMOS technology.

Further, this thesis utilizes the CNFET-based Current conveyor for the design of the active filter, current follower, instrumentation amplifier, and transconductance amplifier. These circuits have their usefulness in analog signal processing. Active filters are widely used in the signal processing and instrumentation fields. At present, there is a growing interest in designing of active filters for high-frequency analog applications. The short-range wireless communication technologies like ZigBee and Bluetooth are widely used in modern day electronic equipment. ZigBee operates in the ISM band with frequencies ranging from 868 MHz to 2.4 GHz while Bluetooth band ranging from 2.4 GHz to 2.48 GHz. In the view of above, a tunable voltage-mode active filter is realized which covers the full operating range of Bluetooth frequencies. Additionally, a voltage-mode universal filter is presented which covers the entire ZigBee band. Moreover, integrated sensor interface circuits are in current demand for low-power industrial and healthcare applications. In this work, a CCII-based low-power resistive interface is realized using CNFETs.

The differential voltage current conveyor (DVCC) is a very versatile active device and used to process the differential input signals. In this thesis, CNFET-based DVCC is realized for the analog circuit applications. The performance of CNFET

DVCC is superior to its CMOS counterpart regarding bandwidth and power consumption. Further, the design of Carbon nanotube-based digitally programmable current follower is presented. The digital control feature enhance the functionality of the device. As the gain of the current follower can be controlled by digital word using the appropriate voltage (logic) level to the gate of the CNFETs. Further, this current follower is used to implement a programmable gain instrumentation amplifier which is used for test equipment, signal conditioning, and low noise applications.

Additionally, RF filters are required in several applications from RF to across the complete spectrum of frequencies. These filters are used in communication systems such as satellite communication, transponders, *etc.* This work presents a CNFET-based Ku-band filter which can be used for satellite communications, mainly for fixed and broadcast based services.

Further, circuits for acquisition and pre-processing of physiological signals from the human body (*e.g.* ECG, EEG, EMG, EOG), require analog signal processing blocks operating at very low frequencies typically in the 0.001–3000 Hz range. The conventional opamp-RC design methodologies are not suitable for such very low frequencies due to the requirement of large values of the passive components. Thus, the design of ultra-low transconductance amplifier has gain the attention of researchers for physiological signal processing applications. A novel ultra-low transconductance amplifier based on Carbon nanotube field effect transistors (CNFET) is presented in this thesis. The proposed OTA circuit achieved transconductance (g_m) up to sub-10 pA/V range. Additionally, the transconductance of the OTA is tuned with the digital control word.

RESEARCH CONTRIBUTIONS

The major research contributions are listed below:

1. In-depth parameter variability analysis of the proposed analog circuits (ICCII) has been carried out to demonstrate their suitability in real-world applications. Further, active filters for Bluetooth and ZigBee are realized in the work.

2. CNFT-based DVCC is realized and Ku-band RF filter application is presented.

3. A CNFET-based Digitally Controlled Current Conveyor has been proposed. This is indeed a novel addition to the existing repertoire of analog building blocks.

4. A new Instrumentation Amplifier with digitally programmable gain is also proposed in this thesis.

5. A new CNFET based ultra-low gm operational transconductance amplifier has been designed. This is also a worthy contribution to the field of analog circuit design.

Contents

List of Figures

List of Tables

LIST OF ABBREVIATIONS

CNT	Carbon Nanotube
CNFET	Carbon Nanotube Field Effect Transistor
CCII	Current Conveyor Second Generation
CMOS	Complementary Metaloxide Semiconductor
DOICCII	Dual Output Inverting Current Conveyor Second Generation
DVCC	Differential Voltage Current Conveyor
DPDVCC	Digitally Programmable Differential Voltage Current Conveyor
ICCII	Inverting Current Conveyor Second Generation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
HSPICE	High-speed Simulation Program with Integrated Circuit Emphasis
OTA	Operational Transconductance Amplifier
TFET	Tunnel Field Effect Transistor
NWFET	Nano Wire Field Effect Transistor
SET	Single Electron Transistor
LPF	Low Pass Filter
BPF	Band Pass Filter
HPF	High Pass Filter
Op-Amp	Operational Amplifier
CM	Current-mode
VM	Voltage-mode
CFOA	Current Feedback Operational Amplifier
SWNT	Single walled Carbon Nanotube
MWNT	Multi walled Carbon Nanotube
QCA	Quantum Dot Cellular Automata
ISM	Industrial, Scientific and Medical
RNMC	Reversed Nested Miller Compensation
RHP	right-half-plane
ECG	Electrocardiogram
EEG	Electroencephalogram
EOG	Electrooculogram
EMG	Electromyogram

Chapter 1

Introduction

1.1 Background

Analog signal processing has been getting significant research interest over the last few decades. The basic modules include the design of continuous-time active filters, current followers, amplifiers, and transconductance amplifiers. These circuits find several applications in present communication and instrumentation field. Further, the processing of signals in analog domain cannot be stopped as the real world is analog. Though, the majority of the computation taken out in present systems is in digital form. Thus, analog circuits are essential in the applications such as processing of natural signals, amplification, continuous time filtering, rectification, A/D and D/A conversion, are unfeasible to be replaced by digital techniques apart from of their advances [7].

Since last four decades, the Current conveyor is used for various analog signal processing functions including amplification, continuous-time filtering, sampled data, *etc.* It has advantages in terms of inherently wide bandwidth, greater linearity, wide dynamic range, simple circuitry and lower power consumption [8]. The key application areas of Current conveyors are high-frequency wireless and radio frequency design. The advancement of CMOS has brought these circuit and system techniques into a versatile building block in the field of analog design [9, 10]. The second generation current conveyor (CCII), a variation of the current conveyor, has been presented [11]. It is a multipurpose current-mode (CM) analog building block which has gained recognition as a versatile active element. Further, a variant of current conveyor named the second generation inverting current conveyor is proposed [12]. The second generation inverting current conveyor (ICCII) has become very popular for implementing a wide range of electronic functions in voltage-mode and current-mode because of its high performance and versatility.

The CMOS is predominantly serving the electronics industry since last 40 years. The time-to-time advancement in the technology and performance has played a prominent role in electronic circuit design. The idea of device scaling has always been used for many technology generations. It has resulted in steady improvement in performance and device density. In the last three decades, the electronics industry has seen remarkable miniaturization of transistor sizes with the number of elements on an IC approximately doubling every 18–24 months. It could be reached due to the innovation of new materials, like high-k dielectrics, various nitrides, and silicides. It was the roadmap for down-scaling of MOS device. However, it has been predicted that CMOS will attain its limit in the near future with the channel length of MOS transistor below 10 nm. As the transistor size approaches

sub-10 nm regime, short channel effects and source (S) - drain (D) tunneling occur, posing a challenge in the further scaling of MOS [13, 14, 15, 16].

The physical constraints of device scaling dictate a shift in the elementary building blocks of IC technology. However, in the view of the present research, emerging nano-electronics can permit further device size scaling. The essential elements of present integrated systems are silicon-based transistors and copper/aluminum wires [17, 18, 19]. These wires may be replaced by carbon nanotubes (CNTs) and nanowires (NWs), and the transistors can be replaced by carbon nanotube transistors, thereby resulting in Nanowire-FETs which are suitable to nanoelectronics. Other emerging nanoelectronic devices are tunnel field effect transistor (TFET), single electron transistor (SET), quantum cellular automata (QCA) *etc.* [20, 21, 22]. Additionally, the CNT is used as a transistor component in the carbon nanotube field effect transistors (CNFET). It looks like the channel material (silicon) is replaced by Carbon nanotubes. The carbon nanotube-FET shows inherent characteristics to be exploited in futuristic low power and high-performance circuit design [23, 24, 21].

The nanowire field effect transistor (NWFET) is similar to carbon nanotube field effect transistor except silicon nanowires are used in place of CNTs to form the conductive channel below the gate [25]. The NWFET has gained attention in nanoelectronic research because of several important factors such as high-yield reproducibility, low power requirement, cost-effective fabrication, higher drive current (attributed to reduced scattering) and ability to create radial and axial nanowire structures [1, 26, 27]. Fig. 1.1 shows a simpler schematic of nanowire-FET, where unlike the conventional MOSFET channel material is replaced by nanowires. Besides their various advantages, NWFETs have some challenges too. The alteration in nanowire dimension can cause scattering and degrade the transport of charge carrier with the perturbation in the potential of carrier [1, 28]. Moreover, the change in diameter of nanowire could modify the threshold voltage of FET. In addition to this, compact models are required to understand physics related to the operation of NWFET while considering ballistic transport [29, 30].

Single-electron transistor (SET) is also a promising candidate for the present research area of nanoelectronics that can offer lower power consumption and higher operating speed than MOSFET [2, 31]. SET is a new type of switching device that uses tunneling of the electron in a controlled manner to amplify current [32, 33, 34]. Present research in SET explores novel ideas which can transform the current memory and data storage technologies. Considering Fig.1.2, a single

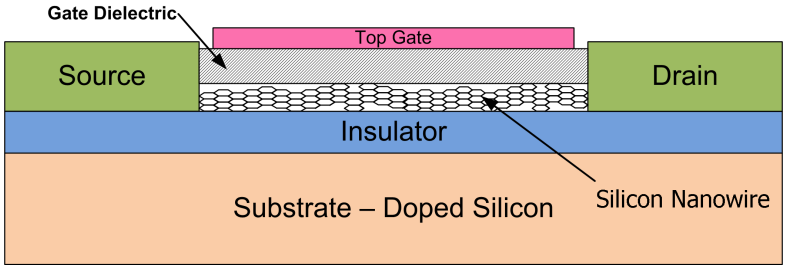

Figure 1.1: Schematic of Nanowire Field effect transistor [1]

electron transistor (SET) consists of an island coupled by two tunneling junctions with a drain and a source terminal, and a capacitor formed at the gate terminal [31, 32]. SET is a new kind of transistor, in which the electrons are restricted to a tiny volume and move by tunneling. Thus, it is the type of transistor that turns ON and OFF, each time one free electron has been added to it [2, 35]. The single electron transistor has very remarkable applications like charge sensor, infra-red detector, ultra-sensitive microwave detector, sensitive electro-meter *etc.* The SET also has as the issue regarding actual implementation. It is difficult to fabricate large quantities of SETs by optical lithography and semiconductor processes. Moreover, another problem with SET is to have the randomness of the background charge which polarizes the island [31].

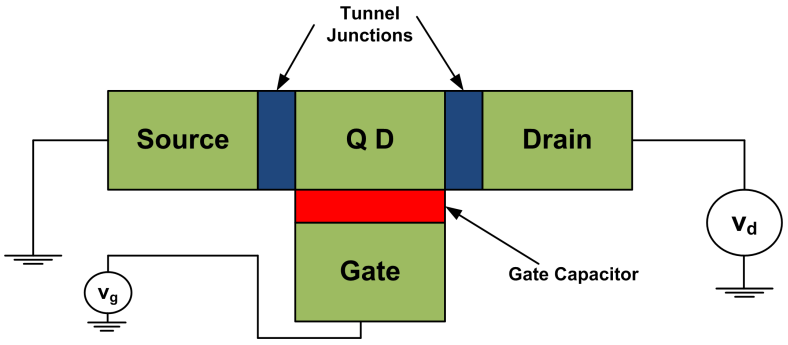

Figure 1.2: A General structure of Single Electron Transistor [2]

Tunnel Field Effect Transistor (TFET) is another promising active device due to not only its high similarity and also compatibility with the existing MOSFET fabrication for VLSI circuits. Because of their potential for sub-60 mV/decade sub-threshold swing, TFETs are suitable for ultra-low power, ultra-low voltage and high-speed operation of next generation VLSI circuits [3, 4]. A simplified structure of tunnel-FET shown in Fig. 1.3(a), it consists of highly doped N regions and undoped middle region. Moreover, the characteristic between the drain current

and gate voltage is shown in Fig. 1.4 which reflects that TFET has the sub-threshold swing less than 60 mV/decade [36, 37, 38]. Further, the significance of small sub-threshold swing is the transistor with better channel control, improved I_{on}/I_{off}, which usually result in less leakage, and less power requirement [4, 3].

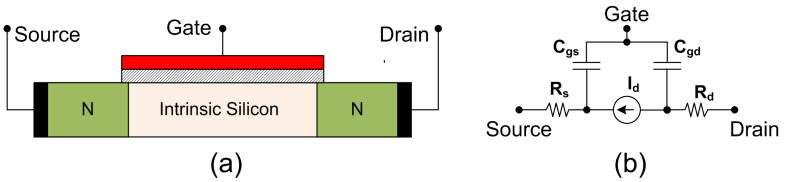

Figure 1.3: (a) Schematics of Tunnel Field Effect Transistor (b) Equivalent Circuit [3]

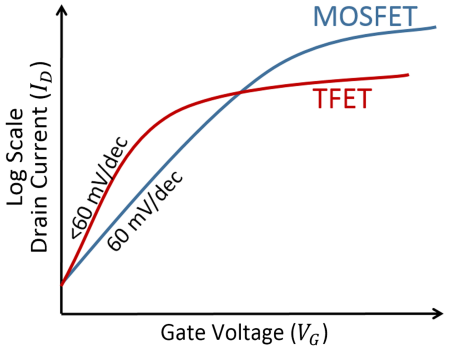

Figure 1.4: $I_D - V_G$ Curve of Tunnel-FET with Sub-threshold Slope Less than 60 mV [4]

Like the MOSFET, TFET has three terminals: source, gate, and drain (but not bulk/body/substrate). Distinct from conventional MOSFETs, where an inverted region (channel) is created to allow conduction, TFETs operate by creating sufficient amount of potential between the source and channel so that charge carriers could tunnel from the conduction band to the valence band from a region to the other. TFET has the drawback of low on-state current, which obstruct the device's performance [4].

A Carbon Nanotube-FET (CNFET) refers to a field-effect transistor that utilizes one or more carbon nanotubes as the channel material in place of bulk silicon in the traditional MOSFET structure. Theoretically, carbon nanotubes are also capable of conducting heat almost as diamond or sapphire, and due to their miniaturized size, the CNFET should switch consistently using much less power than a Silicon device [39, 40]. The CNTs can be metallic or semiconducting as per the arrangement of carbon atoms in the CNT's chirality (twist). Additionally, a CNT

is called metallic if a small amount of energy is needed to excite an electron into a vacant excited state. But, if a finite energy gap exists between the occupied and vacant states, the CNT is said to be semiconducting.

A cross-sectional view of CNFET is given in Fig. 1.5, where the gate electrode is placed above the CNT channel [5]. A thin layer of gate dielectric separates the electrode from the channel. The configuration of drain and source electrodes is similar to MOSFET. Further, N and P-type CNFETs can be taken with the same size as the mobility of electrons and holes in a CNT is equal. Thus, it also helps to solve the matching of transistor sizing in complex circuits [41]. CNFET could be a suitable alternative device to extend conventional Silicon devices. Because it has the properties like higher carrier mobility ($10^4 - 10^5 cm^2/V - s$), strong chemical bonding, better integration of high-K dielectrics, higher thermal conductivity (1700 - 3000 W/mK), and ballistic transport of carrier [42, 43, 44].

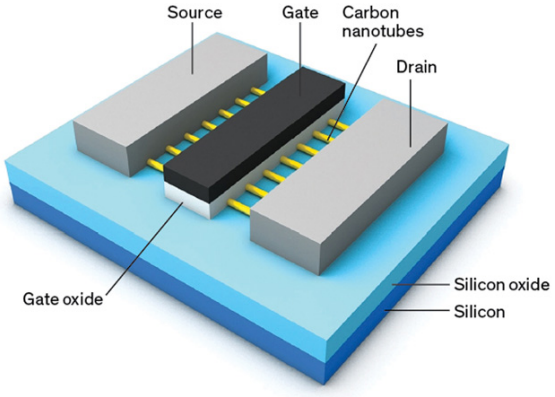

Figure 1.5: A Simplified Cross-sectional View of CNFET [5]

The above emerging technologies have potential to take the place of Silicon CMOS in coming future. The carrier mobility in CNFET, NWFET is higher than Si-MOSFET, which gives fast switching. CNFET and NWFET are 1-D devices which facilitate ballistic transport conduction. The ballistic conduction minimizes the scattering and thus, accomplish better performance than CMOS and other 2-D/3-D devices. However, due to the absence of the dangling bond, CNFET attain easy integration with the high-K dielectric material. All these properties make CNFET a promising device for low-power high-performance circuits in near future [45].

1.2 Motivation

From 2006, 65 nm technology turned into the mainstream, and in 2007, 45 nm technology node came into the picture. Further, as transistor reaches to nano-scale regime, different device non-idealities begin to substantially different I-V characteristics from standard MOSFETs. Thus, it causes a challenging task to improve device performance further by decreasing the gate length [17, 46, 47]. To conquer these issues, device/circuit engineers are exploring novel alternatives to Silicon MOSFET. Recently, device research shifted in the area of nanotechnology and/or nanoelectronics which gives the opportunity to design electronics circuits using emerging & cutting-edge technologies such as carbon nanotube-FET, nanowire-FET, single electron transistor (SET), and Tunnel-FET [20, 48, 49].

The Carbon Nanotube Field Effect Transistor was demonstrated the first time in 1998. The CNT-based circuits have good switching characteristics and small leakage current. For the fabrication of CNFET, an oxide film is constructed in between the gate and the SWNTs which form the channel of the MOS device. Further, the conductive metal contacts on the ends of the SWNTs served as the source and drain. The CNFET is also compatible with existing CMOS technology [50, 51]. The CNFETs exhibit many distinct properties over MOSFET such as high drive current, higher carrier mobility, and integration of high-K dielectric material [7, 52, 53]. Moreover, the band-gap of CNT is directly affected by its chirality and diameter [54, 55]. If these properties could be controlled, CNFETs would be capable candidates for potential nano-scale devices. Moreover, the band-gap of carbon nanotubes can in-principle be varied by synthesizing nanotubes with the suitable diameter which is not possible in MOSFETs [56, 57]. Therefore, a lot of research moved towards conclusively proving the superiority of a Carbon Nanotube Field Effect Transistor (CNFET) over its standard CMOS counterpart [58, 59, 60, 61, 62].

1.3 Problems Addressed in the Thesis

The motivations for reducing power consumption are application-specific. Such as, for mobile phones, the objective is to maintain long battery lifetime and light-weight with reasonable and low-cost packaging. In the case of portable computers such as laptops, the goal is to decrease the power requirement of the electronics portion of the system to a point which is approximately half of the whole power

consumption [63]. The emerging electronic devices such as CNFET, TFET, SET, *etc.* consume less power than CMOS [64, 59]. Among these emerging electronic devices, CNFET has emerged as the most promising candidate for low power integrated circuits.

The carbon nanotube has specific geometrical parameters like chirality and pitch. For example, chirality decides the diameter of CNT, and pitch reflects the distance between two CNTs in a CNT-based device. Therefore, the effect of the CNT parameter variations on the performance of CNFET-device should be investigated. In the view of analog signal processing, the Current conveyor is widely used as the basic building block.

The current conveyor is playing an important role as an active device in different applications such as amplifiers, signal processing, communication, instruments, data converters, *etc.* Various works based on CMOS current conveyor have been presented in the literature. By putting the CMOS issues in mind, it is obvious to explore this active block using CNFET too.

Additionally, active filters play a vital role in signal processing. However, the effect of parasitics dominates at the high-frequencies in the CMOS-based circuits. The issue could be resolved by emerging technologies as they have a less parasitic effect than CMOS. Thus, the design of active filters using CNFET could be explored as a challenging research area. In addition to this, present sensor systems require signal conditioning and interfacing on the same board. It is a growing demand for low-power interface circuits for present sensor technology. So there is a scope to design low-power sensor interface modules based on emerging electronic devices.

Recently, there is a trend to develop active devices with the feature of digitally controlled current/voltage gain. Various CMOS-based techniques have been presented in the literature. Thus, it is still a research problem to develop the CNFET-based digitally programmable active device.

The operational transconductance amplifier is predominately used for physiological signal processing. The $g_m - C$ structures are more flexible than Opamp-RC structures, especially for low-frequency filters. The current demand for ultra-low-power hand-held/wearable applications forced the researchers to look up new design options for next-generation electronics. Thus, the design of an ultra-low g_m transconductance amplifier based on emerging technologies could be a demanding research problem.

The problem addressed in the thesis are described as follows:

1. To analyse of Parameter Variability of CNFET on a Current conveyor block.
2. To realize of the CNFET-based current conveyor and its applications to active filters.
3. To design the CNFET-based differential voltage current conveyor and its applications.
4. To implement of digitally controlled current follower based on CNFET.
5. To design the ultra-low transconductance amplifier using Carbon Nanotube-FET.

1.4 Contributions of the Thesis

To get the benefits of CNFET technology, such as high speed, low power, and minimizing short-channel effects, the circuits should be realized using CNFET. This fact forms the motivation for the work included in this thesis. Implementation of analog circuit for signal processing/acquisition is still an open area of research in this field [65, 66, 52, 67, 68, 69].

As CNFET has three vital parameters such as diameter (chirality), pitch and number of CNTs for the design variability. Therefore, the performance of CNFET is also examined by varying the mentioned parameter of a CNT transistor [70, 71]. Further, an active filter using CNFET current conveyor is designed for the application in the Bluetooth range (2.40 - 2.48 GHz). In addition to this, another design of active filter is proposed which can operate for the ZigBee (868 MHz to 2.4 GHz) applications. Further, a CNFET-based resistive interface circuit is presented which is useful in applications like the potentiometer, strain gauge, photocell *etc.*

Further, in current-mode circuits, to process differential input signals, differential voltage current conveyor (DVCC) is used. The differential voltage current conveyor is a very versatile active device, and its CMOS-based applications are discussed in literature [72, 73, 74, 75]. But, CNFET-based DVCC is realized for the analog circuit applications. The performance of CNFET DVCC is superior to its CMOS counterpart concerning bandwidth and power consumption. Additionally, the digital control feature enhances the functionality of the device.

This work proposed a CNFET based digital control technique for DVCC. An Instrumentation amplifier with digitally control gain is also described. Additionally, CNFET-based DVCC is used to realize an RF filter which could be used for the satellite communication in the Ku-band frequencies.

After that, the work emphasizes on transconductance amplifier design using CNFET. The Operational Transconductance Amplifier (OTA) is a fundamental block for analog signal processing in low-frequency applications. These applications require the design of OTA with ultra-low transconductance (g_m). The processing of biomedical/physiological signal needs filters with very low (sub-Hz to few kHz) cut-off frequencies. The passive filters are not preferred because of the high value of capacitors and resistors, which result in a larger time constant [76, 77]. In this work, a sub-10 pA/V transconductance amplifier is designed using carbon nanotube field effect transistor (CNFET). The digital control feature added to the proposed circuit for tuning the transconductance (g_m) of the amplifier.

1.5 Organization of the Thesis

The thesis is organized in the following manner:

Chapter 2 presents the literature survey. First, details of CNT and CNFET are discussed, and then the overview of CMOS scaling challenges are reviewed. Further, a CNFET-based circuits and their applications are discussed, which also included the merits of CNFET over MOSFET. Moreover, a brief overview is presented on current-mode circuits, active filters, physiological signal acquisition, and sensor interface circuits.

Chapter 3 deals with the realization of the CNFET-based current conveyor. This section is followed by the analysis of the performance of CNFET current conveyor by varying the CNT parameter such as diameter (chirality), pitch and number of tubes. Further, active filters are realized using CNFET current conveyor for Bluetooth and ZigBee applications. In addition to this, a CNFET CCII-based resistive sensor interface is included in the work.

Chapter 4 presents the transistor level implementation of CNFET differential voltage current (DVCC) conveyor. The performance is then compared with CMOS DVCC. Various digital control techniques are described in the literature which have the issues of transistor sizing (NMOS and PMOS) with increased complexity. Here,

a novel CNFET based digitally programmable DVCC is presented. This design uses multiple CNTs to increase the drain current of the transistor. Further, a simplified circuit of Instrumentation amplifier based on CNFET DVCC is described which is further modified with digitally controlled technique. In the last section, a CNFET-based active filter is presented. The filter has covered the entire Ku-band (12- 16 GHz) frequencies, which are used in satellite communication. Finally, the results of proposed work are compared with existing RF filtering circuits at the end of the chapter.

Chapter 5 is based on the designing the ultra-low transconductance amplifier. First, a transconductance amplifier is described which is based on carbon nanotube-FET. The circuit offers very low value of transconductance (g_m) which is very suitable for low-power physiological signal processing circuits. This transconductance amplifier further enhanced with the property of digitally programmable (g_m). The results of the proposed technique are also compared with the existing work.

Finally, **Chapter 6** presents the summary of work included in this thesis. The key findings, important observations, and contributions are also discussed. The future scope of the work is pointed out at the end of the chapter.

Chapter 2

Literature Review

2.1 Introduction

In Chapter 1, the perspective of CNFET for low-power high-performance circuits has been presented which is due to its variety of properties like as ballistic transport conduction, 1-D structure of the band, and higher carrier mobility [78]. The motivation of developing CNFET-based circuits of the current conveyor, transconductance amplifier, and active filters has also been discussed. Moreover, CNFET possesses unique characteristics to control threshold voltage by the diameter of the carbon nanotube. It is also considered as an emerging technology for low power analog designs [79, 80, 81, 82]. The Carbon Nanotube Field Effect Transistor (CNFET) is one of the promising candidate among various nano-scale devices from the point of their integration into future nano-electronic circuits [22, 20, 21].

The design of CNFET based analog circuit is now one of the upcoming research area for modern VLSI Technology. There have been few work reported in the literature but, still, there is a lot of scope to explore the design and optimization of high-performance CNFET based circuits. This chapter gives a brief outline of various circuit (analog/digital) design in CNFET technology.

2.2 CMOS Scaling Challenges

It has been observed that as the MOS transistor moves into the 22 nm node and beyond, considerable technology challenges occurred by silicon device scaling. There are two critical problems, variability in device characteristics and the rising standby power dissipation. Since the last 10-15 years, chip power and power density have appeared as the fundamental problem. Further, device downscaling increases subthreshold leakage current, gate tunneling current, and device temperature. There are some significant challenges related to CMOS such as; (i) Physical Challenges (ii) Material Challenges (iii) Power-thermal Challenges (iv) Technological Challenges (v) Economical Challenges.

2.2.1 Physical Challenges

The physical challenges in CMOS arise because of the rising of tunneling and leakage currents as the transistors are becoming smaller, therefore degraded the

performance of CMOS transistor. Moreover, the scaling of a transistor by a factor x would result in the variation in the transistor parameters, as given in Table 2.1.

Table 2.1: Effect of Transistor's Downscaling on Different Parameters

Parameter	**After Scaling**
Channel Length- L	L/x
Channel Width- W	W/x
Oxide Thickness- $t_o x$	$t_o x/x$
Doping Level- N_A, N_D	$N_A.x, N_D.x$
Supply Voltage- V	V/x
Threshold Voltage- V_{th}	V_{th}/x
Power Consumption/Device- P	P/x^2

However, in future MOS generations will become challenging to scale t_{ox} further because as t_{ox} approaches 1 nm, the leakage current from the gate to channel increases sharply due to tunneling, and power consumption and heat generation become inappropriately large. This problem has gained the interest of the semiconductor industry in high-k dielectrics as a replacement of SiO_2, because these deliver similar capacitive coupling at greater oxide thickness, and thus reduce the gate leakage [14, 83]. Fig. 2.1 reflects the increment in the number of transistors integrated on a microprocessor chip as a function of time. The integration density doubles in approximately every 18 months. The gate length of a transistor is scaled down by a factor of 0.7 in every two years.

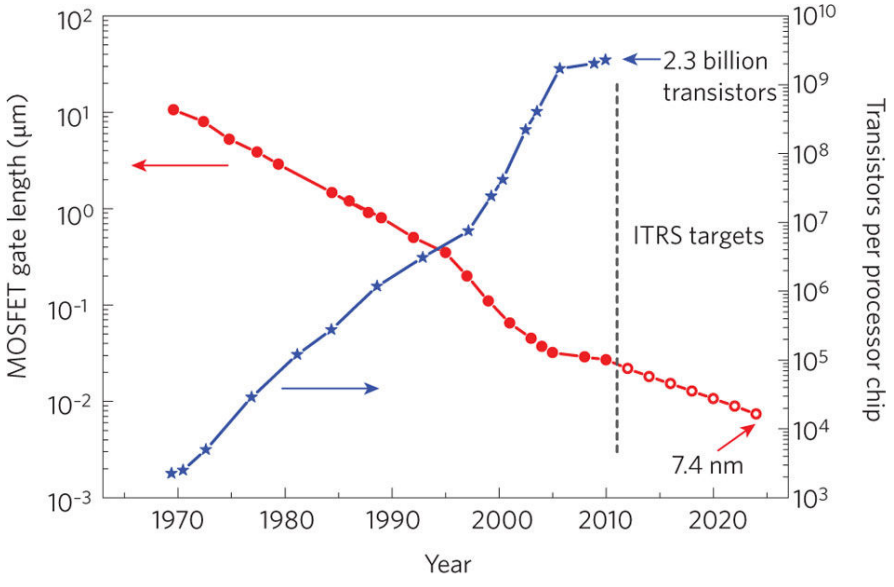

Figure 2.1: Evaluation of MOS Gate Length and Complexity of Microprocessor Chip [Source: ITRS 2014]

2.2.2 Material Challenges

Material challenges come from the inability of the dielectric and wiring materials to provide reliable insulation and conduction, respectively, with continued scaling. The physical capabilities are relative dielectric constant (E), carrier mobility (μ), carrier saturation velocity (V_s), breakdown field strength (E_C), and conductivity. As the materials like Silicon (Si), Silicon dioxide (SiO_2), Aluminum (Al), Copper (Cu), and Silicides reach their physical limit, devices cannot keep up with their performance. The SiO_2 reliability degrades as it becomes thinner and result in breakdown [84]. Carbon nanotubes have superiority over Silicon, such as higher carrier mobility in semiconductor, higher driving current capability, and material stability [7, 52]. Thus, Carbon nanotube-based devices can further persist the material challenges.

2.2.3 Power-thermal Challenges

Power-thermal challenges are because of the ever-increasing the number of transistors integrated per-unit-area; this demands larger power consumption and higher thermal dissipation. The V_{DD} is not reducing as rapid as the channel length (L) of the transistor, thus the power density of the circuit is growing with higher rate. The IC chips dissipate the power, namely dynamic power and static power [85, 86]. Dynamic power is dissipated when the transistor is switched on. The static power dissipation originates from the leakage source-drain current when the transistor is switched off. As can be observed in the literature, CNFET requires less power than CMOS and exhibits lesser leakage current. So, CNFET can be an alternative to minimize the power consumption and thermal dissipation.

2.2.4 Technological Challenges

Technological challenges are the results of the incompetency of lithography-based techniques to provide the resolution under the wavelength of the light to manufacture to MOS devices. CMOS transistors are patterned on the wafer by the process of masks and lithography. Thus, the lithography is one of the primary drivers behind the transistor scaling. Additionally, the lithography processes cannot overcome with the shrinking feature of CMOS transistors layout. The lithography techniques such as proximity X-ray steppers and ion beam are limited by problems in controlling the mask-wafer gap and uniform exposure of photoresists on

the wafer, respectively. Another issue is the inability of the polishing process to maintain the consistent thickness of the wafer and reliable mask [87]. However, as CNFET offers easy integration with present IC process technology, it could be a potential candidate for CMOS alternatives.

2.2.5 Economical Challenges

The cost in the semiconductor sector is contributed by the cost of production, and testing, which is growing exponentially with time as the CMOS size is miniaturizing [14]. The semiconductor industries require huge investment for success in future CMOS scaling. Though, this enormous investment could not guarantee for good profit margin due to the increase in the cost of the production operation and testing. Because of numerous limitations of CMOS alternative devices like CNFET, tunnel field-effect transistor (TFET), nanowire-FET (NWFET), and single-electron transistor (SET) are needed to be the complement or even the replacement to CMOS in future circuits.

Among these listed broad categories of CMOS scaling challenges, the number of effects occurs in the MOSFET nanometer regime which limits the performance [88, 89, 40].
(i) Short channel effects
(ii) High field effect
(iii) Interconnect delays
(iv) Tunneling effects with thin gate oxide

As a result of this, the industry is looking for substitute materials and devices to integrate with present CMOS technology [85, 90]. Additionally, energy efficiency is the significant challenge for the sustrained integration of systems. Issues in transistor scaling combined with requirements of low-power dissipation have forced the research into alternative 'beyond-CMOS' technologies. CNFET emerges as the alternate device to the conventional MOSFET. Referred to as the Carbon Nanotube Field Effect Transistor (CNFET), the device has the potential to be a valuable replacement for CMOS in the future [91, 92, 93, 94].

2.3 CNFET Technology

The carbon nanotube field effect transistor (CNFET) is an emerging technology which can be a suitable alternative to deal with the limitations of present CMOS technology. A CNFET utilizes single or an array of carbon nanotubes (CNTs) as the channel. The CNTs exhibit near ballistic transport of charge carriers which make them excellent channel materials for high-speed and ultra-low-power electronics design [95, 96, 97, 98].

2.3.1 Carbon Nanotubes

Japanese scientist Sumio Iijima discovered the Carbon Nanotube in 1991 [99]. CNTs are cylindrical Graphene's nano-structures with excellent electrical, thermal, and mechanical characteristics. A CNT can be semiconducting or metallic as per the arrangement of carbon atoms in the CNT's twist. Moreover, a CNT is said to be metallic if a little amount of energy is needed to excite an electron into an unfilled excited state. Alternatively, if a finite energy gap exists between the occupied and vacant states, the CNT is known as semiconducting. The CNFETs have several distinctive properties over MOS such as higher mobility in semiconductor tube, higher drive current and easy incorporation of high-k dielectrics. Based on single-walled carbon nanotube (SWNT), carbon nanotube-FET demonstrates better functionality in terms of higher carrier velocity, lesser scattering to their silicon MOSFET counterpart. These circuits have small leakage current and good switching characteristics [100]. Moreover, for fabricating a CNFET, an oxide film is deposited in between the gate and the SWNTs [101, 102]. Additionally, metal contacts are made on either end of the SWNTs to serve as the source and drain. The CNTs based transistors are also compatible with present MOS technology fabrication processes [42].

The carbon nanotubes have commonly two forms, (a) Single-walled carbon nanotubes (SWCNTs) and (b) Multi-walled carbon nanotubes (MWCNTs) as presented in Fig. 2.2. The SWCNTs are tubes of Graphene layer rolled in cylindrical form [6]. The diameter is 1-2 nm and length a few microns (0.2 - 5 μm). The MWCNTs emerge as the coaxial tube with layers of SWCNTs. Their diameter range from 2-25 nm and inter-layer spacing is about 0.36 nm. The performance of SWCNTs is better to MWCNTs, but MWCNTs are easy to produce in large quantity [103].

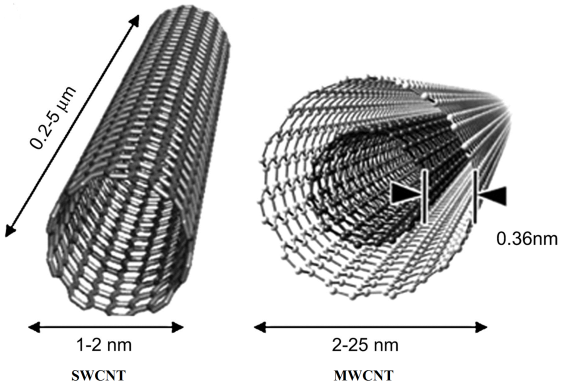

Figure 2.2: Type of CNTs [6]

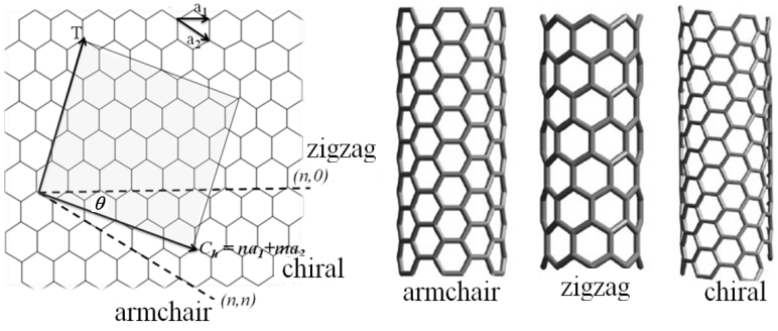

Figure 2.3: Type of CNTs based on Chiral Vector [6]

The SWCNTs are further classified into three types, based on the chiral vector $(m,\ n)$. A CNT is known as zigzag, if $m = 0$ or $n = 0$. If $m \neq n$ and non-zero, CNT is said to be the chiral type, and if $m = n$ as CNT is called armchair, as depicted in Fig. 2.3.

2.3.2 Carbon Nanotube Field Effect Transistor

Carbon nanotube-FET is a kind of field effect transistor that uses one or more CNTs as a channel created between two electrodes namely source and drain. The working principle of CNFET is alike to that of conventional MOSFET. The channel of semiconducting CNTs link the source and drain contacts. The CNT transistor is turned on/off via the gate potential [104, 105]. Fig. 2.4 shows the top view of carbon nanotube field effect transistor. The main design parameters of carbon nanotube-FET, are the number of CNTs in a transistor (N), inter-CNT space (S) and diameter of carbon nanotube (D_{CNT}). The gate length and width are represented by L_{gate} and W_{gate} respectively. The CNT's diameter (D_{CNT}) and

threshold voltage (V_{th}), the width of CNFET-based transistor (W), number of CNTs in channel (N), inter CNT spacing (S) and energy gap (E_g) are related by equations (2.1) through (2.4).

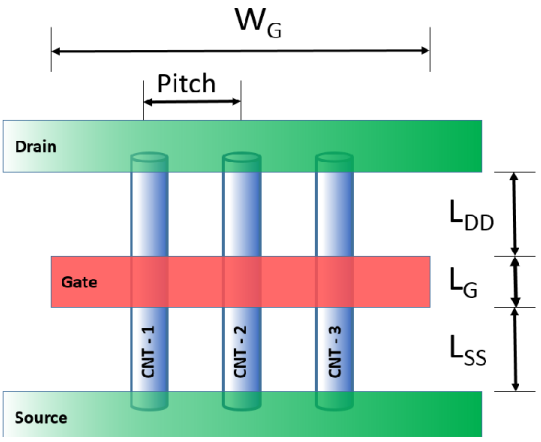

Figure 2.4: Top View of Carbon Nanotube Field Effect Transistor

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \tag{2.1}$$

$$V_{th} = \frac{aV_\pi}{qD_{CNT}\sqrt{3}} \tag{2.2}$$

$$W = (N-1) * S + D_{CNT} \tag{2.3}$$

$$E_g = \frac{0.84eV}{D_{CNT}} \tag{2.4}$$

Here, terms m and n are the indices of chiral vector of Graphene lattice and $a = 2.49\mathring{A}$ (lattice constant). Also, q is electronic charge and $V_\pi = 3.033 \;\; eV$, is the Carbon π-π bond energy.

The drain current of the transistor is represented by (2.5), and it depends upon mobile charge densities (ξ_S & ξ_D) which are given in (2.6) and (2.7). The mobile charge densities of CNFETs are closely related to surface potential (ϕ_S) as given in (2.8).

$$I_D = \frac{4qkT}{h}[ln(1 + exp(\xi_S))–ln(1 + exp(\xi_D))] \tag{2.5}$$

$$\xi_S = \frac{(\phi_S - \delta_1)}{V_T} \tag{2.6}$$

$$\xi_D = \frac{(\phi_S - \delta_1 - V_{DS})}{V_T} \tag{2.7}$$

$$\phi_S = \frac{V_{GS} - qN_{mobile}}{C_{ox}} \tag{2.8}$$

Here, N_{mobile} is the carrier's densities in the channel. Also, (2.9) shows the relation among diameter of nanotube (D_{CNT}), oxide thickness (t_{ox}) and oxide capacitance (C_{ox}) of CNFET with some constants. The relation of thermal voltage is given in (2.10).

$$C_{ox} = \frac{2\pi\epsilon_0\epsilon_{ox}}{ln(2t_{ox}/D_{CNT}) + 1} \tag{2.9}$$

$$V_T = \frac{kT}{q} \tag{2.10}$$

Here, δ_1 is the equilibrium sub-band minima of first sub-band ($E_G/2$). The constant terms q, k, h and T represent charge of electron, Boltzmann's constant, Planck's constant and absolute temperature receptively, while V_{GS} and V_{DS} are the gate-source and drain-source voltages of the CNFET model [106, 107].

The merits of CNFET which make it a promising candidate for high efficient electronics circuit design can be summarised as:

1. It possesses high carrier mobility (10^4-10^5 cm^2/V-s) in CNTs which gives high ON current (>1 mA/μm).
2. CNFET has long scattering mean free path (approx. 1 μm) which offers lower delay & less heating.
3. It has high thermal conductivity (1700-3000 W/mK) and chemical stability which results in high current density (approx. 10^{10} A/cm^2).
4. The property of easy integration with high-k dielectric material leads to better gate electrostatics.

5. CNFET exhibits excellent matching of (complimentary) N and P-type CNFETs with equal sizes having same carrier mobility which gives similar drive currents. It is very beneficial in the prospects of transistor sizing of complex electronic circuits.

CNFET has following limitations which avoid its usage in commercial applications. The following problems are mentioned:
(i) The problem of CNT misalignment
(ii) The issue of Metallic-CNT growth
(iii) CNT diameter and density variation

Table 2.2: Technology Parameter and their Nomenclature for CNFET

Parameter	**Description**	**Value**
L_{ch}	Physical channel length	32 nm
L_{geff}	Mean free path in the intrinsic CNT channel region	100 nm
L_{ss}	Length of doped CNT source-side extension region	32 nm
L_{dd}	Length of doped CNT drain-side extension region	32 nm
E_{fi}	Fermi level of the doped S/D tube	0.6 eV
K_{gate}	Dielectric constant of high-K top gate material	16
T_{ox}	Thickness of high-K top gate dielectric material	4 nm
C_{sub}	Coupling capacitance between the channel & substrate	40 pF/m
V_{fbn}	Flat band voltage for n-CNFET	0.0 eV
V_{fbp}	Flat band voltage for p-CNFET	0.0 eV
$L_{channel}$	Physical gate length	32 nm
Pitch	Distance between the centers of two adjacent CNTs	20 nm
L_{eff}	Mean free path in p+/n+ doped CNT	15 nm
phi_M	Work function of Source/Drain metal contact	4.6 eV
phi_S	CNT work function	4.5 eV

Various CNFET device model are proposed in the literature [108, 107, 109, 110, 111, 112]. In this thesis, Stanford CNFET model [109] with 32 nm technology node is used to design CNFET-based circuits for different applications. This model is designed Carbon nanotube-FET which used one or more carbon nanotube as the channel of the device. The model has considered the scattering effect, parasitics, source/drain, & gate resistances and capacitances, back-gate effect, Schottky barrier effect, *etc.* Table 2.2 includes the CNFET technology parameters and their numerical values.

2.4 Review of the CNFET-based Circuits

The properties of carbon nanotubes (CNTs) have also been verified experimentally. The ON-current of CNFET is controlled by the height of Schottky barriers at metal/nanotube interface. At low frequencies, the current fluctuations are dominated by 1/f noise. It also correlates with the number of transported carriers [113]. Further, Bandaru [114] presented a study on the electrical properties of carbon nanotubes which are studied with the phenomena like thermoelectricity, superconductivity, electroluminescence, and photoconductivity. The study also provides information on the transistor application, high-frequency nano-electronics, field emission and biological sensing related to CNTs [115].

In addition to this, the carrier velocity in CNT is two times than Silicon due to ballistic conduction and the band structure. The band gap of a CNT is inversely related to its diameter. Thus, CNTS with the small diameter can be used for electrical switching/transistor associated applications [116]. Additionally, the property of chemical inertness of CNTs helps to reduce the effects such as surface recombination, leakage current, and sub-threshold conduction [117, 118, 119, 120].

Further, the work [121] investigated the effect of major CNTs process related imperfections on the circuit level performance. These are the doping variation in CNFET source and drain regions, CNT diameter variations and variations due to the removal of metallic CNTs. The results show that metallic CNTs should be less than 8% of total grown CNTs and CNTs density should be 250 CNTs/μm to ensure the performance [122, 61].

Thus, the electrical properties of CNTs give the opportunity to the designers to come up with the integration of CNTs with the transistor. Kim [123] has presented the scope of CNFET technology among various emerging nano-electronics technologies. The CNFET technology can take over the existing CMOS technology due to certain reasons; (a) operation principle and device structure are similar to CMOS (b) the fabrication process is compatible with CMOS (c) the existing infrastructure can be reused by CNFET. The study of the electronic structure and carrier transport properties of CNT has been illustrated [124]. The work discussed the fabrication of CNFET and further included performance characteristics of CNFET which are then compared with CMOS. The work also describes the growth mechanism of SWCNTs without the use of a metal catalyst. The results predict that CNFET has better performance than existing silicon devices.

2.4.1 Overview of CNFET Experimental Results

The early work on the fabrication of CNFETs was reported on individual single – and multi-wall carbon nanotubes in 1998 [125]. The conduction started at room temperature, and it would be diffusive but not ballistic. The conductance of single-wall CNFET could be raised by greater than five orders of magnitude. The transfer characteristic revels that it has higher carrier density than Graphite. Moreover, large diameter multi-wall CNTs exhibit no gate effect on it, but structural deformation can achieve FET like characteristic. Further, Sander J. described the fabrication of CNFET with one semiconducting single-wall carbon nanotube [126]. The device operates at room temperature. The transistor characteristics can be explained by the semi-classical band-bending models.

Javey [103] presented the modification in the nanotube-metal junction to reduce Schottky barrier in 2003. The contacts of single-walled CNT made by Palladium (high work function material) which reduced the barriers to transport the valence band of nanotubes. Semiconducting CNT behaves like ohmically contacted ballistic metallic tube and conductance near ballistic transport limit of $4e^2/h$ (Current carrying capacity 25 μA/tube). Javey started the use of CNTs on the interconnect which explored the fabrication of CNFET with ohmic contacts and high-K dielectrics [122]. The CNFET with HfO_2 as the gate insulator, ohmic metal-tube contacts, and electro-statistically doped nanotube segments as source/drain exhibits higher ON and lower OFF currents. The sub-threshold swing of approximately 70-80 mV/decade has been achieved.

2.4.2 CNFET Simulation and Modelling Work

The performance of CNFET circuits based on simulation and modeling is presented in the literature [127, 56, 109]. The models demonstrate better performance results over CMOS circuits. Deng [109] proposed a full device model which was circuit compatible with an intrinsic channel region of single-walled CNFET in 2007. The model includes the non-idealities like quantum confinement effect on circumferential and axial directions, acoustic and optical phonon scattering in channel and screening effect by parallel CNTs. The results illustrate thirteen time CV/I improvement of intrinsic CNFET over the bulk n-type MOSFET with 32-nm node. This model was SPICE compatible and reported as SPICE-based CNFET model. After that various works have been reported on SPICE/HSPICE-based CNFET models [128, 129, 130].

Luo [131] presented a semi-analytical CNFET model which was based on the virtual-source model. The model calibrated with 9-nm gate length experimental data and included series resistance, parasitic capacitance, direct source-to-drain tunneling leakage, *etc.* The source-to-drain tunneling in CNFET causes the leakage current while contact resistance plays a key role to limit the performance. The device performance of 7-22 nm technology nodes has been presented, and it is analyzed that gate delay can be improved by 10% at 11 nm and 7 nm technology nodes as compared with 30% transistor dimensions scaling. Wong [132] has given two models for carbon nanotube transistors. The first model is based on SPICE while second on Schottky barrier model. The SPICE simulation used for circuits based on CNFETs. The Schottky barrier model is more suitable for device design and performance optimization.

Additionally, Sebastien [133] explored a physics-based compact model for MOSFET-like CNFET. The model includes the channel of CNFET, and Boltzmann Monte Carlo simulation is performed to cross-link it with compact modeling formulation. The model also determines the threshold voltage distribution using study of CNT diameter dispersion. Kazmierski [134] proposed an algorithm (of implementation) of a numerically efficient CNFET model in HSPICE. The model is based on cubic spline non-linear approximation of the non-equilibrium mobile charge density. The I-V characteristics of the proposed model are compared with existing Stanford HSPICE model. The model shows better accuracy with same CPU time performance. This work explored the performance by ballistic as well as non-ballistic effects. The HSPICE based modeling opens wide opportunity to explore the CNFET-based analog and digital circuits.

Further, Yamacli [130] added the SPICE compatible interconnect and CNFET models in Verilog-A. It is explained that metallic CNTs show current saturation above a threshold voltage. This effect is modeled with piecewise linear functions. CNFET model uses the calculation of the self-consistent potential of the CNT channel which depends on the gate and drain voltages.

2.4.3 Brief Discussion on CNFET Circuit Applications

The SPICE-based models help the circuit designers to explore the wide utility in designing high-performance low-power circuits using CNFETs. Various applications of CNFET-based analog and digital circuits have been investigated [135, 44, 136, 50, 57, 137, 138, 139, 140, 141]. A comparison of MOSFET and

CNT based transistor has been presented on the performance parameters like current drive strength, the current on-off ratio (I_{ON} /I_{OFF}), energy-delay product, and power-delay product for logic gates [135]. The results show that nanotubes can significantly reduce the drain-induced barrier lowering effect and subthreshold swing in the channel. The CNFET based design has less parasitic capacitances than CMOS. The CNFET and MOSFET design rules are taken for compatible to 45-nm technology node.

In 2009, a methodology to optimize the CNFET parameters presented [24]. This methodology achieved the optimum performance regarding the fan-out factor, delay, and power consumption. The proposed method provided 56% reduction in dynamic power and 22% less delay by using optimum pitch and number of CNTs. Cho et al. [44] compared the performance of logic gates using CMOS and CNFET. The results show that CNFET-based gates have ten times lower delay than CMOS. Additionally, leakage power and power delay product are also improved. These performances are also achieved during PVT variation.

Further, Kureshi [50] compared the feature of CMOS and CNFET based 6T SRAM cell. The results predict that CNFET memory cell has 21% improvement in reading static noise margin. Further, standby leakage of CNFET cell is 84% less than CMOS design. The SRAM using CNFET is 1.84 times faster than CMOS. Another work on the comparison of SRAM in CMOS and CNFET technologies is presented by [136]. The results show that Static-Noise-Margin of SRAM increases 52.7% using CNFET with 5% faster cell. It indicates that CNFET is more suitable for circuit design than its CMOS counterpart.

In addition to this, Moaiyeri [141] proposed a high-speed full adder for the low-voltage application using CNFET. The circuit has a short critical path as it uses only two CNT pass-transistors. The work also utilized the property of CNT diameter variation to adjust the threshold voltage of the CNFET device. The results show that CNFET based design is better regarding speed, power consumption, and PDP than CMOS design. Besides the digital circuits discussed in the literature, a variety of works on analog design using CNFET have also been explored.

An Op-Amp based Inverting amplifier using CNFET has been investigated [138]. It presented the design of an inverting amplifier using CMOS, CNFET, and hybrid technologies. It concludes that CNFET amplifier has good amplification and that the hybrid (pCNFET-nMOS) amplifier provides better frequency response. Moreover, pMOS-nCNFET exhibited better transient response than CMOS.

Further, CCII is realized using CNFET [60]. The result showed that CNFET-based CCII gives the better high-frequency response and also consumes lower power than CMOS.

Moreover, the analysis and comparison of a carbon nanotube-FET based 10μA current mirror had been presented with MOSFET for 32 nm technology node [137]. A comparison showed the superiority of the CNFET design in terms of 97% increase in output resistance, 24% decrease in power dissipation and 40% decrease in minimum voltage required for constant saturation current. Sun et al. [142] explored the electrical characteristics of 16-nm N-type CNFET. It examined the variation in on-state to the off-state current relation from the different number of CNTs. The work also investigated the effect of substrate voltage on the device performance. It also suggested the technology development guidelines for high-speed, low-leakage, area efficient CNFET based circuits.

Rahman [143] presented the design of elliptical filter using CMOS and CNFET based Op-Amp. Further, results showed that CNFET based filter achieved higher phase margin and improved power dissipation. There would always be a trade-off between the number of CNTs against power consumption. If the number of CNTs is large, then there would be more power consumption. Another application of CNFET based four-quadrant analog multiplier is proposed by [139]. The results showed that CNFET based design was superior to it CMOS design regarding % THD, input range, and bandwidth. Further, in 2012, Possani [144] proposed the CNFET based operational transconductance amplifier and compared with CMOS. CNFET based transconductance amplifier consumes less power than CMOS. The work was done on simulation-based optimization engine (UCAF).

Hayat [57] presented the comparison between CMOS and CNFET based circuits such as the inverter, ring oscillator, and LC oscillator. CNFET based inverter has 10-times faster than CMOS and ring oscillator can perform three times higher oscillation frequency than its CMOS counterpart. Another important work presented on the effect of oxide thickness on gate capacitance in various devices like single and double gate MOSFET, silicon nanowire-FET and CNFET [145]. The results show that CNFET and silicon nanowire-FET have the characteristics of decreasing gate capacitance with the reduction in oxide thickness in deep nanometer regime. It is not possible in single or double gate MOSFET. The CNFET and nanowire-FET also have lower leakage current compared to MOSFET.

In the view of above discussion, it is concluded that there is still a lot of scope in the designing of CNFET-based analog circuits for signal processing/acquisition

applications. From the literature, it is found that the CNFET can be explored for the application areas covered in subsequent sections.

2.5 Brief Discussion on Current conveyor

Since their introduction in 1968 by Sedra and Smith and subsequent modification, current conveyors have proved to be functionally versatile, quickly getting recognition as both a theoretical and practical analog device [146, 11, 9, 147].

Current conveyor is a very versatile building block and can be used to realize voltage-mode and current-mode circuits [10, 148, 149, 150]. At present, some current-mode circuit techniques such as current conveyors (CCs), operational and transconductance amplifiers (OTAs) *etc.* have been developed [151, 152]. In these techniques, the Current conveyors have proved to be a functionally flexible and versatile current-mode building block.

The second generation current conveyor (CCII), a variation of the current conveyor, has been presented [11]. It is a multipurpose current-mode (CM) analog building block which has gained recognition as a versatile active element. The CCII, with a high impedance input port, one low impedance input terminal and a high impedance output port, is suitable for both voltage-mode (VM) and CM electronic circuits. Further, a variant of current conveyor named the second generation inverting current conveyor is proposed. The second generation inverting current conveyor (ICCII) has become very useful for implementing a wide range of electronic functions in voltage-mode or current-mode because of their high performance and versatility [12].

However, CCII/ICCII are not suitable for differential input signals, as they have the one high impedance node (Y). The differential voltage current conveyor (DVCC) filled this gap, as DVCC has an extra Y terminal to manage differential inputs [153]. The details of the active building blocks are discussed in the subsequent chapters of the thesis. The mentioned variants of current conveyor were realized using CMOS. Thus, in this work, the implementation of Inverting Current Conveyor (ICCII) using CNFET is included which is further extended to be used in different analog applications.

2.6 Overview of Active Filters using Current Conveyor

As the name reflects, active filters have components such as operational amplifiers, OTA or Current Conveyor, *etc.* in their circuit design. They take their power from an external source and employ it to enhance or amplify the output signal. Filters play a significant role in an electronic system such as telecommunication, consumer electronics, radar, instrumentation systems, *etc.*

Since 1950's it was documented that significant size and cost reduction could be accomplished by replacing large and costly passive inductors with active circuitry. But, active components as operational amplifiers developed commercially accessible up to mid of 1960's. These filters also use other active devices such as operational transconductance amplifiers (OTA), current conveyors, *etc.* with capacitors and resistors in their feedback loops. Active filters are easier to design than passive filters. The key advantage of these filters is that they do not have inductors so that they can reduce the problems associated with inductors.

The design of active filters using current conveyor is the interest from last two decades. Several recent VM and CM circuits have been discussed in literature [154, 148, 150, 155]. In 2012, Horng et al. proposed a cascadable current-mode universal filter using only two active elements and grounded capacitors [154]. A voltage-mode fully differential biquadratic filter was proposed with the advantage of digital control of filter parameters [148]. Also, a high order current-mode filter was proposed in [156] using CCII. The circuit is useful to perform all filter functions without any component matching conditions. Additionally, the circuit having low input and high output impedances. A differential voltage current conveyor (DVCC) based VM filter has been proposed [150] having only grounded components with orthogonal control of resonant angular frequency and condition of oscillation. Also, a current-mode universal filter with low total harmonic distortion (THD) and tuning through external currents is reported [155].

2.7 Brief Overview on Sensor Interface Circuits

The present era of sensor technology requires interface circuits to have less chip area, ultra-low power consumption and the possibility of integration on a monolithic substrate. Integrated sensors, which are mostly electronic and sometimes

electro-mechanical, can be put in the broader class of mixed-signal systems in which the interface circuitry is analog, and the processing is performed in a digital environment [157, 158].

Sensors generate a continuous output signal or voltage/current which is usually proportional to the quantity being calculated. For example, the physical quantities like temperature, displacement, speed, pressure, strain, *etc.* are all analog quantities as they are liable to be continuous. These signals are likely to be very small in the range of few micro-volts to several milli-volts. Thus amplification of these signals is essential. The analog sensors, generally required amplification (gain), impedance matching, isolation between the input & output and filtering before the final output for reading. These mentioned tasks are performed by active elements such as Op-Amp, Current conveyor, OTA, *etc.* [159, 160].

2.8 Research Gaps & Scope of this Work

1. The MOSFET technology is about to reach its scaling limits. So there is a lot of scopes to explore new technologies for high-performance devices. Various emerging technologies have arisen such as CNFET, Tunnel-FET (TFET), Single Electron Transistor (SET), *etc.* CNFET technology is one of the promising candidates for future electronics.

2. As discussed in the literature that CNFET has unique parameters like pitch, diameter, and number of CNTs to enhance/alter the performance of the device. So, testing the variability of these parameters can be explored for the research work.

3. The works based on logic design, analog, and digital circuits using CNFET have been published in the literature, yet there is a significant scope in developing CNFET-based circuits in the analog domain. We have focused on active filter design and analog signal processing applications. Moreover, today's smart sensor systems need signal conditioning and interfacing circuits within the sensor board. So, the design of low-power sensor interface circuits could give an opportunity to explore the research work in this domain also.

4. Recently, there is a demand to develop digital control/programmable techniques using active devices. Various MOSFET-based techniques have been presented in the literature. Thus, it is still a research problem to develop the CNFET-based digitally programmable active devices.

5. The operational transconductance amplifier is predominately used for the physiological signal processing. The $g_m - C$ structures are more flexible than Opamp-RC structures, especially for low-frequency filters. The current demand for ultra-low-power hand-held/wearable applications forced the researchers to look up new design options for next-generation electronics. Thus, the design of an ultra-low g_m transconductance amplifier based on emerging technologies can be a demanding research problem.

6. In this work, HSPICE software is used to simulate the circuits. Further, CNFET 32 nm model parameters are taken from Stanford University.

Chapter 3

CNFET Current Conveyor: Design & Applications

3.1 Introduction

The Current Conveyor was commenced in 1968 by Sedra and Smith. After subsequent modification, it has proved to be functionally flexible and versatile, building block used in analog and digital domains efficiently [161, 162, 163, 164]. The current conveyor plays an important role in designing the voltage-mode (VM) and current-mode (CM) circuit applications. However, current-mode circuits outperform the voltage-mode circuits regarding inherently wide bandwidth, greater linearity, simpler circuitry, wide dynamic range, and lower power consumption [165]. Current conveyor is also appropriate for integration with CMOS process technology [166, 167]. CMOS-based circuits were very popular from the last few decades eventually approaches its scaling limit. Hence CNFET-based circuits may be utilized for better performance, especially in very high-frequency applications [168, 128].

3.2 CNFET-based Current Conveyor

The inverting current conveyor (ICCII) was introduced by Soliman *et al.* to realize the CM circuits from their VM counterparts [12]. The block diagram of ICCII is shown in Fig. 3.1, it has a high-impedance input, a low-impedance input, and two high-impedance output terminals. Therefore it becomes suitable for voltage-mode as well as current-mode circuit designs. The driving equation of inverting current conveyor is given in equation (3.1).

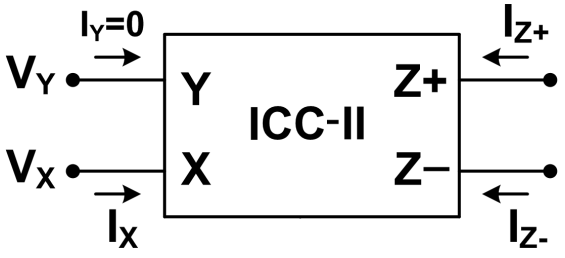

Figure 3.1: Circuit symbol of ICCII

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z-} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.1}$$

The MOS technology has severe performance issues which can be solved by emerging CNFET technology [169, 60]. The CMOS realization of ICCII has been discussed in the literature [12, 170]. In proposed work, CNFET-based implementation of Current conveyor is presented as shown in Fig. 3.2. The design uses SPICE-based 32 nm CNFET model, developed by Stanford University [169]. Some important model parameters are given in Table 3.1.

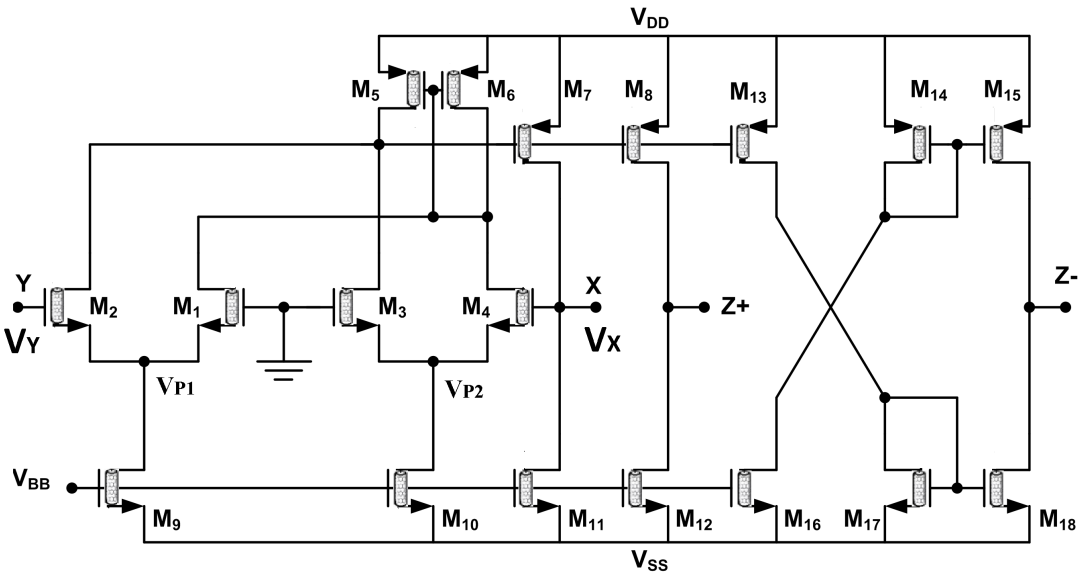

Figure 3.2: Transistor Level Realization of ICCII with one Z+ and one Z− output

Table 3.1: CNFET Design Parameters

Parameters	**Value**
Oxide Thickness (T_{ox})	4 nm
Dielectric Constant (K_{ox})	16
Power Supply	±0.9 V
Chirality of the tube (n, m)	19, 0
Physical channel length (L_{ch})	32 nm
No. of tubes in the device	6
Pitch (S)	14 nm
Diameter of CNT (D_{CNT})	1.5 nm

In Fig. 3.2, the transistors M_5 and M_6, work as a current mirror which is set to drive two differential amplifiers consisting of transistors M_1 & M_2 and M_3 & M_4. Additionally, transistors M_7 and M_{11} offer the feedback action to create the voltage V_X independent of current drawn from the node X. The current in terminal X is conveyed to the $Z+$ terminal with the help of transistors M_7, M_8, M_{11} and M_{12}. By extra current mirror stage (M_{13} - M_{18}), the current is conveyed in an inverted manner to the $Z-$ terminal.

Moreover, the sum of drain currents of M_1 and M_4 is equal to drain currents of M_2 and M_3. Further, since transistors M_9 and M_{10} are biased with equal gate voltages (and since their source voltages are also equal), they would have equal drain currents. For matched M_9 and M_{10}, this would result in $V_{P1} = V_{P2}$. Thus, the equation for node voltages of two differential pairs can be written as (3.2). After solving, the relation between X and Y nodes presented as (3.3).

$$V_Y - V_{P1} + V_{P1} - 0 = 0 - V_{P2} + V_{P2} - V_X \tag{3.2}$$

$$V_X = -V_Y \tag{3.3}$$

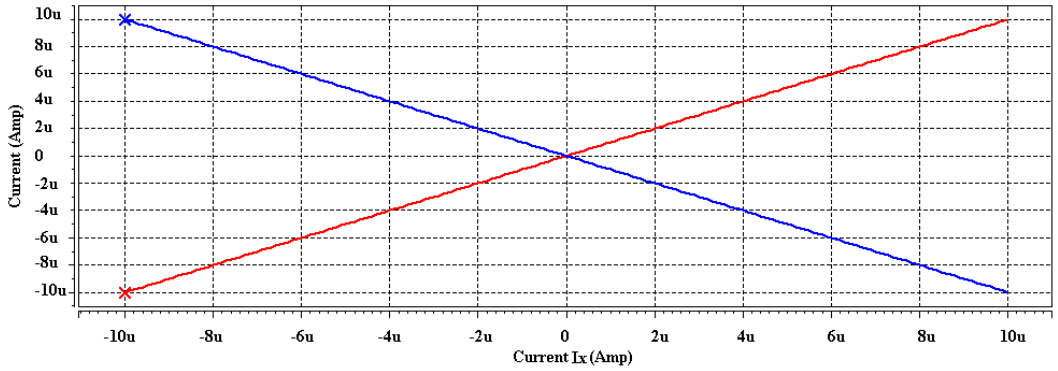

Figure 3.3: Current transfer characteristics at 32 nm

The performance of the circuit of Fig. 3.2 is tested through HSPICE simulation with 32 nm CNFET model parameters. The power supplies were kept at ±0.9 V. The AC, DC and transient characteristics of node voltages and currents have been verified as per (3.1).

First, the input-output DC current transfer characteristics of $Z+$ and $Z-$ terminals with respect to a current input swept at the X terminal, are shown in Fig. 3.3. The relations $I_{Z+} = I_X$ *and* $I_{Z-} = -I_X$ are verified.

Fig. 3.4 gives the frequency response of voltage gain between terminal X and Y. From the results of the AC analysis, it may be observed that the proposed CNFET-based ICCII exhibits the 3-dB bandwidth 19.28 GHz. This implies that the device is suitable for both voltage-mode and current-mode for high-frequency circuit applications.

Lastly, the transient analysis is also carried out to verify the functionality of the proposed analog building block. Fig. 3.5 illustrates the input-output voltage responses and is found to satisfy the relation $V_X = -V_Y$.

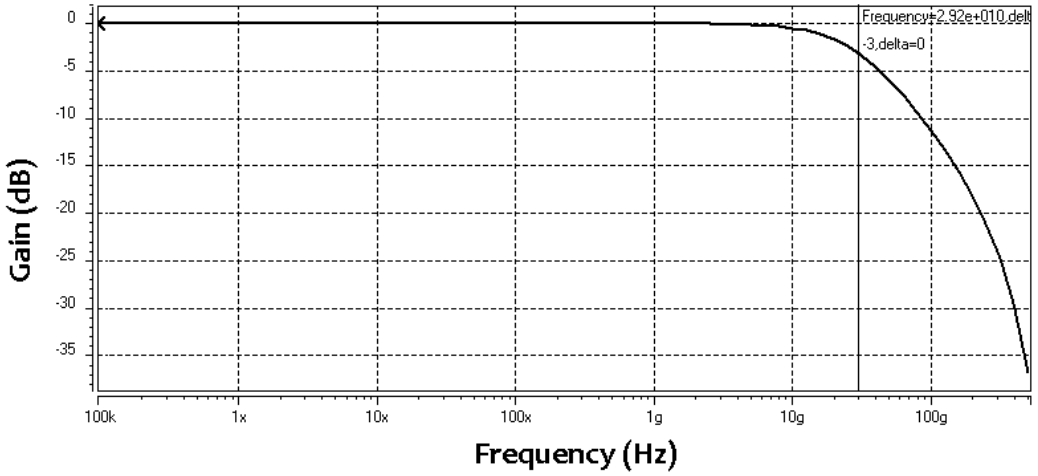

Figure 3.4: Simulated frequency response of voltage gain (V_X/V_Y) for the proposed CNFET-based ICCII

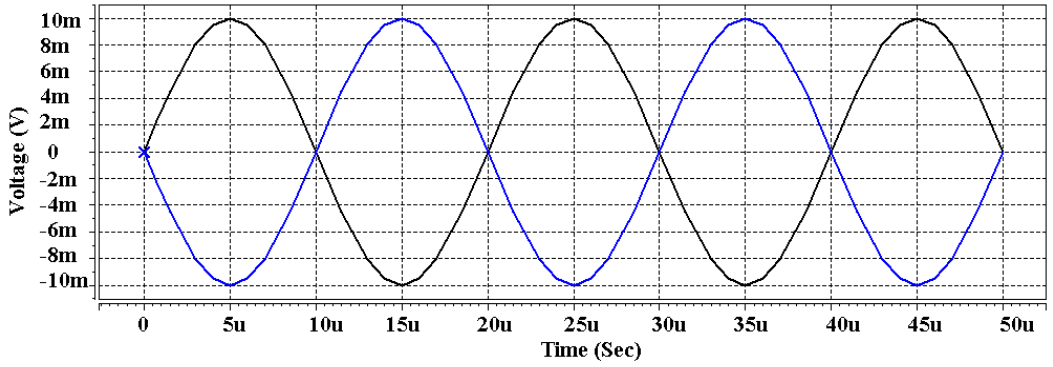

Figure 3.5: Result of transient analysis of relevant node voltages for the proposed CNFET-based ICCII

The simulation results of current transient responses are shown in Fig. 3.6 (depicting I_X and I_{Z-}) and Fig. 3.7 (depicting I_X and I_{Z+}), from where the relations $I_{Z-} = -I_X$ and $I_{Z+} = I_X$ are verified.

The results of HSPICE simulations are presented which confirm the desired operation of the proposed ICCII. The CNFET-based implementation of Current conveyor has higher bandwidth than their CMOS counterparts as given in Table 3.2.

3.3 CNT Parameter Variability Analysis

Various parameters like diameter of CNT (D_{CNT}), threshold voltage (V_{th}) *etc.* are considered in the design of CNFET-based devices. The important relations are

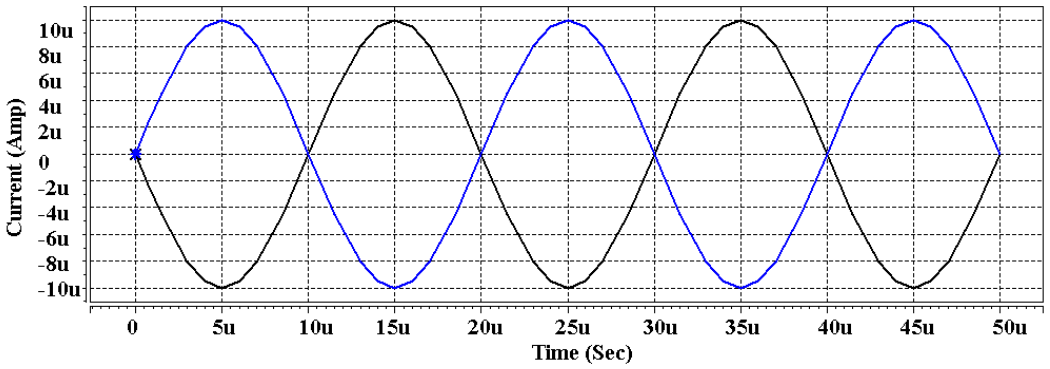

Figure 3.6: Result of transient analysis of current transfer from the X to $Z-$ terminal for the proposed CNFET-based ICCII

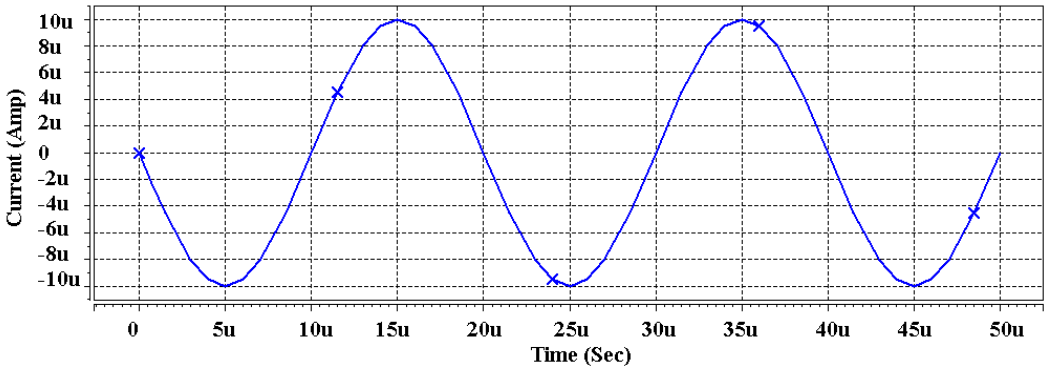

Figure 3.7: Result of transient analysis of current transfer from the X to $Z+$ terminal for the proposed CNFET-based ICCII

presented in equations (3.4), (3.6).

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \tag{3.4}$$

$$V_{th} = \frac{aV_{\pi}}{qD_{CNT}\sqrt{3}} \tag{3.5}$$

$$E_g = \frac{0.84eV}{D_{CNT}} \tag{3.6}$$

Also, the width of CNFET-based transistor (W), number of CNTs in channel (N), and inter CNT spacing (or *pitch*) (S) are related by equation (3.7) and illustrated in Fig. 3.8.

Table 3.2: Performance of CNFET- and CMOS-based Current Conveyor

Parameters	**CMOS**	**CNFET**
Model/Node	PTM/32 nm	Stanford/32 nm
V_{DD}	$\pm$0.9 V	$\pm$0.9 V
No. of Transistors	18	18
Power Requirement	3248.2 μW	390 μW
3-dB Bandwidth	4.75 GHz	19.28 GHz

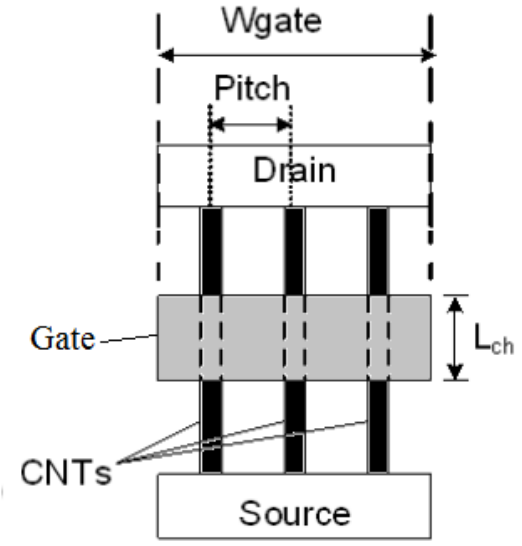

Figure 3.8: Schematic of a CNFET

$$W = (N-1) * S + D_{CNT} \tag{3.7}$$

The terms n and m are the indices of chiral vector of Graphene lattice and $a = 2.49\ \mathring{A}$ (lattice constant). Also, q is electronic charge and $V_\pi = 3.033$ eV, is the π-π bond energy of Carbon.

The parameter variability analysis is useful because the structural parameters of the CNTs affect the device performance and should be chosen carefully. The number of CNTs in the channel relates the driving current for capacitive loads. Pitch of CNT also affects the performance of a device. The diameter of CNT is key parameter as the threshold voltage of the device is directly controlled by it.

3.3.1 Variation in the Diameter of CNT

The diameter of the carbon nanotube is a physical property that closely depends on the indices of Graphene lattice (n, m) given in (3.4). The single-walled CNT is obtained from the Graphene layer, and its diameter has the impact on the threshold voltage and band gap of the device as shown in (3.5) and (3.6). The modification of band gap in MOS transistor is critical, but in CNFET, it can be controlled by the diameter of the nanotube. The width of the transistor also depends on the diameter of CNT [128].

As discussed earlier, the diameter of CNT affects various parameters of CNFET, and it has the impact on the performance of CNFET-based inverting current conveyor. Results show that 3-dB bandwidth of the device is improved by increasing the diameter as illustrated in Fig. 3.9. Because the transconductance also sets up with the decrement in the threshold voltage. The threshold voltage reduces with the increment in CNT diameter.

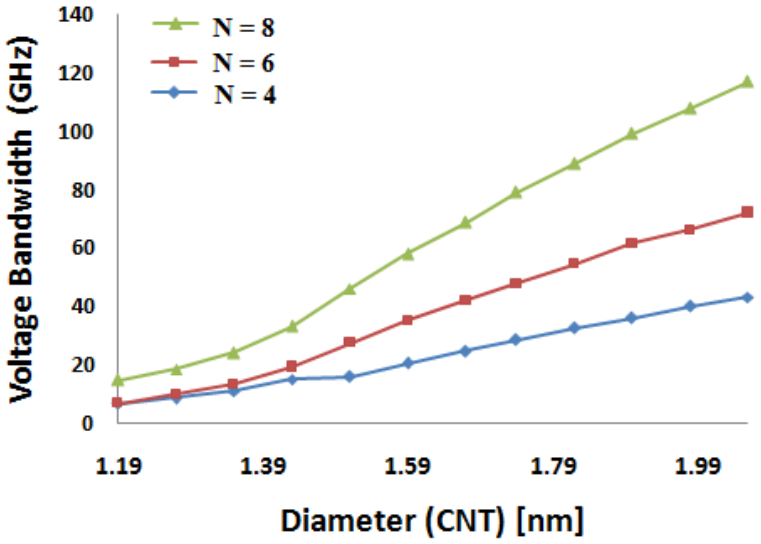

Figure 3.9: CNT Diameter versus 3-dB Voltage Bandwidth with the Number of CNT

3.3.2 Variation in the Number of Tubes

It is also attempted to see the effect of variation in the number of tubes with the 3-dB bandwidth of the device. Fig. 3.9 shows that 3-dB voltage bandwidth enhanced with the increase in the number of tubes. The number of tubes in the

channel controls the current supply for the load [171, 172]. A transistor with single-CNT could not provide sufficient current to meet the desired performance. This is because parallel CNTs enhance the driving capability of the transistor which results in a substantial increase in the transconductance.

Fig. 3.10 gives the effect of the number of tubes variation on the 3-dB current bandwidth of building block. The power requirement is an important issue in modern low power nano-scale circuit design.

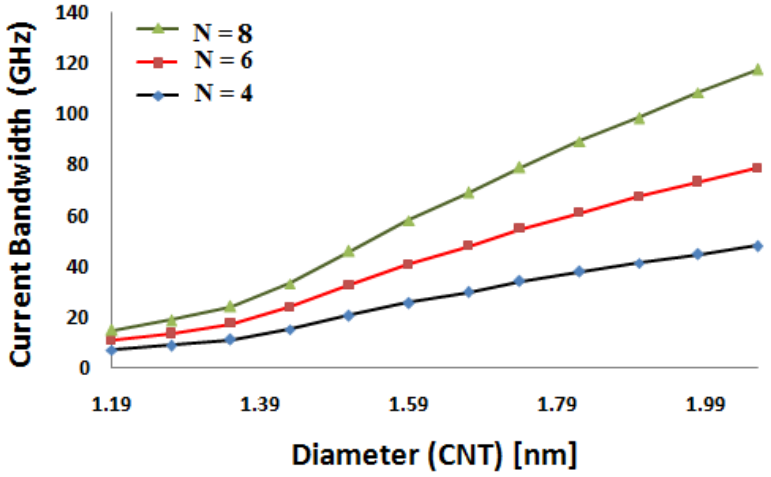

Figure 3.10: CNT Diameter versus 3-dB Current Bandwidth with the Number of CNT

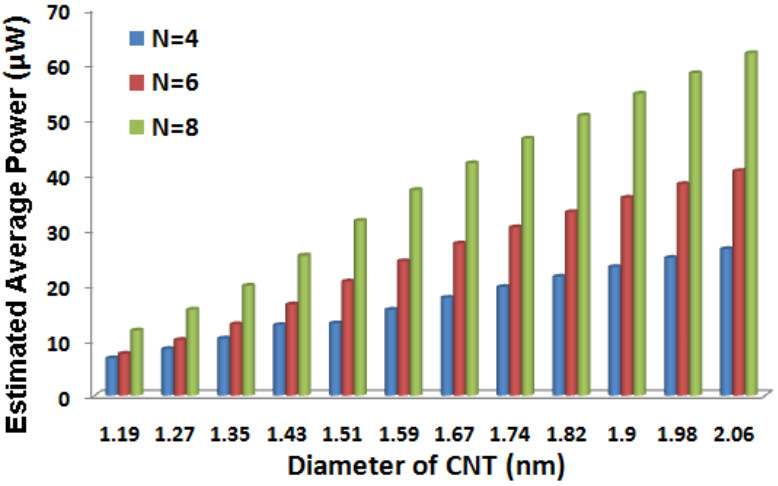

Figure 3.11: CNT Diameter versus Average Power with the Number of CNT

The main contributions to the power consumption are short circuit, leakage and switching currents. The CMOS circuits have broadly two types of power consumption i.e. dynamic and static . In electronic applications, it is important to

know the instantaneous power in a circuit. Such estimation is important for the design of voltage drop on lines, power and ground lines [97]. In MOS circuits, the capacitive load of a logic gate can be estimated by the fan out of the gate. Thus the dynamic power dissipation due to two consecutive input vectors can be represented as (3.8):

$$P_{avg} = C_{load}(V_{DD})^2 f * nT \tag{3.8}$$

Here, nT shows node transition factor which is the effective number of power consumption would be analysed.

The proposed circuit has been simulated using HSPICE. HSPICE would give the total power of the circuit directly which includes all the power components as discussed above.

Fig. 3.11 illustrates the effect of diameter variation versus average power dissipation with the number of tubes as an additional parameter. For this particular analysis, the other design parameters except for diameter (D_{CNT}) and the number of CNT (N) are kept as given in Table 3.1.

3.3.3 Variation in Power Supply

The main feature of CNFET is to operate at lower supply voltages. The effect of power supply variation in the performance of ICCII is explored in the proposed work. The low supply voltages have more effect of parasitics and so on the performance [173].

Fig. 3.12 depicts that 3-dB voltage bandwidth reduces with lower supply voltages. Although, the low supply voltages have the negative effect on frequency response yet reduces the average power of the device that is needed for low power circuit design. The similar effort is repeated for current-mode design.

Fig. 3.13 shows the variation in 3-dB current bandwidth with supply voltage, and it reflects that downscaling of supply voltage limits the current bandwidth also. Therefore, it is always a trade-off between bandwidth and power requirements to choose the optimum values for specific applications [57].

Fig. 3.14 represents the effect of power supply on the average power requirement of the device (CNFET). The other design parameters like inter-CNT pitch (S), the

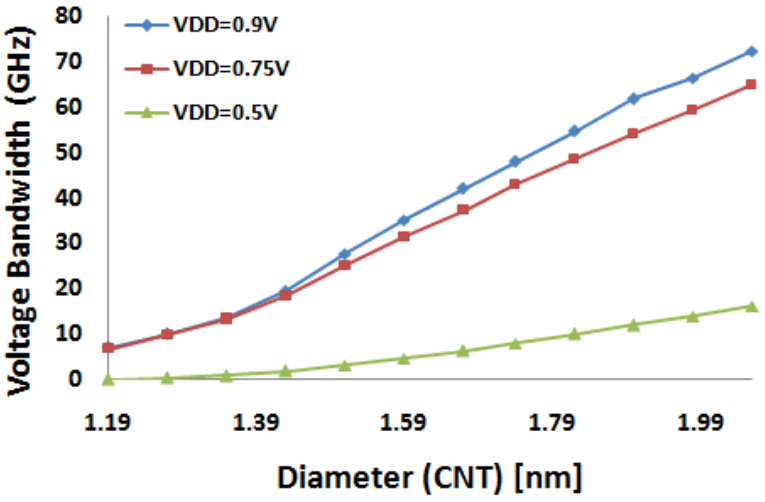

Figure 3.12: CNT Diameter versus 3-dB Voltage Bandwidth with Power Supply

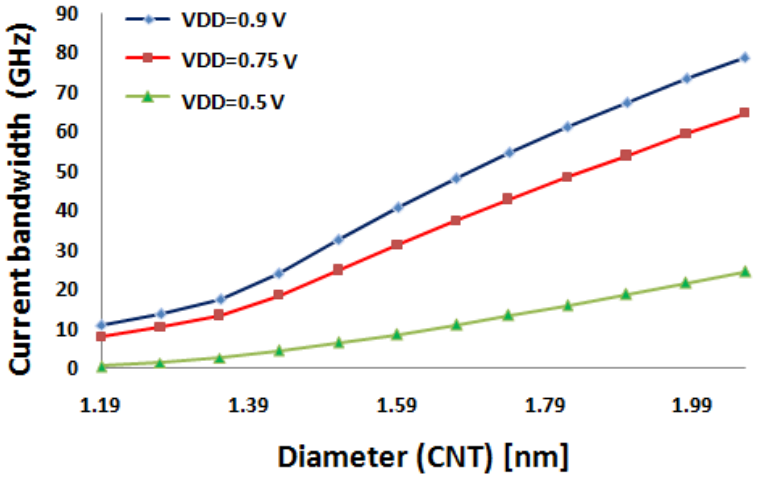

Figure 3.13: CNT Diameter versus 3-dB Current Bandwidth with Power Supply

number of CNTs (N), oxide thickness (T_{ox}), dielectric constant (K_{ox}) are referred from Table 3.1.

3.4 Applications of CNFET ICCII/CCII

3.4.1 Tunable Active Biquad Filter

Analog filter design using a number of active building blocks has been the major research area for the past several decades [174, 175, 176, 166, 161]. Here, a

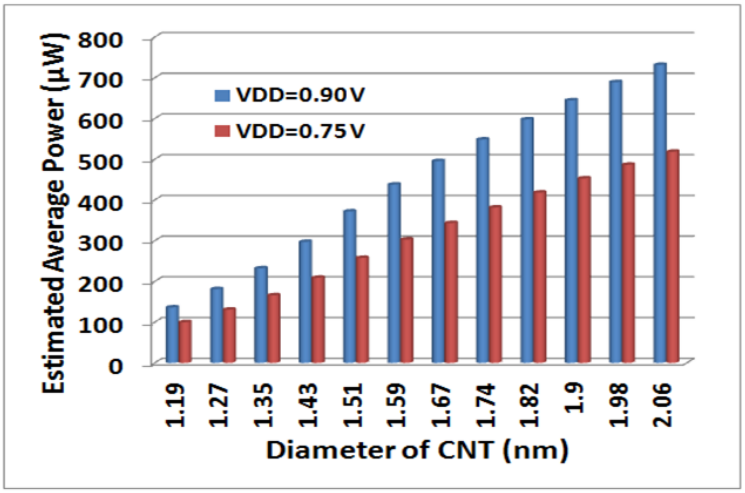

Figure 3.14: CNT Diameter versus Average Power with Power Supply

tunable voltage-mode active filter is proposed as shown in Fig. 3.15. The filter uses CNFET-based inverting current conveyor as an active element. It contains two resistors and two grounded capacitors. After analyzing the circuit of the tunable filter, the transfer functions of high pass, low pass, and band pass have been obtained. Additionally, the proposed filter can realize the full operating range of Bluetooth frequencies *i.e.* from 2.40 - 2.48 GHz and tuning of frequency is obtained by a variable resistor.

The voltage-mode multifunction filter shown in Fig. 3.15 is characterized by (3.9) and (3.10). The transfer functions for input conditions, $V_1 = V_i$ and $V_2 = 0$ and $V_2 = V_i$ and $V_1 = 0$ have been expressed in Table 3.3. The proposed circuit is able to perform the basic filter functions in two input conditions as follows:
(a) The low pass and inverting band pass filter functions are obtained, when $V_2 = 0$
(b) The non-inverting band pass and high pass filter functions are obtained, when $V_1 = 0$
In all the cases, resonance angular frequency (ω_0) and quality factor (Q) are given by (3.11) and (3.12).

$$V_{out1} = \frac{-V_1 + V_2 s C_2 R_1}{s^2 C_1 C_2 R_2 R_1 + s C_1 R_1 + 1} \tag{3.9}$$

$$V_{out2} = \frac{-V_1 s C_1 R_2 + V_2 s^2 C_1 C_2 R_2 R_1}{s^2 C_1 C_2 R_2 R_1 + s C_1 R_1 + 1} \tag{3.10}$$

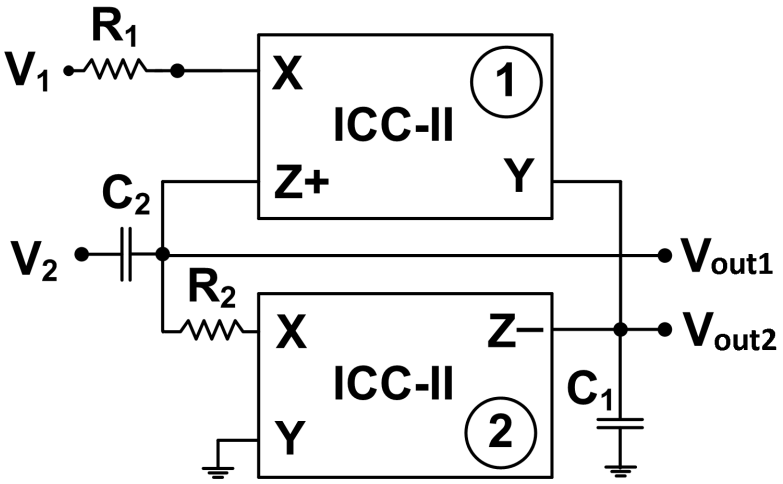

Figure 3.15: Tunable Active Biquad Filter

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}} \tag{3.11}$$

$$Q = \sqrt{\frac{C_2 R_2}{C_1 R_1}} \tag{3.12}$$

Table 3.3: Input Conditions for Active Filter

Input	Case-1 ($V_1 = V_i, V_2 = 0$)	Case-2 ($V_2 = V_i, V_1 = 0$)
$\frac{V_{out1}}{V_i}$	$\frac{-1}{(s^2C_1C_2R_2R_1+sC_1R_1+1)}$	$\frac{sC_2R_1}{(s^2C_1C_2R_2R_1+sC_1R_1+1)}$
$\frac{V_{out2}}{V_i}$	$\frac{-sC_1R_2}{(s^2C_1C_2R_2R_1+sC_1R_1+1)}$	$\frac{(s^2C_1C_2R_2R_1)}{(s^2C_1C_2R_2R_1+sC_1R_1+1)}$

(a) Non-ideal Analysis

The port relations of a non-ideal ICCII may be illustrated as (3.13) and (3.14).

$$V_X = \beta V_Y \tag{3.13}$$

$$I_Z+ = \alpha_1 I_X, \quad I_Z- = -\alpha_2 I_X \tag{3.14}$$

Here, α_1 and α_2 are the current transfer gains from X to Z+ and X to Z- ports, and β is the voltage transfer gain from X to Y port respectively. For the proposed filter function, the non-ideal transfer function can be given as (3.15) and (3.16).

$$V_{out1} = \frac{-\alpha_1\alpha_2 V_1 + V_2 sC_2R_1}{s^2C_1C_2R_2R_1 + sC_1R_1 + \alpha_1\alpha_2\beta} \tag{3.15}$$

$$V_{out2} = \frac{-\alpha_1 V_1 sC_1R_2 + V_2 s^2C_1C_2R_2R_1}{s^2C_1C_2R_2R_1 + sC_1R_1 + \alpha_1\alpha_2\beta} \tag{3.16}$$

The non-ideal pole frequency and quality factor are written as (3.17) and (3.18).

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2\beta}{C_1C_2R_1R_2}} \tag{3.17}$$

$$Q = \sqrt{\frac{C_2R_2}{C_1R_1\alpha_1\alpha_2\beta}} \tag{3.18}$$

(b) Sensitivity Analysis

As described in the literature, the passive component sensitivities should be less or equal to unity [177, 178]. Sensitivity analysis of proposed filter circuit is calculated regarding the sensitivity of pole frequency (ω_0) and quality factor (Q) concerning passive components variation. Sensitivity analysis with respect to passive components C_1, C_2, R_1,and R_2 is shown by (3.19) and (3.20).

$$S_{R1}^{\omega_0} = S_{R2}^{\omega_0} = S_{C1}^{\omega_0} = S_{C2}^{\omega_0} = -\frac{1}{2} \tag{3.19}$$

$$S_{C2}^{Q} = S_{R2}^{Q} = \frac{1}{2}, \quad S_{C1}^{Q} = S_{R1}^{Q} = -\frac{1}{2} \tag{3.20}$$

(C) Parasitic Analysis of Proposed Tunable Filter

From Fig. 3.16 it is reflected that the X-terminal shows intrinsic resistance R_X. Additionally, Y terminal possesses parasitic capacitance C_Y and parasitic resistance R_Y. The Z+ and Z terminals acquire parasitic resistances R_{Z1} and R_{Z2} in parallel with capacitances C_{Z1} and C_{Z1} respectively.

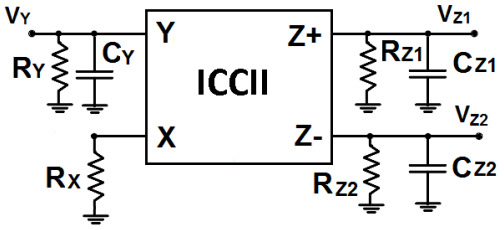

Figure 3.16: Parasitics associated with ICCII

Now, consider the parasitics of Inverting current conveyor and $R_{P1} = R_Y||R_{Z2}$, the output voltages are given by (3.21) and (3.22).

$$V_{out1} = \frac{[-V_1(1+\frac{sC_2R_{Z1}}{1+sCZ1R_{Z1}})}{\frac{s^2C_1C_2R_{P1}(R_1+R_X)(R_2+R_X)}{1+sR_{P1}(C_Y+C_{Z2})}+(1+\frac{sC_2R_{Z1}}{(1+sC_{Z1}R_{Z1})})[\frac{(R_{P1}}{1+s(C_Y+C_{Z2})R_{P1}}}$$

$$\frac{+V_2sC_2(R_1+R_X)](R_2+R_X)(1+\frac{sC_1R_{P1}}{1+sR_{P1}(C_Y+C_{Z2})}}{+(R_1+R_X)(1+\frac{sC_1R_{P1}}{1+s(C_Y+C_{Z2})R_{P1}})]+sC_2(R_1+R_X)(R_2+R_X)} \tag{3.21}$$

$$V_{out2} = \frac{-V_1R_A(1+\frac{sC_2R_{Z1}}{(1+sC_{Z1}R_{Z1})})}{\frac{s^2C_1C_2R_{P1}(R_1+R_X)(R_2+R_X)}{1+sR_{P1}(C_Y+C_{Z2})}+(1+\frac{sC_2R_{Z1}}{(1+sC_{Z1}R_{Z1})})[\frac{(R_{P1}}{1+s(C_Y+C_{Z2})R_{P1}}}$$

$$\frac{+V_2sC_2R_A(R_1+R_X)}{+(R_1+R_X)(1+\frac{sC_1R_{P1}}{1+s(C_Y+C_{Z2})R_{P1}})]+sC_2(R_1+R_X)(R_2+R_X)} \tag{3.22}$$

Further, assume the resistances R_A and R_B in term of parasitics of Inverting current conveyor, $R_A = R_{P1}||C_Y||C_{Z2}$ and $R_B = R_{Z1}||C_{Z1}$. The output voltages of the proposed tunable filter are modified as given in equations (3.23) and (3.24).

$$V_{out1} = \frac{[-V_1(1+sC_2R_B)+V_2sC_2(R_1+R_X)]}{s^2C_1C_2R_A(R_1+R_X)(R_2+R_X)+(1+sC_2R_B)[R_A+(R_1+R_X)(1+sC_1R_A)]}$$

$$\frac{(R_2+R_X)(1+sC_1R_A)}{+sC_2(R_1+R_X)(R_2+R_X)} \tag{3.23}$$

$$V_{out2}=\frac{-V_1R_A(1+sC_2R_B)}{s^2C_1C_2R_A(R_1+R_X)(R_2+R_X)+(1+sC_2R_B)[R_A+(R_1+R_X)(1+sC_1R_A)]}$$

$$\frac{+V_2sC_2R_A(R_1+R_X)}{+sC_2(R_1+R_X)(R_2+R_X)} \tag{3.24}$$

For more simplification consider $R_1'=R_1+R_X$ and $R_2'=R_2+R_X$, the modified equations are written by (3.25) and (3.26).

$$V_{out1}=\frac{[-V_1(1+sC_2R_B)+V_2sC_2R_1']R_2'(1+sC_1R_A)}{s^2C_1C_2R_1'R_2'R_A+(1+sC_2R_B)[R_A+R_1'(1+sC_1R_A)]+sC_2R_1'R_2'} \tag{3.25}$$

$$V_{out2}=\frac{-V_1R_A(1+sC_2R_B)+V_2sC_2R_1'R_A}{s^2C_1C_2R_1'R_2'R_A+(1+sC_2R_B)[R_A+R_1'(1+sC_1R_A)]+sC_2R_1'R_2'} \tag{3.26}$$

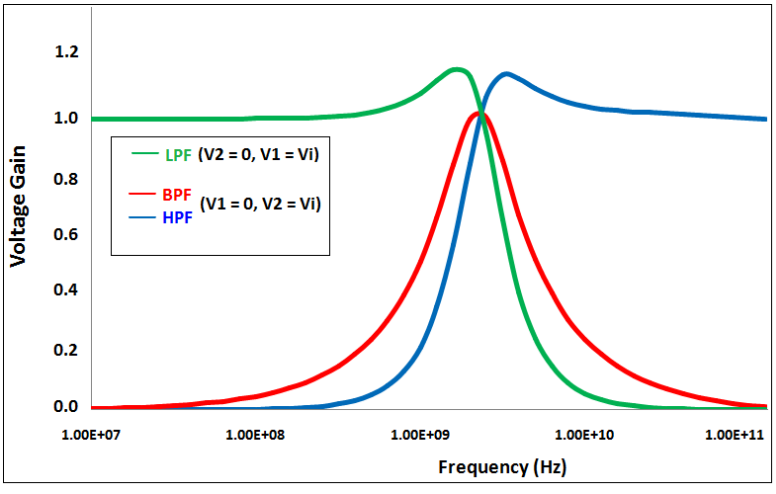

Figure 3.17: LP, BP and HP Responses of Proposed Active Filter

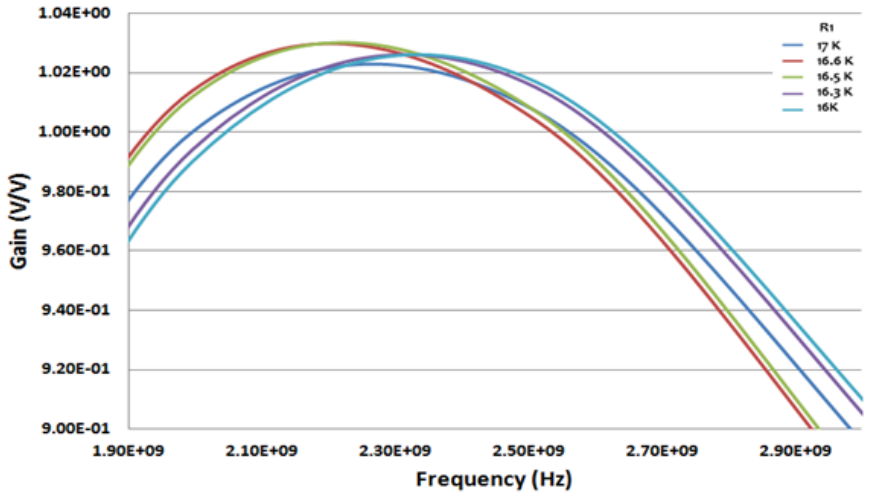

Figure 3.18: Tuning of Center Frequency of Band Pass Filter with R_1

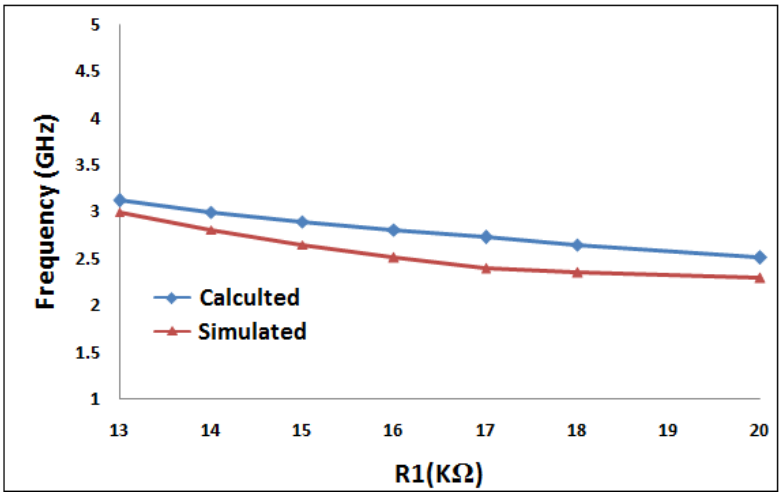

Figure 3.19: Calculated vs. Simulated Frequencies of the Band Pass Filter

Fig. 3.17 shows SPICE simulation results of the low-pass, band-pass and high-pass filter responses. The simulated frequency is 2.40 GHz with passive component values $R_1 = 17$ KΩ, $R_2 = 2$ KΩ, $C_1 = C_2 = 10fF$. The fruitful property of the circuit as band pass filter (BPF) is to achieve the complete operating range of Bluetooth frequencies (2.40 - 2.48 GHz).

Fig. 3.18 reflects the tuning of the center frequency of BPF with the variable resistor (R_1). Fig. 3.19 shows the calculated and simulated values for the tuning of band-pass center frequencies for the entire Bluetooth range.

Additionally, % error between calculated and simulated frequencies is given by Fig. 3.20 which reflected the error in the range of 3–12%.

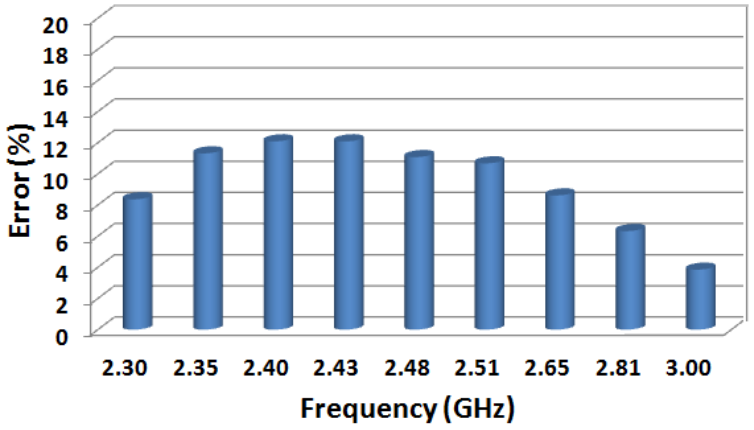

Figure 3.20: Illustration of % Error in Calculated and Simulated Frequencies of Tunable Filter

3.4.2 Voltage-Mode Universal Filter

The short-range wireless communication technologies like ZigBee and Bluetooth are widely used in modern day electronic equipment. ZigBee operates in the ISM band with frequencies ranging from 868 MHz to 2.4 GHz. Proposed work deals with the design and implementation of a VM universal filter using the CNFET-based ICCII. Fig. 3.21 shows the circuit diagram of the continuous-time analog filter capable of simultaneously performing the Low-Pass, Band-Pass and High-Pass functions. It employs two active elements, two grounded capacitors and three resistors (out of which two are grounded), to allow the ease of integration. The analysis of the circuit of Fig. 3.21 results in the following transfer functions of the various analog filters:

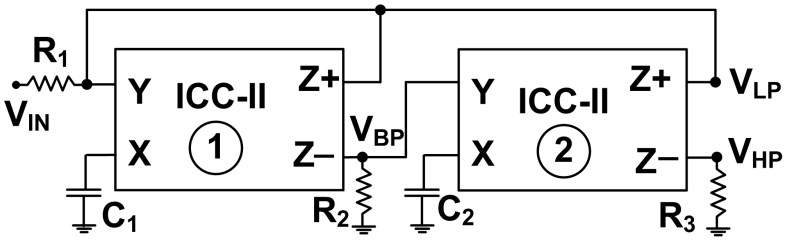

Figure 3.21: Proposed Voltage-Mode Universal Filter

$$\frac{V_{HP}}{V_{IN}} = \frac{\frac{S^2}{R_3 R_1}}{S^2 + \frac{S}{C_2 R_2} + \frac{1}{C_1 C_2 R_1 R_2}} \tag{3.27}$$

$$\frac{V_{BP}}{V_{IN}} = \frac{\frac{S}{C_2R_1}}{S^2 + \frac{S}{C_2R_2} + \frac{1}{C_1C_2R_1R_2}} \tag{3.28}$$

$$\frac{V_{LP}}{V_{IN}} = \frac{\frac{1}{C_1C_2R_2R_1}}{S^2 + \frac{S}{C_2R_2} + \frac{1}{C_1C_2R_1R_2}} \tag{3.29}$$

From (3.27–3.29), the pole frequency ω_o and the quality factor Q can be deduced as:

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \tag{3.30}$$

$$Q = \sqrt{\frac{C_2R_2}{C_1R_1}} \tag{3.31}$$

The quality factor (Q) of an active band pass filter (Second-order) relates to the sharpness of the filters response around its centre frequency (f_c). It is a measure of how Selective or Un-selective the band pass filter is towards a given range of frequencies. The lesser the value of the Q factor the wider is the bandwidth of the filter and consequently the larger the Q factor the narrower and more selective is the filter [179].

(a) Non-ideal Analysis

The transfer functions of the proposed filter can be deduced by considering the non-idealities in the current- and voltage transfer gains of the inverting current conveyor. Considering (3.13) and (3.14) β is taken as the voltage transfer gains from X to Y terminal. Also, α_1 is the current transfer gain from X to Z+ terminal and α_2 is current transfer gain from X to Z- terminal respectively.

For the proposed universal filter the non-ideal second-order high pass band pass and low pass transfer functions are written by (3.32), (3.33), and (3.34).

$$\frac{V_{HP}}{V_{IN}} = \frac{\frac{S^2\beta}{R_3R_1}}{S^2 + \frac{S}{C_2R_2} + \frac{\alpha_1\alpha_2}{C_1C_2R_1R_2}} \tag{3.32}$$

$$\frac{V_{BP}}{V_{IN}} = \frac{\frac{S\alpha_2}{C_2R_1}}{S^2 + \frac{S}{C_2R_2} + \frac{\alpha_1\alpha_2}{C_1C_2R_1R_2}} \tag{3.33}$$

$$\frac{V_{LP}}{V_{IN}} = \frac{\frac{\alpha_1\alpha_2}{C_1C_2R_2R_1}}{S^2 + \frac{S}{C_2R_2} + \frac{\alpha_1\alpha_2}{C_1C_2R_1R_2}} \tag{3.34}$$

The non-ideal pole frequency and quality factor are expressed as (3.35) and (3.36).

$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2}{C_1C_2R_1R_2}} \tag{3.35}$$

$$Q = \sqrt{\frac{C_2R_2}{C_1R_1\alpha_1\alpha_2}} \tag{3.36}$$

(b) Sensitivity Analysis Sensitivity analysis of the proposed universal filter is also performed. Sensitivities of pole frequency (ω_0) and quality factor (Q) are calculated with variation in passive components (C_1, C_2, R_1,and R_2). Sensitivity analysis for pole frequency (ω_0) with respect to passive components is given by (3.37). Also, sensitivity analysis for quality factor (Q) is presented by (3.38).

$$S_{R1}^{\omega_0} = S_{R2}^{\omega_0} = S_{C1}^{\omega_0} = S_{C2}^{\omega_0} = -\frac{1}{2} \tag{3.37}$$

$$S_{C1}^{Q} = S_{R1}^{Q} = -\frac{1}{2}, \quad S_{C2}^{Q} = S_{R2}^{Q} = \frac{1}{2} \tag{3.38}$$

The sensitivity of filter parameters with respect to passive components should be less or equal to unity [177]. Here, it is observed from (3.37) and (3.38) that sensitivities for ω_0 and (Q) are in acceptable figure.

(C) Parasitic Analysis of the Proposed Universal Filter

Taking into account the parasitic of ICCII from Fig. 4.19 and assume $R_{P2} = R_2||R_{Z2}$ and $R_{P3} = R_3||R_{Z2}$, the transfer functions of high pass, band pass, and low pass filter can be written by (3.39), (3.40) and (3.41).

$$\frac{V_{HP}}{V_{IN}} = \frac{s^2C_1C_2(\frac{R_{P2}}{1+sC_{Z2}R_{P2}})}{s^2C_1C_2(\frac{R_Y}{1+sC_YR_Y})\frac{(}{R_{P2}}1 + sC_{Z2}R_{P2})}$$

$$\frac{(\frac{R_{P3}}{1+sC_{Z2}R_{P3}})}{+sC_1\frac{R_Y}{1+sC_YR_Y}(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.39}$$

$$\frac{V_{BP}}{V_{IN}}=\frac{(\frac{sC_1R_{P2}}{1+sC_{Z2}R_{P2}})}{s^2C_1C_2(\frac{R_Y}{1+sC_YR_Y})\frac{(}{R_{P2}}1+sC_{Z2}R_{P2})}$$

$$\frac{(1+sC_2R_X)}{+sC_1\frac{R_Y}{1+sC_YR_Y}(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.40}$$

$$\frac{V_{LP}}{V_{IN}}=\frac{(1+sC_1R_X)}{s^2C_1C_2(\frac{R_Y}{1+sC_YR_Y})\frac{(}{R_{P2}}1+sC_{Z2}R_{P2})}$$

$$\frac{(1+sC_2R_X)}{+sC_1\frac{R_Y}{1+sC_YR_Y}(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.41}$$

To simplify equations further, consider $R_1' = R_Y||C_Y$, $R_2' = R_{P2}||C_{Z2}$, and $R_3' = R_{P3}||C_{Z2}$. The high pass, band pass, and low pass transfer functions are expressed by (3.42), (3.43) and (3.43).

$$\frac{V_{HP}}{V_{IN}}=\frac{S^2C_1C_2R_2'R_3'}{S^2C_1C_2R_1'R_2'+sC_1R_1'(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.42}$$

$$\frac{V_{BP}}{V_{IN}}=\frac{sC_1R_2'(1+sC_2R_X)}{S^2C_1C_2R_1'R_2'+sC_1R_1'(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.43}$$

$$\frac{V_{LP}}{V_{IN}}=\frac{(1+sC_1R_X)(1+sC_2R_X)}{S^2C_1C_2R_1'R_2'+sC_1R_1'(1+sC_2R_X)+(1+sC_1R_X)(1+sC_2R_X)} \tag{3.44}$$

Further, the performance of the circuit of Fig. 3.21 was analyzed using the HSPICE simulation. The power supplies are kept at ±0.9 V, and 32 nm CNFET model from Stanford University are used for all the simulation tests [109].

The passive components are considered as $R_1 = R_2 = R_3 = 10$ KΩ, $C_1 = C_2 = 10fF$. From (3.30), the designed filter frequency (f_o) for the chosen values of resistances and capacitances comes out to be 1.59 GHz. The obtained high pass, low pass and band pass filter responses are illustrated in Fig. 3.22 from where it has been verified that the cut-off frequencies for LP and HP filters, and center frequency for the BP filter, is almost similar with the theoretical value.

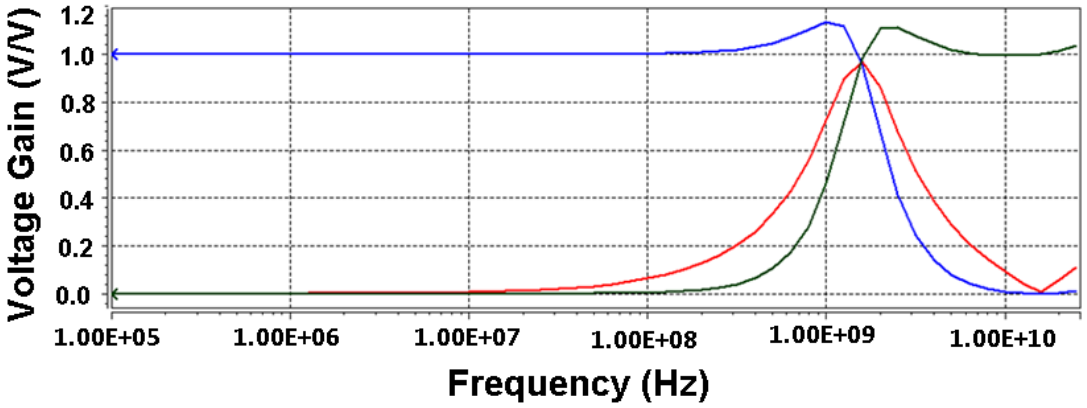

Figure 3.22: Frequency Response of Voltage Mode Filter

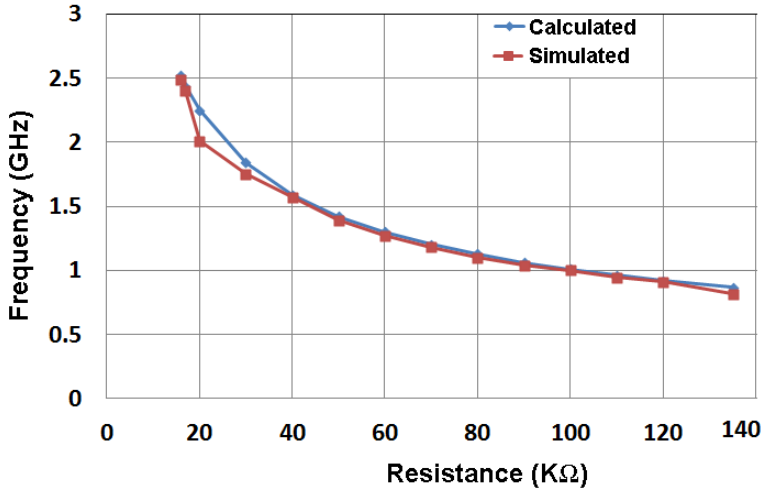

Figure 3.23: Calculated & Simulated Frequencies of the Proposed Filter

The simulation test results are shown in Fig. 3.22 for one particular frequency (1.59 GHz) in the ZigBee operating range. The entire range of ZigBee operation can be addressed by the proposed VM universal filter. To illustrate this point, the

passive elements are kept as $C_1 = C_2 = 5$ fF, $R_1 = R_3 = 10$ KΩ and R_2 is varied from 17 KΩ to 135 KΩ to cover the ZigBee band from 868 MHz to 2.4 GHz.

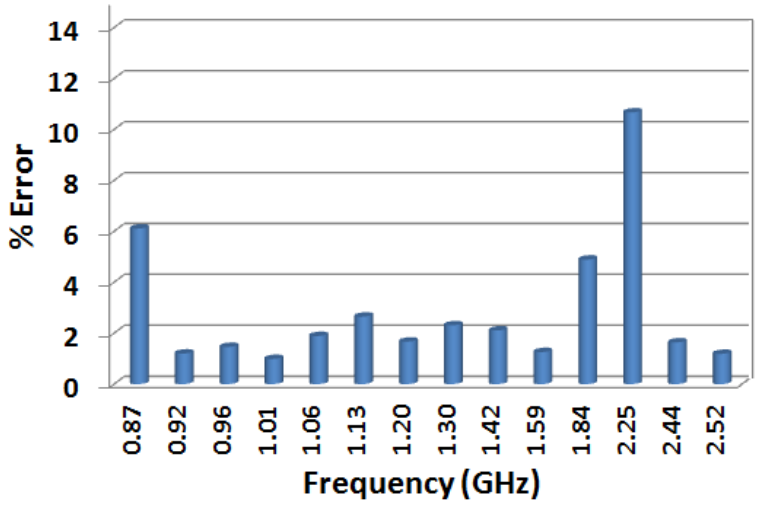

Figure 3.24: Presentation of % Error in Calculated and Simulated Frequencies of the Proposed Filter

Fig. 3.23 depicts the calculated and simulated frequencies over an entire range of interest. Fig. 3.23 confirms that as the resistance (R_2) is increased, the filter frequency decreases as defined by (3.30). Further, Fig. 3.24 shows the percentage error between calculated and simulated frequencies of the proposed filter. The result predicted that error in the simulated frequency is 1–10.6 %.

3.4.3 CNFET based Resistive Sensor Interface

The benefit of integrated circuit-based sensing and signal conditioning is the calibration through on-chip techniques. The overall performance of a system can be improved effectively and cost reduced by merging the functions of the sensing device, actuators and analog interfacing circuits in one design. Wherever technology allows, the complete system may be realized on a common integrated circuit or chip [180]. In smart systems, the functions combine sensing and signal conditioning for a dedicated application [181]. Second generation current conveyors (CCII) is used in variety of realizations of active network elements and current-mode circuits [182, 183, 184]. In this work, a CNFET based resistive sensor interface is proposed which utilized CCII as the active element.

The second generation current conveyor (CCII) is a very versatile analog building block and widely used for voltage and/or current-mode circuit design for various

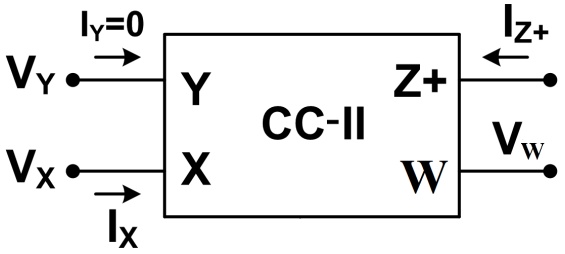

Figure 3.25: Symbol of CCII with Buffered Output Node

diverse applications [183, 184, 185]. The symbol of CCII is depicted in Fig. 3.25 with an additional voltage buffer output. Additionally, the port relations are illustrated in (3.45).

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ +1 & 0 & 0 \\ 0 & 0 & +1 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \tag{3.45}$$

Fig. 3.26 shows the current conveyor based resistive sensor interface circuit. It uses two resistors R_1 and R_2 for setting the proper voltage reference at the high impedance Y-terminal. The resistive sensor can be attached to the low impedance terminal X. The change in resistance of the resistive sensor will affect the current I_{SENS}, which can be measured from Z-terminal. The additional buffer stage is used to obtain equivalent voltage output as illustrated in the transistor level implementation of CCII in Fig. 3.27. The parameters of CNFET which used in the design are given in Table 3.4. The equations (3.46) through (3.50) give the various node voltages, and branch currents of the proposed resistive sensor interface circuit using the properties of building block given in Fig. 3.26. Moreover, the CNFET technology is expected to provide low power consumption, higher reliability, and space reduction for very low power applications [103].

The resistive sensor interface circuit shown in Fig. 3.26 is analyzed and simulated to investigate the relation between sensor resistance (R_{SENS}) and electrical outputs of interface circuit *i.e.* I_{SENS} and V_W. As predicted from (3.48) and (3.50), I_{SENS} as well as V_W decreases with increase in R_{SENS}. Fig. 3.28 depicts the simulation responses between R_{SENS} and I_{SENS} for the range of R_{SENS} from 1–100 KΩ. The passive components of circuit are taken as $R_1 = 8$ KΩ and $R_2 = 1$ KΩ. The proposed circuit consumes 447.3 μW only with supply voltage of ±0.9 V.

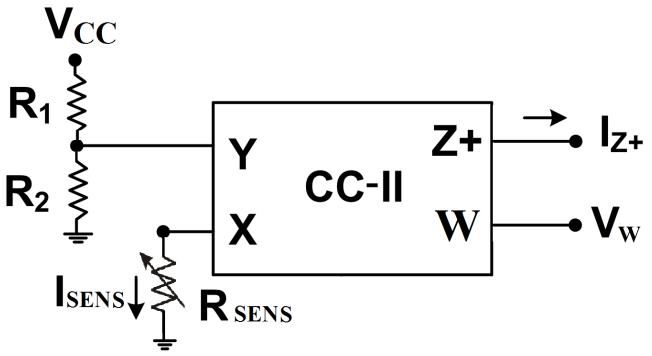

Figure 3.26: Block Diagram of Proposed Resistive Sensor Interface

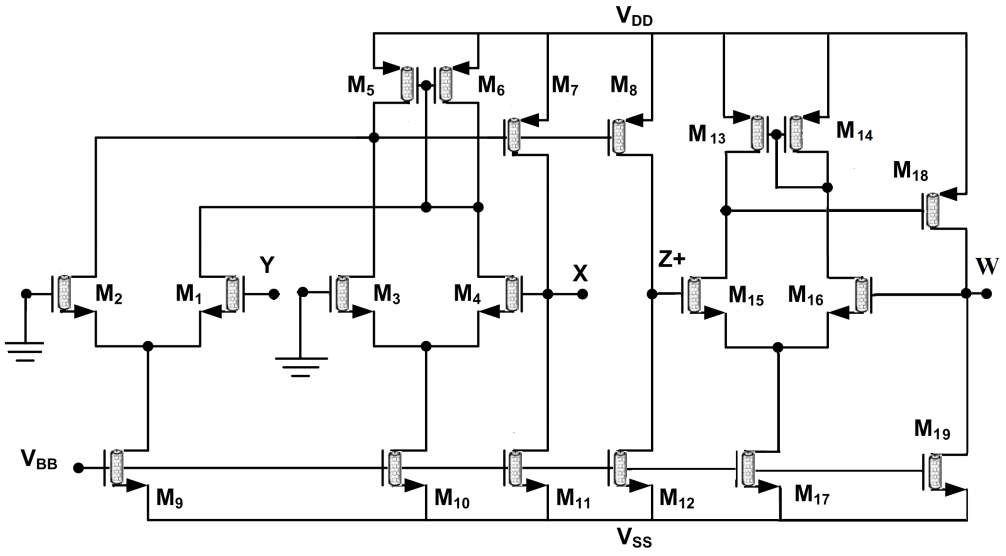

Figure 3.27: Transistor Level Implementation of CCII

$$V_Y = \frac{R_2.V_{CC}}{R_1 + R_2} \tag{3.46}$$

$$I_{SENS} = \frac{V_X}{R_{SENS}}, \quad V_X = V_Y \tag{3.47}$$

$$I_{SENS} = \frac{R_2.V_{CC}}{(R_1 + R_2)R_{SENS}} \tag{3.48}$$

$$I_Z = \frac{R_2.V_{CC}}{(R_1 + R_2)R_{SENS}}, \quad I_Z + = I_{SENS} \tag{3.49}$$

$$V_W = \frac{R_2.V_{CC}.R_Z}{(R_1 + R_2)R_{SENS}}, \quad V_W = V_Z \tag{3.50}$$

Here, R_Z is the port Z resistance and V_Z is the port Z voltage.

Table 3.4: Design Parameters for CNFET-based CCII

Parameters	**Value**
Oxide Thickness (T_{ox})	4 nm
Dielectric Constant (K_{ox})	16
Power Supply	±0.9 V
Chirality of the tube (n_1, n_2)	19, 0
Physical channel length (L_{ch})	32 nm
No. of tubes in the device	6
Pitch (S)	20 nm
Diameter of CNT (D_{CNT})	1.5 nm

Table 3.5: Some Specific Applications of Resistive Sensors

Resistive Device	**Application**	**Resistance Range**
Strain Gauge	Force Sensor	2.1-3.5 KΩ
Photo Cell	Light Sensor	30-60 KΩ
Potentiometer	Position Sensor	Few KΩ -– Few MΩ
Resistive Bend Pads	Collision Sensor	10-35 KΩ

An additional benefit of proposed circuit is that it gives the voltage-mode output too. Fig. 3.29 illustrates the similar effect of R_{SENS} for output voltage (V_W). The resistive sensors is useful for strain gauge, photo cell, potentiometer and resistive bend pads applications as given in Table 3.5.

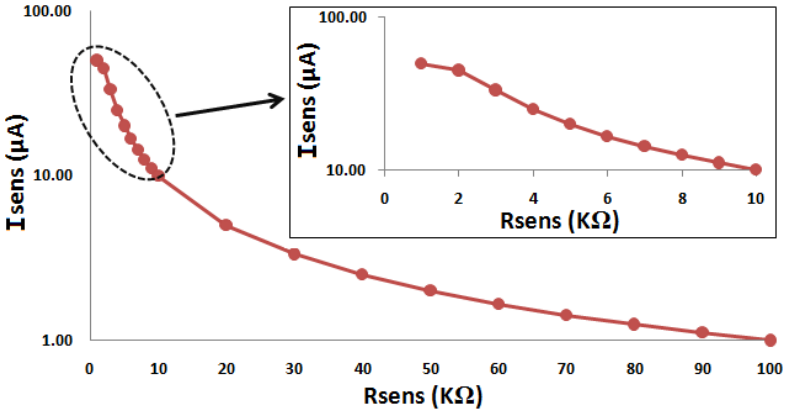

Figure 3.28: Current-mode Response of Proposed Resistive Sensor Interface, I_{SENS} vs. R_{SENS}

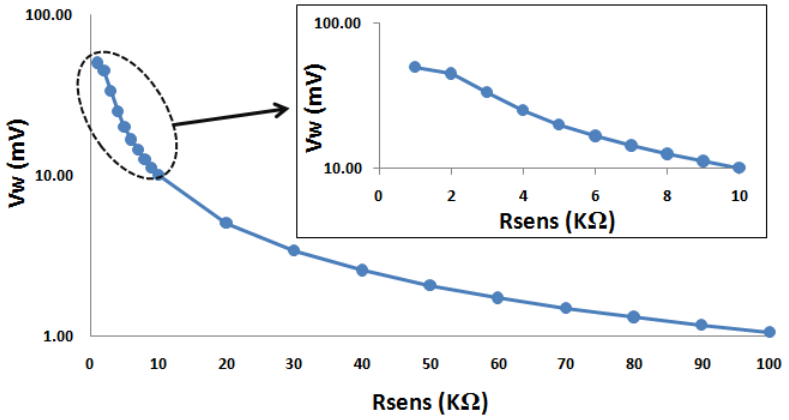

Figure 3.29: Voltage-mode Response of Proposed Resistive Sensor Interface, V_W vs. R_{SENS}

3.5 Summary

This chapter has presented the performance analysis of CNFET-based Current conveyor with variation in the parameters of the CNFET such as the diameter of CNT, pitch, and number of CNTs in the channel. Further, the performance of CMOS- and the CNFET-based Current conveyor is also presented. The result show that CNFET-based Current conveyor has better performance than CMOS-based circuit regarding 3-dB bandwidth and power dissipation. A tunable active filter is realized for Bluetooth frequency range (2.40 GHz to 2.48 GHz). Moreover, a voltage-mode universal is implemented for Zigbee band (868 MHz to 2.40 GHz). Both filter circuits utilize CNFET-based Current conveyor as the active element. Additionally, the work is extended to design a resistive sensor interface using CNFETs. The proposed interface circuit is useful in various industrial applications.

Chapter 4

CNFET DVCC for Analog Signal Processing Applications

4.1 Introduction

The processing of real-world signals using analog techniques is easier than digital. Analog signals in nature have physical quantities like force, speed, temperature, sound, light, acceleration *etc.* However, some signals are the response of other the signal processed. For example, the returned signal from a radar or ultrasound imaging result from a transmitted signals [186]. On the other hand, there is another classification of signals, called digital, where the actual signal has been conditioned and formatted to some logic level. These digital signals may or may not be associated with real-world analog signal(s), like data transmitted over local area networks (LANs). Moreover, the ultimate reason for the processing of real-world signals is to extract the valuable information from them. This information normally exists in the form of frequency, phase, signal amplitude or timing relations with other variables [187].

In the field of analog signal processing, current-mode (CM) circuits are preferred because of their larger dynamic range, higher bandwidth, lower power requirement and simpler circuitry, as compared to voltage-mode (VM) circuits [166, 188]. The overall benefits can be categorized in the following manner:

(i) *Performance improvement*
Current-mode circuits have high switching speed due to fewer parasitics as compared to high voltage swing in VM circuits. Also, they consume low power consumption at high frequency with the feature of high signal dynamic range. Moreover, CM circuits exhibit lower cross-talk and switching noise [189].

(ii) *Structural advantages*
These circuits have a well-known advantage that current summing can be achieved without passive components. Moreover, the controlled gain is obtained without feedback components with schematic simplicity.

(iii) *Specific features*
The CM circuits are well suited for low voltage applications and also extensively applied in current switching technique.

In next Section, implementation of the CNFET-based differential voltage current conveyor (DVCC) is presented. It is used to realize a programmable gain instrumentation amplifier and a low power RF filter.

4.2 CNFET-based DVCC

Since the introduction of current conveyor by Sedra and Smith [163], many versions of current conveyors have been discussed [175, 10, 190, 191, 192, 193] but the second generation current conveyor (CCII) proved to a versatile active element for realization of CM and VM circuits. Although the CCII includes high slew rate, higher bandwidth, wide dynamic range and simple circuitry but it has one Y input node of high impedance, which can be a drawback to process differential input signals as in differential amplifier. The differential voltage current conveyor (DVCC) has extra Y terminal to manage differential input signals. The symbol of DVCC is given in Fig. 4.1. DVCC is a very versatile building block, and its applications are discussed in literature [72, 73, 74, 166].

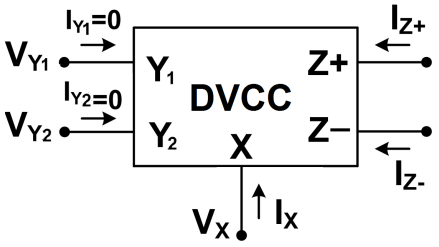

Figure 4.1: Circuit Symbol of DVCC

The transistor level realization of CNFET-based DVCC is shown in Fig. 4.2. Here, the performance of CNFET-based DVCC with 32 nm feature size of CNFET is presented. The differential voltage current conveyor shown in Fig. 4.2 has been simulated and tested through HSPICE, satisfying the characteristics as depicted in (4.1). HSPICE 32 nm CNFET parameters are used for the design [169].

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ I_X \\ V_Z \end{bmatrix} \tag{4.1}$$

Fig. 4.3 shows the frequency response of the building block in voltage-mode configuration. Moreover, proposed DVCC block is also verified for current-mode signals and Fig. 4.4 represents the frequency response of current gain. The outcomes depict that 3-dB bandwidths is 29.8 GHz.

The DC current and voltage transfer characteristics of CNFET-based DVCC are also verified. Fig. 4.5 and Fig. 4.6 illustrate the current and voltage transfer curves

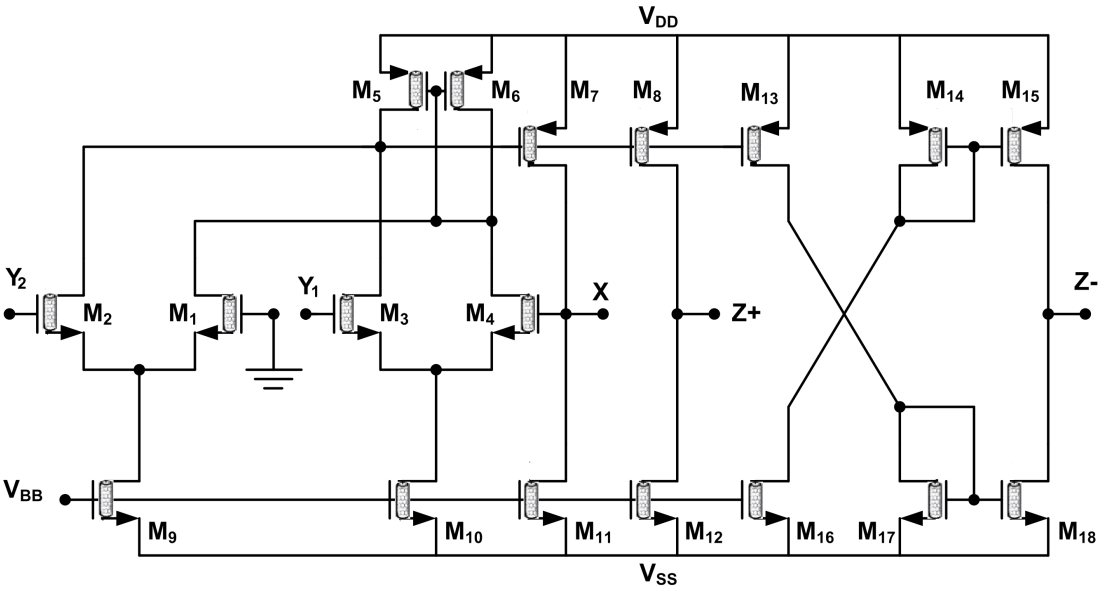

Figure 4.2: Transistor Level Realization of DVCC using CNFET

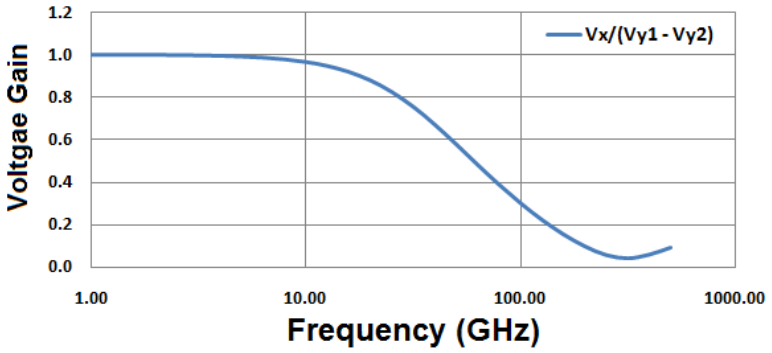

Figure 4.3: Frequency Response of Voltage Gain of CNFET-based DVCC

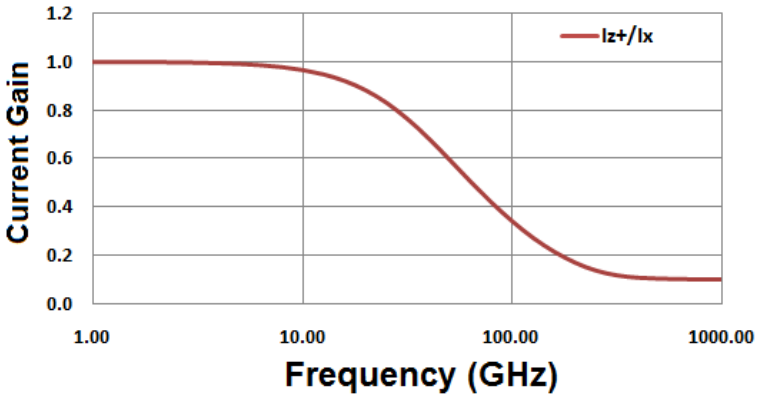

Figure 4.4: Frequency Response of Current Gain of CNFET-based DVCC

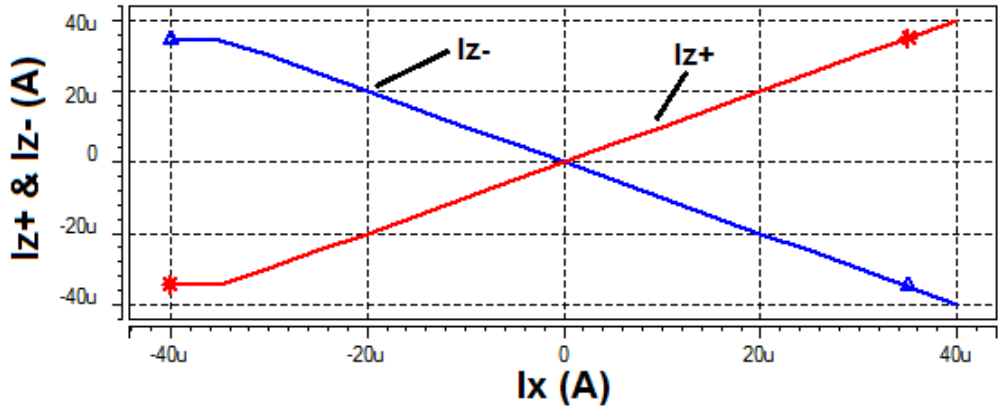

Figure 4.5: DC Current Transfer Characteristics of CNFET-based DVCC

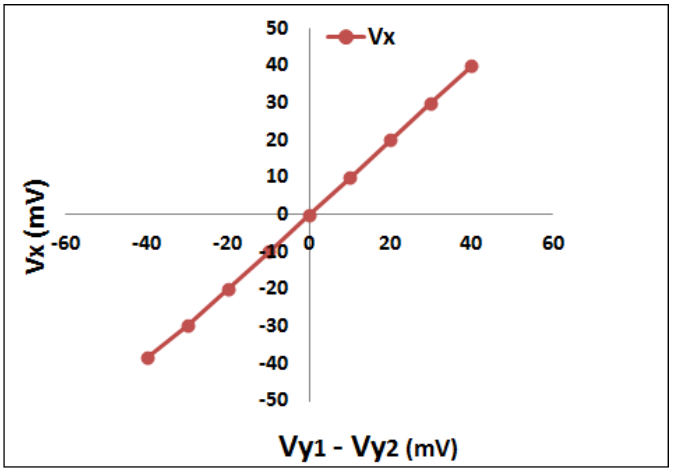

Figure 4.6: DC Voltage Transfer Characteristics of CNFET-based DVCC

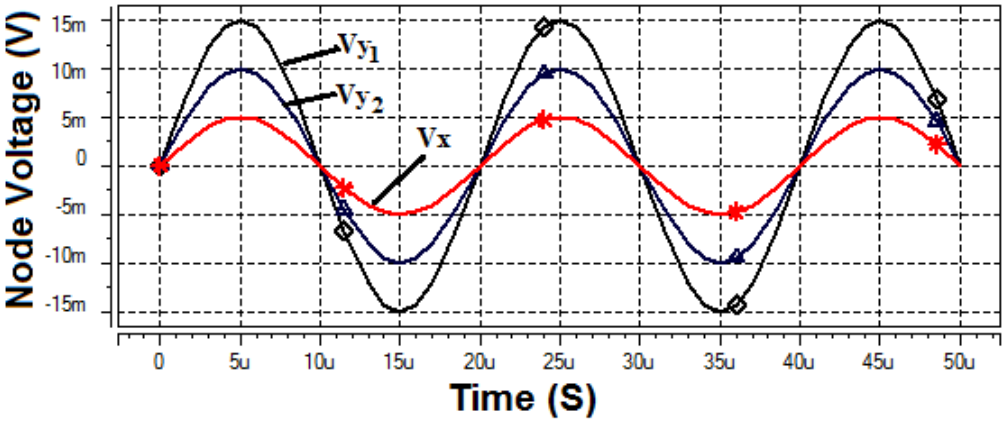

Figure 4.7: Transient Voltage Characteristics of V_X, V_{Y1} and V_{Y2}

of the CNFET-based current conveyor. The input and output voltages have the linear relation *i.e.* $V_X = (V_{Y1} - V_{Y2})$. The performance satisfies the theoretical

aspects of the device, given in (4.1).

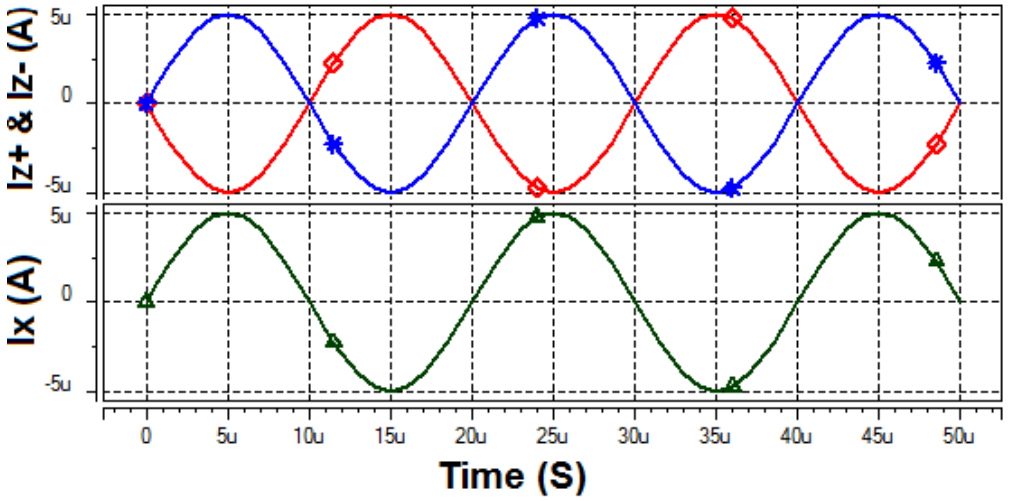

Figure 4.8: Transient Current Characteristics of I_X, I_{Z+} and I_{Z-}

To test the validity of DVCC circuit, transient-mode simulations have also been performed. The response of input-output voltages is given in Fig. 4.7, while Fig. 4.8 reflects the currents of X and Z terminals of DVCC, as given in relations described by equation (4.1).

Table 4.1: Performance of CNFET- and CMOS-based DVCC

Parameters	**CMOS**	**CNFET**
Model/Node	PTM/32 nm	Stanford/32 nm
V_{DD}	±.9 V	±0.9 V
No. of Transistors	18	18
Power Requirement	1000.8 μW	389.7 μW
3-dB Bandwidth	4.55 GHZ	29.8 GHz

The performance of CMOS- and CNFET-based designs should be compared so that the actual benefits of the proposed circuit should be evaluated. Therefore, the simulation of CMOS based DVCC is also performed. Table 4.1 shows the performance of CMOS- and CNFET-based differential voltage current conveyor. The CNFET represents its superiority with improvement in bandwidth and reduction in the power consumption as compared to CMOS-based design.

Moreover, as for a differential amplifier case, there is a growing usage of frequency compensation techniques. In the case of differential voltage current conveyor (DVCC), Reversed Nested Miller Compensation (RNMC) frequency compensation technique can also be applied [194, 195]. The RNMC compensation network

is feedback and feed-forward path concurrently. The feed-forward gives right-half-plane (RHP) zero, which degenerate frequency response and phase margin equally.

4.3 Digitally Programmable DVCC

The differential voltage current conveyor (DVCC) is proved to a versatile active element for the realization of CM and VM circuits. The applications such as oscillators, filters, and analog computation have been discussed [187, 73, 75, 196, 150]. In the proposed work, a CNFET-based differential voltage current conveyor is used for digital control application, as shown in Fig. 4.9.

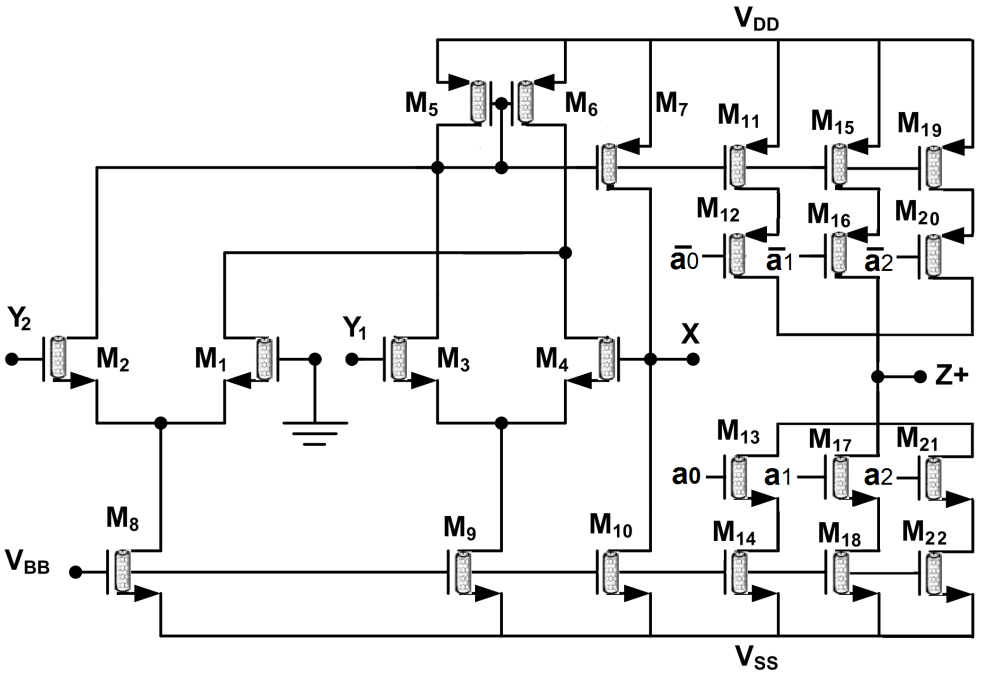

Figure 4.9: CNFET-based Digitally Programmable Differential Voltage Current Conveyor with only Z+ node

In the CMOS based digital control techniques [197, 198, 184], the additional stages of transistors are added to Z terminal of current conveyor to get the current gain n^th-times that can be controlled by the digital word. For getting current two times of I_X, the width of the transistors is increased by two times, and for $4I_X$ current the width of transistors should be four times. It means that transistors must be of different sizes even for Z port of current conveyor. Thus design complexity would increase for actual circuit implementation. Table 4.2 illustrates the comparison of different digital control techniques.

Table 4.2: Comparison of Various Digital Control Techniques for Three Binary Bits

Reference	**Device**	**Model**	V_{DD}	**Transistors**	**Aspect Ratio**
[198]	CCCII	0.25μm CMOS	$\pm$5.0 V	44	Different
[184]	CCII	0.25μm CMOS	$\pm$0.75 V	32	Different
[199]	FDCC	0.5μm CMOS	$\pm$1.5 V	44	Different
[148]	DVCC	0.5μm CMOS	$\pm$1.25 V	32	Different
This work	DVCC	32 nm CNFET	$\pm$0.9 V	22	Constant

The proposed circuit uses the transistors of the same size for the active device *i.e.* DVCC. It is possible in CNFET transistor only to double the current by doubling the number of CNTs, not by doubling the width as in conventional MOSFET. The width of CNFET is constant by adjusting the number of tubes (N), and pitch (S).

In MOSFETs, the drain current (I_D) increases by increasing the transistor width, while in carbon nanotube-FETs the drain current only rises by increasing the number or the diameter of CNTs [184]. A n-channel CNFET has been simulated to plot the V-I curve with changing the number of CNTs. It is found that the drain current raises double by increasing number of CNTs twice as shown in Fig. 4.10.

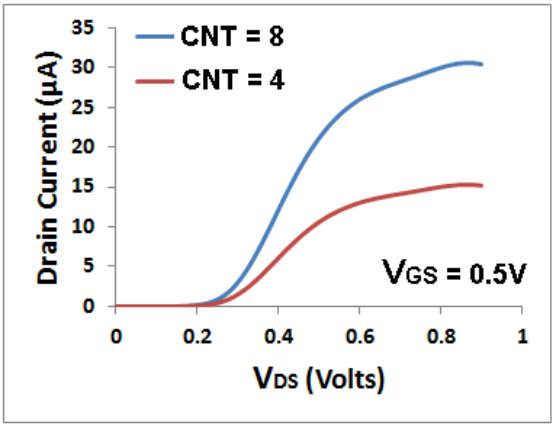

Figure 4.10: Dependence of Drain Current with no. of CNTs of a n-channel CNFET

It means, we can double the current by doubling the number of tubes in a carbon nanotube-FET. But, in the CMOS based design, doubling of current occurred by changing the width of the transistor. Therefore, the width of the transistors can be kept constant with the proposed design of digitally programmable analog block. In Fig. 4.9, transistors stage ($M_1 - M_{14}$) has 4 CNTs. Now, lets take the pitch of CNFET 75 nm for this stage. The calculated width of transistor is 226.5 nm.

Further, to double the current in next stage ($M_{15} - M_{18}$), number of CNTs should

Table 4.3: Digital Control Bits in DPDVCC

$a_2\ a_1\ a_0$ **(n)**	**Transistors (ON)**	**Transistors (OFF)**	**Current (I_Z+)**
0 0 0	NONE	$M_{12,13,16,17,20,21}$	0
0 0 1	$M_{12,13}$	$M_{16,17,20,21}$	I_X
0 1 0	$M_{16,17}$	$M_{12,13,20,21}$	$2I_X$
0 1 1	$M_{12,13,16,17}$	$M_{20,21}$	$3I_X$
1 0 0	$M_{20,21}$	$M_{12,13,16,17}$	$4I_X$
1 0 1	$M_{12,13,20,21}$	$M_{16,17}$	$5I_X$
1 1 0	$M_{16,17,20,21}$	$M_{12,13}$	$6I_X$
1 1 1	$M_{12,13,16,17,20,21}$	NIL	$7I_X$

be doubled *i.e.* 8. The pitch of CNFET adjusted in such away that the width become 226.5 nm. At constant width, the calculated pitch for the stage ($M_{15}-M_{18}$) is 32.14 nm. Similarly, stage ($M_{19}-M_{22}$) contains 16 CNTs, and pitch calculated 15 nm, keeping the width of CNFET constant.

$$W = (N-1) * S + D_{CNT} \tag{4.2}$$

The widths of transistor stages ($M_1 - M_{14}$), ($M_{15} - M_{18}$) and ($M_{19} - M_{22}$) are calculated by (4.3), (4.4) and (4.5) respectively. Thus, in all the stages, widths of transistors are same.

$$W = (4-1) * 75\ nm + 1.5\ nm;\ W = 226.6\ nm \tag{4.3}$$

$$W = (8-1) * 32.14\ nm + 1.5\ nm;\ W = 226.6\ nm \tag{4.4}$$

$$W = (16-1) * 15\ nm + 1.5\ nm;\ W = 226.6\ nm \tag{4.5}$$

Further, DC and AC analysis of digitally programmable differential voltage current conveyor (DPDVCC) have been performed with SPICE simulation. The current transfer characteristic and frequency response of DPDVCC have been shown in Fig. 4.11 and Fig. 4.12 respectively.

The current (I_Z) has been digitally programmed by digital word (a_2, a_1, a_0). Table 4.3 illustrates the ON/OFF state of the transistors ($M_{12}-M_{13}, M_{16}-M_{17}, M_{20}-M_{21}$) to understand the digital control action.

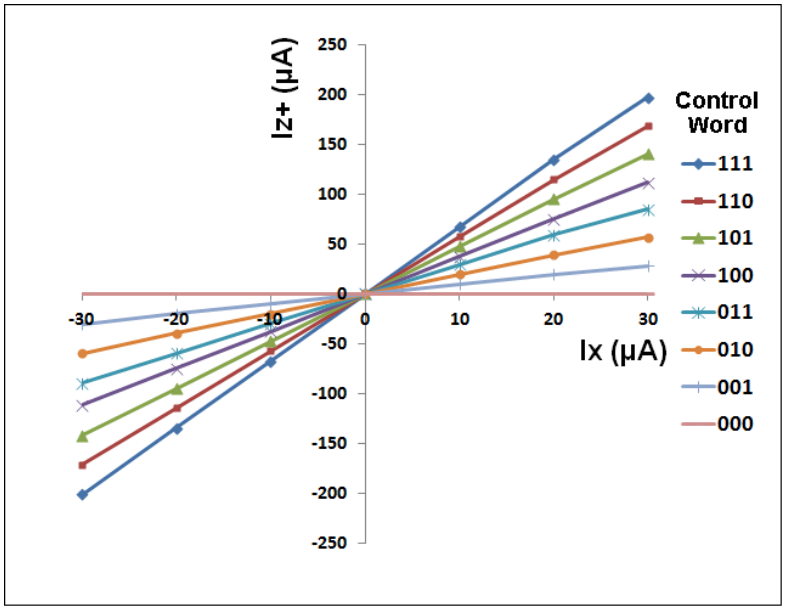

Figure 4.11: Transfer Characteristic of Digitally Programmable DVCC with Control Word

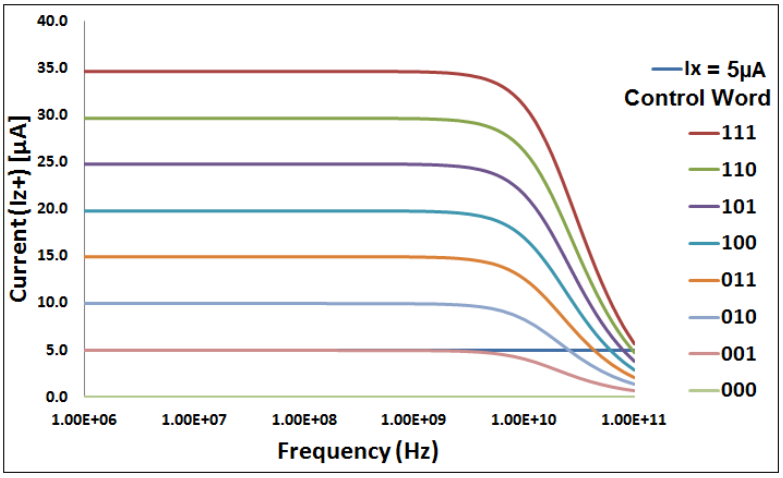

Figure 4.12: Frequency Response of Digitally Programmable DVCC with Control Word

The current (I_Z) can be digitally programmed by digital word (a_2, a_1, a_0), composed of the transistors ($M_{12} - M_{13}, M_{16} - M_{17}, M_{20} - M_{21}$) of Fig. 4.9, has been illustrated in Table 4.3. Moreover, the control word can be of 4 to 5 (even more) bits by putting an additional transistor stages at $Z+$ node. It means the maximum current gain (I_Z/I_X) can be achieved 15 to 31 times (or more). The transistors of the additional stage must have the number of CNTs double than their previous stage.

4.4 Applications of CNFET DVCC

4.4.1 Instrumentation Amplifier based on Digitally Programmable DVCC

A typical instrumentation amplifier receives differential input voltages and gives a single-ended output, suitable for measurement and test equipment [200, 201]. The basic circuit of instrumentation amplifier has been extensively configured using three Op-Amps. In proposed work the instrumentation amplifier is implemented by only one CNFET-based differential voltage current conveyor [202], which could work efficiently for both voltage-mode as well as current-mode circuit applications.

The concept of digital controlling is used to program the gain of the Instrumentation amplifier digitally. The proposed circuit of Fig. 4.13 utilizes the digitally programmed DVCC (DPDVCC) to control the gain, instead of using resistors [203, 204, 205].

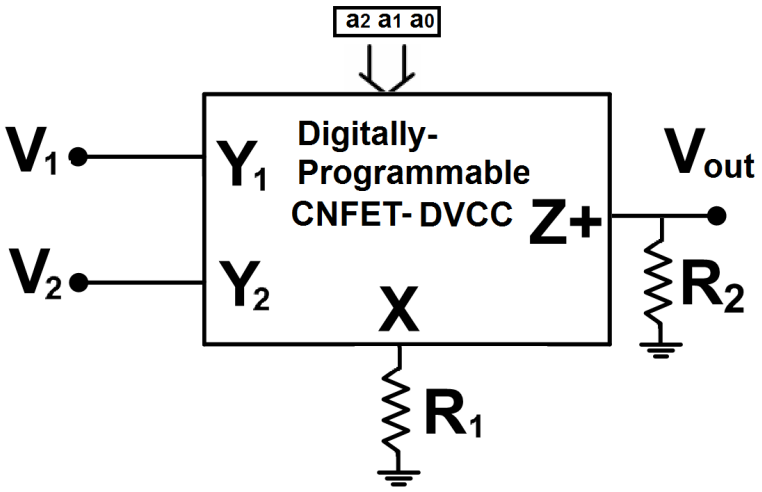

Figure 4.13: Instrumentation Amplifier with Programmable Gain

The current I_{Z+} of the DPDVCC circuit is responsible for this action because it is digitally programmed by transistors stage ($M_{11} - M_{22}$). The voltage transfer curve of the amplifier circuit is illustrated in Fig. 4.14. The gain of the Instrumentation amplifier is controlled by digital word (a_2 a_1 a_0) which has been depicted in Table 4.4.

$$V_{out} = n * (V_1 - V_2)\frac{R_2}{R_1} \tag{4.6}$$

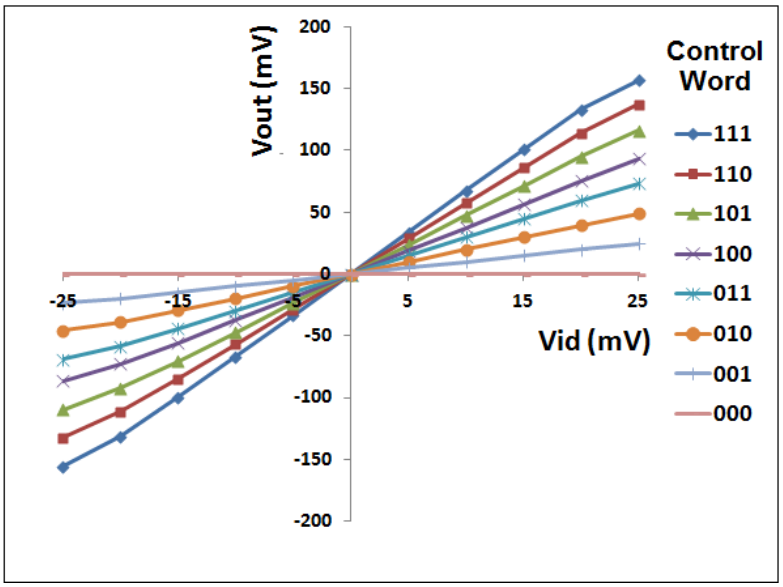

Figure 4.14: Transfer Characteristic of Instrumentation Amplifier with Variation in the Digital Control Word

Table 4.4: Digital Control Bits for Instrumentation Amplifier

$a_2\ a_1\ a_0$ **(n)**	000	001	010	011	100	101	110	111
Gain	0	1	2	3	4	5	6	7

The performance of CNFET-based instrumentation amplifier is tested with HSPICE simulations keeping $R_1 = R_2 = 1$ KΩ, and control word (a_2, a_1, a_0) being varied from (000–111). Here, n gives the equivalent decimal value of control word (a_2, a_1, a_0) with range from 0 to 7. The output voltage of the Instrumentation amplifier is expressed by the relation (4.6). The frequency response of instrumentation amplifier is shown in Fig. 4.15. A comparative study of current-mode Instrumentation amplifiers with CMOS and CNFET (this work) is given in Table 4.5.

Table 4.5: Comparative Study of Current-mode Instrumentation Amplifiers

Reference	**Model**	**Device**	V_{DD}	**Transistors**	**Bandwidth**
[202]	0.25μm CMOS	DVCC	±1.5 V	32	85 MHz
[203]	0.35μm CMOS	CCCII	±3.3 V	28	70 MHz
[204]	CMOS/BJT	CCII	–	26	2.97 MHz
[205]	CMOS/BJT	CCII	–	>26	1.2 MHz
This work	32 nm CNFET	DVCC	±0.9 V	22	11.78 GHz

The 3-dB bandwidth of Instrumentation amplifier is approximately 11.78 GHz. Fig. 4.16 presents the 3-dB and unity gain bandwidth of the amplifier. The bandwidth of the CNFET-based amplifier is large because the intrinsic capacitance of

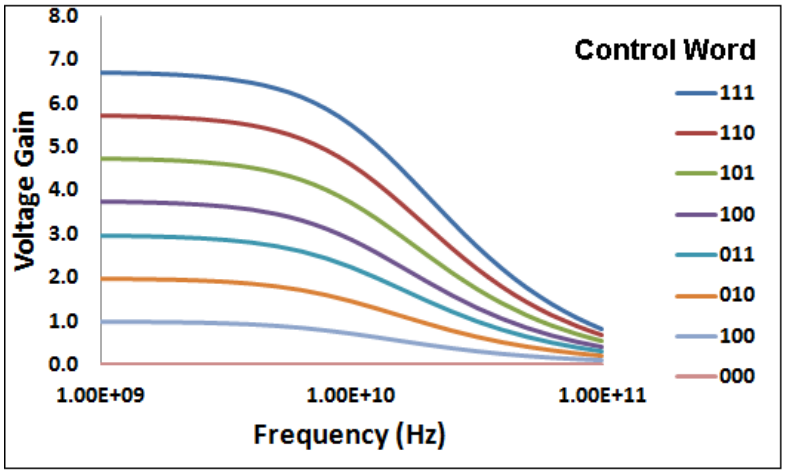

Figure 4.15: Frequency Response of the Instrumentation Amplifier with Variation in the Digital Control Word

CNFET is less than MOSFET. Another reason behind higher bandwidth is the significant increase in the transconductance of CNFET due to the parallel CNTs improving the driving capability of the device. In the proposed circuit transistors use multiple CNTs in the channel region.

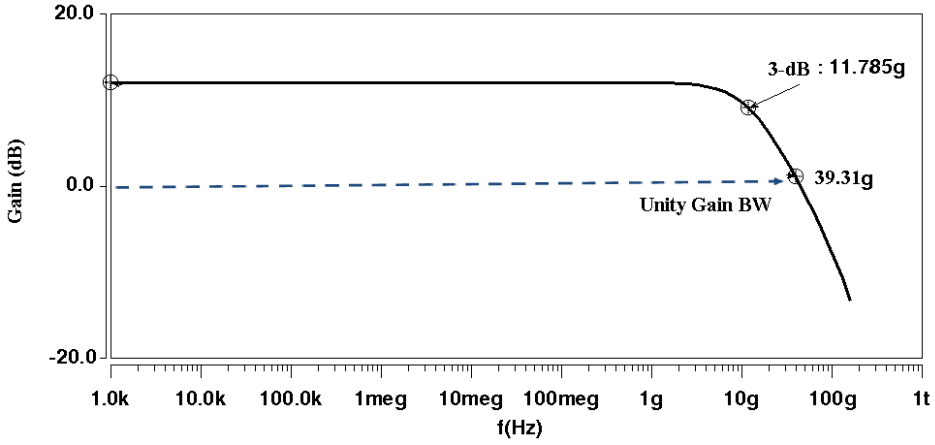

Figure 4.16: Representation of 3-dB and Unity Gain Bandwidth of the Amplifier

Moreover, the 3-dB current and voltage bandwidths increased slightly with the increase in CNT pitch as the current per tube gets raised for the higher pitch. Further, in the application areas like navigation, radar instrumentation, *etc.*, the instruments operate concurrently over different frequency band within the 160 MHz to 18 GHz range. Therefore, it is required to have the higher bandwidth in such kind of applications. The proposed CNFET-based circuit has the very wide bandwidth to operate at these frequencies and thus suitable for the above-

Table 4.6: Performance Parameters of the Instrumentation Amplifier

Parameter	Value
ICMR	0.806 V
Unity Gain BW	39.31 GHz
3-dB BW	11.78 GHz

mentioned application. The performance parameters like input common-mode range (ICMR) and unity gain bandwidth of the Instrumentation amplifier have been measured using SPICE simulation and shown in Table 4.6. Further, the results show that it has the 3-dB bandwidth of 11.78 GHz as compared to 85 MHz reported in literature [202].

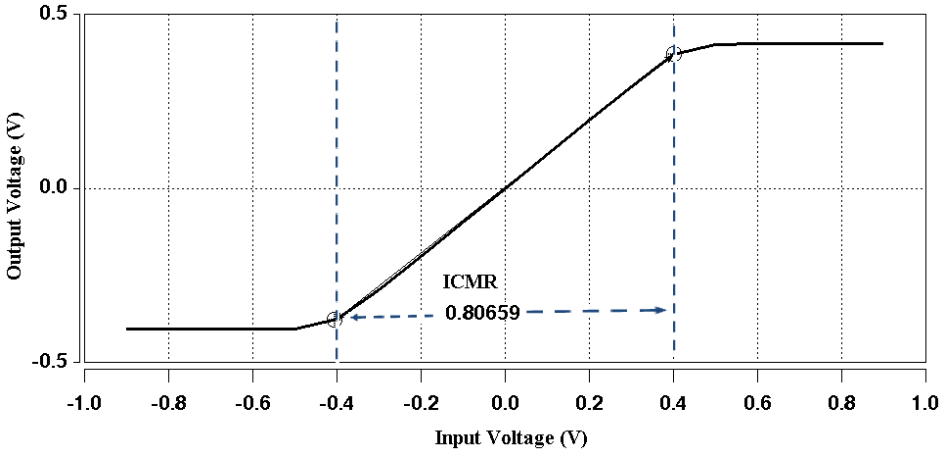

Figure 4.17: Input Common-mode Range of the Instrumentation Amplifier as obtained through HSPICE Simulations

Moreover, the input common-mode range of the instrumentation amplifier is measured 0.806 V and presented in Fig. 4.17.

(a) Non-ideal Analysis of Instrumentation Amplifier

The output voltage of the Instrumentation can be determined by the relation (4.6). The performance of the DVCC-based Instrumentation amplifier (IA) differs from ideal behavior because the voltage and current conveying acts are not exact, thus leading to deprivation in performance in the DVCC-based IA. Therefore, to account for non-ideal analysis, two parameters the current transfer gain from X node to Z node, α and voltage transfer gain, β are considered. The performance will be affected by considering non-ideal analysis.

$$V_X = (V_1 - V_2) \tag{4.7}$$

The voltage of terminal X is expressed by (4.7) but after the consideration of voltage transfer gain (β), voltage V_X can be written as (4.8). Further, current I_X is described in terms of input voltages (4.9). The current I_Z is shown by (4.10) with the current gain α (X to Z terminal) and control word n. Finally, the output voltage is expressed by (4.11).

$$V_X = (\beta_1 V_1 - \beta_2 V_2) \tag{4.8}$$

$$I_X = \frac{(\beta_1 V_1 - \beta_2 V_2)}{R_1} \tag{4.9}$$

$$I_Z = n * \frac{\alpha(\beta_1 V_1 - \beta_2 V_2)}{R_1} \tag{4.10}$$

$$V_{out} = n * \alpha(\beta_1 V_1 - \beta_2 V_2)\frac{R_2}{R_1} \tag{4.11}$$

Here, β_1 and β_2 are the voltage transfer gains from input terminals Y_1 and Y_2 respectively to the X terminal. α is the current transfer gain from X node to Z node [206]. Further, α = 1-ϵ_i and β = 1-ϵ_j, where ϵ_i and ϵ_j denote the current and voltage tracking errors of the DVCC. The transfer gains (α, β) deviate by unity because of the current and voltage tracking errors, which are fairly small and technology dependent.

(a) Parasitic considerations

A study is carried out on the effect of parasitics of the DVCC used in the Instrumentation amplifier of Fig. 4.13. The various parasitic of DVCC are port X parasitic in terms of R_X, port Z parasitic in form of $R_Z||C_Z$, and port Y parasitic as $R_Y||C_Y$. The modified expression for the gain of Instrumentation amplifier is written by (4.12):

$$V_{out} = n * (V_1 - V_2)\frac{R_2'}{R_1'} \tag{4.12}$$

here, $R_1' = R_1 + R_X$ and $R_2' = R_2||R_{Z1}||C_{Z1}$.

4.4.2 DVCC-based Low-power RF Filter

RF filters are required in several applications from audio to RF and across the complete spectrum of frequencies. These filters are used in communication systems such as satellite communication, transponders *etc.* Military radios for multi-band frequency-hopped transceivers also employ these filters. Additionally, Ku-band [12–18 GHz] is used for satellite communications, mainly for fixed and broadcast based services [207, 208].

Various techniques of RF filtering have been described in the literature [207, 209, 210, 179]. An active inductor-capacitor based band pass filter has been presented [209]. This technique has been applied to RF filter with center frequency of 1 GHz. A CMOS based high-Q RF filter has been presented [210], which utilizes Q-enhancing technique over the frequency range of 625 MHz to 1.68 GHz. A PMOS cascode structure has been used as the negative transconductance of a gyrator to reduce noise [207]. The cascode structure was utilized for tunable active RF band pass filter for the frequency range 3.9 - 12.3 GHz. Finally, a 12th-order complex filter structure has been illustrated for Bluetooth and Zigbee applications [179]. This filter was based on controllable transconductors with low power requirement. All these techniques have implemented with CMOS technology.

The active building block (DVCC) has been realized by CNFET, which is further used for the implementation of the proposed filter. The circuit uses two capacitors (C_1&C_2) and two resistors (R_1&R_2). The actual implementation of the RF filtering stage using DVCC is shown in Fig. 4.18. The filter has following features: (i) use of CNFET-based DVCC as active elements with low power requirement; (ii) the employment of all grounded resistors; (iii) operated with the low supply voltage of 0.9 V; (iv) suitable alternative for CMOS-based design.

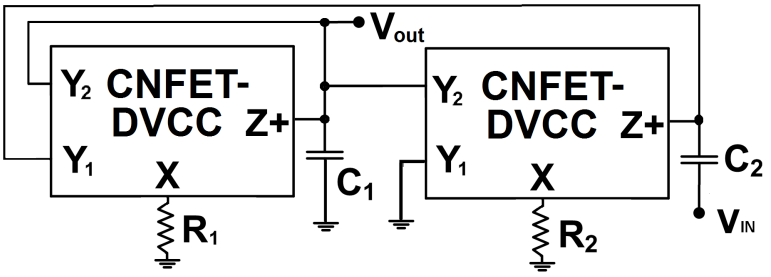

Figure 4.18: Proposed DVCC-based RF Band Pass Filter

The analysis of circuit of Fig. 4.18 gives the transfer function of proposed Ku-band filter and is given by (4.13). The equations for pole frequency and quality factor

of proposed filter are represented as (4.14) and (4.15).

$$\frac{V_{out}}{V_{in}} = \frac{\frac{s}{C_1R_1}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{C_1C_2R_1R_2}} \tag{4.13}$$

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \tag{4.14}$$

$$Q = \sqrt{\frac{C_1R_1}{C_2R_2}} \tag{4.15}$$

(a) Non-ideal Analysis This section describes the non-ideal analysis of the circuit shown in Fig. 4.18. The port relations of a non-ideal DVCC may be illustrated as (4.16).

$$V_X = [\beta_1 V_{Y1} - \beta_2 V_{Y2}], I_Z+ = \alpha I_X \tag{4.16}$$

where α is the current transfer gain from X to Z+ port and β_1 & β_2 are the voltage transfer gains from X to Y_1 and Y_2 ports respectively.

For the second-order filter function, the non-ideal second-order transfer function can be expressed as (4.17). The non-ideal pole frequency and quality factor can be written as (4.18) and (4.19). From (4.18), it is reflected that these non-idealities affect the performance of the circuit.

$$\frac{V_{out}}{V_{in}} = \frac{\frac{s\alpha}{C_1R_1\beta_1\beta_2}}{s^2 + \frac{s\alpha}{C_1R_1\beta_2} + \frac{\alpha^2}{C_1C_2R_1R_2\beta_1\beta_2}} \tag{4.17}$$

$$\omega_0 = \sqrt{\frac{\alpha^2}{C_1C_2R_1R_2\beta_1\beta_2}} \tag{4.18}$$

$$Q = \sqrt{\frac{C_1R_1\beta_2}{C_2R_2\beta_1}} \tag{4.19}$$

(b) Sensitivity Analysis The sensitivity analysis of the filter circuit is illustrated in terms of the sensitivity of ω_0 and Q with respect to the variation in passive components. Sensitivity analysis with respect to passive components R_1, R_2, C_1 and C_2 is given by (4.20) and (4.21).

$$S_{C1}^{\omega_0} = S_{C2}^{\omega_0} = S_{R1}^{\omega_0} = S_{R2}^{\omega_0} = -\frac{1}{2} \tag{4.20}$$

$$S_{C1}^{Q} = S_{R1}^{Q} = \frac{1}{2}; \quad S_{C2}^{Q} = S_{R2}^{Q} = -\frac{1}{2} \tag{4.21}$$

The sensitivity figures for the proposed filter circuits are obtained to be less than unity in magnitude which reflects good sensitivity performance.

(c) Parasitic Analysis of the DVCC-based Filter

Fig. 4.19 shows the parasitic impedances of the differential voltage current conveyor. Terminal X has low value parasitic resistance R_X while terminals Y_1 and Y_2 have high value parasitics resistances R_{Y1} and R_{Y2} and low-value parasitic capacitances C_{Y1} and C_{Y2} respectively. The node terminals $Z+$ and $Z-$ exhibit high value parasitic resistances R_{Z1} and R_{Z2} and low value parasitic capacitances C_{Z1} and C_{Z2} respectively [211, 73].

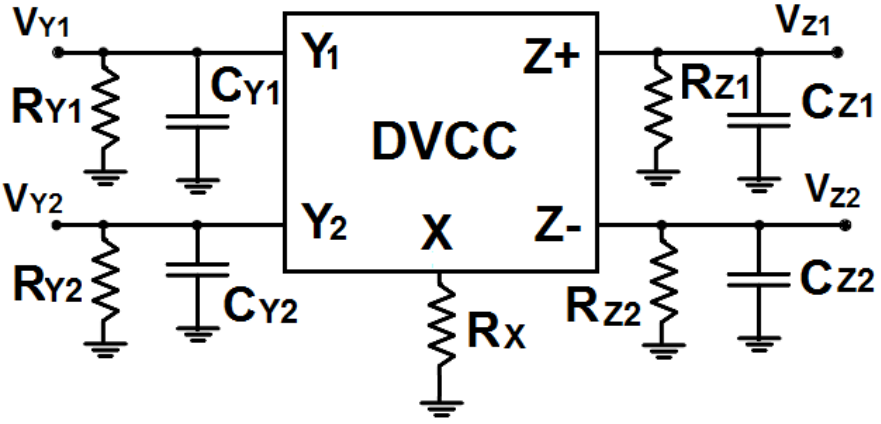

Figure 4.19: Parasitics associated with DVCC

Further, considering the parasitics of DVCC appear as the undesirable factors in (4.13) and $R_{P1} = R_{Y2}||R_{Z1}$ and $R_{P2} = R_{Y1}||R_{Z1}$, the modified transfer function of the proposed filter is expressed by (4.22).

$$\frac{V_{out}}{V_{in}} = \frac{(1 + \frac{sC_2R_{P2}}{1+sR_{P2}(C_{Y1}+C_{Z1})})(R_2 + R_X)}{(1 + \frac{sC_1R_{P1}}{1+sR_{P1}(C_{Y2}+C_{Z1})})(1 + \frac{sC_2R_{P2}}{1+sR_{P2}(C_{Y1}+C_{Z1})})(R_1 + R_X)(R_2 + R_X)}$$

$$\frac{\frac{R_{P1}}{1+sR_{P1}(C_{Y2}+C_{Z1})}}{+(1+\frac{sC_2R_{P2}}{1+sR_{P2}(C_{Y1}+C_{Z1})})\frac{(R_2+R_X)R_{P1}}{1+sR_{P1}(C_{Y2}+C_{Z1})}+\frac{R_{P1}}{1+sR_{P1}(C_{Y2}+C_{Z1})}\frac{R_{P2}}{1+sR_{P2}(C_{Y1}+C_{Z1})}} \quad (4.22)$$

For further simplification, assume the resistances R_A and R_B in term of parasitic components of DVCC $R_A = R_{P1}||C_{Y2}||C_{Z1}$ and $R_B = R_{P2}||C_{Y1}||C_{Z1}$, the transfer function is given by (4.23).

$$\frac{V_{out}}{V_{in}} = \frac{(1+sC_2R_B)(R_2+R_X)R_A}{(1+sC_1R_A)(1+sC_2R_B)(R_1+R_X)(R_2+R_X)+(1+sC_2R_B)(R_2+R_X)R_A+R_AR_B} \quad (4.23)$$

By solving equations (4.23) the transfer function of the filter are written by (4.24):

$$\frac{V_{out}}{V_{in}} = \frac{(1+sC_2R_B)R_2'R_A}{(1+sC_1R_A)(1+sC_2R_B)R_1'R_2'+(1+sC_2R_B)R_2'R_A+R_AR_B} \quad (4.24)$$

where, $R_1' = (R_1 + R_X)$ and $R_2' = (R_2 + R_X)$.

(d) Results and Discussion

The proposed filter is analyzed which satisfies the band pass filter function. HSpice simulations have been carried out to test the performance of the proposed circuit. To simplify (4.14), let take $R_1 = R_2 =$ R and $C_1 = C_2 =$ C. The center frequency can be expressed as (4.25). To cover the entire Ku-band range, four different center frequencies are considered as 12 GHz, 14 GHz, 16 GHz & 18 GHz. Now, to realize these frequencies the value of RC (time constant) should be approximately equal to $1/\omega_0$. If the value of resistor is taken few KΩ, then the value of capacitor should be in the range of femto-farad (fF). Now, let $C_1 = C_2 = 5$ fF then the calculated values of resistor are found to be 2.6 KΩ, 2.3 KΩ, 2.1 KΩ, and 1.7 KΩ. The characteristics of the proposed filter have been illustrated in Table 4.7.

Table 4.7: Characteristics of the Proposed Filter as Measured by HSpice simulation

Factor	**Value**
Power Supply	±0.9 V
Power Consumption	524 μW
Center Frequency (Case 1)	12.34 GHz
3-dB Bandwidth	10.11 GHz

$$\omega_0 = \frac{1}{CR} \tag{4.25}$$

Fig. 4.20 shows the center frequency tuning of the proposed filter. The frequencies f_1 to f_4 correspond to simulation result of four different cut-off frequencies *i.e.* 12.4 GHz, 14.5 GHz, 16.5 GHz and 18.5 GHz.

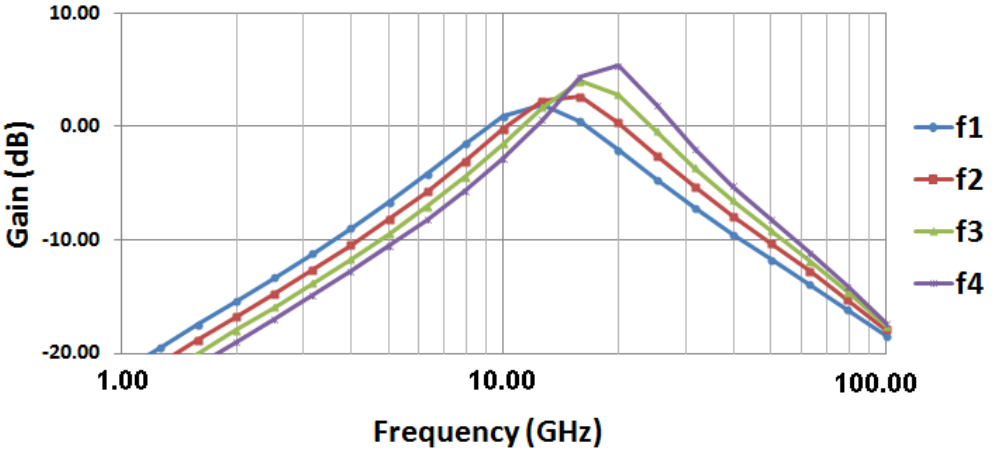

Figure 4.20: Tuning of Center Frequency of the Filter

The filter is also suitable for low power applications. HSPICE simulation has calculated the power requirement of 524 μW only.

4.5 Summary

This chapter presented the realization of CNFET-based DVCC and compared its results with CMOS-based DVCC. Further, a novel Carbon nanotube-based digitally programmable DVCC was proposed which enhances the functionality of the device. The work is extended to realize a programmable gain Instrumentation amplifier based on digitally programmable DVCC. The Instrumentation amplifier is suitable for the use in signal processing, measurement, and test equipment. Additionally, a DVCC-based low power RF filter was designed which can operate the complete range of Ku-band frequencies and useful for satellite communication.

Chapter 5

Design of Ultra-low Transconductance Amplifier

5.1 Introduction

The processing of physiological signals such as Electrocardiogram (ECG), Electroencephalogram (EEG), *etc.* requires analog signal processing blocks operating at very low frequencies typically in the sub-3000 Hz range. Table 5.1 presented the amplitude and frequency ranges of some conventional biomedical/physiological signals [212, 213]. Conventional Opamp-RC design methodologies are not appropriate for such very low frequencies due to the requirements of large values of passive components, as shown in (5.1). The frequency range of ECG signals is from 0.01—300 Hz. The Opamp-RC based filter design needs high values of resistances and capacitances.

$$f \propto 1/RC \tag{5.1}$$

A substitute is to utilize the g_m-C technique which offers to a resistor-less design. However, even in the g_m-C design technique, the required values of capacitors tend to be large if the transconductance of the OTA is high. Therefore, research attention has been going towards the design of ultra-low transconductance OTAs which can be used with small-sized capacitors to design analog circuits for very low-frequency applications, as given in (5.2).

$$f \propto g_m/C \tag{5.2}$$

Table 5.1: Amplitudes and Frequency Ranges of Biomedical/Physiological Signals

Signal	**Amp. Range (mV)**	**Freq. Range (Hz)**
ECG	0.05-3	0.01-300
EEG	0.001-1	0.1-100
EOG	0.001-0.3	0.1-10
EMG	0.001-1000	50-3000

The previous works were based on the various low-g_m techniques like current division, current cancellation, series-parallel current division *etc.* to achieve transconductance g_m, from few nA/V to pA/V range. An OTA using floating-gate MOS with input-voltage attenuation has also been discussed [214]. Additionally, OTA based on current division technique has been explored. This technique achieved g_m of 0.1 μA/V. Moreover, by current cancellation technique transconductance was achieved 10 nA/V. Thus, g_m up to nA/V range obtained by above technique [215]. In addition to this, a series-parallel current division technique was also exploited.

It was based on series-parallel current mirror structure and reduces the g_m to the range of pA/V. The minimum achieved g_m by this technique was 33 pA/V [216].

The work contained in this Chapter presents a very low-g_m operational transconductance amplifier using carbon nanotube-FET. Moreover, it is possible to reduce g_m up to sub-10 pA/V using the proposed technique.

5.2 Ultra-low Transconductance Amplifier

The operational transconductance amplifier (OTA) takes two input voltages and generates the output current that is directly proportional to the difference between the two input voltages. The output current of transconductance amplifier is expressed by (5.3), where g_m is transconductance of the amplifier [217, 218, 219].

$$I_{out} = g_m * (V_1 - V_2) \tag{5.3}$$

The proposed CNFET-based transconductor is shown in Fig. 5.1. In addition to this, the design parameters of carbon nanotube-FET for the proposed transconductor are listed in Table 5.2. The objective of the design to achieve transconductance in the range of sub-10 pA/V. The number of carbon nanotubes (CNTs) in different stages of transistors are different. Such as, transistors M_{1-18} have six CNTs, transistors M_{23-26} contain four CNTs and transistors M_{19-22} with one CNT, to achieve the desired results. The analysis of the circuit gives the relations (5.4)–(5.5) for the currents I_X and I_Z.

$$I_X = \frac{V_X}{R_3} = \frac{(V_{Y1} - V_{Y2})}{R_3} \tag{5.4}$$

By the property of the Current conveyor ($I_Z\pm = \pm I_X$).

$$I_{Z1} = \frac{(V_{Y1} - V_{Y2})}{R_3}; \quad I_{Z2} = \frac{-(V_{Y1} - V_{Y2})}{R_3} \tag{5.5}$$

The voltages of Z_1 and Z_2 nodes are written as (5.6).

$$V_{Z1} = I_{Z1} * R_1; and \quad V_{Z2} = I_{Z2} * R_2 \tag{5.6}$$

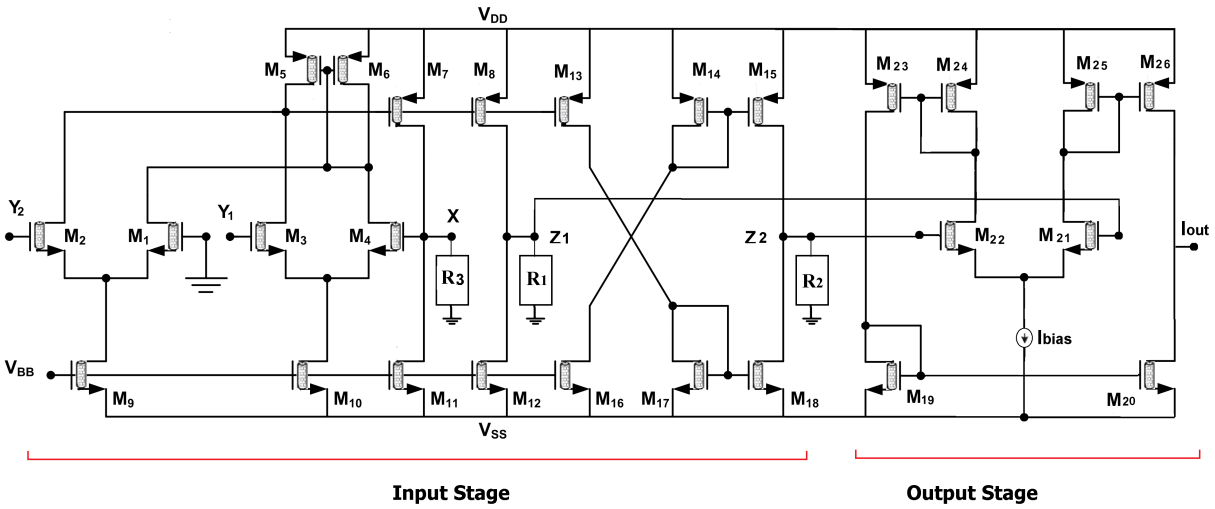

Figure 5.1: Proposed Carbon Nanotube-FET based Transconductor

Moreover, applying the value of I_{Z1} and I_{Z2}, voltages V_{Z1} and V_{Z2} are written as (5.7).

$$V_{Z1} = \frac{(V_{Y1} - V_{Y2}) * R_1}{R_3}, \quad V_{Z2} = -\frac{(V_{Y1} - V_{Y2}) * R_2}{R_3} \tag{5.7}$$

For simplifying the design, consider resistors $R_1 = R_2$ and $R_3/R_1 = R_3/R_2 = A$, equation (5.7) can be written as (5.8).

$$V_{Z1} = \frac{(V_{Y1} - V_{Y2})}{A}, \quad V_{Z2} = \frac{-(V_{Y1} - V_{Y2})}{A} \tag{5.8}$$

Now, consider the properties of OTA, the expression for output current is obtained (5.9). By putting the value of V_{Z1} & V_{Z2}, the expression for an output current is obtained (5.10) & (5.11). Here, term 'A' has been considered as the resistance ratio of the circuit. From equations (5.3) and (5.11), it has been observed that g_m is reduced by a factor of (A/2).

$$I_{out} = g_m * (V_{Z1} - V_{Z2}) \tag{5.9}$$

$$I_{out} = g_m * [\frac{(V_{Y1} - V_{Y2})}{A} - (-\frac{(V_{Y1} - V_{Y2})}{A})] \tag{5.10}$$

Table 5.2: CNFET Parameters for the Proposed Transconductor

Parameters	**Value**
Oxide Thickness (T_{ox})	4 nm
Dielectric Constant (K_{ox})	16
Power Supply	±0.9 V
Chirality of the tube (n, m)	19, 0
Physical channel length (L_{ch})	32 nm
Pitch (S)	20 nm
Diameter of CNT (D_{CNT})	1.5 nm

Table 5.3: Tuning of Transconductance (g_m), [$R_1 = R_2 = 1$ K]

R_3	**Resistance ratio (A)**	g_m **(pA/V)**	**Linear Range**
6 K	6	8	290 mV
8 K	8	6	400 mV
10 K	10	4.8	500 mV
20 K	20	2.59	766 mV

$$I_{out} = \frac{g_m}{(A/2)} * (V_{Y1} - V_{Y2}) \tag{5.11}$$

Thus, g_m depends on resistance ratio (A) of the proposed circuit. Table 5.3 illustrated the tuning of transconductance with the resistance ratio.

The circuit of proposed transconductor is also simulated with 32 nm CMOS technology node (PTM model). The proposed work has excellent results in comparison with previously reported work [216, 214, 220]. The proposed work has superior performance parameters like g_m (lower), linear range (higher) and power requirement (lower) as compared to CMOS design as illustrated in Table 5.4.

Table 5.4: Comparison of CNFET- and CMOS-based Transconductor

Parameters	**CNFET**	**CMOS**
$g_m(minimum)$	2.59 pA/V	40 pA/V
Linear Range	766.8 mV	338.9 mV
Power Supply	±0.9 V	±0.9 V
Power Dissipation	756.7 μW	7574 μW
No. of Transistors	26	26

Considering the circuit of Fig. 5.1, supply voltage and bias voltage (V_{BB}) have been kept ±0.9 V, and −0.36 V. The proposed circuit consumed 549 μW. As discussed earlier, the resistance ratio 'A' depends on resistors R_1, R_2 and R_3. The transconductance value in sub-10 pA/V range is achieved with the resistance ratio

of six and above. Fig. 5.2 illustrates the output current and linear range of the proposed transconductor. The minimum transconductance (g_m) is obtained 2.59 pA/V with the linear range of 766 mV.

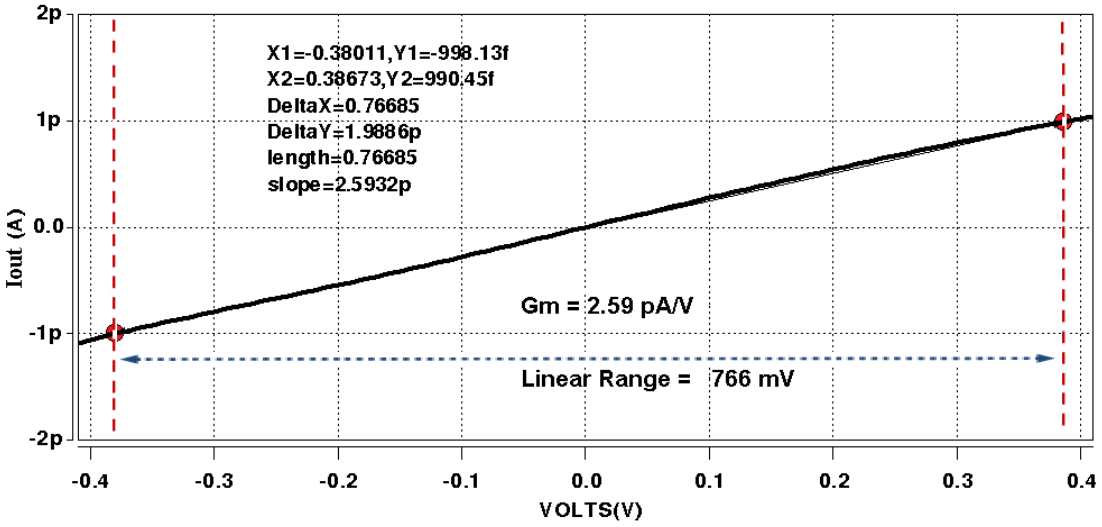

Figure 5.2: Linear Range of the CNFET-based Transconductor

Table 5.5: Comparison of Low-g_m Techniques

Parameters	**[216]**	**[220]**	**[214]**	**This Work**
$g_m(minimum)$	33 pA/V	30 pA/V	15 pA/V	2.59 pA/V
Linear Range	300 mV	500 mV	2 V	766.8 mV
Power Supply	2 V	2 V	2 V	0.9 V

Additionally, the performance of proposed transconductor is compared with existing literature. Table 5.5 presents the comparison among various low-g_m techniques. The proposed work has better results to achieve the minimum value of transconductance.

5.3 Digitally Programmable Transconductance Amplifier

In the previous section, a circuit of ultra-low transconductance amplifier has been discussed. It was an attempt to apply the digital control technique to the transconductance amplifier. There are many digital control techniques discussed in the literature [184, 221, 197, 222]. The digital control technique also adds reconfigurability to the circuit. In 2008, a digitally controlled CMOS voltage gain amplifier

(VGA) was proposed that was used as a digitally programmable current conveyor [197]. Additionally, a CMOS based digitally programmable CCII was discussed [184] which used 4-bits to control the current of Z+ terminal. In addition to this, the techniques of [222] used current division cell (CDC) to realize the digitally programmable current follower (DPCF). Moreover, the work of [221] presented a novel approach of DDCC and R-2R ladder network-based digital control technique. There was requirement of extra passive components in the form of the R-2R ladder structure.

In MOSFETs, the drain current (I_D) enhances by increasing the transistor width, while in carbon nanotube-FETs the drain current rises by increasing the number or the diameter of CNTs [109, 184, 223]. It means the current can be doubled by doubling the number of tubes in a carbon nanotube-FET.

The proposed digitally controlled transconductance amplifier is shown in Fig. 5.3. In the given circuit, transistors stages ($M_1 - M_{14}$) and ($M_{27} - M_{30}$) have four CNTs. Further, to double the current in next stage ($M_{15} - M_{18}$) and ($M_{31} - M_{34}$), number of CNTs should be doubled *i.e.* eight. Similarly, stages ($M_{19} - M_{22}$) and ($M_{35} - M_{38}$) contain sixteen CNTs. Further, in the next stage, transistors ($M_{39} - M_{42}$) have four CNTs and transistors ($M_{43} - M_{46}$) have one CNT.

Table 5.6: Digital Control Bits for Proposed Second OTA

a_2 a_1 a_0	**Decimal Value (n)**
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

Here, 'n' represents the equivalent decimal value of digital control word (a_2, a_1, a_0). For a 3-bit digital control word, value of n ranges from 0 to 7 as given in Table 5.6. The expression for the current can be written as (5.12).

$$I_{Z1} = n * I_X;\ I_{Z2} = -n * I_X \tag{5.12}$$

The analysis of Fig. 5.3 drives the relations (5.13)–(5.15) for the currents I_X and I_Z.

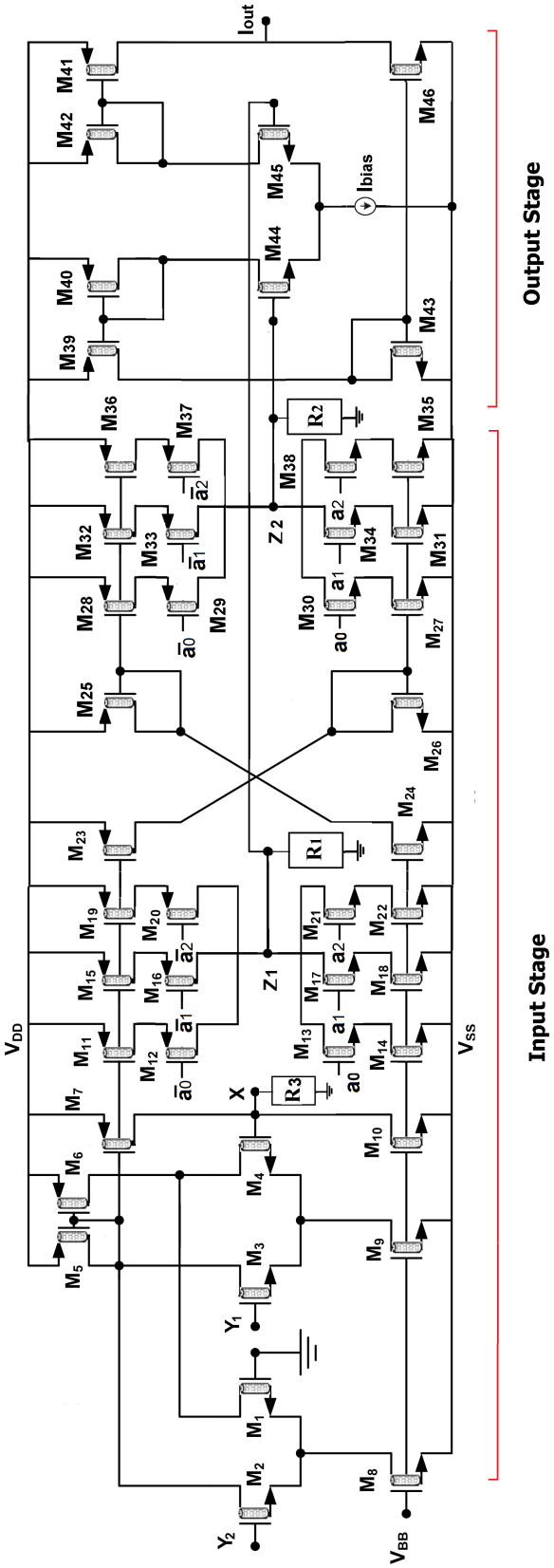

Figure 5.3: Digitally Controlled OTA using CNFET

$$I_X = \frac{V_X}{R_3} = \frac{(V_{Y1} - V_{Y2})}{R_3} \tag{5.13}$$

$$I_{Z1} = n * I_X; \quad I_{Z2} = -n * I_X \tag{5.14}$$

$$I_{Z1} = \frac{n * (V_{Y1} - V_{Y2})}{R_3}; \quad I_{Z2} = \frac{-n * (V_{Y1} - V_{Y2})}{R_3} \tag{5.15}$$

The voltages of Z_1 and Z_2 nodes can be also obtained by (5.16). Applying the value of I_{Z1} and I_{Z2}, the expression for V_{Z1} and V_{Z2} can be written as (5.17).

$$V_{Z1} = I_{Z1} * R_1; \quad V_{Z2} = I_{Z2} * R_2 \tag{5.16}$$

$$V_{Z1} = n * (V_{Y1} - V_{Y2}) * \frac{R_1}{R_3}; \quad V_{Z2} = -n * (V_{Y1} - V_{Y2}) * \frac{R_2}{R_3} \tag{5.17}$$

Now, consider the properties of OTA, the expression of output current expressed by (5.18). If $R_1 = R_2 = R$, $R_3 = 2R$ and putting the value of V_{Z1} & V_{Z2}, the equations can be defined as (5.19) & (5.20).

$$I_{out} = g_m * (V_{Z1} - V_{Z2}) \tag{5.18}$$

$$I_{out} = n * g_m * [\frac{(V_{Y1} - V_{Y2})}{2} - \frac{(-(V_{Y1} - V_{Y2})}{2})] \tag{5.19}$$

$$I_{out} = (n * g_m) * (V_{Y1} - V_{Y2}) \tag{5.20}$$

From equations (5.3) and (5.20), it has been observed that g_m is controlled by digital control word (a_2, a_1, a_0).

Additionally, Fig. 5.4 depicts the linear range of digitally controlled OTA of Fig. 5.3. Here, the resistors $R_1 = R_2 = 1$ KΩ and $R_3 = 2$ KΩ and digital control (a_2, a_1, a_0) word is 001. The simulated value of transconductance is 24 pA/V with the linear range of 94 mV. Fig. 5.5 shows the variation in the linear range of the digitally controlled transconductor with the control word.

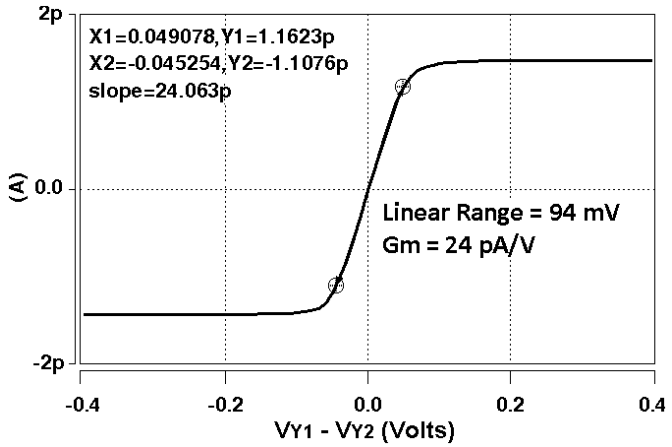

Figure 5.4: Linear Range of the Digitally Controlled Transconductor

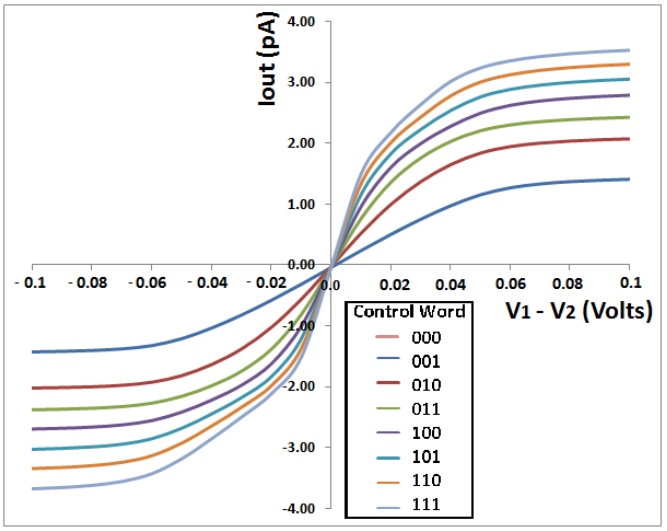

Figure 5.5: Illustration of Linear Ranges vs. Control Word for the Digitally Controlled Transconductor

Table 5.7: Linear Range and Transconductance (g_m) Values of Digitally Controlled OTA

S.N.	**Control Word** (a_2, a_1, a_0)	g_m	**Linear Range**
1	000	0	0
2	001	24 pA/V	94 mV
3	010	42 pA/V	73 mV
4	011	60 pA/V	53 mV
5	100	75 pA/V	45 mV
6	101	90 pA/V	40 mV
7	110	120 pA/V	25 mV
8	111	140 pA/V	22 mV

Table 5.7 presents the simulated values of transconductance and the linear ranges of digitally controlled OTA with the change in the control word (a_2, a_1, a_0). It means there is flexibility to choose the different transconductance values.

5.4 Summary

This chapter explores the approach of low-voltage, ultra-low g_m OTA design using Carbon nanotube-FETs. The circuit uses differential voltage current conveyor (DVCC) as an amplifier block in the design of transconductance amplifier. Simulation results illustrate the minimum transconductance of 2.59 pA/V with the linear range of 766 mV by the proposed design. The proposed circuit requires a supply voltage of $\pm$0.9 V and dissipated 756.7 μW. Moreover, the proposed OTA has been extended with the tuning of transconductance (g_m) digitally.

Chapter 6

Conclusion

6.1 Conclusion

The carbon nanotube field effect transistor (CNFET) is one of the promising candidate among emerging electronic devices like TFET, SET, NWFET to extend the conventional Silicon MOSFET technology. As the characteristics of a CNFET are superior from bulk CMOS, new design methodologies must be established. The continuous development of the models of CNFET and their performance estimation described in the literature. The performance results of CNFET-based circuits are good enough to overcome the bulk CMOS.

In the view of above, this thesis analyzes the characteristics of CMOS & CNFET and proposes new methodologies based on CNFET such as current conveyor, an operational transconductance amplifier, active filters, *etc.*

This thesis contains six chapters including 'Introduction.' The thesis begins with CMOS and its challenges due to continuous downscaling. After that, a brief overview and merits of emerging semiconductor device technologies are presented. The literature helps to find the motivation for research in the present field, and able to develop an understanding of the issues arise in existing CMOS technology. Additionally, the contributions of the thesis are summarized.

The discussion of Chapter 2 has confirmed that the CNFET technology is a feasible solution to replace the traditional bulk CMOS technology. Further, CMOS scaling challenges are described in detail. The electrical properties of CNT are very suitable to explore it for the main stream of emerging semiconductor device applications. The work has also reviewed the distinct features of CNFET with its challenges. The thesis included a brief information about the Stanford CNFET model which is used in this work. A detailed review of CNFET based analog and digital circuits with their merits over CMOS is also presented. Moreover, the overview of current-mode circuits and their applications in the field of analog signal processing have been illustrated. Further, a concise discussion is presented on active filters which has a significant applicability in this work. Finally, various research gaps from the literature review are highlighted.

The research work undertaken in the thesis is initiated by comparing the performance of CMOS- and CNFET-based analog building block named inverting current conveyor (ICCII) and presented in chapter 3. As discussed earlier that CNFET-based realization has exceeded in the parameters such as voltage & current bandwidths, power requirement *etc.* Moreover, the active block is tested for variations in the CNT parameters like diameter (chirality), no. of tubes *etc.* This

exercise helps the researchers to efficiently choose the CNT parameters for specific results/application. In addition, two active filter circuits based on CNFET have been proposed which are designed to operate in certain wireless applications like Bluetooth and Zigbee. Additionally, a resistive sensor interface based on Carbon nanotube-FET is presented which can be utilized in the potentiometer, strain gauge, and photocell.

Moreover, the research work is extended to realize the differential voltage current conveyor (DVCC) using carbon nanotube-FET. To enhance the operability and flexibility, a novel CNFET-based digitally programmable technique is proposed. This method uses multiple CNTs to increase the drain current of the transistor. After that, this digital control approach is used to implement an Instrumentation amplifier with programmable gain which has its utility in analog signal processing. Additionally, CNFET DVCC-based active filter is added in this work which is designed to operate in Ku-band (12- 16 GHz) frequencies and will be a good example for low-power RF front-end design.

The next objective of the thesis was design of ultra-low transconductance amplifier. For this, a CNFET-based transconductance amplifier is presented. It has the minimum value of transconductance (g_m) comparing with existing literature. The transconductance of the amplifier is tuned using the digitally programmable technique.

6.2 Suggestions for Future Work

The CNFET-based designs could be suitable alternatives for the 'beyond-CMOS' era. That would result in low-voltage low-power solutions for applications such as portable electronics and high-frequency communications. CNFET-based low-power circuit design can solve the challenges of current nanoelectronics. The design space of CNFET-based analog circuit can be carried forward for the development of modern high-performance electronics. Many noticeable and feasible areas could be explored further. Some of these areas are mentioned here:

1. A lot of simulation work on the CNFET-based circuit has been presented in the literature. There is broad scope to develop the techniques to reduce the cost of real CNFET circuits. The cost-effective production of aligned semiconducting CNTs will be required for CNFET-based circuits shortly.

2. The present trend in the industry is to design configurable analog/digital blocks. Applications such as the field-programmable analog array (FPAA) and field-programmable gate array (FPGA) could be implemented using CNFET.
3. Recently, there is a growing need for low-power programmable devices. The floating-gate MOSFET (FGMOS) like structure can be extended using carbon nanotube field effect transistor. CNFET could be a suitable candidate for realizing ultra-low power high-density EPROM, EEPROM, and flash memories.
4. For various applications like radio frequency (RF) oscillators, low-noise circuits, and bandgap-based references BiCMOS technology is usually preferred. Thus, CNFET can be integrated with the bipolar transistor for the optimum use of both, for ultra-low power high-speed applications.

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