Simulation, Analysis and Performance Comparison of Multi-level Voltage Shifters

A thesis submitted in partial fulfilment of the requirements

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by

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Certificate

Department of Electronics & Communication Engineering

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This is to certify that the Dissertation Report on " **Simulation, Analysis and Performance Comparison of Multi-level Voltage Shifters**" by **Akanksha Tiwari** is bonafide work completed under my supervision, hence approved for submission in partial fulfillment for the Master of Technology in VLSI Design, Malaviya National Institute of Technology, Jaipur during academic session 2018-2019 for the full time post graduation program of session 2017-2019. The work has been approved after plagiarism check as per institute rule.

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Abstract

Novel nonvolatile memory technologies are gaining notable consideration from the semiconductor industry. Likewise, with distinct semiconductors, the flash memory chip size is the primary contributor to the expense of the device. However, with the evolution of VLSI technology which necessitates scaling down of supply voltages, the high speed switching from low to high voltage becomes difficult. The layout is complex as many blocks are high voltage in nature. Also, there is a lot of focus on the area. Level Shifter is a part of NVM. The on-chip area is increased if separate up and down voltage conversion circuits are used.

Low power design most critical issue in CMOS structure. Hence the multi-supply system is used, which is an efficient method to compress the power dissipation without lowering speed of the circuit. In the multi-voltage system level, the shifter circuit is used which reduce the static current streaming from supply to the ground when the input signal at a low level to high-level transition. The level shifter design in thesis removes the contention problem that is present in conventional voltage level shifter. Also, design a LeveL Shifter has the capability for both up and down conversion and reduced power and delay as compared to other existing level shifters.

Declaration

I declare that,

1. The work contained in this dissertation is original and has been done by me under the guidance of my supervisor.
2. The work has not been submitted to any other Institute for any degree or diploma.
3. I have followed the guidelines provided by the Institute in preparing the dissertation.
4. I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.
5. Whenever I have used materials (data, theoretical analysis, figures, and text) from other sources, I have given due credit to them by citing them in the text of the dissertation and giving their details in the references. Further, I have taken permission from the copyright owners of the sources, whenever necessary.

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Abbreviations

V_{dd}	**S**upply **V**oltage
V_{ddh}	**H**igh **S**upply **V**oltage
V_{ddl}	**L**ow **S**upply **V**oltage
V_{ddm}	**M**edium **S**upply **V**oltage
I_{vddh}	**H**igh **S**upply **C**urrent
I_{vddl}	**L**ow **S**upply **C**urrent
uW	**M**icrowatt
mW	**M**illiwatt
ps	**P**icosecond
ns	**N**anosecond
mA	**M**illiampere
nA	**N**anoampere
V	**V**olt
Pa	**A**ctive **P**ower
Ps	**S**tatic **P**ower
f	**F**requency

Symbols

α	Switching parameter
C	Capacitance

Dedicated To My Family, Teachers and Friends

Chapter 1

Introduction

1.1 Introduction

In ongoing VLSI circuits and system design because of the expanding request of handheld gadget like cell phones necessity of low power utilization configuration is an increment in VLSI design circuit. Presently a day, pretty much a huge number of transistors have been utilized into an individual chip utilizing nanometer technology. Because of this, the dissipation of heat caused by tremendous power consumption makes an issue that can severely affect the reliability and packaging cost of a plan. Every one of these elements has concerned a consideration on low power configuration. Therefore Low power design is a most important parameter in present-day VLSI circuits [2]. Flash memory are also utilized as capacity gadget in compact gadget like sensor and cellular phones. Since flash memories require high supply voltage for programming, read the data, and for data erasing task, the transistor in memory core circuits is available ought to be made to support voltage and therefore a distinctive technique is used for this purpose. Positive level shifters are employed for providing interfacing between memory core circuits working at high supply, and an automated circuit operates in low supply.

1.1.1 Sources of Power Dissipation

There are numerous sources of power leakage in the circuit,i.e., static power, dynamic power, and short circuit power dissipation. Dynamic power leakage is due to charging and

discharging of load capacitance between two distinct voltages. Static power utilization is because of a direct short circuit route linking supply to ground. Power is a because of infusion in a substrate is known as leakage power. So more awareness is to be paid towards leakage power reduction. Numerous sources of leakage power dissipation such as subthreshold leakage, gate leakage are exhibited. The total power dissipation is presented in equation (1.1).

$$P_{total} = \alpha \cdot C \cdot V_{dd}^2 \cdot f + I_{sc} \cdot V_{dd} + I_{sub} \cdot V_{dd} + I_{gateleakage} \cdot V_{dd} \tag{1.1}$$

In equation(1.1) the first term expresses the power dissipation due to switching phenomenon in the system. This sort of power referred as dynamic power. Shown in equation (1),α is the switching parameter, capacitance C is the load capacitance, clock frequency f, and supply voltage is V_{dd}. The second term speaks to power utilization because of static current or DC. This kind of power leakage is referred as static power. The static current rises because of the direct way of a stream of current from the supply voltage to ground, which is troublesome for low power design. Finally, the last two terms shows in equation (1.1) signify the power consumption because of leakage currents. Another class of leakage flow is gate leakage current, emerging from gate oxide relies on the thickness of gate oxide. Among all class of dynamic power, utilization has a severe effect on performance on a device because of switching activity of any design.

1.1.2 Techniques for Power Reduction

A standout amongst the most effective method for decreasing the power utilization in the electronic device diminishes the power supply voltage; however, the propagation delay of the circuit is expanded which influence the speed of the circuit. Another strategy is by utilizing diverse power supply to a various segment. Hence, in moderate speed or in an advanced circuit where distinctive part work in various speed double supply architecture used [1]. In this procedure, We divide the design into submodules depending on the necessity of the power supply voltage. The utilization of various voltage to advance gadget optimization and reliability while keeping up low power utilization. Such sort of gives low supply voltage to circuits that work at low speed to spare power, while higher supply voltages are provided to circuits that have higher speed necessities to the cost of expanded power utilization. There are additionally some other way to overcome power leakage discovered by researchers for instance by varying transistor size, multiple thresholds voltage vt and by using several channel length and oxide thickness for reduction of various

form of power dissipation addressed in equation(1.1). Sizing of the transistor is a decent tradeoff between power minimization and circuit performance [3]. But power reduction by this method is also suffered from leakage current; hence contrast with this method, multi-supply voltage is given in a single chip is a better way to reduce the power without degrading circuit performance. This strategy does not influence the inactivity of the framework. The numerous benefits of this plan is that comparable manufacture systems can be employed for preparing the chip. And furthermore, there is no requirement for making a parallel/pipelined path for data which cause result in the large area; hence, packaging cost is increased [5].

1.2 Need For a Level Shifter

The use of multiple voltages increases circuit complexity, and therefore requires throughout performance and reliability analysis. Level shifters need to be embedded for interfacing of separate voltage domains, and digital logic segments need to be designed for their dedicated voltage supply. The utilization of dynamic voltage scaling empowers for further enhancement among execution and power sparing by varying the supply voltage based on the speed necessities of the integrated circuit (IC) at any point of time. Figure(1.1) demonstrates the rule behind different voltage space use.

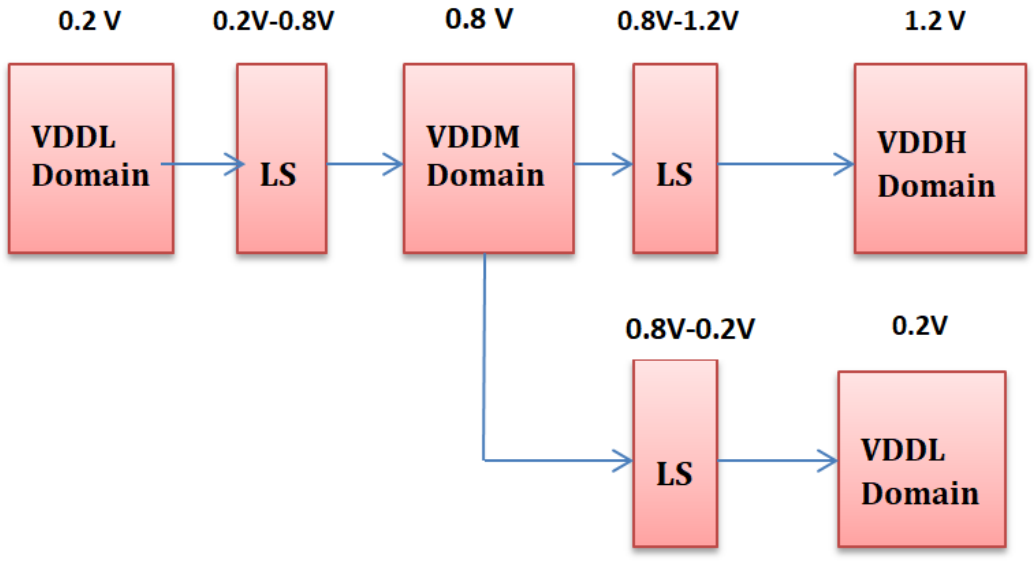

FIGURE 1.1: Multi Voltage Domain With Level Shifter

In figure(1.1) representation is expressed as

VDDL= Low voltage supply

VDDM= Medium voltage supply

VDDH= High voltage supply

LS= Level shifter

The thought behind the utility of this innovation in a single chip is to break the chip into a submodule, which is conducted in different voltages. The critical path module is provided by high voltage V_{ddh}, and non-critical path module is provided by low voltage V_{ddl}. A level shifter relies upon necessity used between the submodule for diminishing static power dissipation. Thus level shifter is a circuit which switches one voltage to several voltages. The level converter is classified into two classes: (1) level up shifter and (2) level down converter. At the point When the input is switched low value voltage V_{ddl} to high-value voltage V_{ddh} known as level up shifter. On the different side, which converts the high input value of voltage V_{ddh} into the low value of voltage V_{ddl} is known as level down shifter.

In this thesis, the level shifter with an auxiliary circuit for dual supply voltage is the design which switches an extremely low level of the input voltage into a high level of output voltage giving low power utilization. Also, design an energy efficient multi-level voltage level shifter, which converts the input level in both ways, i.e., up and down level.

Chapter 2

Literature Review

The level shifter has a massive role in the dualvoltage framework. Now a day, many researchers did different research in the different sorts of level shifter with degrading power utilization by the use of a dual voltage system. In this chapter, a level shifter is given, and related research work is reviewed. in the section 2.1 research work to multiple supplies examined, and in 2.2,2.3, and 2.4 sorts of a level shifter are presented.

2.1 Multi-voltage Supply System

A Multi-voltage system which uses more than one power-supply voltage in a similar framework is a successful method to reduce the power consumption without minimizing working speed. The way to plan a different voltage framework is to separate the design into submodule working at various voltage levels. For designing such type of modules algorithms like clustered voltage scaling (CVS) are broadly utilized. CVS techniques allow synchronous level transformation, which implies that in the wake of separating the single circuit into various submodule or cells working at various voltages. Level converters are embedded particularly at the interface of two cells. Authors in ([6], [7]) address in brief regarding multi-voltage supply frameworks and different calculations pursued distribution of voltage to cells. In [6], the authors have examined the CVS arrangement in detail and introduced a unique design called the extended CVS (ECVS) and they have likewise proposed a combination system of the design. This arrangement allows a level shifter any area there is an enormous slack between the gates. Difference between the required and arrival time of the signal at the gate is referred as slack [6]. In [7]], the authors introduce a technique wherein

it diminishes the number of interface level shifters commencing to a clustered voltage scaling. In [8], authors depict power minimization at the gate level utilizing double supply voltages. The possibility that the authors have proposed is that the part of the design which not requires high voltage are grouped into one part and provide a low supply to them so that power utilization is reduced.

2.2 Level Shifter

The level shifter is a circuit employed to convert signals from one logic level to other logic levels allowing compatibility between ICs with different voltage requirements such as CMOS. In CMOS logic circuits, the dynamic leakage shows the square root proportionality. If the supply voltage is high, then more amount of energy will be wasted. In this manner, if there is a low voltage supply is employed, then dynamic power will also be declined. In blended signal circuit, there can be a circumstance when lower voltage hardware needs to drive huge voltage hardware, for this situation PMOS of high voltage hardware may not turned off totally applying low voltage as input. In this way, there is a need for level shifter where low voltage and high voltage circuits are associated.

2.3 Positive Level Shifter

In the event that there is any interfacing between the circuits that work at a higher positive voltage level and electronic circuits that operate at Vdd that is low-level voltage, then positive level shifter is employed. The details of the structure implementation and obstacles occur in the positive level shifter is discussed by researchers review in section 2.3.1,2.3.2 and 2.3.2 [1].

2.3.1 Conventional Voltage Level Shifter

The conventional up-conversion voltage level shifter shown fig.(2.1) Is used PMOSs that are cross-coupled and used to latch output and settles it to either at V_{ddh} voltage or zero volts according to the state of input that is being supplied to level shifter. The high supply voltage V_{ddh}, and generation of it being done by a charge pump circuit. The charge pump is placed internally to memory, or it can act from some source external. In the beginning, if Q1 node at zero volts and node Q2 at a V_{ddh} voltage level and input pin IN are changed

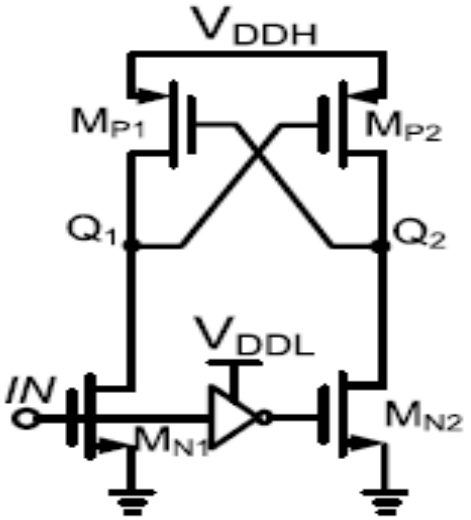

FIGURE 2.1: Conventional Positive Level Voltage Shifter [1]

from low level of voltage to high state of voltage, at that point transistor N1 is in on condition, and N2 is in off condition. Since the Q1 node and Q2 node is at zero volts and V_{ddh} respectively. Before output changes its state driving limit of pull-down transistor N4 needs to over-come latch phenomenon of PMOS. Mp2 transistor and Mn2 transistor are on when the input voltage is changed from low voltage to high state of voltage, immense quantities of hot carriers are produced in the channel between drain and source. Static current is in this way grown and in remain by mode static current utilization. It very well may be seen that, in this design, conflict is available at node Q1 and Q2 between the pull-up devices which are driven by V_{ddh} and pull-down devices that are driven by V_{ddl}.

Furthermore, in this way, if the distinction of voltage in the middle of V_{ddl} and V_{ddh} is huge, when the input voltage level is in the sub-threshold region, above circuit won't be able for change of voltage levels. The purpose of this change of flows of the pull-down transistor those is smaller than the pull-up transistors. Above issue can be rectified by technology-based method, for instance, strong pull-down devices are utilized utilizing less threshold voltage transistors, or weak pull up gadgets which are having high-threshold transistors. Strong pull-down devices can likewise be utilized, which is achieved by extending their width, which additionally builds both delay and utilization of energy.

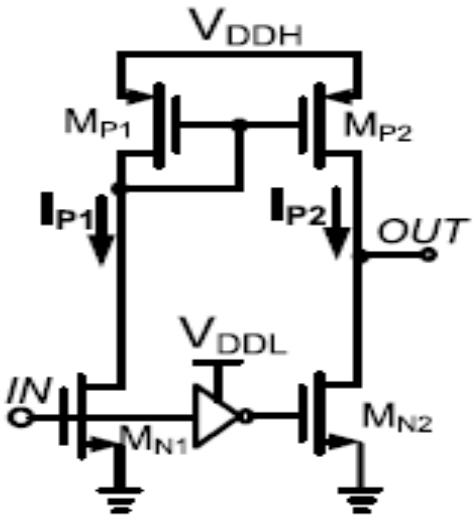

FIGURE 2.2: Level Shifter With a Semi-static Current Mirror [1]

2.3.2 Level Shifter With a Semi-Static Current Mirror

To solve this type of problem, many techniques are used, e.g., employing strong pull-down devices employing lowVth transistors and/or potentially powerless pullup networks by employing highVth transistors. Another methodology is to utilize a strong pulldown device by expanding their width, leading to an expansion in both delay and power utilization.

The arrangement is to decline the strength of the pullup a device when the pulldown device is pulling down the output node by utilizing of semi-static current mirror shown in fig(2.2). This method is used to confine the current and along these lines, the strength of the pull-up device (i.e., MP2) at the point when the pull-down device is pulling down the output node. This structure is experiencing static current that is passing through MN2 transistor and MP2 transistor during the "High" level of the input signal. For the decrease of the static power emission, a dynamic current generator is presented, which is turned on just in the span of change.

2.3.3 Level Shifter With a Dynamic Current Mirror(Wilson Current Mirror)

The structure appeared in Fig(2.3) utilizes a dynamic current generator executed by MP3 connecting in series with an MP1 transistor. Here, MN2 turned off whenever the input

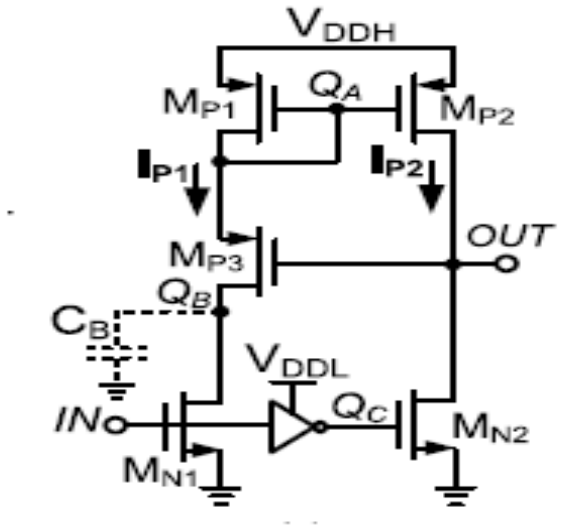

FIGURE 2.3: Level Shifter With a Daynamic Current Mirror(Wilson Current Mirror) [1]

signal IN changes from "Low" value of the voltage to "high state of voltage" and because of which MN1 is turned on, therefore, QB node goes down. MP3 is turned on, since the OUT node in prior case was "Low" (preceding change), in a span where OUT does not compares to level of input. Subsequently, through MN1 transistor, MP3 transistor, and MP1 transistor a change current begins streaming. Reflecting of this current is done to MP2 which prompts haul OUT node up.

Finally, MP3 is switched to off stage when an OUT node is pull up to V_{ddh}, and henceforth there is no static current moving through MN1 transistor, MP3 transistor, and MP1 transistor. Likewise, MN1 turns off when contribution to is changed from "high state" to "Low-level state," and MN2 transistor is turned on attempts to haul OUT down. MP3 turns on as OUT node is pulled down, which attempts to charge node QB, which released to the ground as of now, which means passing current is streaming through MP1 transistor and an MP3 transistor to charge QB. This current is presently replicated to MP2 transistor, and subsequently, it attempts to haul OUT node up, in a similar time MN2 transistor is attempted to pull this node down. One thing that can be understood here that a contention still there. This contention is in the high-to-low transition of input in between the pull-down and the pull-up transistors, which causes to the increment of delay of circuit and energy consumption.

2.4 Negative Level Shifter

The conventional negative level shifter is introduced By ([11],[12]), which is presented in figure(2.4). This class of level shifter is used to switch the high-value voltage to low-value voltage. When we employed a zero voltage to the input of the circuit, then transistor P2 is turned ON, and transistor P1 rests in OFF stage. Hence voltage V_{dd} appears as a supply voltage to the inverter and transistor N3 turned ON, V_{ddn} arises at the output node Vout. Alike when the low input voltage V_{ddl} is applied. In this situation, transistor P1 turned ON, and transistor P2 rests in OFF stage. V_{ddl} of input appears as input to the transistor N2. Hence transistor N2 turned ON, and voltage V_{NN} appears as an input to the inverter, and in this case, transistor P3 turned ON, and zero voltage arise at output node VOUT. Hecne this circuit is used as a level down shifter in the digital block. This level shifter experiences the complexity of the design and no. of transistors utilized in this circuit additionally static power discharge of the circuit turns out to be high. Hence propagation delay is increased consequences speed of the system decreased.

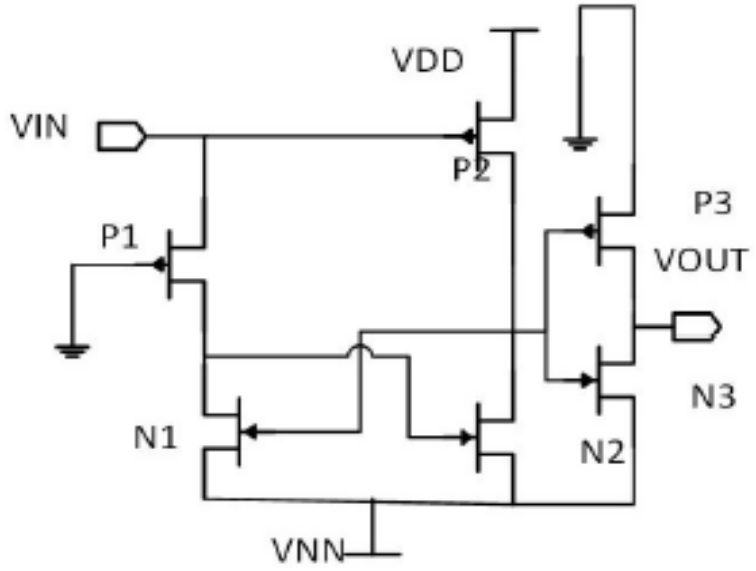

FIGURE 2.4: Conventional Negative Voltage Shifter [[11],[12]]

However, the utilization of level converters causes the costs regarding power Utilizations, delay, and area. Other than the addition of the level converters may raise the complexity in hardware design. Along these lines, one of the major challenges in a multi-VDD system is to diminish the costs brought about by embeddings the level converters. Hence in chapter 3 presented a novel level converter which provides level up converter and a up/down

converter which provides flexibility in hardware design and additionally advantages on low power and high performance compared to another level converter.

Chapter 3

Design of Multilevel Voltage Level Converter

The level shifter circuits with an auxiliary circuit which shown in figure(3.2) is used for level upconversion is discussed in section(3.1) and Multilevel shifter which is used in both type of conversion up and down shown in fig(3.3) is discussed in section(3.2).

3.1 Level Up Coverter With Auxilliary Circuit

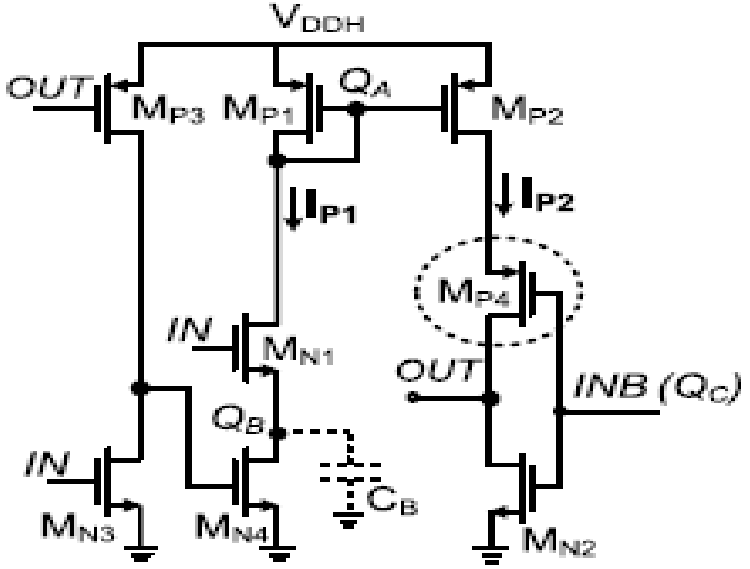

FIGURE 3.1: Modified Level Up Shifter [1]

If we wish to decline the argument mentioned in Chapter 2 that also at the high-level voltage to low-level voltage transition, at that point there ought to be suppressed in IP2 and IP1 current when MN2 transistor is tried to pull down the output node OUT to zero voltage, in light of this reason structure is shown in fig(3.2) is utilized. Circuit's operation, shown in Figure(3.1), can be interpreted as follows. MN1 transistor turned on when a transition occurs in input node "Low-level voltage" to "high-level voltage," and in the meantime, MN4 transistor turned off. MN4 transistor turned on during this change period where OUT corresponds to input level since the overdrive voltage of the MP3 transistorV_{ddh}) greater than that of transistor MN3V_{ddl}. Along these lines, transition current begins to stream through MN4 transistor, MN1 transistor, and transistor MP1 (IP1). Presently, this current is replicated into MP2 transistor (IP2), and output node pulled up. MP3 transistor turned off, a point when output node OUT is pulled up, and in the meantime gate of MN4 transistor is pulled down through MN3 transistor which implies that there is no static current streaming through MN4 transistor, MN1, and MP1 transistor. In the event that we need to have low power utilization, at that point aspect ratio of MP1 transistor ought to be shorter than MP2 transistor. Output node OUT will be pulled down for high level-to-low level shift of input, since MN2 transistor turned on. At this point of time, MN1 transistor turns off which implies that, as opposed to the past configuration shown in figure(2.3), there is no transition current streaming through MP1 transistor (IP1 = 0) which diminishes the strength of MP2 transistor when output node OUT is pulled down by MN2. Node QA is charged to V_{ddh} - Vth, where Vth is on a voltage of MP1 transistor. One end can be drawn here that the current of MP2 transistor (IP2) isn't entirely zero and in-reality there still exists a small dispute. MP4 transistor is utilized for the decline of IP2 shows in figure(3.1). At the point when MN2 is trying pulling down the output node OUT, the gate of MP4 transistor is in "High state" with V_{ddl} and due to which drain to source voltage of MP2 transistor declines. Also, delay and power utilization of circuit reduce.

Pull up device current degrades(IP2) when a gate of MN2 transistor and MP4 transistor are provided by a voltage greater than V_{ddl}, in the meantime strength of pull-down device (MN2 transistor) increases. Subsequently, conflict and thus propagation delay and power declines. Additionally, the level converter can work in sub-threshold input voltages.

On the off chance that we need to apply the principle which discussed earlier, at that point one auxiliary circuit (MP5, MP6, MP7, MN5, MN6, and MN7 transistor) is utilized shows in figure(3.2). During the high-to-low change of input voltage, this additional circuit turned on, which charge the node QC up to a value greater than V_{ddl}.

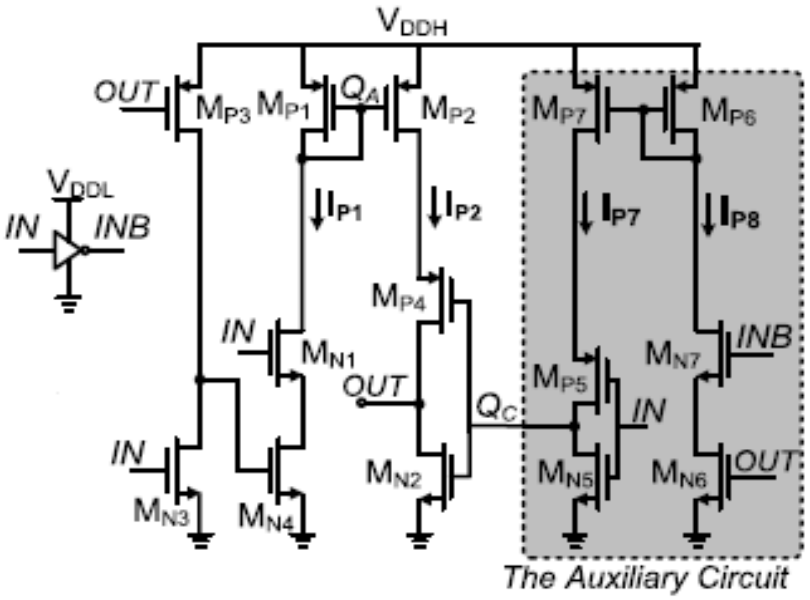

FIGURE 3.2: Level Up Shifter With Auxilliary Circuit [1]

An explanation for activity of this auxiliary portion of a circuit shown in figure 3.2. Output node OUT does not match to input logic level voltage when input switched from "high state" to "Low state," as of now MN6, MN7 and MP6 transistor turned on, and MN5 turned off.

In this manner, a transition current stream through MP6, MN7, MN6 transistor, and this current is reflected in transistor MP7 (IP7) and like this, it pulls up node QC. And consequently, MP4 turned off, and MN2 turned on with voltage larger than that of V_{ddl}, this implies a reduction in contention issue. MN6 turned off at the point when output node pulled down, and around at this instant of time there is no current passing through MP6, MN7, MN6, this implies in the span of high state-to-low state voltage transition of input voltage auxiliary circuit turned into on state.

One conclusion is drawn that there is no need of charge the node QC up to V_{ddh} specifically, with the goal that the plan of the modified circuit should be reasonable so that current streaming through MP7 transistor (IP7) is small.

So dispute that was existing in this branch will likewise be invalidated, this reduces the power leakage and furthermore delay of this auxiliary circuit. Thusly, the profitability of modified circuit is a direct result of the reason that strength of pull up device decreased at whatever point output node is pulled down by pull-down device, and at this instant of time an modified circuit with the help of that low power is attained, strength of the pulldown device is extended.

3.2 Power efficient Multilevel Voltage Level Shifter

Type of level shifter shown in fig(3.3) is used to perform both types of conversion, i.e., low to high and high to low level voltage as per requirement. In this circuit design, two kinds of voltage source are utilized, i.e., V_{ddl} and V_{ddl}. Based on the voltage applied at the input node, either of the voltage is chosen.V_{ddh} and V_{ddl} is selected for up and down respectively with the help of input voltage, ie, VIN, So the output will appear as V_{ddh} or V_{ddl} or 0Volt.

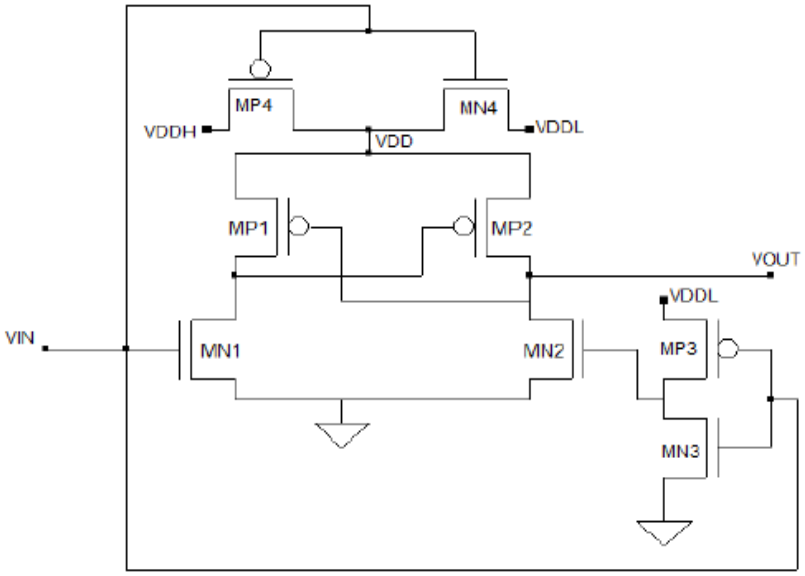

FIGURE 3.3: Power efficient Multilevel Voltage Level Shifter [2]

The circuit displayed in figure(3.3) comprises of two sections and they are as per the following:

1)The transistor organizes MN4, and MP4 acts like a 2X1 multiplexer and V_{ddh} and V_{ddl} is chosen depending on input voltage which is given in node VIN where input node hence VIN is for a chosen signal.

2)The remaining section of the circuit performs level shifting.

MP4 turned ON whenever is 1.2 volts applied to the node VIN, and at the meantime, MN4 turned OFF. So V_{ddh} appear at V_{dd}, at meantime MN1 turned ON, MN2 turned OFF, MP1 turned OFF, and furthermore, MP2 turned ON, and in this way, V_{ddh} will be showed up at Vout terminal.

Therefore output node VOUT is charged to V_{ddh} (5 Volts). A conclusion can be made that whenever 1.2 volts is applied to the input node, hence output node VOUT set to 5

volts. Consequently, level-up shifting is being done. MP4 turned OFF whenever 5 Volt is given at input node VIN, and at the point of time MN4 turned ON. In this case, V_{ddl} appeared at V_{dd}, at this instant MN1 turned ON, MN2 turned OFF, MP1 turned OFF, and MP2 becomes turned ON, and therefore V_{ddl} (1.2 volts) appear at output node VOUT. Since output node sets to 1.2 Volt by applying of 5volts as input node, it indicates level downshifting is being done.

Chapter 4

Comparison and Simulation Results

The level shifter circuits with an auxiliary circuit which shown in figure(3.2) is used for level upconversion and the simulation result for this is discussed in section(4.1) and Multilevel shifter which is used in both type of conversion up and down shown in fig(3.3) and simulation result for this is discussed in section(4.2).

4.1 Level Up Shifter

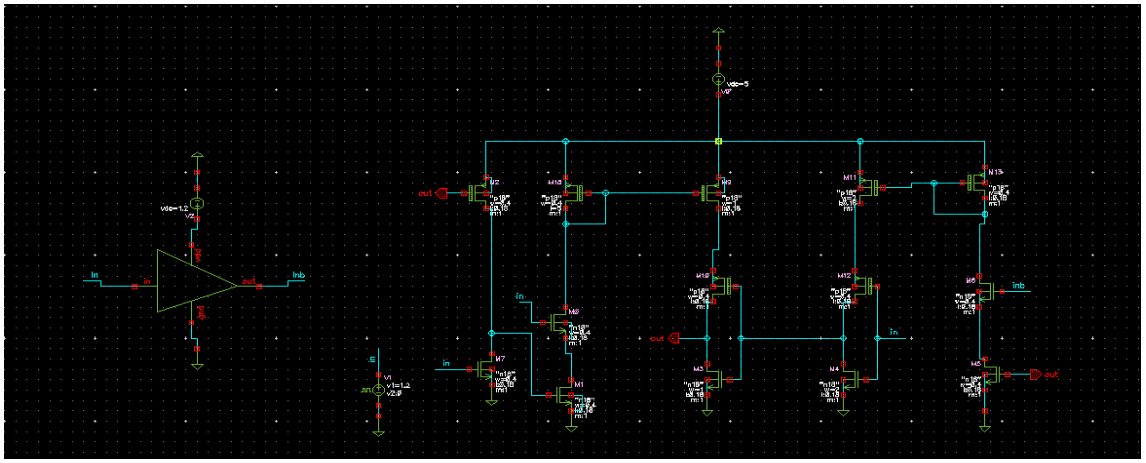

FIGURE 4.1: Schematic design of the level shifter shown in fig(3.2)

The schematic design of this circuit is designed by the use of CADENCE VIRTUOSO, which is shown in figure(4.1). In this circuit, the low voltage value of 1.2v is converted into the high voltage value of 5v shown in figure(4.2).

4.1.1 Simulation Results

4.1.1.1 Voltage Upconversion

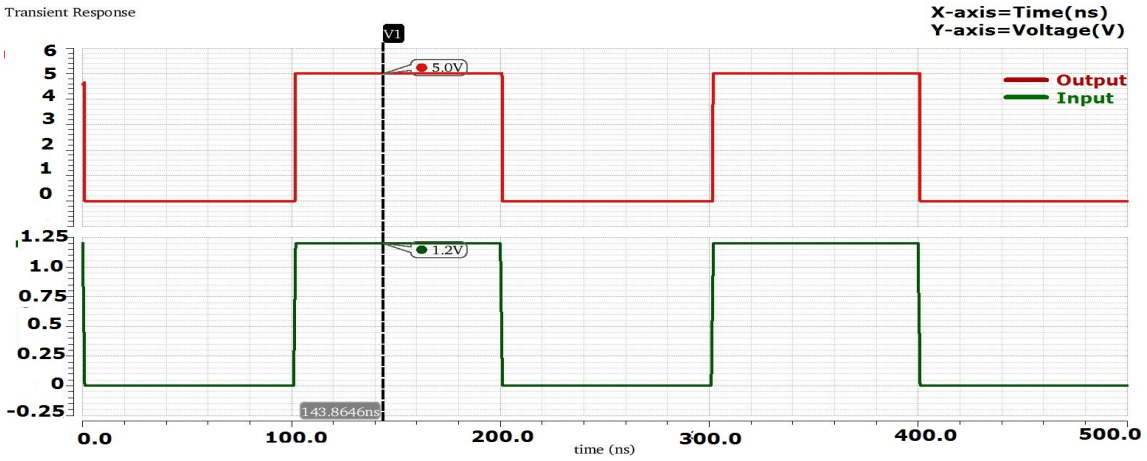

FIGURE 4.2: Simulation result for level-up shifter with V_{ddl} =1.2V, V_{ddh}= 5V.

4.1.1.2 Static Current dissipation

The static current I_{vddl} streaming from low voltage(V_{ddl}) is shown in figure (4.3), and that is I_{vddh} stream through high voltage (V_{ddh}) is shown in figure(4.4).

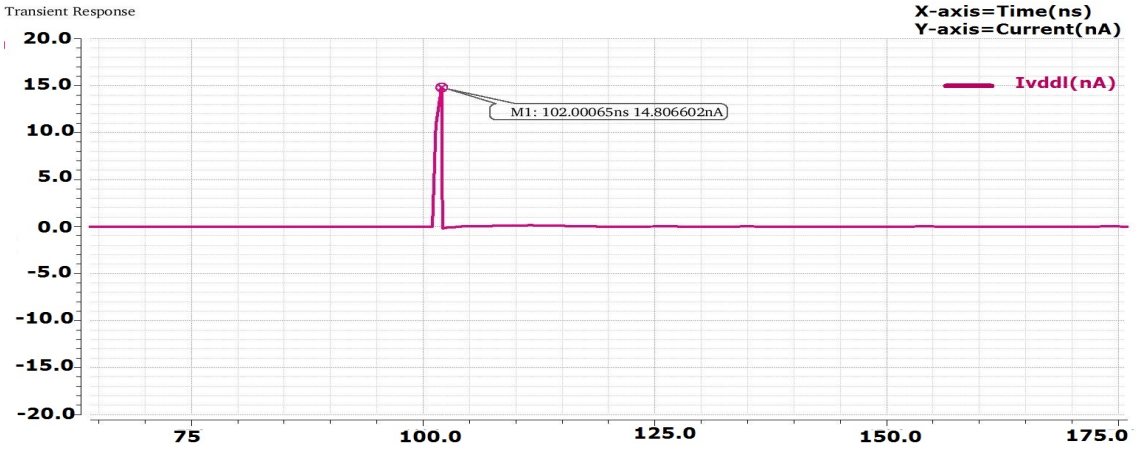

FIGURE 4.3: Static Current I_{vddl} for V_{ddl}=1.2volt.

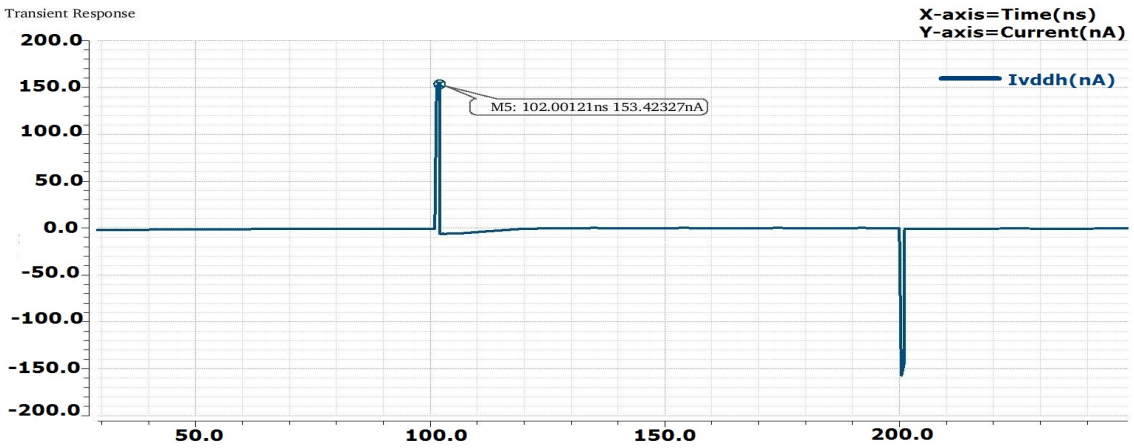

FIGURE 4.4: Static Current I_{vddh} for V_{ddh}=5volt.

4.1.2 Delay and Static Power Dissipation for Level Up Converter

For the power calculation, the static power is calculated by the equation(1.1). The current flow from the supply voltage to ground and supply voltage are used for calculating the static power dissipation.

Circuit	**Frequency (MHz)**	**Delay Rise (ps)**	**Delay Fall (ps)**	**I_Vddh (nA)**	**I_Vddl (nA)**	**Vddh (V)**	**Vddl (V)**	**Static-Power (uW)**
1	5	42.091	91.06	153.432	14.806	5	1.2	0.8
2	5	47.089	121.31	180.662	17.45	5	1.5	0.93

TABLE 4.1: Simulation Results of Level up Shifter

4.1.3 Comparison of Results

Circuit	**Shift Types**	**Delay**	**Static power**
[4]	Up	0.1ns	1.7154mW
[1]	Up	301.93ps	7.34uW
Modified Level Shifter with Auxiliary Circuit	Up	348.21ps	0.8uW

TABLE 4.2: Performance Analysis

From the static power analysis for novel level shifter, which is shown in table 4.1 is shows that the level shifter with an modified auxiliary circuit is utilized less leakage power than level shifter with Wilson current mirror. Comparison between different types of Wilson

level shifter and modified auxiliary level shifter shows in table 4.2, which shows an 88.63% reduction in power dissipation.

4.2 Multilevel Shifter

The level shifter circuit which is used for both type of conversion, i.e., up and down shown in figure (3.3). The function of this circuitry is divided into two part. (1) upconversion for this we used high voltage supply (V_{ddh}) value of 5v and low supply voltage (V_{ddl}) value of 1.2v and input is in pulse form value of 1.2v for the frequency of 5 MHz is used for level upconversion. (2) Downconversion in this input value of 5v in pulse form is used to convert the high voltage value (V_{ddh}) to the low voltage value (V_{ddl}) of 2v and 1.2v. The schematic design of this circuit is designed by the use of CADENCE VIRTUOSO, which is shown in figure(4.5). Input-output waveform for the upconversion shown in figure (4.6) and that is for down conversion shown in figure(4.9) and (4.10).

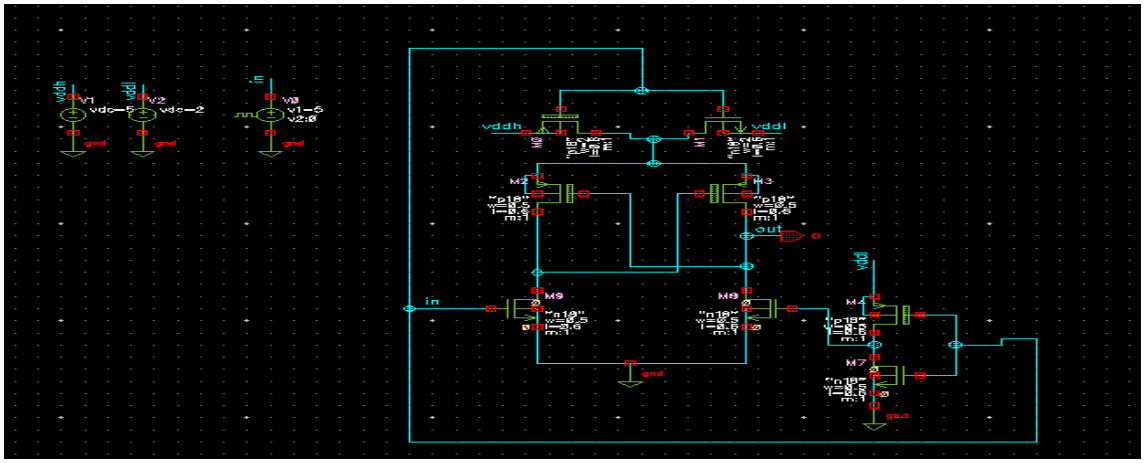

FIGURE 4.5: Schematic design of the multilevel shifter shown in fig(3.3)

4.2.1 Simulation Results for Upconversion

In the multilevel converter for the upconversion, two types of power supply used, i.e., a low power supply value of 2v and high supply value of 5v and input signal in pulse form value of 1.2v with 100ns pulse width is used. The architecture is simulated in the ADEL utilizing the scl_180nm technology model file. For the upconversion used a wide range of input signal and concluded that when the input signal increases the delay of the signal is also increased.

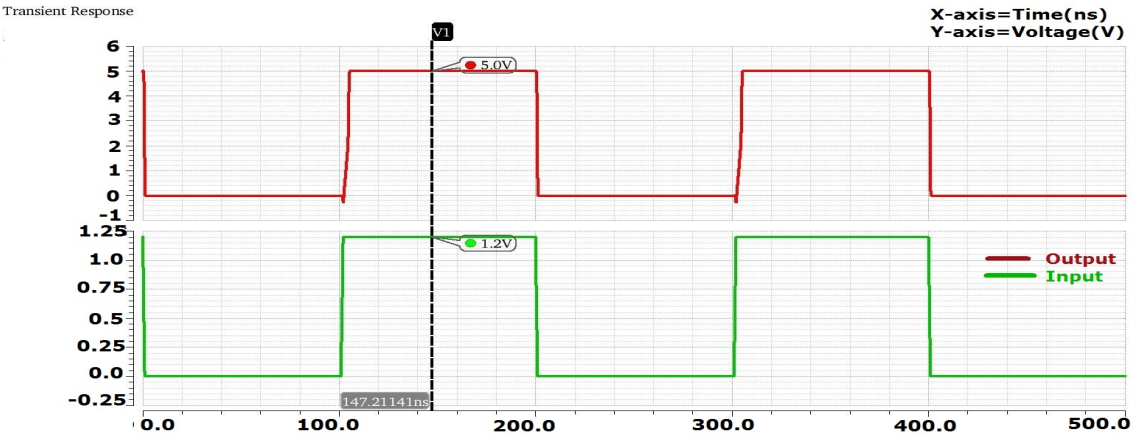

FIGURE 4.6: Simulation result for level-up shifter with V_{ddl} = 1.2V, V_{ddh} = 5V. and V_{in}= 1.2v

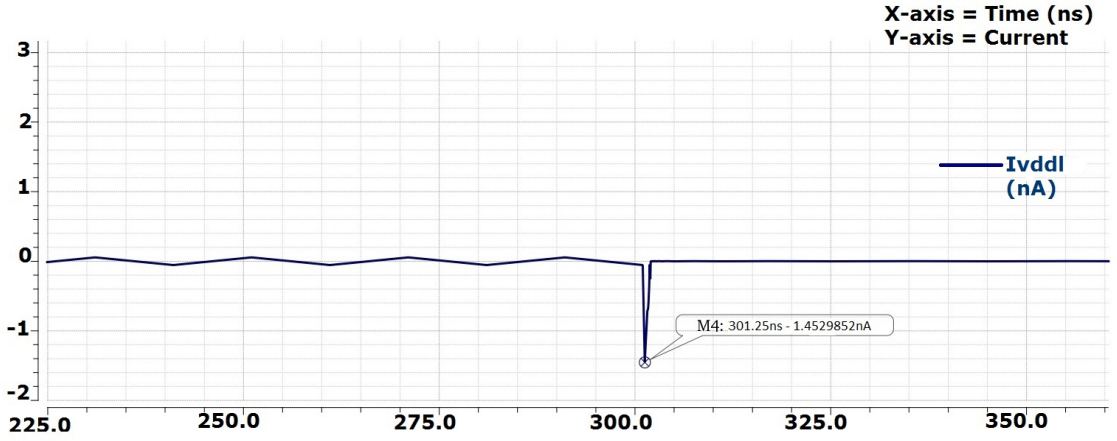

FIGURE 4.7: Static Current I_{vddl} for V_{ddl}=1.2volt.

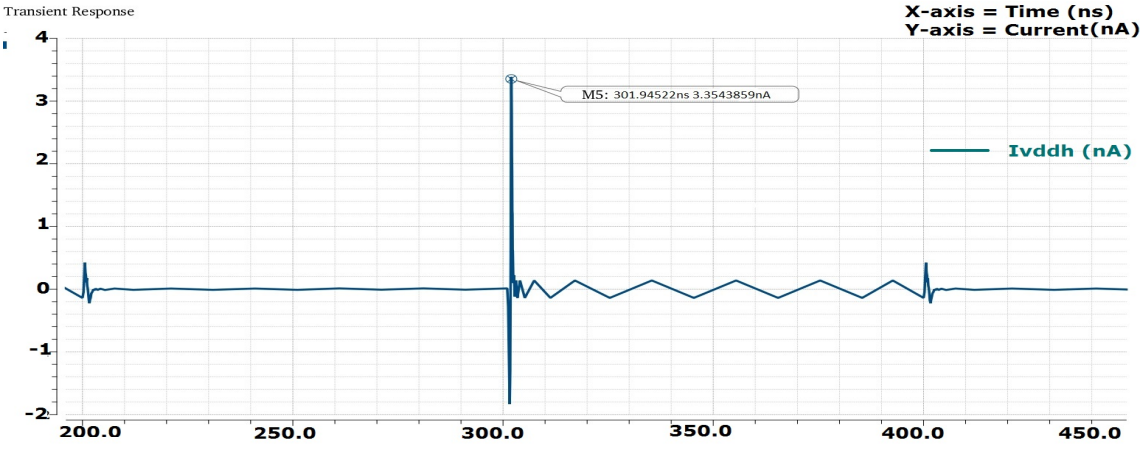

FIGURE 4.8: Static Current I_{vddh} for V_{ddh}=5volt.

4.2.2 Simulation Results for Downconversion

In the multilevel converter for the downconversion, two types of power supply used, i.e., a low power supply value of 2v and 1.2, high supply value of 5v and input signal in pulse form value of 5v with 100ns pulse width is used. In this arrangement high voltage signal is shifted into low voltage value of 2v and 1.2v. Hence in this arrangement, a broad range of input signal is converted into high value and low value.

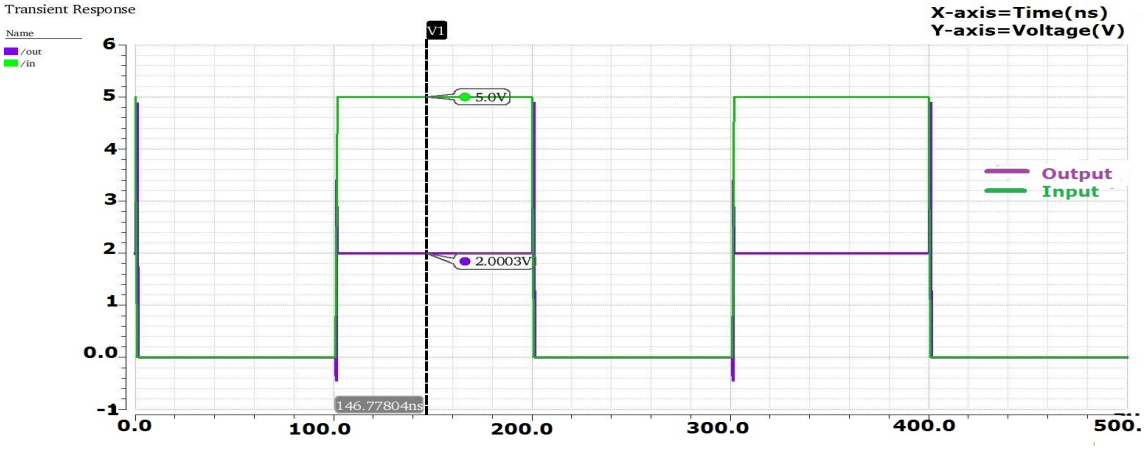

FIGURE 4.9: Simulation result for level-down shifter with V_{ddl}=2v,V_{ddh}=5v and V_{in}=5v

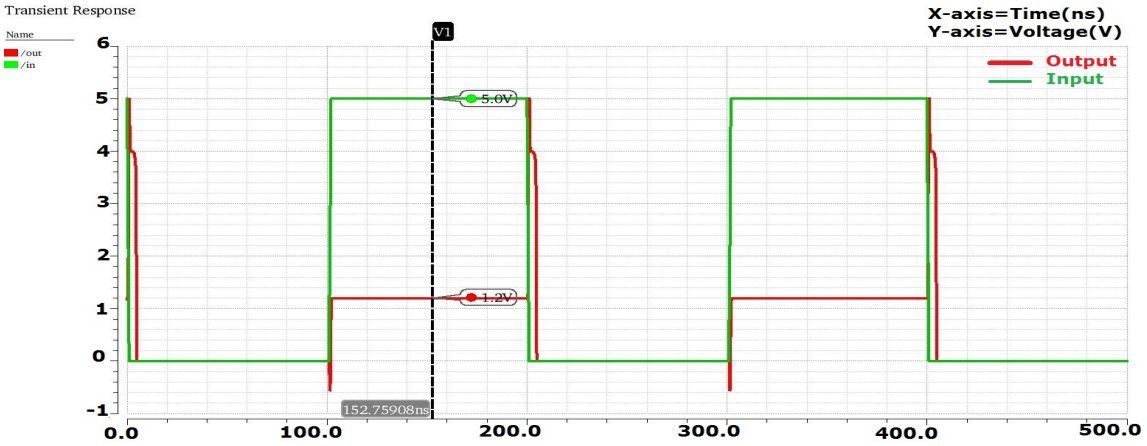

FIGURE 4.10: Simulation result for level-down shifter with V_{ddl}=1.2V, V_{ddh}=5V and V_{in}=5v

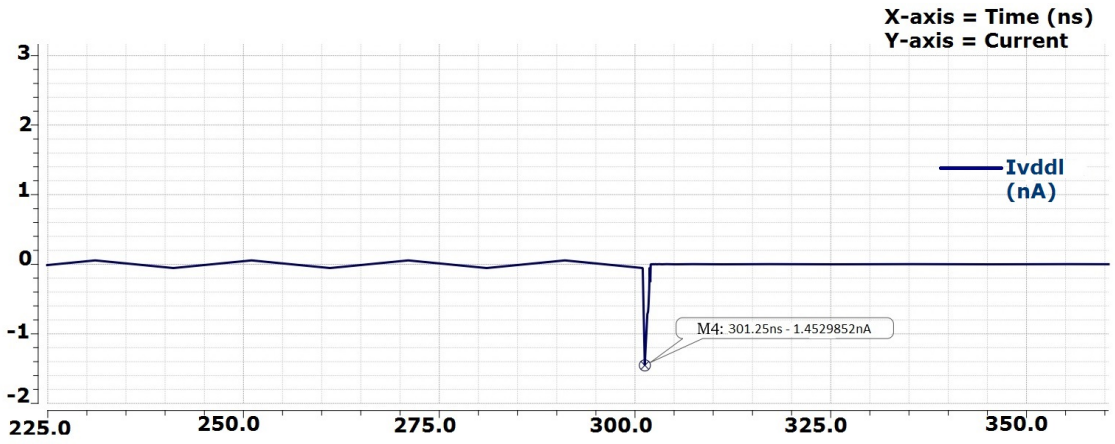

FIGURE 4.11: Static Current I_{vddl} for V_{ddl}=1.2volt and V_{ddh}=5v

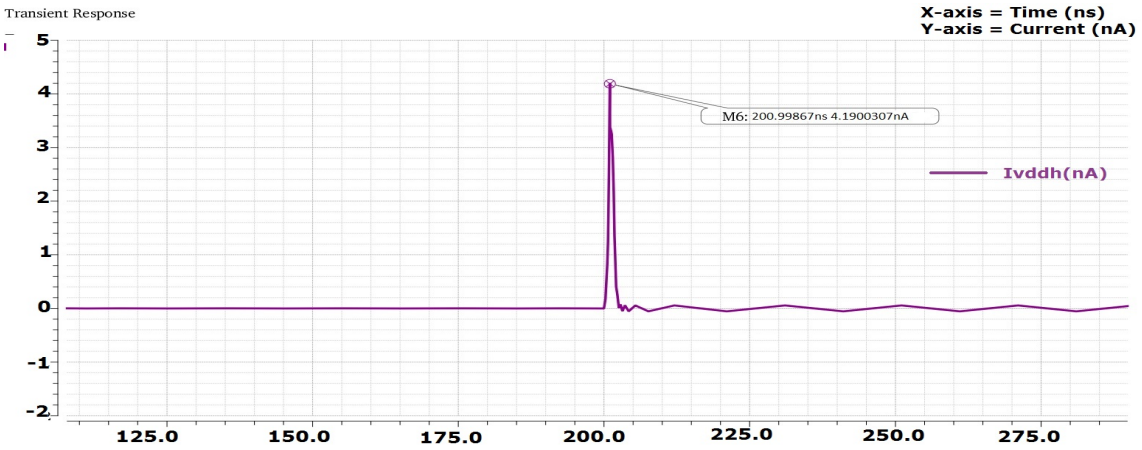

FIGURE 4.12: Static Current I_{vddh} for V_{ddl}=1.2volt and V_{ddh}=5v

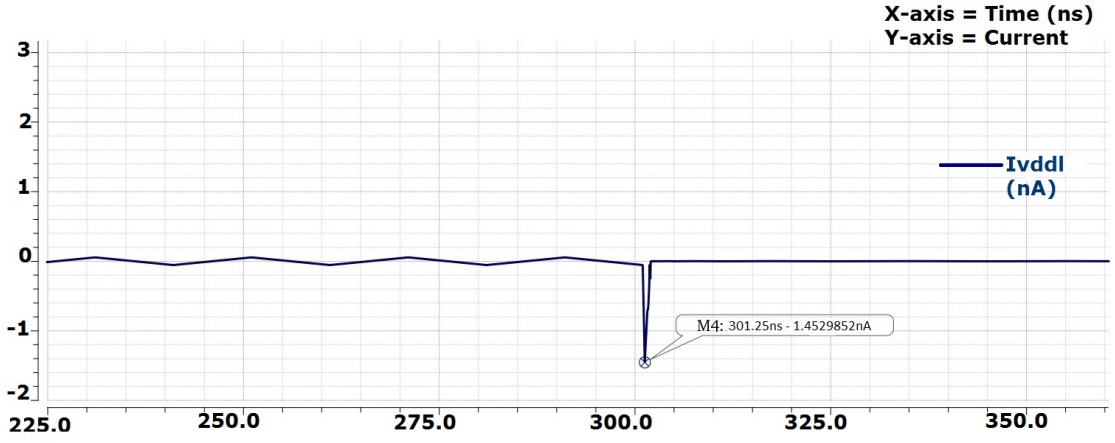

FIGURE 4.13: Static Current I_{vddl} for $V_{ddl} = 2volt$ and V_{ddh}=5v

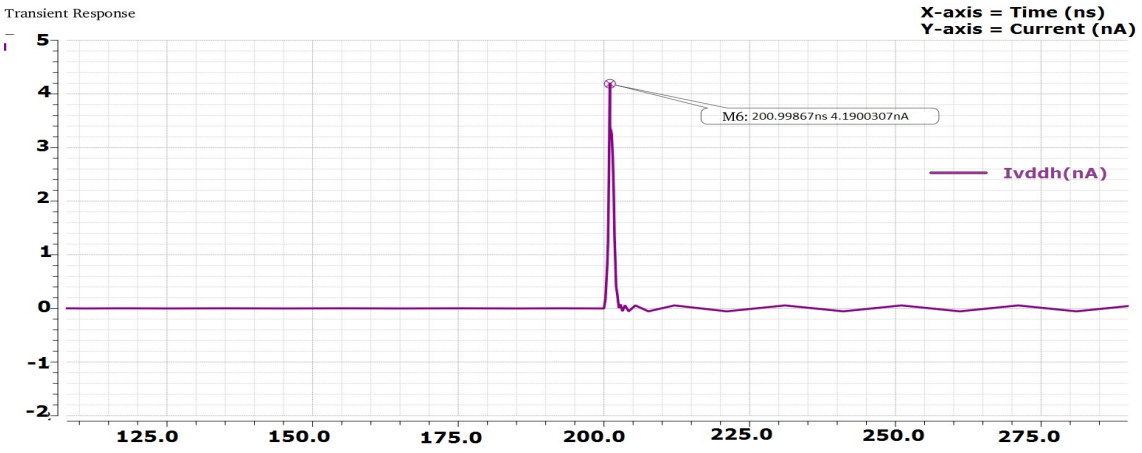

FIGURE 4.14: Static Current I_{vddh} for V_{ddl}=2volt and V_{ddh}=5v

4.2.3 Delay and Static Power Dissipation for Level Down Converter

For the power calculation, the static power is calculated by the equation(1.1). The current flow from the supply voltage to ground and supply voltage are used for calculating the static power leakage. From table 4.3 shows that if the input range is increased power leakage, and delay is also raised in both cases, i.e., upconversion and down conversion.

Mode	**Freq (MHz)**	**Delay Rise (ps)**	**Delay Fall (ps)**	**I_Vddh (nA)**	**I_Vddl (nA)**	**Vddh (V)**	**Vddl (V)**	**Static-Power (nW)**
Up	5	618.845	900.21	3.354	1.451	5	1.2	18.512
Down	5	642.21	981.24	4.191	1.642	5	1.2	22.925
	5	683.667	1013.91	4.562	2.462	5	2	27.734

TABLE 4.3: Simulation Results of multilevel shifter

4.3 Comparison of Results

Work/Reference	**Shift Types**	**Technology**	**Power**	**Delay**
Level Up and Down Shifter	Up and Down	180nm	Ps = 20.828nW	961.31ps
[1]	Up	180nm	Ps = 0.3nW	30ns
[6]	Up	180nm	Ps = 61.5nW	29ns
[8]	Up	180nm	Ps = 58nW	1000ns
[2]	Up and Down	90nm	Pa = 24.71nW	2.05ns

TABLE 4.4: Performance Analysis

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The efficiency of the level up shifter designed in thesis is due to two reasons; one is that the current of the pullup device is degraded when the pulldown device pulled down the output node, and the 2nd reason is that strength of the pulldown device is improved. The level shifter with modified auxiliary circuit is faster for switching low voltage input to high voltage output and also high input voltage to low output voltage at the same time, the effect of variation of temperature. Hence power is reduced to 88.63%, and delay is reduced to 35% in the level shifter as compared to Wilson current level shifter and delay. The static power consumption for the level up shifter with the auxiliary circuit is 0.83uW.

In this work, designed a dual level converter for a multi-supply system. The multilevel converter gives the level up/down conversions for the many input and output voltage levels. It has the benefit of diminishing the complexity during physical design. Also, the multilevel converter has the benefits of low-power and fast operating speed. Results of the simulation indicate that the multilevel converter upgrades the input voltage from 1.2V to 5V and also downgrades the input voltage from 5V to 2V. The average static power leakage for the shifter 20.83nW. Hence power is reduced to 16%, and delay is reduced to 45% than the existing circuits.

5.2 Future Work

The level shifters are employed in pre-decoder in-between the high voltage level memory circuits and the digital gates which operate at operating at V_{ddl} level, they act as address buffers for interfacing purpose. A lot of architectures have been suggested over time for the fast and efficient voltage level shifting.

In this dissertation, we have also tried to open up some new techniques for the arrangement of voltage level shifter, which can upconvert the low input voltage and also downconvert the high input voltage. This work can further help the researchers and engineers working in this field to think in a new dimension to design the level shifter, and it can be modified to reduce the power and delay.

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