A Simulation Based Study of Gate Underlap Double Gate Junctionless MOSFET as a Bio-Sensor

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology
in
Electronics and communication

Under the guidance of

Dr. TARUN VARMA

By:

ARVIND DAUTANIYA 2017PEC5430



Department of Electronics and Communication Engineering

Malaviya National Institute of Technology

Jaipur, Rajasthan India 2019



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR - 302017 , RAJASTHAN, INDIA

CERTIFICATE

This is to certify that the Dissertation Report entitled "A Simulation Based Study of Gate Underlap Double Gate Junctionless MOSFET as a Bio-Sensor" by ARVIND DAUTANIYA is the work completed under my supervision and guidance, hence approved for submission in partial fulfillment for the award of degree of Master of Technology in EC to the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur in the academic session 2018-2019 for full time post-graduation program of 2017-2019.

Jate:	Dr. Tarun varma
Place:	Associate Professor
	(Project Supervisor



Department of Electronics and Communication Engineering Malaviya National Institute of Technology, Jaipur

DECLARATION

•	•	•	i		
	4	\sim	ara	that.	
	u	こしょ	aic	mat.	

The work contained in this dissertation is original and has been done by me under the guidance of my supervisor.

The work has not been submitted to any other institute for any degree or diploma.

I have followed the guidelines provided by the institute in preparing the dissertation.

I have conformed to the norms and guidelines given in the Ethical code of conduct of the institute.

Date:- ARVIND DAUTANIYA (2017PEC5430)

ACKNOWLEDGEMENT

I take this opportunity to express my deep sense of gratitude and respect towards my supervisor of the Dissertation, **Dr. Tarun varma**, Associate Professor, Department of Electronics & Communication Engineering, Malaviya National Institute of Technology. I am very much indebted to him for the generosity, expertise and guidance I have received from him while working on this project and throughout my studies. Without his support and timely guidance, the completion of my project would have seemed a far–fetched dream. In this respect, I find myself lucky to have him as my Project guide. he has guided me not only with the subject matter, but also taught me the proper style and techniques of working.

I would also like to thank **Prof. D.Boolchandani**, Professor of Electronics & Communication Engineering Department for his co-operation and help rendered in numerous ways for the successful completion of this work.

ARVIND DAUTANIYA

(2017PEC5430)

Thesis Objectives

The main objectives of this thesis are to understand the structure design of DG MOSFETs along with its application as a bio molecule sensor. The analysis has been carried out with the help of simulation results by a available two dimensional (2D) ATLAS device simulators.

Motivation

As conventional single gate MOSFETs are unable to perform well in less channel dimensions, because of short channel effects, high leakage currents and less control over threshold voltages, double gate MOSFETs gives the promise to the industry to take away the burden somehow. underlap structure of DGMOSFET makes it suitable for biosensor also its sensitivity is high as compare to other structure.

TABLE OF CONTENTS

ACKNOWLEDGEMENT(iv)
INDEX OF FIGURE(ix)
INDEX OF TABLES(x)
ACRONYMS(xi)
ABSTRACT(xiii)
1. INTRODUCTION(1 - 9)
1.1 MOSFET and its scaling: A Historical Perspective
1.2 Overview of MOSFETs
1.3 MOSFET operation
1.4 MOSFET scaling
1.5 Reasons for MOSFET scaling
1.6 Scaling problems4
1.6.1 Higher subthreshold conduction
1.6.2 Modelling challenges
1.6.3 Lower transconductance
1.6.4 Interconnect capacitance
1.6.5 Heat production5
1.7 Technology Boosters: Solution to Scaling5
1.7.1 Gate Engineering Technique6
1.8 Gate engineered DG MOSFETs
1.9 Advantages of DG MOSFETs8
1.10 Challenges of DG MOSFETs8
1.11 Gate misalignment of DG MOSFETs9
2. SIMULATION METHODOLOGY(10-19
2.1 Introduction

2.2 I	Deckbuild	10
2.3 E	Building the device	12
2.4 T	Cony plot	17
3. DEVI	CE STRUCTURE & SIMULATION	(20-27)
3.1 I	ntroduction	20
3.2 I	Device operation	20
3.3 7	Types of Biosensor	22
	3.3.1 Optical Transducer	22
	3.3.2 Electrochemical Transducers	23
	3.3.3 FET – Based Electronic Transducer	23
3.4 I	SFET VERSUS FET AS A BIO SENSOR	24
3.5 7	TYPES OF BIOMOLECULE	25
3.6 E	Biosensor Performance Charactericstics	26
	3.6.1 Specificity and Sensitivity	26
	3.6.2 Limit of Detection.	26
	3.6.3 Robustness and Repeatability	27
4. RESU	JLTS & DISCUSSIONS	(28-35)
4.1	Introduction	28
4.2	Simulated Structure of Device	28
	4.2.1 Input characteristics of device	29
4.3	Detection of Neutral Biomolecule	29
4.4	Detection of Charged Biomolecule	31
4.5	Calculation of Sensitivity Variation	34
5. CON	CLUSION	(36)
5.1 1	Performance Analysis	36
525	Scope of Future Work	36

INDEX OF FIGURES

Figure 1.1 First IC fabricated by Jay Last's development group Fairchild Corp.	(1)
Figure 1.2 Cross sectional view of conventional bulk MOSFET.	(2)
Figure 1.3 Metal-oxide-semiconductor structures on p-type silicon.	(3)
Figure 1.4 The dual metal gate structure.	(6)
Figure 1.5 Progress of the MOSFET Technology through multiple-gates.	(6)
Figure 2.1 Screenshot of Deckbuild.	(11)
Figure 2.2 Atlas statement hierarchy.	(11)
Figure 2.3 Mesh examples.	(12)
Figure 2.4Tony plot screen shot showing the lay out of the x and y -coordinates	nate system in(14)
Figure 2.5 Screenshot of an <i>x-y</i> plot in Tonyplot.	(17)
Figure 2.6 Screenshot showing the mesh plot display buttons for Tonyplot.	(18)
Figure 2.7 Description of the display buttons in Tony plot.	(18)
Figure 2.8 Tony plot screenshot showing several files opened in the same with movie tool selected.	indow with the(19)
Figure 3.1 The simulated device structure.	(21)
Figure 3.2 MOSFET vs. ISFET	(24)
Figure 3.3 Negavtive charge biomolecule	(26)
Figure 4.1 Simulated Structure of DG JL MOSFET.	(28)
Figure 4.2 Input Characteristics of DG-JL-MOSFET	(29)
Figure 4.3 Variation OF Logid Versus vgs to Detect Different K Values.	(30)
Figure 4.4 Threshold Voltage VS Dielectric Constant.	(30)
Figure 4.5 Logid VS Gate Voltage Variation due to change in charge on biomo	lecule(32)
Figure 4.6 Threshold voltage vs charge biomolecule.	(32)
Figure 4.7 Sensitivity Versus Change in Dielectric constant (k).	(34)
Figure 4.8 Sensitivity Versus Charge COncentration (Q x10 ¹⁵ m ⁻²).	(35)

INDEX OF TABLES

Table 4.1 - show the change in threshold voltage	e and as well as change in subthreshold swing
for neutral biomolecule.	(31)
Table 4.2 - show the change in threshold voltag	e and as well as change in subthreshold swing
for charged biomolecule.	(33)

ACRONYMS

CGAA: Cylindrical Gate-All-Around

CLM: Channel Length Modulation

CMOS: Complementary Metal Oxide Semiconductor

DG: Double Gate

DIBL: Drain Induced Barrier Lowering

DMDG: Dual Material Double Gate

FDSOI: Fully Depleted Silicon On Insulator

GAA: Gate All Around

HCE: Hot Carrier Effect

IC: Integrated Circuit

ITRS: International Technology Roadmap for Semiconductor

LAC: Lateral Asymmetric Channel

MISFET: Metal Insulator Semiconductor Field Effect Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

RF: Radio Frequency

SCE: Short Channel Effect

SMDG: Single Material Double Gate

SEMOI: Semiconductor On Insulator

SOI: Silicon-on-Insulator

ISFET: Ion Sensitive Field-Effect Transistor

TMDG: Triple Material Double Gate

TTL: Transistor Transistor Logic

UTC: Ultra Thin Channel

VLSI: Very Large Scale Integration

ABSTRACT

Currently, the expansion of VLSI industry is primarily focussed on the way to the efficiency of semiconductor devices which in turn is extremely dependent on the advancement in the CMOS technology. As the scaling down of device dimensions are being aggressive, carrier mobility reduced due to dopant fluctuation, gate tunnelling effect increases and p-n junction leakage current increases. More precise and novel device structures are required to be developed for satisfying the above requirements. These needs have led to development of alternative technology.

The double-gate (DG MOSFETs) are the front runner among the sub-100 nm devices because, both front and back gate of DG MOSFETs control the channel region simultaneously and these are also well suited for ultra-low-voltage operation due to the inherent suppression of short channel effects (SCEs), reduced drain-induced barrier lowering (DIBL), excellent scalability and un-doped body doping. However, alignment between the front and back gate is an issue of concern during fabrication because its influences are baleful for device performance. The underlap structure of double gate makes its suitable to detect biomolecule. The underlap is used to sense threshold voltage, Ion current etc

1.1 MOSFET: A Historical Perspective

Over the past thirty years, the growth of microelectronics, automation, information sharing, signal processing has strongly dependent on very large scale integrated circuit (VLSI) industry. Advancement of computer and fascinating gadgets with every possible applications; be it audio, video, any type of game or high speed communication; revolutionized the world of interconnectivity and entertainment. It's all credited to the high speed ultrasmall sized, low power semiconductor devices, sensors, all new materials and their implementation through VLSI design.[1]

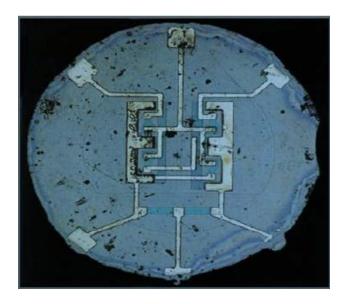


Figure 1.1: First IC fabricated by Jay Last's development group Fairchild Corp.[2]

1.2 Overview of MOSFETs

The metal oxide semiconductor field effect transistor (MOSFET), the heart of integrated circuits is generally used for the purpose of switching and amplifying electronic signals.

Though the MOSFET is recognized as four-terminal device with source (S), drain (D),

gate(G), and body (B) terminals,[3] the body (or substrate) of the MOSFET frequently attached to the source terminal, making it a three-terminal device. Because these two terminals are normally coupled to each other inside, only three terminals appear in electrical diagrams. Till now, MOSFET is the most universal transistor in both analog and digital circuits, even if the bipolar junction transistor was at one time much more recognizable.

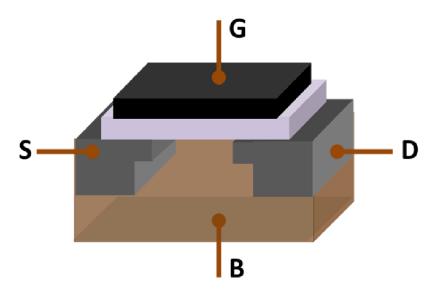


Figure 1.2: Cross sectional view of conventional bulk MOSFET.[4]

In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts due to the field effect. The name enhancement mode refers to enhance of conductivity with increase in oxide field that attract carriers to the channel, also known as the inversion layer. The channel can include electrons (for n-type MOSFET), or holes (for p-type MOSFET), reverse in nature to the substrate, so n-type MOSFET is prepared with a p-type substrate, and p-type MOSFET with an n-type substrate. In the rare used depletion mode MOSFET, the channel contains of carriers in a surface layer of reverse type to the substrate, and conductivity is degrades by application of a field that removes carriers from this surface layer. [5]

1.3 MOSFET operation

The conventional metal oxide semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO₂) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon. As the silicon dioxide is a dielectric substance, its structure is alike to a planar capacitor. When a voltage is applied to a MOS structure, it modifies the

sharing of charges in the semiconductor. Usually, the gate voltage at which the concentrations of electrons in the inversion layer are the same as the concentrations of holes in the body is called the threshold voltage. When the gate to source exceeds the threshold voltage, it is known as overdrive voltage.

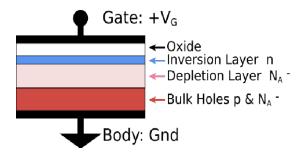


Figure 1.3: Metal-oxide-semiconductor structures on p-type silicon.[4]

1.4 MOSFET scaling

Over the past thirty years, the MOSFET has constantly been scaled down in dimension; typical MOSFET channel lengths were once quite a few micrometres, but recent integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometres. Intel began manufacture of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009. The semiconductor industry maintains a "roadmap", the ITRS,[6] which sets the pace for MOSFET growth. Historically, the difficulties with decreasing the size of the MOSFET have been connected with the semiconductor device fabrication process, the need to use very low voltages, and with inferior electrical performance necessitating circuit reshape and innovation.

1.5 Reasons for MOSFET scaling

Smaller MOSFETs are attractive for a number of reasons. The main reason to build transistors smaller is to group more and more devices in a given chip area. This results in a chip with the same functionality in a lesser area, or chips with more functionality in the identical area. As fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mostly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, decreasing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65nm chip. This doubling of transistor density was first experimented by Gordon Moore in 1965 and is commonly referred to as Moore's law.[7]

1.6 Scaling problem

1.6.1 Higher subthreshold conduction

As MOSFET geometries minimize, the voltage that can be applied to the gate must be reduced to preserve reliability. To preserve performance, the threshold voltage of the MOSFET has to be decreased as well. As threshold voltage is reduced, the transistor cannot be turn-on from complete turn-off with the less voltage swing available; the circuit design is conciliation between strong current in the 'on' case and less current in the off case and the application find out whether to favour one over the other. Subthreshold leakage (including subthreshold current conduction, gate-oxide leakage current and reverse biased junction leakage), which was mistreated in the past, now can consume upwards of half of the total power consumption of recent high-performance VLSI chips.[8] [9] [10]

1.6.2 Modelling challenges

Modern ICs are computer-simulated with the aim of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the difficulty of the processing makes it hard to predict exactly what the ultimate devices look like, and modelling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult.

To minimize the difficulties of small size bulk MOSFETs, Researchers and engineers discover several alternative device structures, by which the technology can further scaled down with a improved performance. These are, double gate (DG) MOSFETs, Strained MOSFETs, gate all around (GAA) MOSFETs etc. Double gate MOSFET is one of the improved device structure for reducing short channel effects.

1.6.3 Lower transconductance

The transconductance of the MOSFET decides its gain and is directly proportional to hole or electron mobility depending on device type, for low drain voltages. As MOSFET dimension is decreased, the fields in the channel improve and the dopant impurity levels increases. Both changes decrease the carrier mobility, and thus the transconductance.

1.6.4 Interconnect capacitance

Conventionally, switching time was roughly proportional to the gate capacitance of MOSFETs. On the other hand, with transistors becoming smaller and number of transistors being located on the chip, interconnect capacitance (the capacitance of the metal-layer connections between different parts of the chip) is becoming a great percentage of

capacitance. Signals have to pass through the interconnection, which leads to amplified delay

and degrade performances.

1.6.5 Heat production

The increasing density of MOSFETs on an integrated circuit makes difficulties of substantial

localized heat generation that can hurt circuit operation. Circuits work more slowly at high

temperatures, and have decreased constancy and shorter lifetimes. Cooling devices and

methods and heat sinks are now necessary for many integrated circuits including

microprocessors.

1.7 Technology Boosters: Solution to Scaling

1.7.1 Gate Engineering Techniques

High-k dielectric

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45 nm

CMOS technology generation. This is the first time that traditional oxides or oxy nitrides have

been replaced in gate stacks.

Multi-Material Gate:

One of the prominent means to get rid of hot carrier effect (HCE) is using cascaded gate

structure consisting of two or more metals of different work functions. This structure is

commonly known as Double-Material-Gate (DMG) structure as proposed in 1999

Triple-Material-Gate (TMG) in 2008 proposed. The metal gates are so cascaded that the gate

near the drain is a metal (M2) with lower work-function and the source side metal (M1) is of

relatively higher work function. As a result of this, the electron velocity and the lateral electric

field along the channel increases sharply at the interface of the two gate material which

further results in the increased gate transport efficiency. Further, the structure creates a

step-like surface potential profile in the channel and thereby ensures screening of the

minimum potential point from drain voltage variations.

5

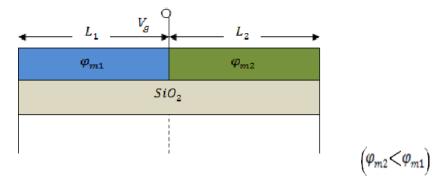


Figure 1.4: The dual metal gate structure

Multiple Gate structure:

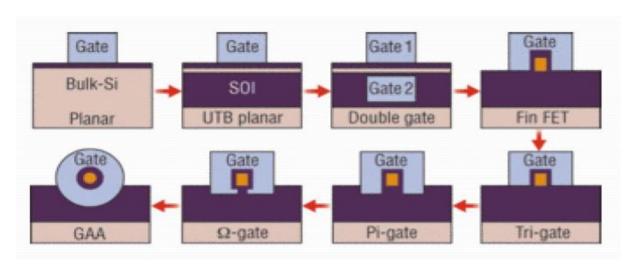


Figure 1.5: Progress of the MOSFET Technology through multiple-gates

A potential candidate to continue the MOSFET scaling further is the fully-depleted silicon on-insulator (FDSOI) MOSFET. Rigorous research of the FD SOI MOSFETs revels that this transistor possesses higher transconductance, lower threshold voltage roll-off and steeper subthreshold slope compare to the bulk MOSFET. In the FDSOI MOSFETs, the front gate parasitic junction (source/drain to channel) capacitances reduces resulting in higher switching speeds. FD SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device despite having excellent short channel characteristics. To prevent the encroachment of electric field lines from the drain on the channel region, special gate structures can be used as shown in Fig.1.5 Such "multiple"-gate devices include double-gate transistors, triple-gate devices such as the quantum wire, the Fin FET, and quadruple-gate devices such as the gate-all around device, the DELTA transistor, and vertical pillar MOSFETs. A much more efficient device configuration is obtained by using the

double-gate transistor structure. Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion or volume accumulation in the thin layer (for enhancement- and depletion-type devices, respectively), leading to an increase of the number and the mobility of electrons and holes as well as driving current (additional gain in performance in a loaded environment), optimum subthreshold swing and the best control of short channel effects and off-state current, which is the main challenge for future nano devices due to the power consumption crisis and the need to develop green/sustainable ICs.[11][12][13]

The triple-gate MOSFETs have made the advent of 22nm technology node feasible at industrial scale in 2011. One among various multi-gate structures, triple-gate MOSFET enjoys the silicon channel engaged from three sides giving enhanced on-current and reduced off-current. As the MOS dimension has attained its physical limit, the scaling beyond 22nm node is thus an insuperable task. The improvement in device performance, however, are believed to be continued in the company of multi-gate MOSFETs as they employ third dimension offering superb gate control over channel from several sides. The degree of gate controllability increases further with the quadruple-gate, the Omega/Pi-gate and the gate-all-around (GAA) structures respectively with better combinations of performance and energy efficiency.[14] [15] [16] As far as the characteristics lengths of the device structures are concerned, the gate-all-around MOSFETs offer the lowest characteristic length and hence the highest capability to be scaled for a given gate oxide thickness. This capability gets coupled with the highest current drive per unit silicon area and demonstrates strong confinement of the electric field owing to the gate surrounding the channel.

1.8 Gate engineered DG MOSFETs

Gate engineering of the MOSFET means, the total gate material of the MOSFET is engineered or divided into two materials or three materials. If the total material length is the combination of two different materials having different metal work function, then the MOSFET structure is known as dual material gate (DMG) MOSFET structure. Similarly, if the total gate material length is the combination of three different materials having different metal work function, then the MOSFET structure is known as triple material gate (TMG) MOSFET structure. In double gate structure the gate engineering technique is applied both the top and the bottom gate. For two metals the structure is known as dual material double gate (DMDG) MOSFET and for three materials the structure is known as triple material double gate (TMDG) MOSFET.

The technique of Gate engineering such as dual metal gate (DMG) MOSFET has been anticipated in which the structure has two gates with different work functions.DMG MOSFET, in which two dissimilar materials having different work functions are combined together to shape a single gate of a bulk MOSFET. In the DMG structure, the work function of the gate material (M1) close to source is chosen higher than the one close to drain end (M2) for n-channel MOSFETs. As a result, the electron velocity and electric field along the channel abruptly increases near the boundary of the two gate materials which results in improved gate transport efficiency. This shows that the threshold voltage under gate material

M1 is higher than that of under gate material M2. When the drain voltage exceeds the drain saturation voltage, the excess voltage is absorbed by gate metal M2 preventing the drain field from penetrating into the channel. This step potential is thus responsible for lower sub threshold leakage current, reduced DIBL effects and increased output resistance in DMG MOSFETS. This so called gate work-function engineering allows the DMG devices to have same threshold voltage for a reduced doping concentration in the channel region, resulting in better immunity to mobility degradation and hence higher transconductance.

1.9 Advantages of DG MOSFETs

- i. reduction of ioff.
- ii. undoped channel eliminates intrinsic
- iii. parameter fluctuations and minimizes
- iv. impurity scattering.
- v. double gate allows for higher current drive capability
- vi. better control of short channel effects.

1.10 Challenges of DG MOSFETs

- i. Control of threshold voltage.
- ii. Fabrication of the DG-FET is difficult.
- iii. Alignment of both gates is hard to achieve.
- iv. Misaligned gates result in extra capacitance and loss of current drive.

1.11 Gate misalignment of DG MOSFETs

Misalignment between top and bottom Gate of the DG MOSFETs are the most common possibility during fabrication. Because of misalignment some part of the channel has only one gate and behaves as a single gate conventional bulk MOSFET. Further more due to the absent of electric field, the electrostatic control over the gate reduces and the channel resistance

increases, therefore drive current decreases. The misalignment can be happened either side of the device; i.e. drain side or source side. If the gate shifted towards source side then it is called as drain side misalignment (DSM) and if the gate shifted towards drain side then it is called as source side misalignment (SSM). The amount of length shifted either side called as misalignment length m_a .[21]

2.1 INTRODUCTION

Silvaco Atlas is a software package used to simulate semiconductor devices. It predicts the electrical behavior of a device, which can be modeled in either two dimensions (2D) or three dimensions (3D). The software consists of several integrated programs that work together to achieve the desired results. The main programs are Deckbuild, Devedit, Tonyplot, and Athena, but there are several subprograms that are accessed during simulation that serve more specific functions.[17]

2.2 DECKBUILD:-

Deck build (see Figure 2.1) is the main program that runs the simulation and calls the associated programs as needed. Deck build uses command line code to designate what and how to run. To run Atlas simply type:

Go atlas

This runs the Atlas program within Deck build and is usually the first command unless running one of the other programs, such as Athena, first. Once Atlas is initiated, the next step is to set the parameters of the device. Atlas has a specific order (see Figure 2.2) in which the statements must be placed, otherwise the program may not function correctly. Even if it does run, it is possible that certain parameters may not be used, which causes inaccurate results. Generally the format is:

<STATEMENT><PARAMETER>=<VALUE>

Statements can have more than one parameter defined. Deck build provides many built-in examples of different devices that allow a user to run the simulation and view the results. The examples are helpful to see how the code is written when unsure how it is used.

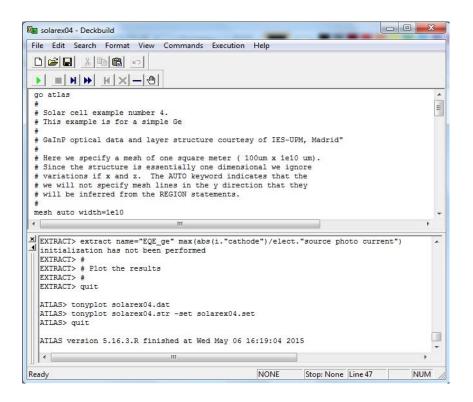


Figure 2.1 . Screenshot of Deckbuild.

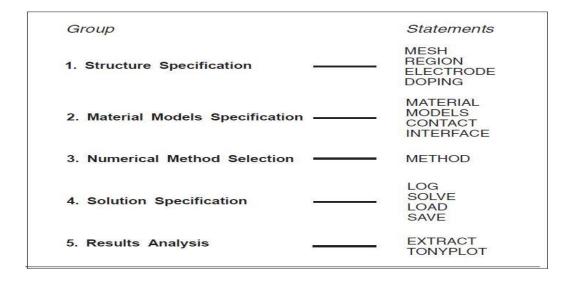


Figure 2.2. Atlas statement hierarchy. [17,p.34]

2.3 BUILDING THE DEVICE

When building the device to be simulated, the first thing to do is to define the mesh that will be the framework for the model. A mesh is a collection of triangles that overlays the device (see Figure 2.3). Each corner of the triangle is called a node. Nodes are where the equations used to solve for a solution are calculated. A finer mesh results in more triangles, which give more nodes and increases the resolution of the solution to give more accurate results.

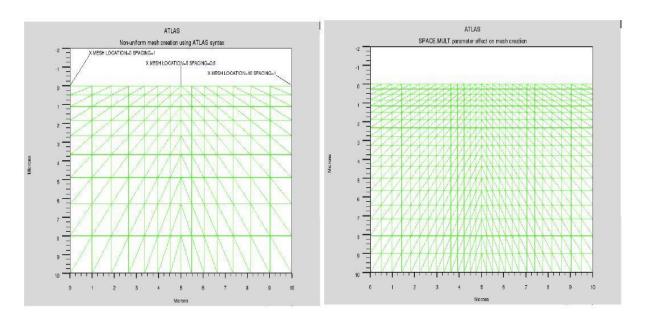


Figure 2.3. Mesh examples.[17, p. 38]

2.3.1.Defining the Structure

There are many ways a structure can be made. The first, is it can be read in by a previously created structure that has been saved in a separate file. This is done by typing the command line:

MESHINFILE=<filename>

The other way to define a structure is to simply use the command language in Deck build to define the structure. The command language for this is:

MESHSPACE.MULT=<value>

Space.mult is a scaling factor that controls the granularity of the mesh. The default value is one. Any value greater than one gives a coarser mesh, and a value less than one results in a finer mesh. The next statements define where mesh lines in the *x* and *y* direction will be:

X.MESHLOCATION=<value>SPACING=<value>

Y.MESH LOCATION=<value> SPACING=<value>

These two statements specify the location of the line and the spacing in microns. At least two *x* and two *y* statements are needed to define the mesh. If a different spacing is used, Deck build automatically inserts extra lines to allow for a gradual transition. An alternate method to the space.mult command is to use the automatic mesh function:

2.3.2. Regions

Once the mesh has been defined, the next step is to define the regions. A typical region statement is:

REGION NUMBER=<integer><material_type><position_parameters>

The material type parameter defines the type of material for the region. The properties for many materials are already stored in the program. They can be changed in a material statement further down in the code once the entire mesh is complete and doping concentrations are defined.

The position parameter defines the location in microns of the region. One way to define the location is with x.min, x.max, y.min, and y.max statements that look like:

X.MIN=<location> X.MAX=<location> Y.MIN=<location> Y.MAX=<location>

The x.min lists the minimum position in the x-direction, and x.max lists the maximum position in the x-direction. The same holds true for the y-axis. It should be noted that the x-axis starts at zero on the left and is maximum on the right, just like a standard x-y Cartesian coordinate system. The y-axis, however, is opposite what one might expect. The y.min starts at zero on the top, and downward is maximum (see Figure 2.4)

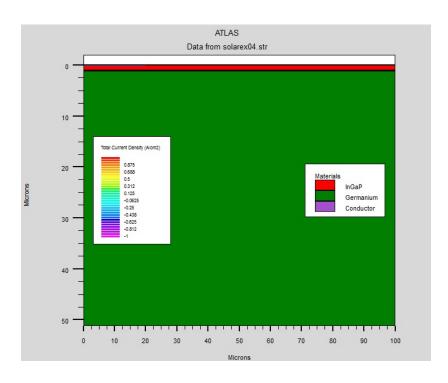


Figure 2.4. Tony plot screen shot showing the lay out of the x and y-coordinate system in Atlas

2.3.3 Electrodes

Once the regions and materials are specified, the electrodes can be defined. There must be a minimum of one electrode (that touches the semiconductor material) defined for the program to work. Up to 100 electrodes can be specified, and if any of the defined electrodes are given the same name, then the electrodes are considered electrically connected. A typical electrode statement is:

ELECTRODE NAME=<electrode name><postion_parameter>

If no y-coordinate is given, then the electrode is placed at the top of the device. The top, bottom, right and left parameters can be used to define the location as well.

2.3.4 Doping

Doping parameters are specified next and are generally in the form:

DOPING dopant_type postion_parameter

The distribution type can be uniform, Gaussian, or complementary error function. The dopant type can be specified as n.type or p.type and the concentration amount can be defined. The position parameter can be specified by region number or the minimum/maximum parameters.

2.3.5 Modifying Parameters

After the mesh. geometry, doping have been defined. and parameters the characteristics of the electrodes can be changed, the material parameters modified, and the physical models chosen. The electrodes in contact with a semiconductor material are ohmic by default. Defining a work function with the contact statement causes it to be treated as a Schottky contact. Using the materials statement allows the user to change properties of the specified material such as electron mobility, bandgap, or carrier lifetime.

2.3.6. Numerical Solutions

The next thing to define is the numerical solution which tell the program which numerical methods to use when calculating solutions for the device. There are three methods that Deckbuild uses. They are Gummel, Block, and Newton which are specified after the method statement. Each numerical method uses a different approach to solving the equations. The Gummel method solves for each unknown while keeping the variables constant. It continues doing this until a stable solution is found. The Newton method solves the total system of unknowns together, and the Block method solves some of the equations the Gummelway and the rest the Newton way. Generally, the Newton method is preferred and is the default if the method statement is not used.

2.3.7. Obtaining Solutions

To obtain solutions for the created device, the user has the options of using DC, AC, small signal, and transient voltages for the calculations. Once the voltages for the electrodes are defined, Atlas calculates the currents and the internal quantities. To set the voltage of an electrode named anode:

SOLVE VANODE=1.0

This sets the anode voltage to one volt. Multiple solve statements can be used in succession to ramp up the voltage or a sweep can be used:

SOLVE VANODE=0 VSTEP=0.5 VFINAL=5 NAME=anode

SOLVE VSTEP=0.5 VFINAL=10 NAME=anode

This sweeps the voltage from zero volts to five volts in one-half volt increments. The second solve statement sweeps from five volts to ten volts in one-half volt increments.

Atlas remembers the last voltage of the electrode, five volts after the first solve statement and ten volts after the second solve statement.

SOLVE INIT

If this statement is not included, Atlas automatically evaluates an initial solution prior to the first solve statement.[18]

2.3.8. Results

When running the simulation it is useful to open a log file to save the terminal characteristics calculated by Atlas. To save the terminal characteristics, open a log file prior to any solve statements:

LOG OUTFILE=<filename>

This opens a log file and saves it under the chosen filename. All outputs from solve statements are saved in this log file until either another log statement is opened under a different filename or the log is closed by using the log statement with the off parameter. Once the simulation is complete, this log file can be used in Tonyplot to view the results. The electrical current values stored in the log file are generally in Amperes per micron, because Atlas is a 2D simulator and sets the z-axis to be one micron. If a width dimension is specified, the cylindrical coordinate system is used, or when simulating a 3D device, then the units are in Amperes. The log file is also useful for extracting parameters by using the extract command:

EXTRACT INIT INF=<filename>

This uses the specified file to perform the extraction. If a log file is currently open, then there is no need to specify a file, as the extract statement defaults to the currently open log file. Calculation can be performed on the extracted data and the results saved in a file for later use such as viewing in Tonyplot. The results from the extraction display in the run-time output and are stored in a file called results.final. The user can also specify a different file in which to store the results by adding a different file at the end of the extract statement:

2.4 TONYPLOT

Tony plot is a graphical tool used to plot data obtained from device simulations. It can be called directly in Deck build by typing:

TONYPLOT <filename> -overlay

If the file is a log file, Tony plot displays the data in an x-y plot. It the file is a structure file, the information is displayed as a 2D mesh plot.

2.4.1 X-Y Plots

When viewing the x-y plot (see Figure 2.5), the user has several quantities to choose from to display on the x-axis and several to choose from for the y-axis. Additionally, the data can be displayed in linear or logarithmic scales. The graph can also be changed to a Cartesian graph, polar plot, or even a Smith chart. With the ruler tool, various aspects of the plot can be measured, such as the slope of a curve, distance between two points, or intercepts. Multiple x-y plots can be opened in the same window. They can also be overlaid for an easier comparison of data. To do this, select the plots and use the overlay option from the edit menu. Another way is to use the overlay option in the command line when calling Tony plot.

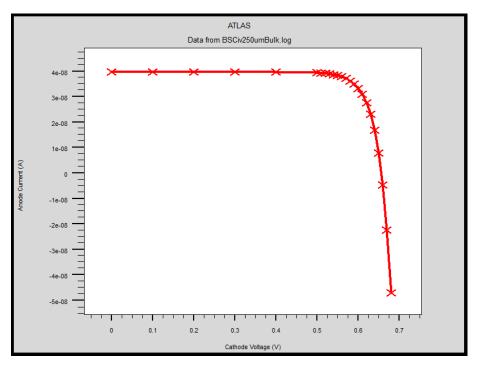


Figure 2.5. Screenshot of an *x-y* plot in Tonyplot

2.4.2 2D Mesh Plot

The 2D mesh plot shows a representation of the device. The user can see the size and shape of different regions, which is useful to make sure the device was constructed as it was intended to be. There are also a variety of options to display information about the characteristics of the device. The mesh plot display in Figure 2.6 contains buttons that control the various display options. A description of these buttons is shown in Figure 2.7.



Figure 2.6. Screenshot showing the mesh plot display buttons for Tonyplot.

(Mesh): The triangular mesh used in the simulation.
(Edges): Sides of triangles classified as region edges.
(Regions): All material regions in the structure.
(Contours): Color plotting of impurity values.
(Vectors): Representation of vectored impurities.
(Light): Light beam and ray information.
(Junctions): Metallurgical junctions in the semiconductor regions.
(Electrodes): Regions defined as being electrodes
(3D): Adds elevation to a plot so that 3D surface is plotted

Figure 2.7 Description of the display buttons in Tony plot.[19, p. 93-94]

The mesh button turns on an overlay of the mesh for the device and shows where all the triangles are located, which gives an indication of areas from which to remove mesh lines, which improves simulation time, or areas to make the mesh finer, which increases accuracy. Another important button is the regions button that turns on the

regions in the device, with each region being colour coded to the material it is made out of. Placing the mouse cursor over a particular region and pressing the "r" key on the keyboard causes a pop-up window to appear that displays the region name and material.

One of the most useful buttons is the contour button. Turning this on shows a contour plot overlaid onto the device. There are several types of information that the user can choose to display. Some examples are the doping concentration, current density, potential, and optical intensity. Using the cutline tool and cutting a cross-section of the device, we can make a plot of the band diagram. Several 2D mesh files can be opened in the same window. If these plots are all highlighted, there is a movie tool (see Figure 2.8) that creates a movie consisting of the data from all of the plots. If the plots span a range of voltages, for example, then the movie shows how the contours of the potential change within the device as the voltages change.

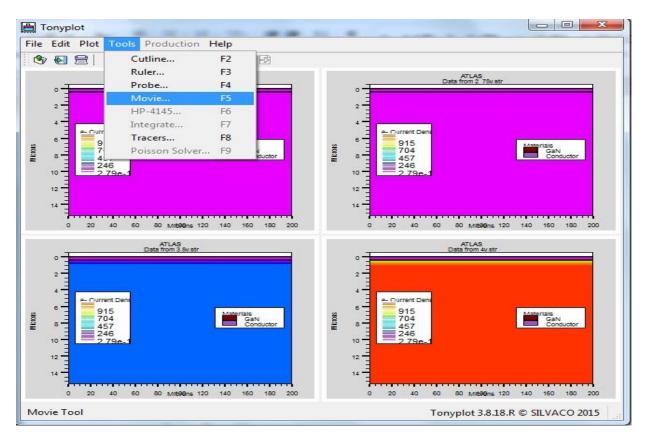


Figure 2.8 Tony plot screenshot showing several files opened in the same window with the movie tool selected.

CHAPTER -3

3.1 INTRODUCTION

In recent years, the research is going on how to restrict the consequenes of short channel effect in the device. To overcome all this multigate structure have been proposed like double gate, triple gate, omega gate, Pi gate and gate all around structure. To implement all these in fabrication very complex process so we are going for double gate structure which is easy to fabricate and simulate also. As 2D device is easier to simulate on silvaco tool. To implement this device as a biosensor is very much in control, there are lots of parameter on which we can detect it as a bio sensor like Ion current, Threshold voltage, subthreshold swing and sensitivity.

3.2 DEVICE OPERATION

The device architecture for n-type gate underlap DG-JLMOSFET based biosensors used in this work is depicted in Fig.3.1. Here, L_g is the length of the gate overlap region, L_{cavity} is the length of the underlap region. t_{cavity} , t_{si} , t_{ox} are the thickness of the underlap region, channel and gate oxide respectively. A SiO₂ layer of thickness 1nm is also considered to account for the growth of native oxide in the open cavity region, whenever silicon substrate is exposed to air ambient which act as the adhesion layer for the immobilization of biomolecules. This open cavity region serves as sensing site, in which the target biomolecules are immobilized.

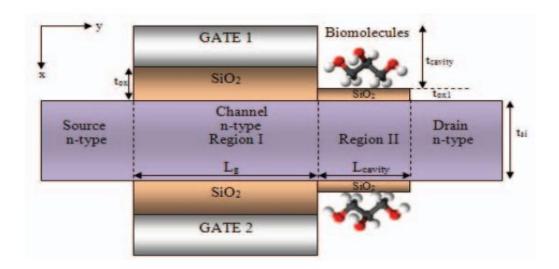


FIGURE 3.1 The simulated device structure

The device structure considered for model development is shown in Fig. 3.1. In the model development, the silicon channel region is divided into two regions, namely, gate overlap, and gate underlap. Double gate is specially designed to have more controllability over channel by applying sufficient gate voltage at constant drain to source voltage.[20] As carrier move towards source to drain they constitute current but due to short channel effect the path followed by the carriers start diverted and we get Ioff current which degrade the performance of the device. The threshold voltage of the device can be approximated by:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s q N_a \phi_F}}{C_{ox}}$$

Also current in the device is approximately governed by this equation:

Cut Off	$V_{GS} \leq V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T , \ V_{DS} \le V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{{V_{DS}}^2}{2} \right] (1 + \lambda V_{DS})$
Saturation	$V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

3.3 TYPES OF BIOSENSOR

A sensor is a detector of a physical entity that is converted to a signal that can be read out. A sensor is thus often composed of three components, a detector element, a transducer and a reader. The role of the detector is to interact with the physical entity of interest. The role of the transducer is to convert the response to a signal that can be analyzed and stored (typically to an electric signal). Thus, a sensor is an analytical device. A biosensor is a sensor that combines a biological detector element with a classical physicochemical detector (or in some disciplines a sensor that measures biological entities). The biosensor element can be a natural biomolecule, an engineered biomolecule or a biomimetic that can interact with the analyte of interest. The analyte is often a biomolecule, which is a biomarker for illness for diagnostic or prognostic purposes. It is true that sensors lacking a biological detector element are also at times referred to as biosensors, if they are measuring biological processes. Typical biological detector elements are such molecules that can interact through a chemical reaction or bind noncovalently to the analyte.

Different types of biosensors are often classified by the transducer element that is used; the reason being that this sets the limitations of the physiochemical property that is detected upon analyte recognition by the biological detector element. a) optical, b) electrochemical, c) electronic, d) piezoelectric, e) gravimetric and f) pyroelectric, of which the optical and electrochemical transducers are the most abundantly used.

3.3.1 Optical Transducer

Signal transduction in optical transducers relies on detection of photons, electrons or other forms of electromagnetic radiation. The wavelength of the electromagnetic radiation determines the resolution that can be achieved. The radiation can be detected through transmission, reflection or fluorescence to mention a few methods. The binding event can be detected through absorption of radiation, or other types of alteration such as change of wavelength or reflection angle. Absorption-based optical transducers often rely on enzymatic reactions that have a substrate or product which will absorb light at a specific wavelength. When light is passed through the sample some of it will be absorbed by the analyte and the transmission is detected.

3.3.2 Electrochemical transducers:

Signal transduction in electrochemical transducers is based on electrochemical reactions that occur when the analyte binds. These transducers can be divided into a) amperometric, b) impedance, c) potentiometric.

Amperometric:

The biological detector element is immobilized on the working electrode and a potential is applied between the working electrode and a reference electrode. When a biomarker binds to the detector element there is a change in the electron transfer reaction and thus the current shift is a measure for biomarker binding.

Impedance:

Transducers measure the dielectric properties of a medium as a function of a frequency that is inserted, which often is a sinusoidal voltage. When a biomarker binds to the biological detector element, the impedance of this three-electrode system changes. The impedance change originates from the electric dipole moment of the sample which is altered by the chemical reaction.

Potentiometric transducers react to accumulation of potential in an electrochemical cell. This accumulation is often the result of an enzymatic reaction involving the biomarker, resulting in ion formation. The ion selective electrode (ISE) has a membrane that interacts with the ions of interest while the reference electrode will not be affected by the biomarker concentration, thus the difference between the ISE and reference electrode can be recorded as the accumulation of charge in the former

3.3.3 FET –based electronic transducer:

Electronic transducers have the benefit of directly translating the reaction between the biological detector element and the biomarker to an electrical signal. There are Field-Effect Transistors (FET)-based technologies where the charges on the biomarker create a modulation of the electrical conductivity of a channel by the externally induced electric field. The external field however penetrates only a short distance into the material. Even in semiconductors that have a lower density of electrons or holes this distance is limited. Thus there is a difference between the bulk and the surface of the material. FET-based electrical transducers have the

potential to make very sensitive, label-free and real time biosensors. The FET-based biosensor will be the focus of this thesis and will be described in detail.

3.4 ISFET VERSUS FET AS A BIOSENSOR

A Field-Effect Transistor (FET) is an electronic device that amplifies a signal. This is the fundamental use of a FET. As mentioned earlier it is composed of three electrodes, a substrate and an insulating layer. The charge carriers being electrons or "holes" depending on doping can pass through the channel or not depending on the gate being open or closed. Thus as the name indicates the gate is a switch, that can generate the zeros and ones of a digital signal. The point where the conducting channels starts opening the channel and allowing contact between source and drain is referred to as threshold voltage (Vth) 115. The threshold voltage depends on intrinsic characteristics of the device such as the doping type and levels, oxide thickness and also on extrinsic parameters such as temperature, and constitution or immobilization with biological detector elements on the device.

When a charged particle is close to the nanowire surface that in FET sensors is the detection element, the field effect of the charges will affect the FET operation in a similar way as a change of gate voltage. A shift of threshold voltage can be seen in the Current-Voltage plot (IdVg). While FET is the type of transistor operation, the term Metal-Oxide-Semiconductor-FET (MOSFET) is the most common physical device and it refers to the physical structure. The MOSFET are an abundant digital circuit used in microprocessors in computers, smartphones and pads.

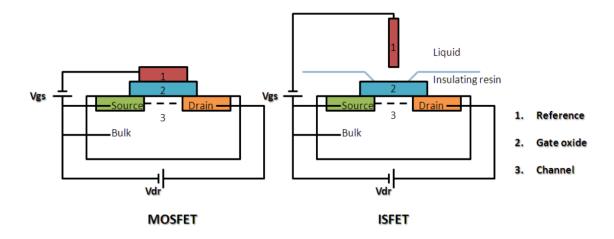


Figure 3.2 -MOSFET vs. ISFET

The charged particle leading to a threshold voltage shift in a FET is in its simplest form an ion, such as H⁺. Being a point-charge and able to react with a non-metal gate oxide surface this enabled Bergveld in the early 1970s to build the first ion sensor. The Ion Sensitive Field-Effect Transistor (ISFET) is essentially a MOSFET where the gate electrode is separated by an ionsensitive barrier and space for the fluid with ions to come into contact with the barrier, meaning that the gate insulator is in direct contact with the electrolyte. The ISFET needs a reference electrode, which is often made of silver/silver chloride to set a reference potential, Vref, instead of fixing the gate potential. The reference gate is also introduced directly to the fluid. Most problems that arise with ISFET sensing are related to the reference electrode, or current drift due to diffusions of ion through the gate dielectric. The ISFET ion sensor has been applied to a novel ion-based semiconductor sequencing method for DNA referred to as Ion Torrent.

3.5 TYPES OF BIOMOLECULE:

- NEUTRAL BIOMOLECULE: These are molecule which do not possess any charge on them, they have dielectric constant as one of its parameter. For example: APTES, Streptavidin, protein etc.
- 2. CHARGED BIOMOLECULE: These are molecule which possess charge which can be positive or negative at their reactive sites for example: Nucleic Acid, Protein etc.

The net charge of proteins is both dependent on the amino acid composition and solvent. The protein can thus have a positive, negative or neutral net charge depending on situation.

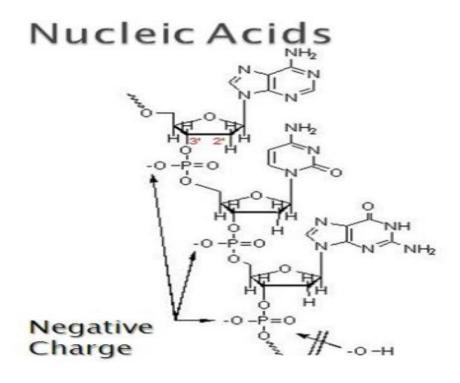


Figure 3.3 Negavtive charge biomolecule

3.6 BIOSENSOR PERFORMANCE CHARACTERICSTICS

3.6.1 Specificity and sensitivity:

There are many ways to define the performance characteristics of a biosensor. Sensitivity is often in scientific literature defined as the lowest concentration of biomarker possible to detect and specificity can often be found in scientific literature to refer to the detection of a specific biomarker. The term sensitivity thus is a measure of the true positive rate and is a proportion of true positives to total positives and a high sensitivity means that true positives are captured by the test. The term specificity on the other hand refers to the proportion of true negatives to total negatives. Thus the specificity refers to the ability to exclude true negatives from the test result. These two performance characteristics are valuable for the medical practitioner.

3.6.2 Limit of Detection:

The lowest concentration that can be identified within statistical confidence limits on the other hand is called the limit of detection (LOD). This term refers to the smallest concentration of the biomarker that can be detected compared to a blank sample within a certain confidence, typically 1% or 2 to 3 standard deviations. Another way of determining what is the performance limit is to determine the signal to noise ratio (SNR). The source of noise can be many, some intrinsic to the technology such as electronic noise or external events and phenomenon such as temperature, vibrations, humidity that can either be controlled or if characteristic of the noise

is known to be filtered out. Depending on which technology is used and what types of noise affect the system different approaches may be taken. However, when the SNR is calculated by dividing the signal power to the noise power it is crucial that they are measured at the same points in the system. Thus once the SNR is known it is possible to interpret a meaningful signal from background noise.

3.6.3 Robustness and repeatability:

A good biosensor used in a medical context needs other characteristics such as precision, which refers to low standard deviation between measurements, and signal stability, which affects the precision of the test if drift and other instabilities occur. These are matters of robustness and repeatability of the test.

4.1 INTRODUCTION

In this chapter, all the simulation results and its discussion are briefly described for the double gate junctionless transistor as a biosensor. The input characteristic of the device has been simulated. Also the characteristic of the device for neutral and charged biomolecule were also simulated. The threshold voltage, subthreshold swing and sensitivity has been calculated in this chapter.

4.2 SIMULATED STRUCTURE OF DEVICE

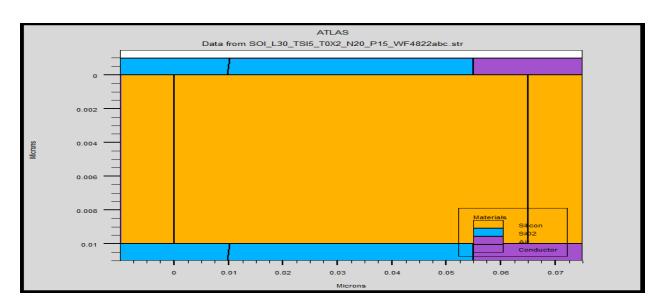


FIGURE 4.1 SIMULATED STRUCTURE OF DG JL MOSFET

The difference between the conventional MOSFET and this device is that the concentration of channel as well as source and drain is same, the channel doping value is same as of source and drain which is equal to $1x10^{25}$ m⁻³.

4.2.1 Input characteristics of device

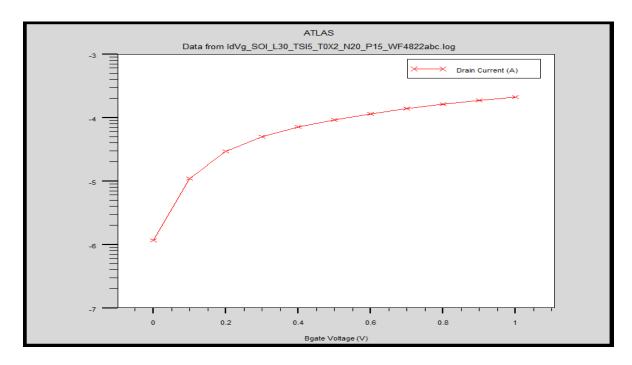


FIGURE 4.2 INPUT CHARACTERISTICS OF DG-JL-MOSFET

As we can see the ON current of the device is in 10^{-3} Amp, which is quite high which can be used as one of the parameter to detect biomolecule. There is increase in the current, But beyond 0.6V of drain voltage there is not much improvement on the I_{ON} , due to the effect of the short channel effect (such as velocity saturation, DIBL and pinch-off mechanism).

4.3 DETECTION OF NEUTRAL BIOMOLECULE

The n-type gate underlap DG-JL-MOSFET which is used has been virtually fabricated by employing process simulation tool Sprocess of Sentaurus. The effect of neutral biomolecules is simulated by introducing different dielectric material having dielectric constant i.e., K > 1 because of biomolecules have their own dielectric constant as reported in literature streptavidin = 2.1, protein = 2.50, biotin = 2.63, APTES = 3.75. on silvaco we extract two thing one is threshold voltage second is subthreshold swing to detect biomolecule.

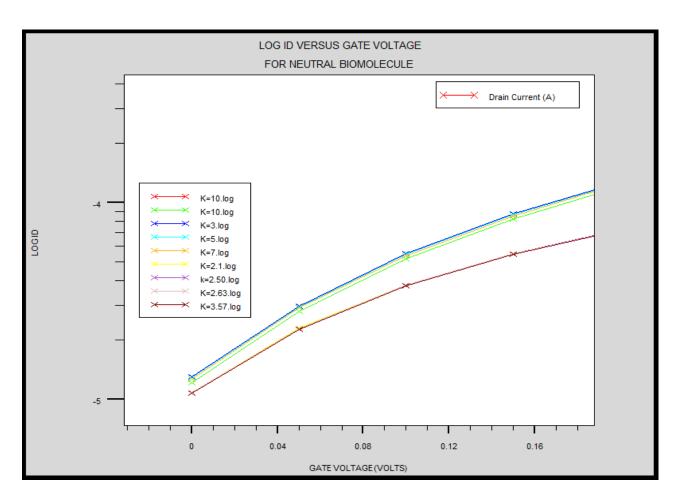


FIGURE NO.4.3 VARIATION OF LOGID VERSUS VGS TO DETECT DIFFERENT K VALUES

As different values of K>1 has been taken to detect change in ION current as well change in threshold voltage to detect neutral biomolecule.

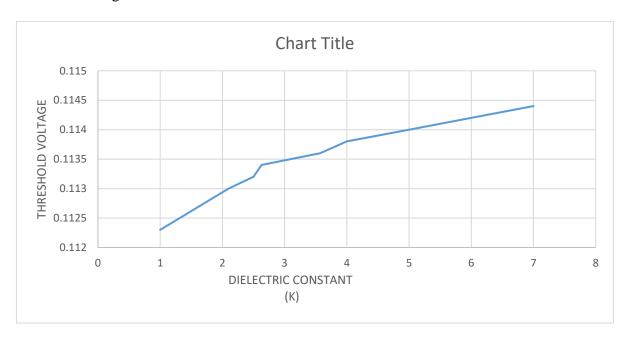


FIGURE :- 4.4 THRESHOLD VOLTAGE VS DIELECTRIC CONSTANT

The given figure 4.4 shows variation in threshold voltage with respect to change in dielectric constant of oxide. There is not completely linear relation between them but threshold voltage increases as value of constant increases.

OBSERVATION TABLE 4.1

BIOMOLECULE NAME	THRESHOLD VOLTAGE	SUBTHRESHOLD SWING
	(Volts)	(mv/decade)
AIR (K=1)	0.109383	103.301
STREPTAVIDIN (K=2.1)	0.112253	103.153
PROTEIN (K=2.50)	0.113295	103.141
BIOTIN (K=2.63)	0.113633	103.048
APTES (K=3.57)	0.116069	103.193

Table 4.1 - show the change in threshold voltage and as well as change in subthreshold swing for neutral biomolecule. There is not much variation in the subthreshold swing.

4.4 DETECTION OF CHARGED BIOMOLECULE

To simulate the effect of charge of the biomolecules, negative or positive fixed charges $(N_{\rm f}=\pm5\times10^{15}\,{\rm m}^{-2})$ at the SiO2 and underlap region interface of the device are considered:

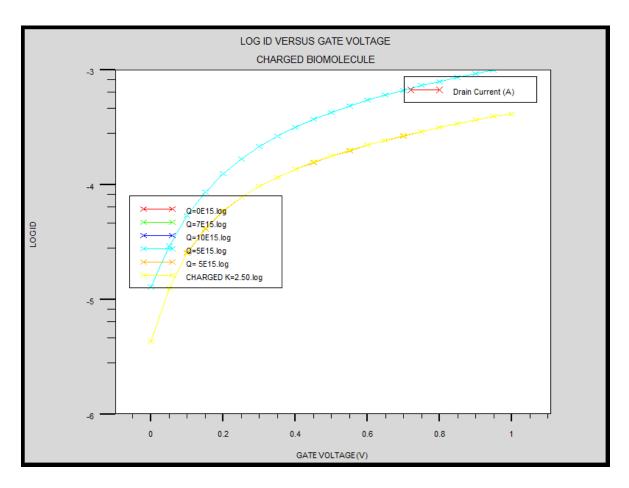


FIGURE 4.5 LOGID VERSUS GATE VOLTAGE VARIATION DUE TO CHANGE IN CHARGE ON BIOMOLECULE

Here detection parameter is Ion current which increases as we changes decreases the charge density in cavity of device. This is because positive value of charge shows more variation as compare to negative charged biomolecule.

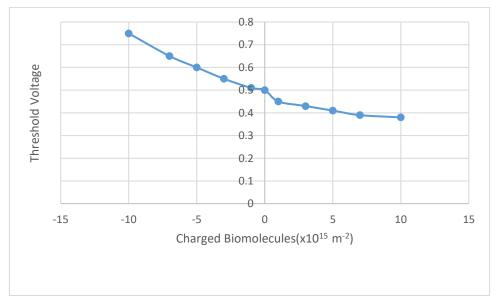


FIGURE 4.6:- THRESHOLD VOLTAGE VS CHARGE BIOMOLECULE

Figure 4.6 shows threshold variation with respect to change in charge value on biomolecule. For negative value of charge the value of threshold voltage is decreasing and for positive value of charge the threshold voltage increases.

CHARGE CONCENTRATION	CHANGE IN THRESHOLD	SUBTHRESHOLD SWING
$(Q \times 10^{15} \text{ m}^{-2})$	VOLTAGE	(mv/decade)
	(milliVolts)	
-10	0.11	103.301
-7	0.12	103.153
-5	0.14	103.141
-3	0.13	103.048
-1	0.15	103.193
0	0	103.193
1	-0.70	103.193
3	-0.22	103.193
5	-0.38	103.193
7	-0.53	103.193
10	-0.29	103.193

Table 4.2 - show the change in threshold voltage and as well as change in subthreshold swing for charged biomolecule.

The given table indicate that there is not much variation in subthreshold swing. The parameter that used to indicate change in charged concentration is threshold voltage and somewhat on Ion current.

4.5 CALCULATION OF SENSITIVITY VARIATION

The sensitivity of the device can be calculated with respect to air in the cavity of the device, the sensitivity can be calculated by this formula which is given:

$$\begin{split} S_{NBio} &= \left| \frac{V_{th}(\mathbf{K} = 1) - V_{th}(\mathbf{K} > 1)}{V_{th}(\mathbf{K} = 1)} \right| \text{ For neutral biomolecules} \\ S_{CBio} &= \left| \frac{V_{th}(\mathrm{Neutral-Biomolecules}) - V_{th}(\mathrm{Charged-Biomolecules})}{V_{th}(\mathrm{Neutral-Biomolecules})} \right| \end{split}$$

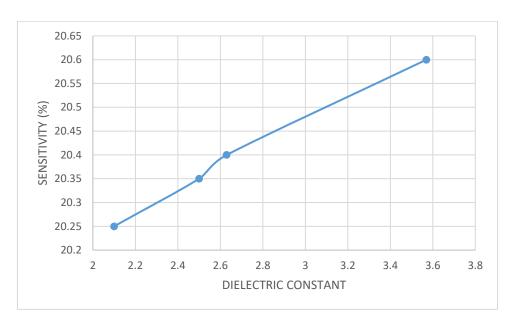


FIGURE 4.7 SENSITIVITY VERSUS CHANGE IN DIELECTRIC CONSTANT (K)

The given figure 4.7 shows sensitivity variation with respect to dielectric constant. The formula that is used to calculate the sensitivity is given in equation no. 4.1

The sensitivity is vary almost linearly in this style as there is change in dielectric constant of the device. And for dielectric constant value equal to 5 the sensitivity is 30% which quite comparable to other device like TFT, triple gate mosfet etc.

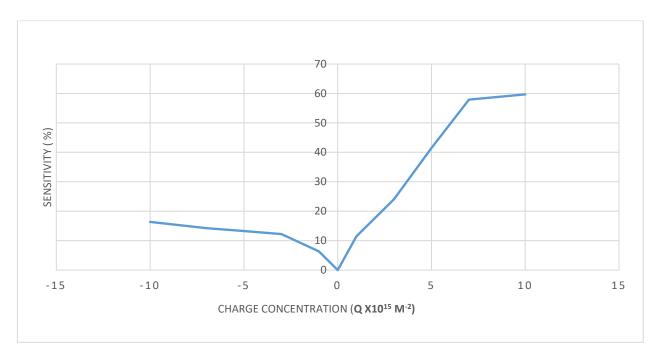


FIGURE 4.8 SENSITIVITY VERSUS CHARGE CONCENTRATION (Q $x10^{15}\ m^{\text{-2}})$

5.1 PERFORMANCE ANALYSIS

In the present work, the effects of change in dielectric constant of oxide MOSFET structures by using a 2D ATLAS device simulator. The parameters which are investigated threshold voltage, subthreshold swing, maximum drain current, maximum transconductance and output conductance.

In this work, an analytical model for n-type gate underlap DGJL-MOSFET has been proposed for the biosensing application for the label free electrical detection of the biomolecules. The impact of neutral and charged biomolecules on the electrical characteristics such as threshold voltage and drain current of n-type gate underlap DG-JL-MOSFET has been studied. Threshold voltage, drain current of n-type gate underlap DG-JL-MOSFET shows the good sensitivity towards the negatively charged biomolecules.

5.2 Scope of Future work

Here in this work, I have only neutral and charged biomolecule. In future one can investigate the hybrid biomolecule performance of the device. It is also possible to fabricate the device, and measuring the accuracy between the experimental data and the simulation results.

REFERENCES:-

- [1] J. E. Lilienfeld, "Method and apparatus for controlling electric current," 1925.
- [2] The Electrochemical Society Interface, Fall 2007.
- [3] Yuhua Cheng, Chenming Hu, "MOSFET classification and operation". Mosfet modeling BSIM3 user's guide. Springer. pp. 13. 1999
- [4] http://en.wikipedia.org/wiki/MOSFET.
- [5] U.A.Bakshi, A.P.Godse, "The depletion mode MOSFET", Electronic Circuits. Technical Publications. pp. 8–12, 2007.
- [6] International Technology Roadmap for Semiconductors, 2010.
- [7] Moore's Law "Predicts the Future of Integrated Circuits". Computer History Museum 1965.
- [8] Kaushik Roy, Kiat Seng Yeo, Low Voltage, Low Power VLSI Subsystems. McGraw Hill Professional. Fig. 2.1, pp. 44, 2004.
- [9] Kaushik Roy, Kiat Seng Yeo, Low Voltage, Low Power VLSI Subsystems. McGraw Hill Professional. Fig. 1.1, pp. 4. 2004.
- [10] Dragica Vasileska, Stephen Goodnick, Computational Electronics. Morgan & Claypool. p. 103,2006.
- [11] A. Orouji, "Nanoscale Triple Material Double Gate (TM-DG) MOSFET for Improving Short Channel Effects," in International Conference on Advances in Electronics and Micro-electronics, 2008.
- [12] L. Jin, "Two-dimensional threshold voltage analytical model of DMG strained siliconstrained silicon- on insulator MOSFETs," Journal of Semiconductors, vol. 31,no.8,pp.084008 (1-6), 2010
- [13] J. P. Colinge, FinFETs and Other Multi-Gate Transistor, New York: Springer-Verlag, 2008.
- [14] M. S. a. T. H. Alexander Kloes, "MOS: A New Physics-Based Explicit Compact Model fot Lightly Doped Short-Channel Triple-Gate SOI MOSFETs," IEEE Trans. on Electron Devices, vol. 59, no. 2, pp. 349-358, 2012.

- [15] A. Yesayan, "Physics-based compact model for ultra scaled FinFETs," Solid State Electronics, vol. 62, no. 1, pp. 165-173, 2011.
- [16] R. Ritzenthaler, "A 2D analytical model of threshold voltage for Pi-gate FinFET transistors," in Proceedings in EUROSOI, Grenoble, France, 2010.
- [17] Atlas User's Manual, Silvaco International, Santa Clara, CA, 2005.
- [18] Devedit User's Manual, Silvaco International, Santa Clara, CA, 2014.
- [19] Tonyplot User's Manual, Silvaco International, Santa Clara, CA, 2014.
- [20] Analytical Model of Gate Underlap Double Gate Junctionless MOSFET as a Bio-Sensor Ajay1, Rakhi Narang, Manoj Saxena and Mridula Gupta. Third International Conference on Devices, Circuits and Systems (ICDCS'16)
- [21] R.Y. Yan, A. Ourmazd, K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk", *IEEE Trans. Electron Devices* vol. 39 pp. 1704-1710, 1992.

International Journal:

- Shiv Bhushan, Santunu Sarangi, Abirmoya Santra, Mirgendra Kumar, Sarvesh Dubey, P. K. Tiwari and S. Jit, "An Analytical Surface Potential Model For Strained-Si on Silicon Germanium MosFet Including The Effects of Interface Charge " Journal of Electron Devices (France) , Vol. 15, pp. 1285-1290, 2012.
- Shiv Bhushan, Santunu Sarangi, Abirmoya Santra, Gopi Krishna S. and P. K. Tiwari, "An Analytical Model of Threshold Voltage for Short-Channel DoubleMaterial-Gate (DMG) Strained-Si (s-Si) on Silicon-Germanium MOSFETs", Journal of Semiconductor Technology and Science (in press).
- Santunu Sarangi, Shiv Bhushan, Abirmoya Santra, Sarvesh Dubey, S. Jit and P. K. Tiwari, "A Rigourous Simulation based study of Gate Misalignment Effects in Gate Engineered Double-Gate (DG) MOSFETs", Superlatice and Microstructure Journal, Elsevier (In Press).
- 4. Gopi Krishna S., Santunu Sarangi, Shiv Bhushan, Abirmoya Santra and Pramod Kumar Tiwari, "An analytical threshold voltage model for a shortchannel dual-metal-gate(DMG) fully depleted recessed- source/drain (ReS/D) SOI MOSFET",

- Superlatice and Microstructure Journal, Elsevier, 2013 (In Press).
- Abirmoya Santra, Santunu Sarangi, Shiv Bhushan, Gopi Krishna S., Sarvesh Dubey and P. K. Tiwari, "A manuscript titled An Analytical Threshold Voltage Model for Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs", IEEE Transaction on Nanotechnology, 2013 (communicated).
- 6. Abirmoya Santra, Santunu Sarangi, Shiv Bhushan, Gopi Krishna S., Sarvesh Dubey and P. K. Tiwari, "An Analytical Threshold Voltage Model for high-k Triple-Material-Gate (TMG) Strained-Si (s-Si) on Silicon-Germanium on Insulator (SGOI) MOSFET", International Journal of Electronics, Taylor and Francis Online, 2013 (Communicated).

International Conference:

- Analytical Model of Gate Underlap Double Gate Junctionless MOSFET as a Bio-Sensor Ajay1, Rakhi Narang, Manoj Saxena and Mridula Gupta. Third International Conference on Devices, Circuits and Systems (ICDCS'16)
- Santunu Sarangi, Gopi Krishna .S, Abirmoya Santra, Shiv Bhushan, and P. K. Tiwari, "A Simulation-based Study of Gate Misalignment Effects in TripleMaterial Double-Gate (TMDG)MOSFETs" IEEE conference proceedings, IMAC4S, Kerala Mar 2013 pp. 41.
- Santunu Sarangi, Shiv Bhushan, Gopi Krishna .S, Abirmoya Santra and P. K. Tiwari, "An Analytical Surface Potential Model of a Gate Misaligned Triple Material Double-Gate (TM DG) MOSFET", Conference proceedings, ICQNM, Italy 2013 (Accepted).
- 4. 2. Santunu Sarangi, A. Santra, S. Bhushan, Gopi Krishna S., and P. K. Tiwari, "An Analytical Surface Potential Modeling of Fully-Depleted Symmetrical DoubleGate (DG) Strained-Si MOSFETs Including the Effect of Interface Charges", IEEE conference proceedings, SCES, Allahabad, Mar 2013.