Scalability Analysis

and

Performance Comparison of

Junctionless Thin Film Transistors

A thesis submitted in partial fulfillment of the requirements

for the degree of Master of Technology

in VLSI Design

by

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(2017PEV5254)

under the guidance of

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July 2019

CERTIFICATE

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This is to certify that the thesis report entitled "**Scalability Analysis and Performance Comparison of Junctionless Thin Film Transistors** ", submitted by **Garima Agrawal, Roll no. 2017PEV5254** in partial fulfillment of the requirements for the award of Master of Technology in Electronics and Communication Engineering with specialization in "VLSI Design" during the session 2017- 2019 at Malaviya National Institute of Technology, Jaipur is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other university/institute for the award of any other Degree.

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July 2019

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DECLARATION

I declare that,

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3. I have followed the guidelines provided by the Institute in preparing the dissertation.
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ACKNOWLEDGEMENTS

At the very outset I would like to express my sincere thanks & gratitude to my Supervisor, Advisor and Mentor **Dr. Chitrakant Sahu** for his invaluable guidance and advices during every stage of this project. His useful comments, remarks and interest in my work helped me to carry out this work with enthusiasm. He has been a constant source of encouragement and support even during the tough times and guided me whenever I ran into a trouble spot or had a question about my research or writing. Being an excellent academician and a devoted teacher with helping mind; he always steered me in the right direction whenever he thought I needed it.

I extend my cordial appreciation to **Prof. D. Boolchandani**, the Head of Department (ECE) for the help in arranging all the administrative procedures of the University and providing all the facilities for the successful completion of thesis.

I also extend my thanks to my colleagues who have willingly helped me out with their abilities during the project development stage. I appreciate the Authority of MNIT Jaipur for providing a congenial and healthy environment of staying at MNIT Campus with all other research scholars. My sincere thanks goes to everyone who created an atmosphere to feel me at home away from home.

I would also like to convey my heartfelt thanks to all my loved ones, i.e. my parents and siblings who always trusted and supported me on my endeavour of research with their love and blessings.

Garima Agrawal

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ABSTRACT

Thin Film Transistors have recently attracted the attention of many researchers due to their affinity with low cost and low temperature processes on flexible substrates. In this work, firstly the importance of using junctionless devices has been described by comparing them with the conventional inversion mode devices. Though the concept of junctionless devices is not new; but it acquires new forms when applied to different type of devices. When applied to thin film transistors; it adds many new features to the existing thin film transistors. At the same time; the scalability analysis of junctionless polysilicon thin film transistor has been done where the impact of variation in the major structural parameters of the device such as channel thickness and channel length is studied on different parameters of the device such as the transfer characteristics, transconductance and the channel capacitance versus gate bias plot; which ultimately affect its device characteristics and its operational ability. Also; a comparative study between Junctionless polysilicon thin film transistors and their amorphous counterparts has been done and it has been illustrated how the transfer characteristics and other parameters e.g. transconductance, unity gain frequency and channel capacitance of the device change by just changing the material of the channel. By comparing the two, we can find out which one is more suitable for a particular type of operation. So choice of material plays an important role in device performance.

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ABBREVIATIONS

TFT	Thin Film Transistor
JL TFT	Junctionless Thin Film Transistor
IM TFT	Inversion Mode Thin Film Transistor
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
LPCVD	Low Pressure Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
OLED	Organic Light Emitting Diode
RGB	Red Green Blue
S	Source
D	Drain
G	Gate
DIBL	Drain Induced Barrier Lowering
LCD	Liquid Crystal Display
AMLCD	Active Matrix Liquid Crystal Display
IGZO	Indium Gallium Zinc Oxide
LTP	Low Temperature Poly Silicon
TCAD	Technology Computer Aided Design

SYMBOLS

V_{GS}	Gate to Source Voltage
Vth	Threshold Voltage
^{o}C	Degree Celsius
SiO_2	Silicon di oxide
V_{FB}	Flatband Voltage
Φ_{ms}	Contact potential difference between metal and semiconductor
Q_{ox}	Effective charge in the dielectric
C_{ox}	Dielectric capacitance
T_{ox}	Oxide thickness
ϵ_{ox}	Oxide permittivity
n-Si	N type silicon
p-Si	P type silicon
a-IGZO	Amorphous Indium Gallium Zinc Oxide
μ_n	Mobility of electrons
μ_p	Mobility of holes
fT	Unity Gain Frequency

Chapter 1

INTRODUCTION

1.1 Introduction:

In recent years; electronic devices fabricated on flexible substrates have drawn a great attention among many research communities. Flexible word can signify many traits: bendable, elastic, non breakable, light weight, roll-to-roll manufacturable or large area. Such devices are able to fulfill the demand of low power, portable and inexpensive electronics for the rapidly developing wireless telecommunication. The development of flexible electronics started in 1960s.

1.1.1 Flexible substrates:

The use of flexible substrates has following advantages:

- It makes the development of new products possible. These products can be integrated into light weight displays e.g. flexible solar cells which can be well integrated into cylindrical or spherical cameras for security purposes.
- It reduces the fabrication cost of devices as compared to the existing flat-panel or planar technology.
- It enables use of materials that need less processing temperature.
- It allows wider variety of materials to be used e.g. Low cost plastics, paper etc.
- It reduces the thermal deformations of substrate hence mechanical stress is reduced in the device to a much greater level. This mechanical stress is generally because of difference in the thermal coefficient of expansion that exists between the films and the substrate.
- It uses materials that have already well established material science and device physics.

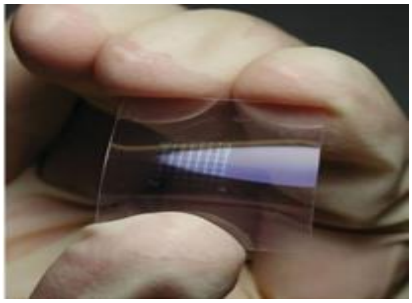


Fig 1.1 Flexible sheet of thin film transistor bent at radius of 30 mm[24]

1.2 Thin Film Transistors:

TFTs are the key elements of flexible electronics due to their affinity with low cost and low temperature processes on flexible substrates. The basic definition of TFT can be stated as follows**: "TFTs are those electronic devices that are based on FET (Field Effect Transistor) principle where the semiconductor material is allowed to deposit in a form of thin film on a substrate of insulating nature such as glass, metallic oxides or plastic substrates."**

TFT is such a transistor whose active layer which carries current is in a form of a thin film (usually a film of silicon). We know that in a flat-panel display, it is essential for the light to cross the substrate to reach the eyes of viewer. For such displays; wafers of Silicon which are opaque in nature will not be suitable so glass; which is highly transparent; is used as substrate and it is also compatible with the conventional processing steps of semiconductor. But since glass cannot be considered as a semiconductor material like silicon, so a thin film made of silicon is allowed to deposit on the top and the transistors are then fabricated by using this thin layer. Hence, named as "thin- film transistor." Many different type of TFTs based on different materials can be made.

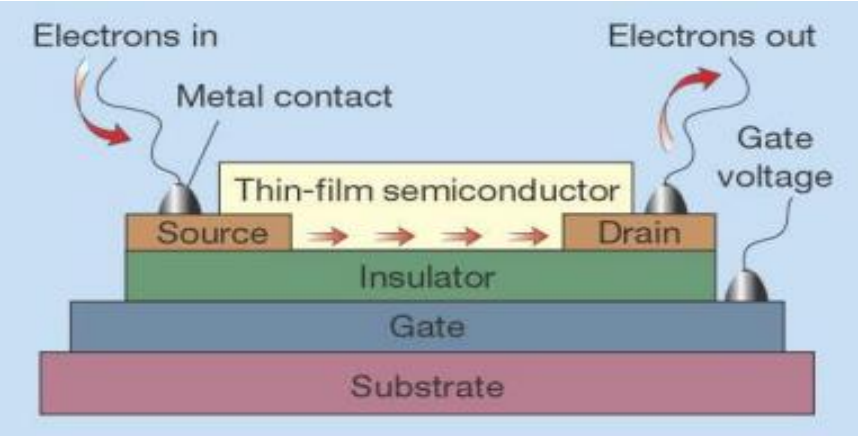
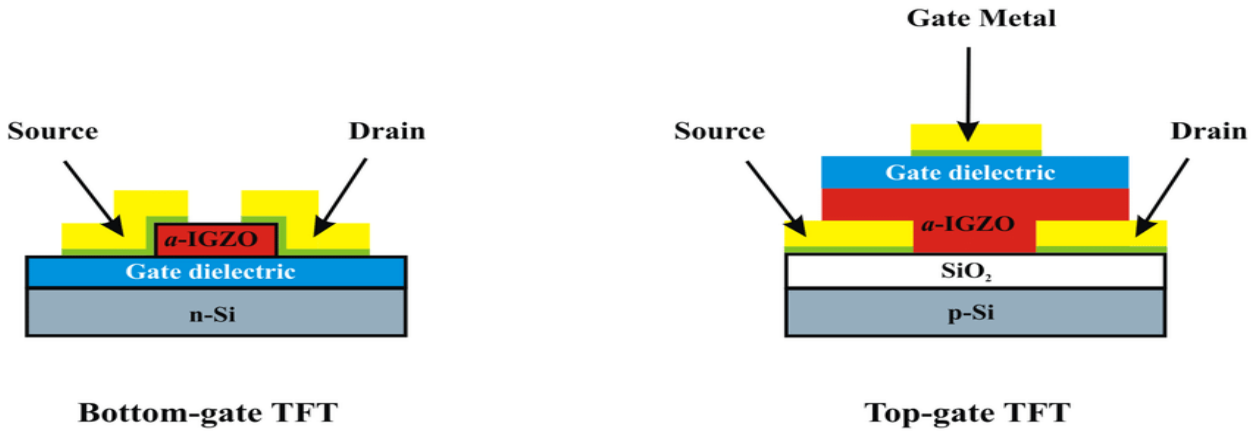


Fig1.2 TFT: basic schematic

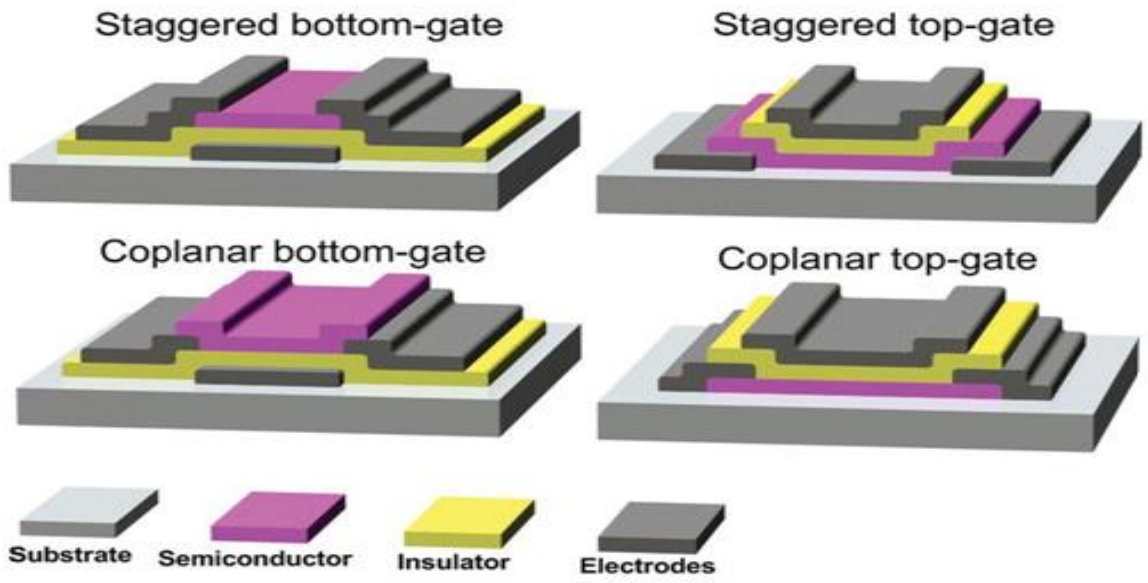
1.2.1 TFT structure and its operation: TFT is a three terminal device with source, gate and drain as the three terminals; just like MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Difference lies in its operation where it behaves as a FET working in accumulation mode unlike MOSFET which works in inversion mode.

According to Weimer's definition; we can classify TFTs in mainly two categories based on the position of gate (it is on top or bottom of the structure) i.e. **Top Gate and Bottom**

Gate TFT. Another type of structural classification of TFT can be done based on position of source and drain electrode and the semiconductor thin film layer (whether the source and drain are existing on the opposite sides or on the same side of the semiconductor):**Staggered TFT and Coplanar TFT**. Hence the four possible combinations that can be made for a TFT are as follows: 1. Top-gate staggered TFT 2. Top-gate coplanar TFT 3. Bottom-gate staggered TFT 4. Bottom-gate coplanar TFT



(a)



(b)

Fig 1.3 (a) Front View of top gate and bottom gate TFT[5] (b) Most conventional structures of TFT , based on gate position and electrodes distribution with respect to the semiconductor.[24]

The staggered bottom gate arrangement is generally used for fabricating hydrogenated amorphous silicon TFTs whereas a coplanar top gate configuration is usually used for polysilicon TFTs. The main problem in bottom gate arrangement is that there is direct exposure of air to the semiconductor surface therefore it can bring certain instability effects which are not desired but this can be seen in other way that such direct contact with air can change its properties easily such as; by the easy and fast adsorption of impurities at the time of annealing or plasma treatments in an appropriate environment.

1.2.2 Parameters of TFT:

- **Threshold Voltage:**
  Drain current depends on V_{th} in similar manner as in MOSFET. V_{th} of TFT varies with the changing gate insulation capacitance or the semiconductor film thickness. Thicker film devices with short channel length possess small V_{th} hence making the device suitable for low power operation.

  If we take n-type TFT for example, based on whether V_{th} is positive or negative, the devices are said to work in enhancement or depletion mode, respectively. As far as circuit fabrication is concerned; both the mentioned types are useful but usually the preferable one is the enhancement mode. Reason behind this is that no gate voltage is needed in it to enable the transistor to go in turn off state hence the design of circuit becomes much simpler and also reducing the consumption of power in that circuit.

- **Mobility:**
  It determines the reliability of the device. It is related to the fact that how efficiently carriers move in a material; therefore has effect on the maximum drain current and maximum possible frequency of operation. In any given substance, μ gets altered by some scattering mechanisms. Some examples of such mechanisms are vibrations associated with the lattice, grain boundaries, ionized impurities, and other structural defects. In a TFT, since the charge carriers move in a very confined region which is in proximity to the interface between the dielectric and the semiconductor, therefore some extra scattering sources should also be taken into consideration e.g. Coulomb scattering from charges present in dielectric layer and interface states or scattering related to surface roughness. Inspite of all this we can say that in a TFT; μ experiences modulation due to V_G, so the mentioned mechanisms of scattering do not remain much significant at any given bias conditions. TFT's mobility can be varied by changing the doping concentration of semiconductor layer. Higher mobility is a merit because it leads to

- Higher cut off frequency
- Higher current

μ for amorphous TFT is about $0.1cm^2/Vsec$

μ for polySilicon TFT is about $500cm^2/Vsec$

- **Ion/Ioff Ratio:**

  It is the ratio of accumulation mode current to the depletion mode current where Ioff and Ion indicate the current flowing between source and drain at a particular drain voltage. Ioff is generally given by the leakage current of gate, whereas Ion is dependent on the semiconductor material used and on the fact that how effective is the capacitive injection due to the field effect. Ion/Ioff exceeding 10^6 are generally achievable in thin film transistors. High value of this ratio is needed for these devices to work efficiently as electronic switches in display and memory devices etc. Its value is high for a thinner semiconductor layer as well as short channel devices.

1.2.3 Areas of Application:

- **Flat panel displays:**

  TFTs find application mainly in the flat panel displays due to increasing demand for low power, portable, light weight, rugged and high resolution displays.

  The LCD consists of Liquid crystals; which is nothing but a state that exists between liquid and solid i.e. the matter is capable to change its form from liquid to solid and vice versa. It flows almost like a liquid and has the tendency to orient itself to form solid. These crystals possess light modulation property when used in displays. A number of pixels are arranged in matrix form i.e. an array of rows and columns. Millions of such pixels when combined together; they create an image on the display. Each pixel possesses a liquid crystal kept between two conductive layers hence behaves like a capacitor. Each pixel is connected with a switching transistor.

  TFT LCD is a variant of LCD in which TFT is used as the switching transistor to enhance image qualities such as contrast and address ability. The dominant technology currently prevailing in the flat panel display is the AMLCD i.e. the Active Matrix Liquid Crystal Display where TFTs are embedded within the panel itself. These TFTs function individually as switches allowing the pixels to change their state with a fast rate hence enabling them to get turn on-off rapidly.

Prior to the development of AMLCDs, the technique of direct pixel addressing, also known as the passive matrix; was used as the basic form for LCDs. The main problem in addressing the pixels directly is that leakage routes exist which make the adjacent pixels get turned on partially. Therefore method of addressal of each pixel by the help of a transistor removed these leakage routes and enabled acive matrix LCDs to lead the display industry.

Following are the advantages of using TFT in LCD displays:

- It enables the flat panel displays to be made of larger dimensions larger dimensions. The diagonal dimension of the substrates used these days for TFT LCD is about 64 inches.
- We can view the TFT monitors from any desired angle without any distortion in the image; unlike the LCD monitors.
- We get very crisp and sharp text from TFT monitors with increased response time compared to ordinary LCD.

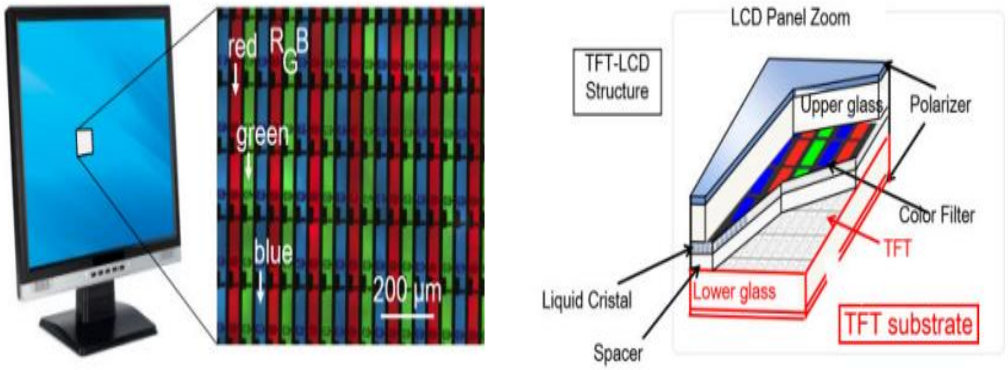


Fig 1.4(a) Observation of screen at microscopic level: RGB pixels can be clearly seen[2]

(b)TFT LCD panel: crosss-sectional view [2]

Working principle:

Inside part of the screen sends light at the array substrate's bottom part of the thin film transistor; which further passes through the entire device. The liquid crystal experiences a change in its configuration in that pixel area where any pixel gets turn on. Therefore there will be no longer crossing of light through the upper glass in that pixel area. RGB (Red, Green, Blue) colors can be chosen in this manner.

In above diagram; two polarizer filters, color filters and two alignment layers are able to find accurately the amount of allowable light that can cross and the colors that are seen. The layers are placed between the two glass panels. When a particular voltage is given to the alignment layer, it creates an electric field; due to

which the liquid crystals get aligned. Hence every pixel present on the screen needs three components, one for red, green and blue .

Description of array of TFT pixels:
The TFTs present in one line have same source line and the TFTs present in one column have same gate line. When one gate line and one source line is applied with a voltage, then the TFT present at the intersection point of both lines gets turn on. However, all the other TFTs remain still off.[2]

- **Sensors, LED:**
  TFTs of different structures and composed of various type of materials can be easily coupled to other devices to detect biological, chemical or optical changes that occur because of charge carrier transport, photon emission etc. Ion-sensitive field-effect transistor (ISFET) sensors are the most common chemical sensors where TFT gate is extended to increase the surface area for detection. A thin insulator layer such as silicon nitride is used to cover these sensors. The active layer acts as a transducer, which transforms the chemical signal (concentration etc.) into a physical one by absorbing the molecules. This changes the electrical characteristics causing a change in the gate voltage or in the current flowing between the source and drain.[2]

  Gas sensing: Environment related applications and hazard detection tasks have been accomplished. TFT gas sensors are able to give tough competition to the commercially available gas sensors. Merits of TFT gas sensors are higher sensitivity, functioning at room temperature and shorter response time.

  Commercial X-ray detectors which are flat panel based are used for medical diagnosis of fractures, tumor etc. where X Rays are detected using photodiodes fabricated on top of TFTs. When X Ray reaches the photodiode, a proportional electric charge is produced which moves towards the pixel electrode and is stored by the capacitor integrated inside the TFT array.

1.2.4 Comparative study of CMOS and TFT Technology:

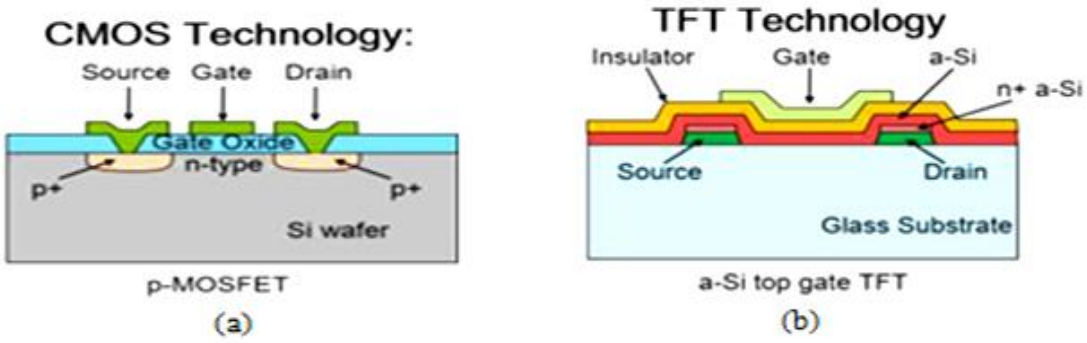


Fig 1.5 View of CMOS and amorphous Si top gate TFT [2]

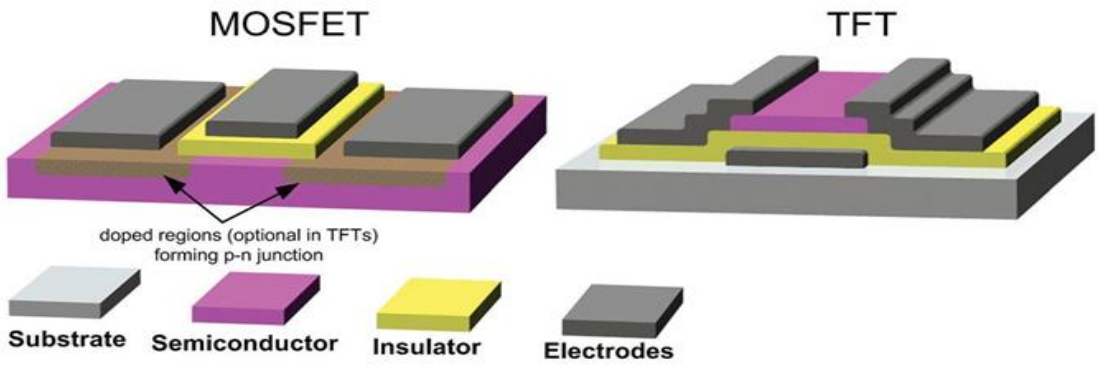


Fig 1.6 Structures showing MOSFETs and TFTs. comparison[24]

S.No	Property	CMOS technology	TFT Technology
1.	Technology used for layer growth	Implantation, layered growth from the substrate, and deposition	Deposition i.e. methods like sputtering, PECVD
2.	Layer quality	Highly crystalline channel, source and drain.	Amorphous or polycrystalline
3.	Carrier mobility in the channel ($cm^2V^{-1}s^{-1}$)	500	0.5 to 200
4.	Processing Temperature	High (>600^{o}C) ~ 1000^{o}C	Low (<600^{o}C) . It is constrained by the factors such as the substrate's softening point, which does not exceed 600–

			650^0C for most common glass substrates.
5.	Type of substrate used	Semiconductor in nature : opaque	Any type of substrate can be used including glass or plastic: transparent
6.	Dimensions of substrate used	mm	cm to m

Table 1.1 Differences between CMOS and TFT

In this table; S.No. 2, 3, 5 and 6 are consequences of S.No.1. Implantation technique helps to preserve crystallinity in CMOS. Since only a deposition process is involved in the layer growth of TFT therefore transistor can be fabricated on any kind of substrate. This is an advantage of TFT over CMOS.

A simple active-matrix circuit is shown below in Fig. 1.7 where a switching TFT, a storage capacitor and a liquid crystal are present in parallel to each other and are driven by a switching TFT which is connected to the scan and data circuits.

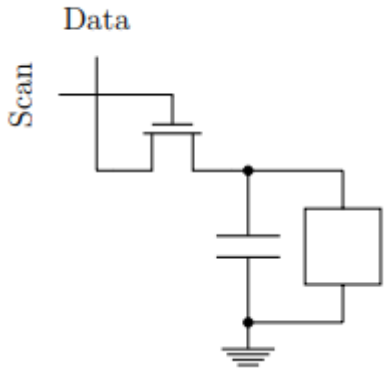


Fig 1.7 Active matrix display:Equivalent circuit

1.3 Thesis Organisation:

After the introduction part of this thesis, following chapters have been included:

- Chapter 2: It mainly contains differences between Junctionless and conventional inversion mode devices and also discusses about the works done by the research communities related to Junctionless polysilicon TFTs in the past.

- Chapter 3: This chapter is about the simulation parameters and obtained results of Junctionless polysilicon TFTs in the past.
- Chapter 4: This chapter is about evolution of semiconductor materials used in thin film transistors. It also elaborates the performance comparison of different junctionless devices by changing the material of the active channel layer in the device.
- Chapter 5: It contains explanation of the conclusion derived from this project along with the future scope of the same device.

Chapter 2

JUNCTIONLESS THIN FILM TRANSISTORS

2.1 Introduction:

MOSFET scaling is following the Moore's law prediction for almost the past forty five years to enable the IC industry to meet the everlasting demand for higher performances. However, this process of scaling becomes increasingly problematic because of the several limitations that arise from both device and process capacities as the technology node reaches 28nm and beyond. Hence to tolerate this era of downscaling, some non classical devices are currently being introduced in the roadmap. One of such devices is the Junctionless transistor which reduces the challenges associated with the scaling of CMOS devices. As the name suggests, it does not need any junctions and this is the main advantage of Junctionless transistor.

It consists of a heavily doped channel of doping concentration greater than or equal to 10^{19} cm^3.This channel has same type of doping as of source and drain hence formation of source/drain junctions can be avoided unlike the inversion mode thin film transistors. As a result; junction formation issues do not exist anymore and fabrication also becomes simple. Such device also has the ability to eliminate the issues present in ultra short channel devices in the future because it has a very good control over the gate, lower leakage current, an expected increment in movement of carriers etc.

For Junctionless devices; a gate material having large work function difference to the channel is needed. It should be noted that JLT is fully depleted in off state. Gate bias is needed to bring the channel out from depletion and to allow conduction between source and drain. As there exists a single semiconductor layer with uniform doping from source to channel; it can be modeled as a resistor whose resistance can experience modulation by the gate. However the semiconductor layer doping needs to be kept very high so that reasonable conduction is able to occur between the source and drain. At the same time; the depletion width in a heavily doped semiconductor is very small which requires an ultra thin silicon body for a JLT.

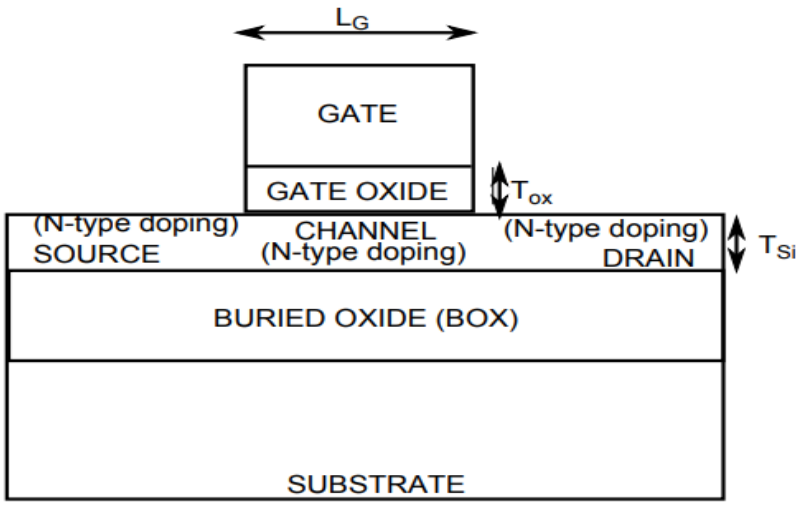


Fig2.1 Schematic of a Junctionless Transistor

2.2 Review of Research Papers:

Junctionless thin film transistors have been an area of interest in the past few years due to their numerous benefits over the conventional inversion mode thin film transistors.

2.2.1 Differences between Junctionless and Inversion mode TFT:

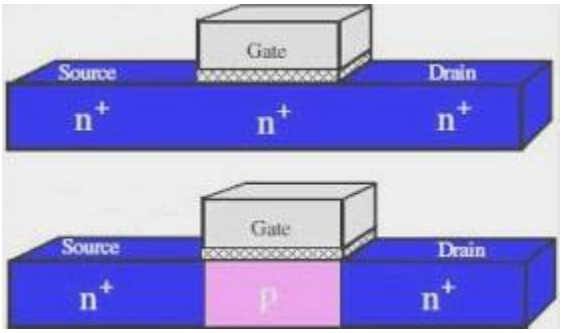


Fig 2.2 (a) Junctionless Transistor (b) Inversion Mode Transistor [5]

S.No	Author/Date	Property	IM-TFT	JL-TFT
1.	Hong Chih Lin et al. (2013) [8]	Basic Difference	p-n Source Drain junctions are present	In JL-TFT; p-n Source Drain junctions are not formed because channel is heavily doped with the same type of doping as Source and Drain.
2.	Hong Chih Lin et al. (2013) [8]	Operating Principle	IM TFT depends on the formation of a surface inversion layer between the source and the drain.	In JL TFT; when a large gate overdrive voltage is applied to a JL device, the current starts flowing through almost the whole channel region; hence we can say that JL devices have a superior current drive ability .
3.	Hong Chih Lin and Tiao-Yuan Huang (2012) [7]	Current Drive Capability	The induced inversion charge per unit gate area for conduction, denoted as Qc, is $C_{ox}(V_G - V_{th})$ where V_{th} is Threshold voltage V_G is Gate voltage and C_{ox} is the Gate Oxide capacitance per unit area Therefore the number of the induced conduction carriers is given by Q_c/q (q is the electron charge) which is about 10^{12} cm^{-2} for common operations.	Such a value is easily exceeded by a planar JL device, in which Q_c/q has a simple relation to the product value of channel thickness and the carrier concentration, as the effects due to gate bias and the oxide charges are ignored. For this, it only demands an ultra thin channel **(**≤10nm**)** to attain these high Q_c/q values if the carrier concentration is greater than 10^{19} cm^{-3}. Hence a very high current drive can be achieved with JL devices which inherently contain ample amount of carriers inside the channel.

4.	Ya Chi Cheng et al. (2013) [10]	Nature of Electric Field	In all Inversion mode devices; the electric field is concentrated at the two side edges of the gate i.e. at the depletion region between the source/drain pn junction and the channel.	In JL devices, the electric field is divided somewhat like a resistor. As a consequence; we observe the maximum electric field in JL device to be lesser than that in IM device.
5.	Ya Chi Cheng et al. (2013) [10]	Breakdown Voltage	The measured V_{BD} of IM devices is low.	The measured V_{BD} of JL devices is much greater than that of IM devices because of the reduced electric field in JL TFT.
6.	Chia Tsung Tso et al. (2017) [12]	Threshold Voltage shift with temp-erature	Variation in threshold voltage with temperature is small (specifically in the range of 300 to 473K).	This variation is high in JL TFT.
7.	Chia Tsung Tso et al. (2017) [12] Dong-Ru Hsieh et al. (2016) [15]	Short Channel Effects	Higher in inversion devices because they possess a smaller physical channel length as compared to that in JL device. This results in serious short channel effects such as poor sub threshold swing and DIBL.	Short channel effects in junctionless devices are less than in inversion devices. So they have better SCE immunity because effective gate length is longer than the physical gate length.[15]
8.	Dong-Ru Hsieh et al. (2016) [15]	Carrier mobility	IM TFT has low carrier mobility.	JL TFTs are less sensitive to the non ideal interface between the gate oxide and semiconductor and carrier mobility obtained is higher because of bulk transport mechanism.

Table 2.1 Differences between Junctionless and inversion mode TFT

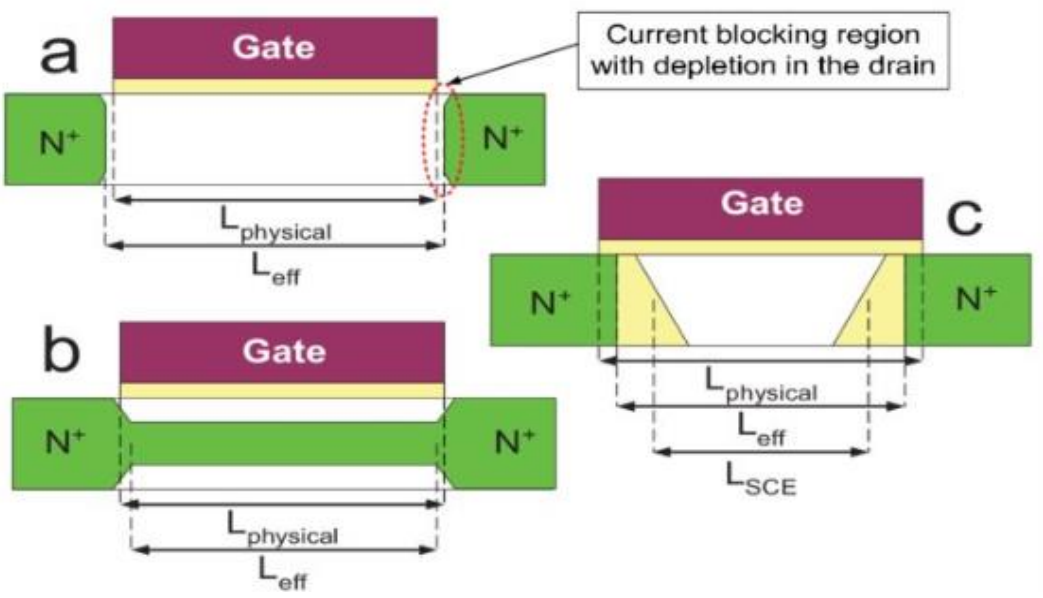


Fig2.3 Different Effective gate lengths in (a) Junctionless Transistor in OFF state (b) Junctionless Transistor in ON state (c) Inversion Mode Transistor [5]

2.2.2. Junctionless Polysilicon Thin Film Transistors:

In [7], N-type Junctionless Poly-silicon TFTs were fabricated and their characteristics were studied with an ultrathin channel heavily doped with phosphorus. TFT allows grain boundaries to be assigned within the channel as different regions.Some important observations were made which are as follows:

- Ion/Ioff greater than 10^7 is achievable in both JL as well as IM devices.
- SS of JL devices is of high value than that of IM devices. Reason given in the paper is that as the JL device is turned off; the depleted channel region leads to an increment in the equivalent oxide thickness of the device.
- The increment in the On state current at a particular gate overdrive voltage in JL TFT is about 23 times than that in IM TFT.

In 2013; Horng Chin Lin et al. [8] proposed the N type JL planar polySi TFTs which have in situ heavily doped channel with Phosphorus as dopant atom. Following were the main findings of their research:

- They did the CV characterization of the device and found the fixed charge carrier density to be surprisingly negative. The main cause for this negativity is still under investigation but they said that perhaps setting apart of Phosphorus species at the channel oxide interface is the reason for this.

- They illustrated Reverse Short Channel Effect for ultra thin channel where there is increment in threshold voltage with the decreasing channel length value. This was named by them as the Reverse Vth Roll off phenomenon.

In 2013; Ya Chi Cheng et al. [10] compared the breakdown mechanism and the breakdown voltage of JL Poly Si TFT with the conventional IM TFT. The electrical properties of both the devices were presented at high voltage. These researchers came to following conclusions:

- Breakdown voltage of JL TFT is larger than IM TFT keeping the device size same. Hence JL TFT devices are suitable for high voltage power MOS devices and three dimensional stacked purposes.

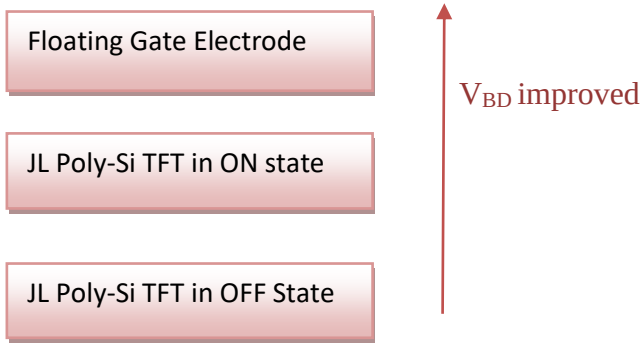


Fig. 2.4 Improvement in Breakdown voltage from Off to On state

- In ON state; the film of silicon can be considered as three resistances present in series where resistance of the channel differs from source/drain extension regions hence electric field is also different in these regions. In OFF state; channel is depleted and increment in drain voltage causes larger depletion than with the zero bias hence behaves similar to IM device.
- Floating gate electrode possesses the largest $V_{BD.}$

In 2014; P type raised source/drain JL TFTs with dual gate structure were analyzed by Ya Chi Cheng et al. Such structures can be used to adjust the threshold voltage to implement the multi threshold voltage circuit designs hence useful for further scaling applications. The temperature of these devices was also discussed for the electrical parameters such as SS and threshold voltage.[11]

In 2017, Chia Tsung Tso et al. proposed the behavior of JL devices with varying doping concentrations at different temperatures. They found that SS, DIBL and Vth; all depend on temperature in both JL as well as IM devices.[12]

In 2018, Jer Yi Lin et al. did a comparative analysis of Positive Gate Bias Stress reliability of JL TFT and IM TFT. They found that the degradation rates of threshold voltage in both the devices are different due to the different methods of transport and dissimilar electric fields created at same stress level.[13]

In 2018; Nianduan Lu et al. at Beijing; China described theoretically the compact models of TFTs with different active layers e.g. Poly-Silicon, Amorphous Silicon etc. Models based on surface potential were given special attention. These compact models act as a bond between the fabrication phase and the circuit design phase by capturing the device properties mathematically.[14]

2.3 Research Gap:

Above review of literature suggests that a lot of study work has been done on Junctionless Thin Film Transistors, specifically with Poly-Silicon material as the active layer. After studying the work done so far, the area which I feel has not been yet explored is the scalability analysis of Junctionless Poly-Silicon TFTs. There is a need to analyze the scaling effect on different parameters of the device which ultimately affect its operation. Also; I feel that a comparative performance analysis between different junctionless thin film transistors is needed as it is an area that has not yet been addressed adequately.

Chapter 3

JUNCTIONLESS POLY-SILICON THIN FILM TRANSISTORS

3.1 Introduction:

The evolution of low temperature polysilicon TFT has many advantages like reduced price of substrate, lower temperature for synthesis and an improved device resolution. And when this polysilicon TFT is made junctionless then it has the advantageous features of both: polysilicon as well as Junctionless device. It helps to get superior current drive capability and many similar benefits. This device has become quite popular in past few years. Different researchers have identified numerous benefits that are present in these devices and have modified them in different ways e.g. using dual gate structure etc. Previous works used nanowire channel and multiple gate configurations in order to enable the device to get turn off effectively i.e. their conduction can be stopped much easily; which is necessary for the Junctionless device to operate successfully.

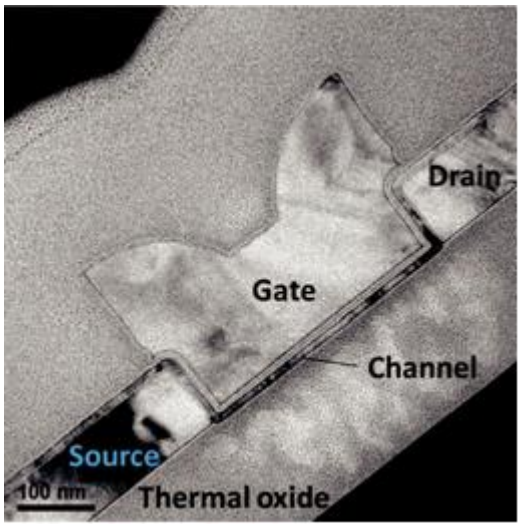


Fig 3.1 JL poly-Si TFT's cross-sectional TEM image having channel thickness equal to 10 nm, gate oxide thickness of 8.5 nm, and with channel length of 0.4 μm.[7]

3.2 Device Geometry & Simulation Parameters:

3.2.1 Device Fabrication:

LTPS is made by deposition of a-Si:H and then doing the process of crystallization of a by excimer laser annealing (ELA). This method has the ability to allow the a-Si:H to get crystallized without heating the substrate. Here, the fabrication of this device involves deposition of polysilicon using Low Pressure Chemical Vapor Deposition (LPCVD) with in-situ doping of phosphorus atoms. By such geometry this device operates in quite different manner than the conventional MOSFET. Polysilicon thickness of 12,10 and 8nm has been used to work as channel. Subsequently; deposition of a thick oxide of 8 nm thickness has been done to work as the gate dielectric. The doping concentration of 10^{19} cm^{-3} has been measured by the secondary ion mass spectroscopic method. After defining the gate electrode; CVD oxide has been deposited at 700 ^{0}C to serve as passivation layer for this device. By this process; the dopants present in the films get activated. After this; standard back end process has been performed and with this fabrication process is completed.

3.2.2 Device Geometry:

A heavily doped channel (doping concentration = 10^{19} cm^{-3}) with same type of doping as the source/drain is taken into consideration so that it can function as a junctionless transistor. Polysilicon channel thickness is taken to be low; here 8nm and a 8nm thick oxide is used as gate dielectric in the device.

3.2.3 Simulation Parameters:

- Simulation is done using Atlas Silvaco TCAD software (version: 5.19.20.R) which is a device simulator that can work in both:second as well as third dimension.
- The main command in simulation of TFT is the **defect** statement which is used for defining a continuous density of trap states present in silicon and the trapping cross-sections associated to it.

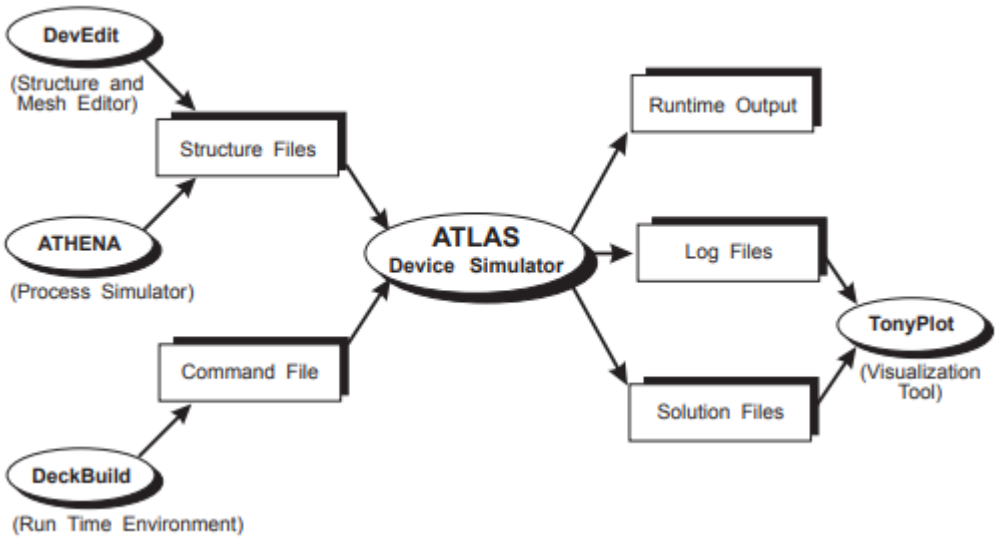


Fig 3.2 Inputs and Outputs of ATLAS Software [18]

- Structure Specification: Mesh, Region, Electrode, Doping
  - Firstly, we define mesh which is nothing but a series of horizontal and vertical lines with certain spacing existing between them.
  - Different materials are allocated different regions so that the device can be constructed. Three regions are taken here in current simulation: Buried oxide, Polysilicon channel, Oxide.
    Polysilcon channel thickness is taken 8nm.
    Gate Dielectric thickness is taken 8nm.
    W=1µm; L=10 µm

Region	Ymin	Ymax	Material
1	--	0	Oxide
2	0	0.008	Silicon
3	0.008	--	Oxide

  - After defining the regions; we specify the location of electrodes. Three electrodes: Gate, Source and Drain are defined. Gate, Source and Drain extends from x=5 to x=15, x=0 to x=2 and x=18 to x=20 respectively.
  - Doping=10^{19} cm-3 has been taken throughout the source, channel and the drain to make the device junctionless.
- Structure Specification: Material, Models, Contact, Interface
  - Polysilicon material is taken as the channel which has been specified by mobility values µn=300 cm^2/Vsec and µp=30 cm^2/Vsec.
  - Models used in simulation: temp=300, conmob (Concentration Dependent), fldmob (Parallel Electric Field Dependence), srh (Shockley-Read-Hall), auger.
  - Work function of the gate material is taken to be high i.e. 5.75

- Numerical Method Selection: Method: Newton
- Solution Specification: Log, Solve, Load, Save.
- Results Analysis: Extract, Tonyplot: Visualization is done on tonyplot which shows many features like plotting the structure and graph, overlay of multiple graphs to do comparative analysis, usage of functions which enable the user to define any new function and plot it, exporting the data etc.

3.3 Scalability Analysis - Simulation Results & Discussion:

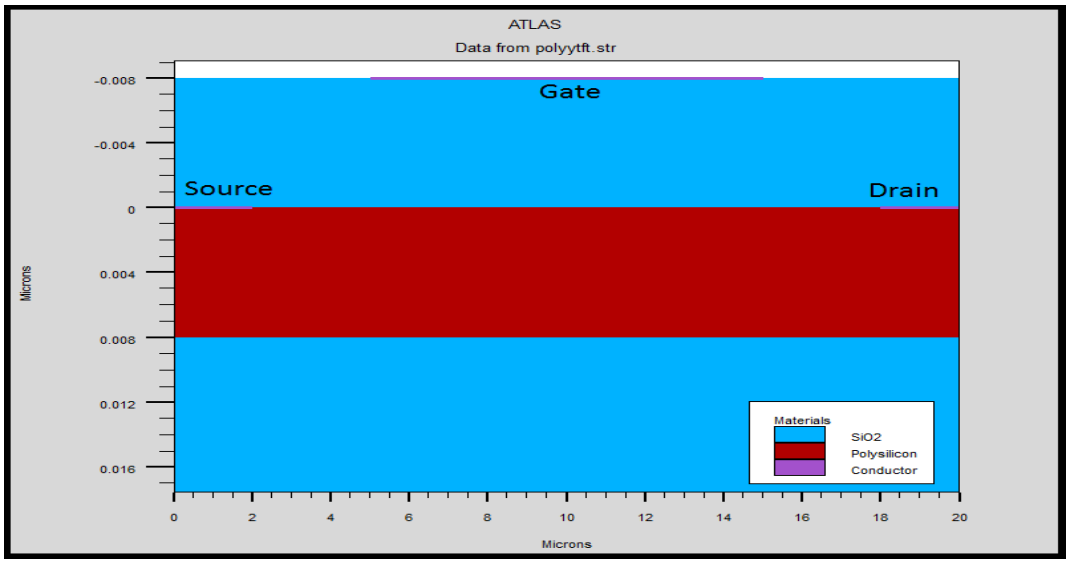


Fig 3.3 Junctionless Polysilicon Thin Film Transistor structure file

3.3.1 Sensitivity towards Channel Thickness:

- **Considering channel length of 10 µm:**Transfer characteristics is as shown:

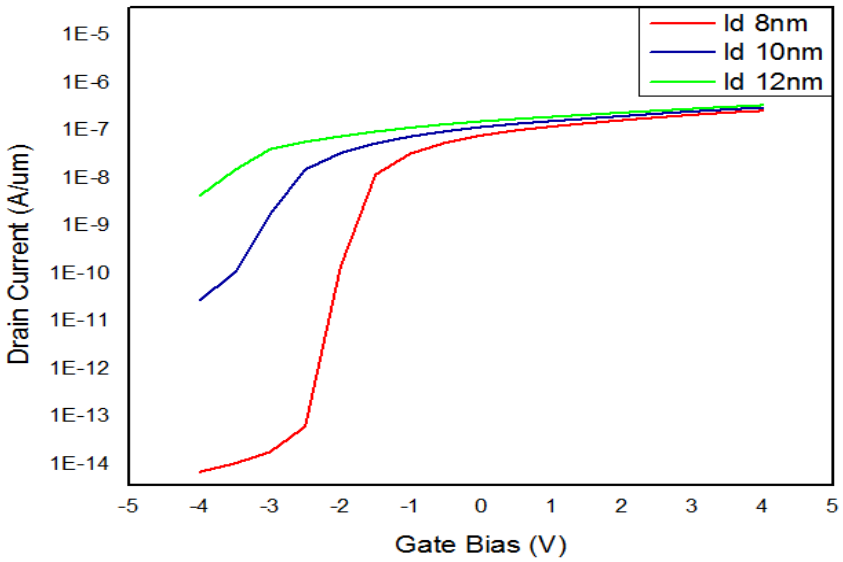


Fig3.4 Device's transfer characteristic for varying channel thickness

We observe that as the thickness of channel is increased, the threshold voltage of the device decreases considerably. This can be considered as a Reverse Vth roll off phenomenon with respect to the channel thickness instead of relying on the channel length. Hence switching property of the device is improved as channel thickness is increased because we know that; lower the Vth of the device; the more easily it gets turn on and is capable for conduction. So it can be very well said that Junctionless devices exhibit switching time to have a proportional relation with the threshold voltage. Also; we can conclude that the sub threshold slope of the device gets improved as we go on decreasing the channel thickness. Higher slope indicates higher speed of operation and lower power consumption. It is the maximum slope of the transfer characteristic. The inverse of it is the sub threshold swing which indicates the necessary V_G to increase I_D by one decade.

We know that Ion/Ioff current ratio is extracted from the Id vs. Vgs characteristic plotted on a semilog scale.

Ion/Ioff ~ 10^7 for channel thickness of 8nm

Ion/Ioff ~ 10^4 for channel thickness of 10nm

Ion/Ioff ~ 10^2 for channel thickness of 12nm

So we can say that Ion/Ioff ratio exceeds the value of 10^7 only when the thickness of the channel is reduced to 8nm or below that. It is justified also because we know that in general; Ion/Ioff current ratio is higher for a thinner semiconductor layer as well as short

channel devices. For applications like memory and display devices; Ion/Ioff ratio should necessarily exceed 10^6 value so we can say that lowering the channel thickness is a favourable condition for polysilicon junctionless TFT to be used in such areas of application.

- **Considering channel length of 0.4µm and channel width of 10µm**

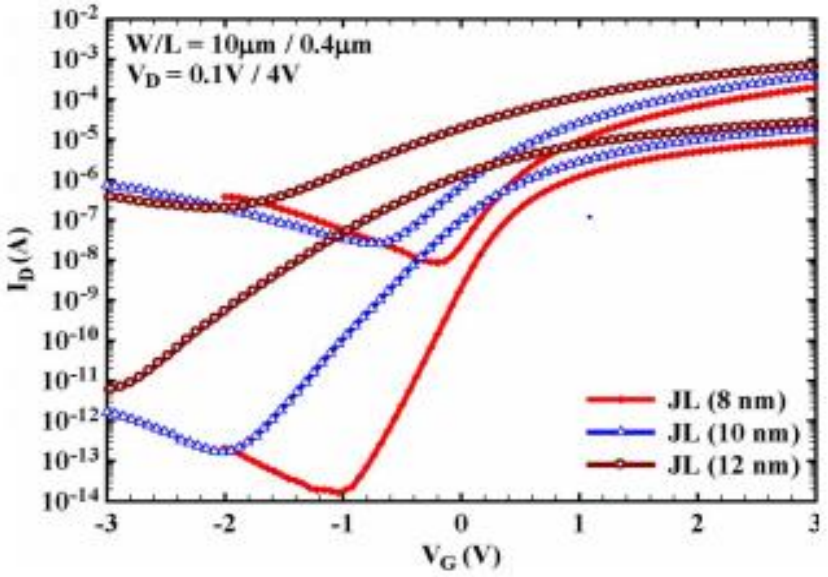


Fig 3.5 Transfer Characteristics considering channel length and channel width: both equal to 0.4 µm[8]

DIBL increases significantly when the thickness of the channel exceeds 10nm. At the same time; the off state leakage current rises dramatically as V_{DS} is incremented to 4 volt. This current is mainly because of drain leakage induced by the gate as we know that it has strong dependency on the difference between drain and gate voltage. Also, this current is much greater than the leakage current.

3.3.2 Sensitivity towards Channel Length:

If we study the transfer characteristics of the device at different channel length values say 10µm, 6 µm and 2 µm; we observe that threshold voltage is same for all lengths i.e. Vth = -2V but for VGS > Vth; the graphs move ahead in different manner and then intersect each other at V_{GS} =1.5V as shown. The graph at 10µm is almost linear whereas graphs at 6 µm and 2 µm are bent as shown.The degree of bending is greater for 2 µm than that in 6 µm. Hence the graph becomes more bent as the channel length is reduced.

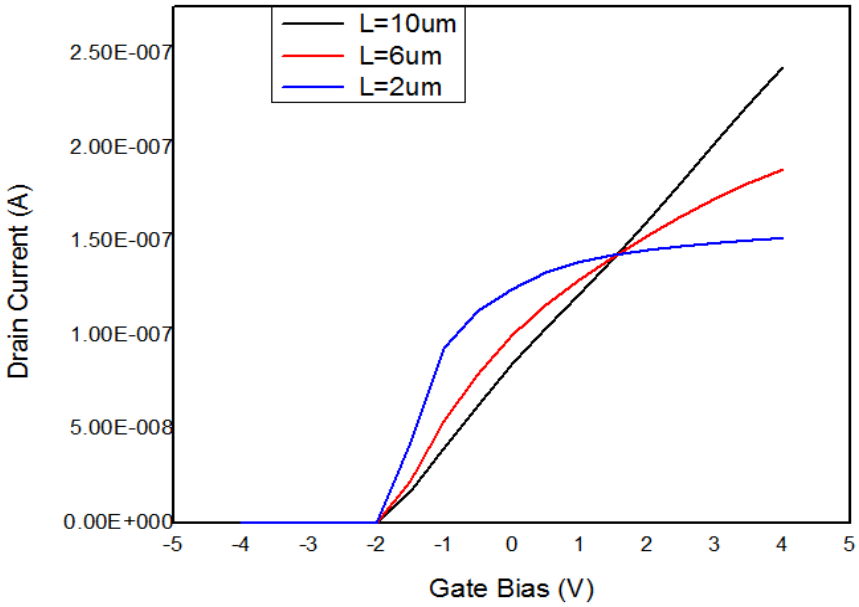


Fig 3.6 Typical transfer characteristics of the device for varying channel length

3.3.3 Impact of varying Channel Length on Device Transconductance:

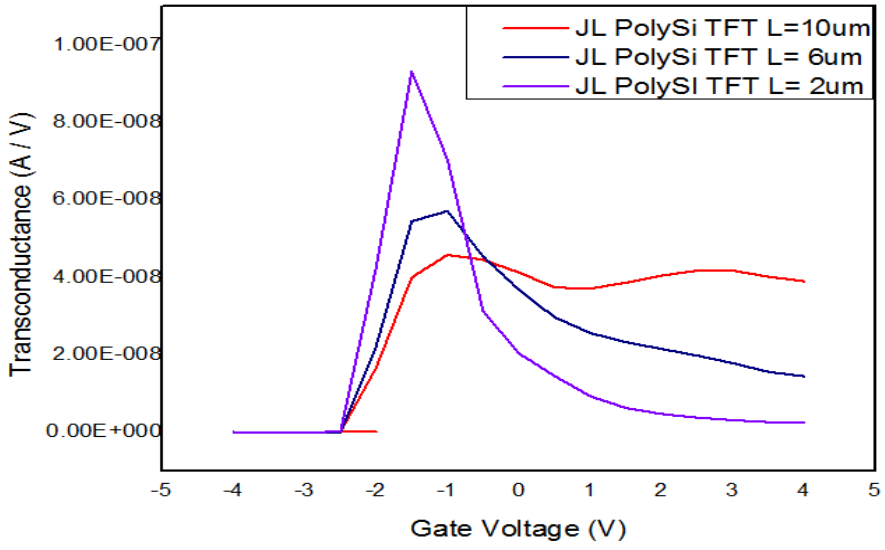


Fig 3.7 Impact of varying Channel Length on Device Transconductance

So we observe from above graph that transconductance has an inverse relation with the channel length i.e it increases with decreasing channel length. And we know that in

general, larger the transconductance figure for any device, the more is its power of amplification keeping all other factors constant i.e. it is capable of delivering more gain. So keeping that in mind we can say that device with lower channel length will be a better choice for amplification purpose.

3.3.4 Impact of Gate Bias on Channel Capacitance:

- **Capacitance-Voltage Characterization:**

This has been implemented under 1KHz frequency with the feature size that eliminates parasitic elements related to the S/D and test pads. The set up for this measurement has been kept same as illustrated in [16] where the bulk silicon substrate is at ground potential. It helps to find out the channel capacitance component per unit area. Below figure shows the typical C-V plot when device is operated at 1KHz with channel thickness of 8nm.

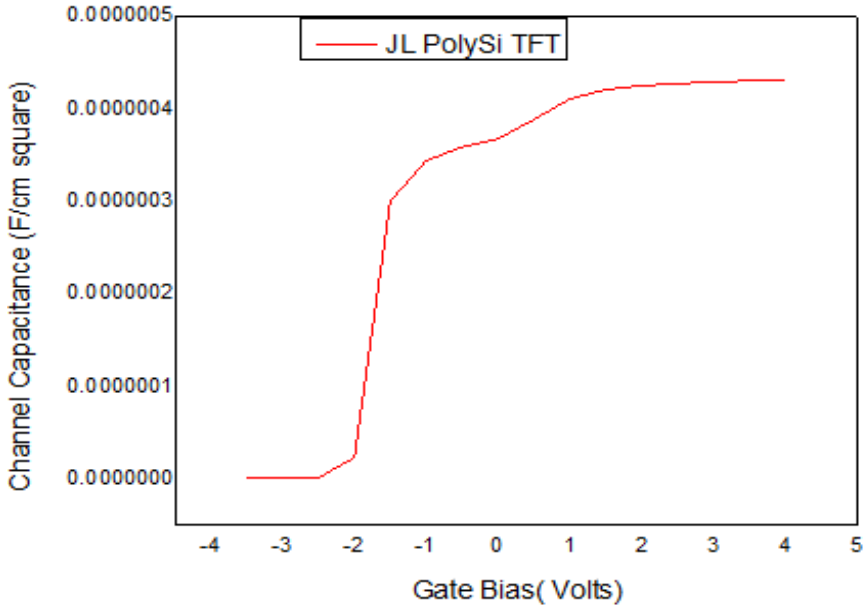


Fig 3.8 Channel Capacitance versus Gate Voltage for JL device keeping channel thickness 8nm

From above plot it can be said that the channel capacitance tends to saturate and gradually becomes constant as the gate bias becomes sufficiently large. This happens because electrons start accumulating at the interface between the gate oxide and the channel. The constant value of capacitance is nothing but the gate oxide capacitance per unit area. The saturation happens at gate voltage equal to or larger than the flatband

voltage. The measured capacitance can yield the value of oxide thickness. However as the gate voltage becomes lesser than the flatband voltage, a surface depletion region starts appearing at the channel surface. In that situation the net capacitance is equal to the series connection of gate oxide capacitance and the capacitance associated with the depletion region in the silicon channel.

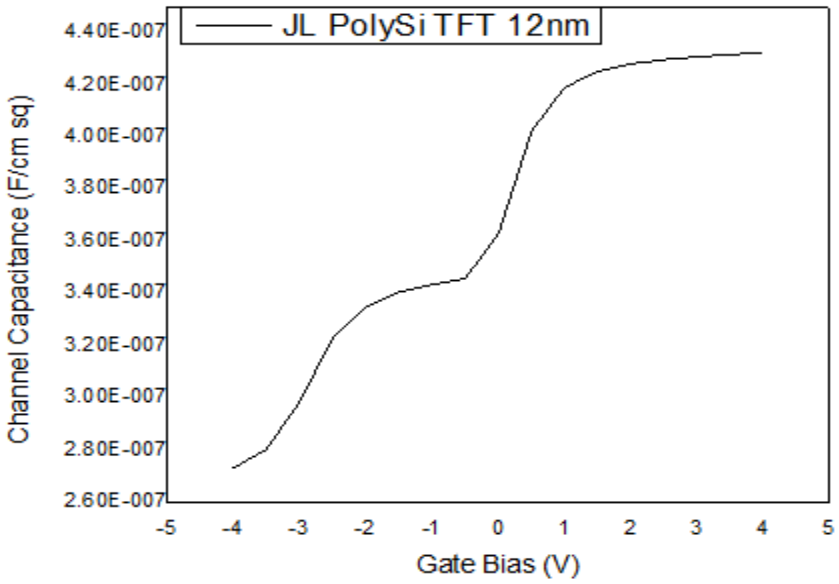


Fig3.9 Channel Capacitance versus Gate Voltage for JL device keeping channel thickness 12nm

3.3.5 Parameters Extracted from Capacitance Voltage Curves:

- **Determination of Flatband Voltage and Gate Oxide Capacitance per unit area:**

  Flatband voltage is one of the most important parameters of a thin film transistor because it has an influence on the threshold voltage of the device. Hence its precise and accurate measurement becomes quite important. It is nothing but the work function difference between the semiconductor and the gate material provided that the oxide charges and the charges at the oxide semiconductor interface are absent. Here; to determine the flatband voltage, we adopt an approach which is based on analysis of channel capacitance versus gate voltage characteristics. Therefore this method does not need knowledge of gap density of States and needs no fitting parameters.

  state

Channel Thickness	Extracted Flatband Voltage	Gate Oxide Capacitance per unit area (F/cm^2)
8nm	2.9 V	$4.25x10^{-7}$
10nm	2.6 V	$4.32x10^{-7}$
12nm	2.1 V	$4.39x10^{-7}$

Table 3.1 Parameters Extracted from Capacitance Voltage Curves

Hence V_{FB} is found in the range of 2.1 to 2.9 volts. We observe that as the channel thickness increases; the value of flatband voltage decreases whereas the gate oxide capacitance per unit area increases slightly. Smaller the flatband voltage; more is the ease with which we can get a flat energy band in that semiconductor.

Theoretically flatband voltage is given by the formula:

$$V_{FB} = \phi_{ms} - (Q_{ox}/C_{ox})$$

Where ϕ_{ms} is the contact potential difference

Q_{ox} is the effective charge in the dielectric

C_{ox} is the dielectric capacitance (F/cm^2)

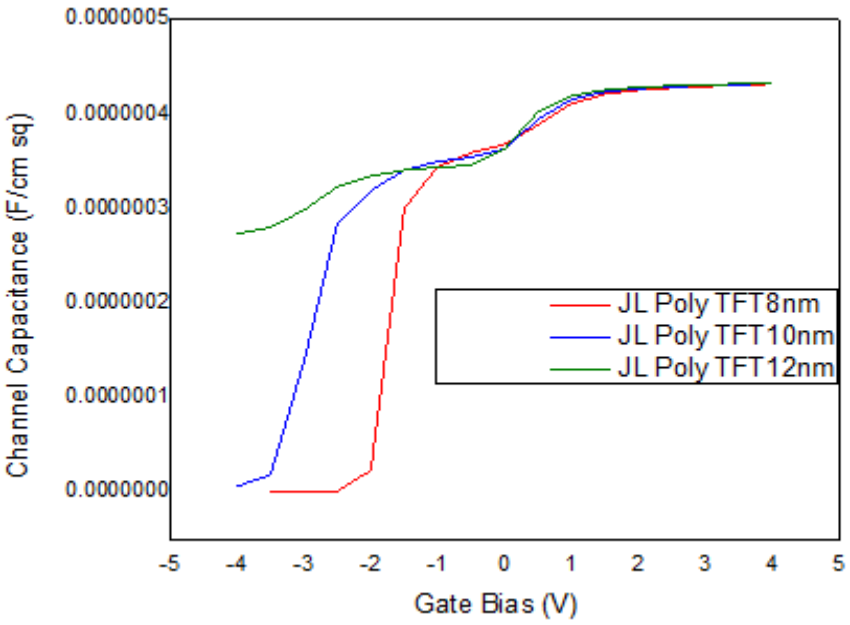


Fig 3.10 Overlay plot of Channel Capacitance with varying channel thickness

- **Determination of Oxide Thickness:** The oxide thickness can be easily found out from the constant Capacitance value obtained from the above Capacitance Voltage characterization. This is achieved by using the following formula:

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

Channel Thickness (nm)	Gate Oxide Thickness per unit area (F/cm^2)	Oxide Thickness(nm)
8	4.25×10^{-7}	8.12
10	4.32×10^{-7}	7.98
12	4.39×10^{-7}	7.86

Table 3.2 Determination of Oxide Thickness

So we observe that the oxide thickness values for each of the channel thickness values is lying in the range of 7.8 to 8.1 hence can be approximated to 8nm which is justified because the oxide thickness in the structure of our device was taken as 8nm.

Limitations of LTPS:

Large scale electrical uniformity is caused in LTPS due to grain boundaries present in the film.

Chapter 4

PERFORMANCE COMPARISON OF JUNCTIONLESS TFTs

4.1 Evolution of Semiconductor materials used in Thin Film Transistors: Thin film transistors can be made with many kind of materials. Interest in using TFTs in active matrix displays began in 1971.

Type of Semiconductor used	**Year of Development**	**Deposition Technology**	**Carrier Mobility ($cm^2V^{-1}s^{-1}$)**	**Description**
CdSe	1971	PECVD	40	High mobility but problems arise in processing on large scale
a-Si:H	1979	PECVD	1	Suited for large scale processing
Poly-Si	1996	a-Si : H deposition + laser annealing	100	High mobility
Organic	2000	Evaporation	0.1-30	Easy, transparent, cheap fabrication. Many semiconductor polymers.
IGZO	2004	Sputtering	10-20	Transparent material, high mobility.

Table 4.1 Evolution of Semiconductor materials used in Thin Film Transistors

Now a days, amorphous-oxide semiconductors are proving to be strong competitors to the existing a-Si:H because of their higher mobility value as compared to a-Si:H. At the same time; they can have a low tail states density in their conduction band.This makes them almost immune to the bias stress than a-Si:H. They also do not have electrical non-

uniformities like LTPS because of their structure being of amorphous nature and are also suitable to be used at low temperature.

Semiconductor	Electron Mobility ($cm^2/V \cdot s$)	Bias Stress V_T Shift (V)	Large Scale Uniformity	Transistor Type
a-Si:H	< 1	> 10	Good	NMOS
LTPS	$30 - 100$	< 0.5	Poor	CMOS
ZnO	$10 - 30$	~ 25	Poor	NMOS
a-IGZO	$10 - 20$	< 1	Good	NMOS

4.2 Comparative study of Amorphous and Polysilicon TFT: Polysilicon TFTs offer many advantages compared to the amorphous TFTs for application in AMLCD (Active Matrix Liquid Crystal Displays). Main reason behind this is that the carrier mobility values in polysilicon TFT are much higher than their amorphous silicon counterparts (almost by two orders of magnitude) therefore both n and p channel PolySi devices can be realised with much higher drive currents.[19] This high value of current is helpful in allowing TFTs of small size to be used as switching elements for the pixels, hence resulting in lower parasitic gate-line capacitance and higher aperture ratio for better display performance [20]. Also; integration of driver circuitry of lower power can be done well with the active matrix so that display module price is decreased and reliability can be improved.

4.2.1 Introduction to Amorphous silicon: Amorphous material possesses disordered nature hence some atoms present in it have a dangling bond. In physical aspect, these bonds represent defects in the continuous and random network and they cause abnormal electrical behavior. Unhydrogenated a-Si has a demerit that it shows high defect density which results in undesirable semiconductor properties such as poor photoconductivity and also resists doping which affects semiconductor properties. So, Amorphous silicon TFT is generally used in hydrogenated form. Hydrogen does the work of passivating it i.e. it cancels few existing dangling bond states. The passivation process is done by exposure of the film to hydrogen plasma at a temperature of about 300^{o}C or by H ion implantation.

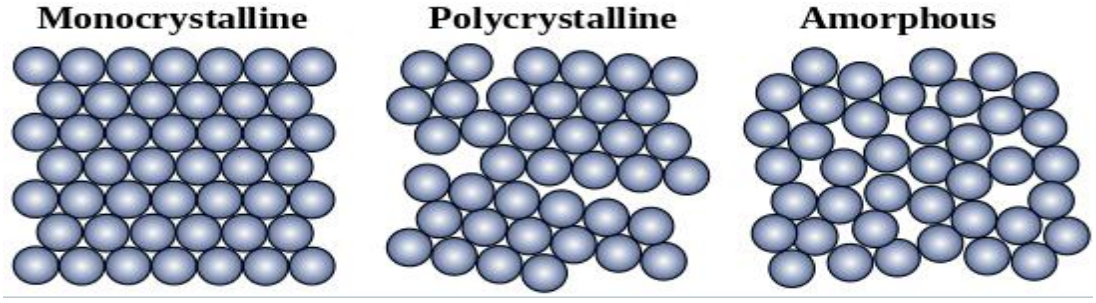


Fig 4.1 Schematic of allotropic forms of silicon: [22]

Main problem with polycrystalline material: Polycrystalline material is made up of many small crystalline domains which are joined together at the grain boundaries. The grains are the crystalline regions having atoms arranged periodically. These grain boundaries are the transition regions in which differently orientated grains attempt to align. This creates a disorderly arrangement of atoms and dangling bonds. The grain boundaries are the primary reason for polysilicon transistors to be inferior to devices fabricated in crystalline silicon because disorder at the grain boundaries presents a significant hindrance to channel conduction due to trap states at the grain boundaries. The traps seize the carriers, hence reducing the number of carriers available for current conduction. As a result, charge builds up at the trap location, causing a potential barrier.

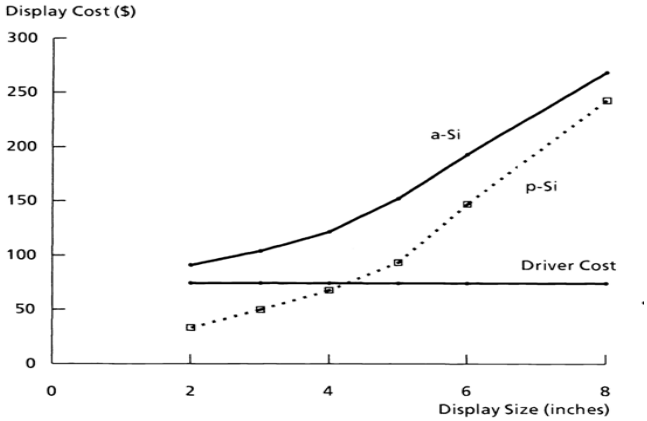


Fig 4.2 Comparison of cost as function of size for a-Si and p-Si AMLCDs[21]

Property	Polysilicon TFT	Amorphous TFT
Mobility	Larger mobility than amorphous TFT (almost by two orders of magnitude); therefore capable of high frequency operation and also helps to reduce the integrated driver areas.	Smaller mobility than polysilicon TFT hence generally used for low frequency operation.
Dimension	Dimension can be made smaller therefore results in high density, high resolution AMLCDs.	That is not the case with amorphous TFT.
Process Comparison	Requires two additional steps which are less mature and large area processes. These are namely Hydrogenation and Ion Implantation. So this TFT is difficult to produce.	Simpler process technology and also the process steps in amorphous TFT are more mature.

Required Fabrication Temperature	It can be categorized into two categories: a)Low temperature (600^{o}C): allows use of considerably cheaper glass substrates. b) High temperature(950^{o}C) :requires quartz substrate: offers higher current drive: costly therefore not preferred so we go for LTPS (Low temperature Polysilicon)	Requires lower fabrication temperature therefore it allows use of cheaper, low temperature substrates of glass. It can be deposited with PECVD below 350^{o}C.
Current Drive Capability	More current drive	Lesser current drive
Leakage Current	High leakage current. Remedy: use multi gate TFT.	Have lower intrinsic leakage.
Threshold Voltage Stability	The bias stress Vth stability is satisfactory for driving the OLED.	Bias stress threshold voltage instability is a major problem while using a-Si:H in the OLED displays. It has been seen that there is almost a 20 % change in the brightness if the driving TFTs have shft by 0.1 V in their Vth. Compensation circuits exist which are able to eliminate such errors .

Table 4.2 Differences between polysilicon and amorphous TFT

Parameters	**poly-Si TFT**	**a-Si:H TFT**
Switching TFT (W/L)	70µm/4µm	15µm/10µm
Driving TFT (W/L)	200µm/4µm	60µm/10µm
Mobility	0.56 cm^2/Vs	50-70 cm^2/Vs
Slope	0.68 to 0.76V/dec	0.50-0.59 V/dec
Vth	3.3V	1.7-1.9V
Ion at Vd=5V	>1x10-5 at Vg=15V	>1x10-4 at Vg=10V
Ioff at Vd=5V	<1x10-12 at Vg=-3.5V	<1x10-12 at Vg=-2.5V

Table 4.3 Characteristic Parameters of a-Si:H and polySilicon TFTs.[23]

4.2.2 Comparison on basis of the Transfer Characteristics: When comparing various TFT treatment combinations it is useful to look at the $I_D - V_{GS}$ transfer characteristics for a preliminary qualitative comparison and for a quantitative comparison parameter extraction from these measured transfer characteristics must be performed.

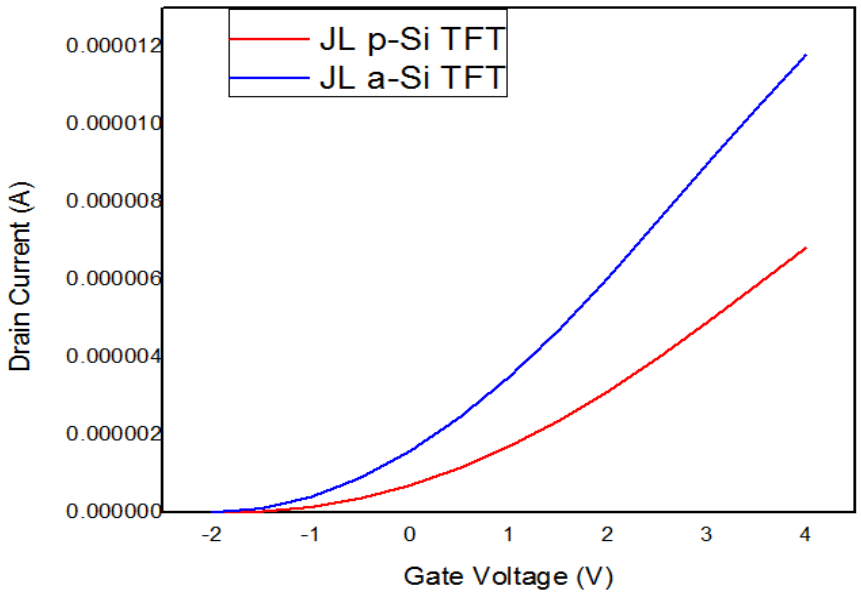


Fig 4.3 Transfer characteristics of Junctionless Polysilicon and Amorphous TFTs

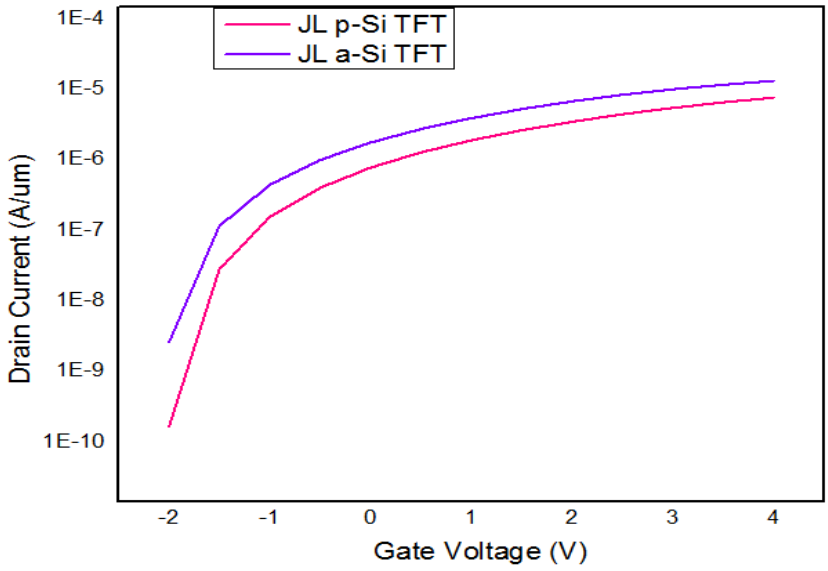


Fig 4.4 Transfer characteristics of JL Polysilicon and Amorphous TFTs on Semilog scale

4.2.3 Comparison on basis of Transconductance versus Gate Biasing:

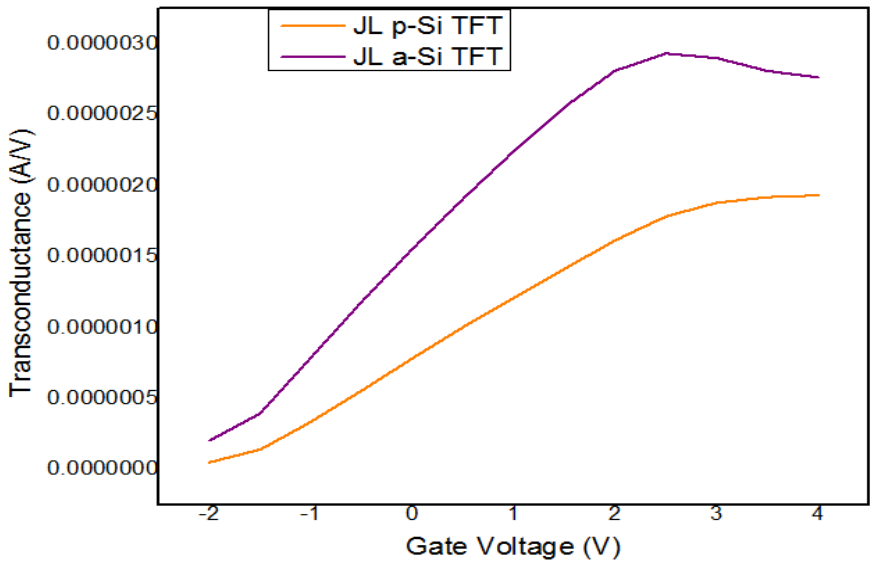


Fig 4.5 Transconductance comparison of JL Polysilicon and amorphous TFT

In the transfer characteristics of a FET, we know that transconductance is nothing but the ratio of variation in drain current to the corresponding variation in gate voltage over an arbitrary small but defined period. In general, larger the transconductance parameter for any device, the greater is its amplifying power keeping all other parameters as constant i.e. it is capable of delivering more gain. From above graph; Junctionless amorphous TFT gives a higher transconductance than its polysilicon counterpart.

4.2.4 Gate Bias Impact on Unity Gain Frequency:

fT is that frequency at which the short circuit current gain of TFT falls to unity value. This puts a limitation on the actual gain bandwidth product of amplifiers. Below graph suggests that fT rolls off quickly below the sub-threshold region. It also suggests that if the TFT is biased with a gate to source voltage much lower than that device's threshold voltage; then the cut off frequency decreases proportionally. Hence from the speed point of view in sub-threshold region; it is desired to have a less steep sub-threshold slope and bias the TFT with a gate to source voltage closer to the threshold voltage.

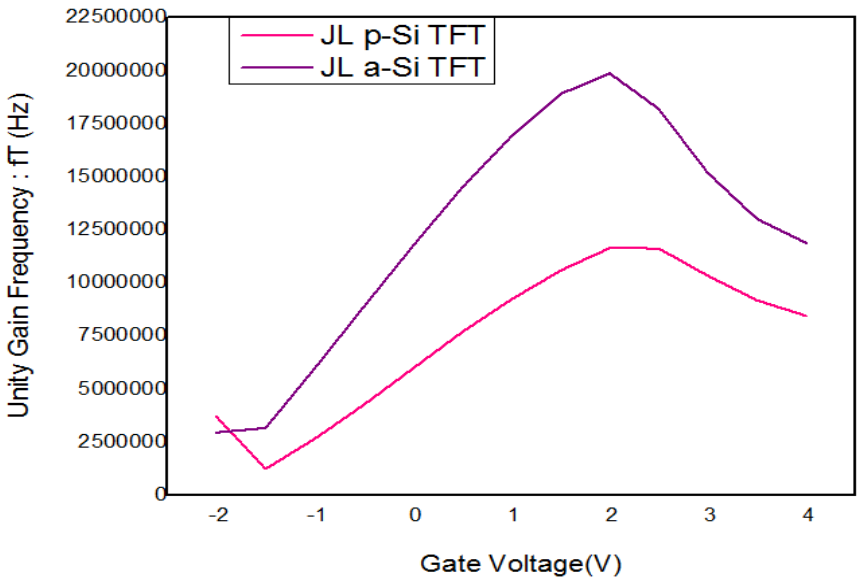


Fig.4.6 Gate Bias Impact on Unity Gain Frequency

4.2.5 Variation of the Overall Capacitance with the gate voltage:

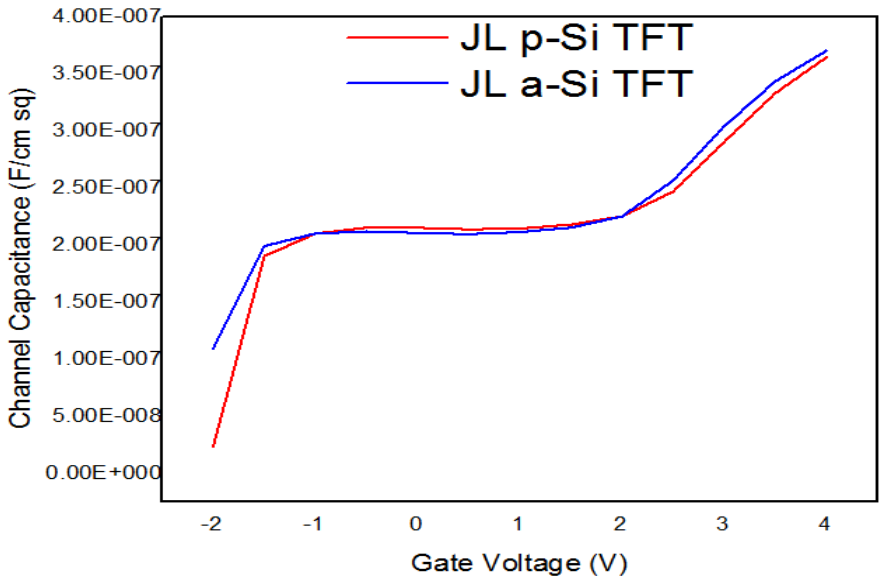


Fig 4.7 Gate Bias Impact on Channel Capacitance

Keeping frequency of operation to be 1MHz and V_{DS}=5V; we get above graph whose observation says that below subthreshold region and in the linear region i.e.after V_{GS}=2V, Junctionless amorphous thin film transistor possesses a slightly higher channel

capacitance value than its polysilicon counterpart. Both the curves remain in saturation mode upto V_{GS}=2V and then rise linearly with the increasing gate bias. During saturation; they almost show same value of constant channel capacitance.

Gate oxide capacitance per unit area = 2.2 x 10-7 F/cm^2

Flatband Voltage = -0.9 V

The flatband voltage i.e. the gate to source voltage required to obtain a flatband in the semiconductor is obtained as a negative value. So that means to obtain a flatband; we need to go below V_{GS}=0V.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion:

In this thesis, an attempt has been made to do the scalability analysis for N-type junctionless polysilicon TFTs which were composed of in situ heavy doping of same type throughout the source, channel and the drain. The impact of the major structural factors such as the channel thickness and length has been obtained on the characteristics of the device. The main conclusion drawn out from this analysis is that the polysilicon JL TFTs possess a high current drive capability which is a useful desirable property in any application. The CV characterization also revealed interesting features of the device such as the decrement of flatband voltage and increment in the gate oxide capacitance per unit area with the increasing channel thickness.

Secondly we have done performance comparison between the polysilicon junctionless TFT and its amorphous counterpart. It can be concluded from the obtained simulation results that even under similar operating conditions; Junctionless TFT behaves in a different manner if its active channel layer material is changed. Amorphous junctionless TFT exhibits higher value of transconductance and unity gain frequency than the corresponding polysilcon device at 1MHz operating frequency and at a high drain voltage of 5V. So we can very well come to conclusion that amorphous one will be more suitable for a high frequency operation. Results also reveal that their channel capacitance curves with respect to gate biasing are almost the same except at regions of subthreshold and in linear regions. The transfer characteristics of both the devices is also moving apart from each other as the gate bias is increased. So depending upon the requirement; we can select the material for the channel to get desired performance of the device.

5.2 Future work:

- Circuit implementation of these Junctionless thin film transistors can be done so that TFT integrated circuits can be designed that can act as gate drivers on LCD

panels in which we can adopt steps such as formation of current & capacitance LUTs, then developing corresponding Verilog A models and then do circuit simulation.

- RF analysis of the device is another domain of study that can be done in case of Junctionless TFTs.

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