FREQUENCY SWEEP AND WIDTH OPTIMIZATION OF MeMOS BASED DIGITAL LOGIC GATES

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for the degree of Master of Technology

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by

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(2017PEV5210)

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June 2019

Certificate

Department of Electronics & Communication Engineering

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This is to certify that the thesis work entitled " **FREQUENCY SWEEP AND WIDTH OPTIMIZATION OF MeMOS BASED DIGITAL LOGIC GATES**" has been carried out by **Rajveer Mali** for the degree of Master of Technology in VLSI Design at Malaviya National Institute of Technology under my supervision.

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Prof. Lava Bhargava

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Declaration

I declare that,

1. the thesis comprises my original work towards the degree of Master of Technology in VLSI Design at MNIT and has not been submitted elsewhere for a degree.
2. due acknowledgement has been made in the text to all the material used.

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Abstract

Memristor is a fourth class of fundamental circuit element proposed by Leon Chua in 1971. Chua found out the missing link between flux and charge and reasoned that there should be another fundamental circuit element called Memristor. Memristor is a resistor with memory. The resistance of memristive devices directly depends on the amount of charge passing through the device.

In 2008, Strukov et al. developed physical memristor, which consists of a thin film of titanium dioxide sandwiched between two platinum electrodes, which shows the pinched hysteresis I-V curve at the nanometer scale.

Memristive Devices (MD) are electrical devices which have many applications, including logic design, memory devices, and neuromorphic systems. MD is lucrative due to its non-volatility, no leakage current, better scalability and compatibility with CMOS. Here we have shown the effect on current-voltage hysteresis curve by varying frequency, threshold voltage and dimensions of the device. MeMOS(Memristor metal oxide semiconductor) based digital logic gates are designed and simulated in this thesis. We are using voltage threshold adaptive memristor (VTEAM) model in cadence virtuoso. MeMOS based design leads to a reduction in the die area as compared to conventional CMOS.

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Abbreviations

VTEAM	**V**oltage **T**hreshold **A**daptive **M**emristor
TEAM	**T**hreshold **A**daptive **M**emristor
DRAM	**D**ynamic **R**andom **A**ccess **M**emory
RRAM	**R**esistive **R**andom **A**ccess **M**emory
NIL	**N**ano **I**mprint **L**ithography
MD	**M**emristive **D**vices
NVRAM	**N**on **V**olatile **R**andom **A**ccess **M**emory
MIM	**M**etal **I**nsulator **M**etal
TiO_2	**T**itanium **D**ioxide

Symbols

ϕ	flux
q	charge
μ	average ion mobility
G	device conductance

Chapter 1

Introduction to Fundamental Circuit Elements

1.1 Origin of the Memristor

The memristor is known as the 4th class of fundamental circuit element. Earlier, there exist three circuit elements, which are resistor, capacitor and inductor. Professor Leon Chua in 1971 gave the relationship among all the four cornerstones of a network system, i.e. current(i), charge(q), voltage(v) and flux(ϕ). The author found symmetry among all these four cornerstones. Furthermore, he found the conclusive evidence of such symmetry and suggested memristor as a missing link between flux and charge. He also presented the mathematical equations and circuit implementation on the breadboard. The relationship between fundamental elements is shown in Figure 1.1.

HP Labs in 2008, build the device in nanometer scale, which has the same characteristic as Chua postulate in 1971. The device is made up of titanium dioxide.

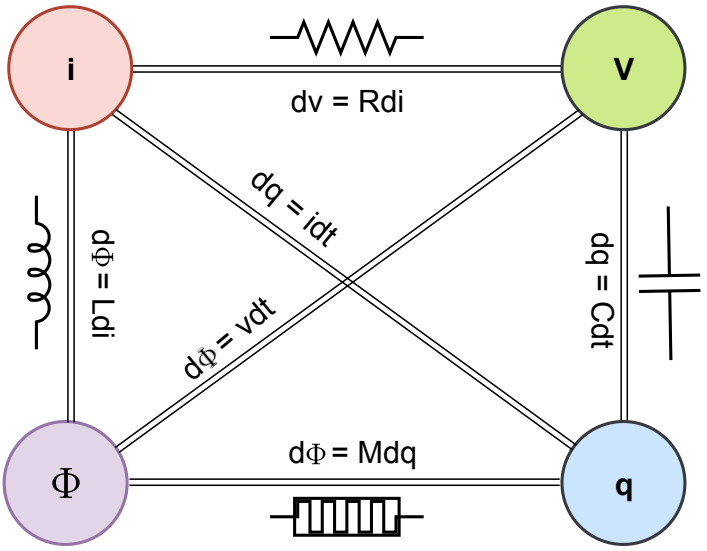

FIGURE 1.1: Relation between four cornerstones of network system

1.2 Literature Survey

Leon Chua in 1971 [1] presented the mathematical modeling of four key circuit variable. In his paper, he concluded that there is a missing link between charge & flux. He named this element as Memristor. Memristor stand's for memory resistor. He also developed memristive circuit on the breadboard and postulated memristor device characteristics and properties.

In 1976 Kang and Chua [19] gave a detailed analysis and properties of the memristor. They concluded that the most salient feature of the memristor is it's zero crossing property. They observed that the memory effect which causes phase shifts in the conventional system, memristive systems are free from phase shift problem that arises in dynamic regime. The output of memristive system remains zero until we are not applying any energy source. The Lissajous pattern, which is drawn by them between input and output, always passes through the origin. As frequency approaches towards infinity, the Lissajous pattern shrinks to a linear curve.

Strukov et al. [2] in 2008 developed the 1st working prototype of the memristor as postulated by Chua in 1971. They revealed the titanium dioxide based two terminal device sandwiched between two platinum electrode. The MD shows the same properties and characteristics as Chua postulated. They also proposed mathematical device modeling

equations known as Linear ion drift model which assumes the doped and undoped regions as two series resistance.

J.J. Yang et al. [3] in 2008 demonstrated the switching dynamics in metal-insulator-metal based structure. In this paper, they provide experimental testimony to confirm the generic model of memristive switching in the oxide. They built the titanium dioxide based device, which shows fast nonvolatile switching.

M. D. Pickett et al. [16] in 2009 showed the mathematical definition of memristive devices that presents the framework for understanding the physical procedures needed for bipolar switching. They also yield formulas which can be utilized to calculate and estimate the important features(dynamical & electrical) of the design. The analysis unveiled an essential property of nonlinear memristors, i.e. energy needed to switch a metal-oxide device decreases exponentially with the rising current.

N. Hackett et al. [20] in 2009 illustrated a rewriteable, nonvolatile and physically flexible memristor device capable of low-power operation. The active component of the device is cost effective as it is fabricated at the normal temperature(27 °C) by whirling a titanium dioxide sol-gel on a polymer sheet. This device shows behavior like memory and is compatible with the memristor, illustrates the ON/OFF ratio exceeding 10000 : 1, is nonvolatile for about 1.210^6s (14days), needs less than 10V, & operational even after being physically bent more than 4,000 times. Inside view of flexible TiO_2 device structure is given in Figure 1.2.

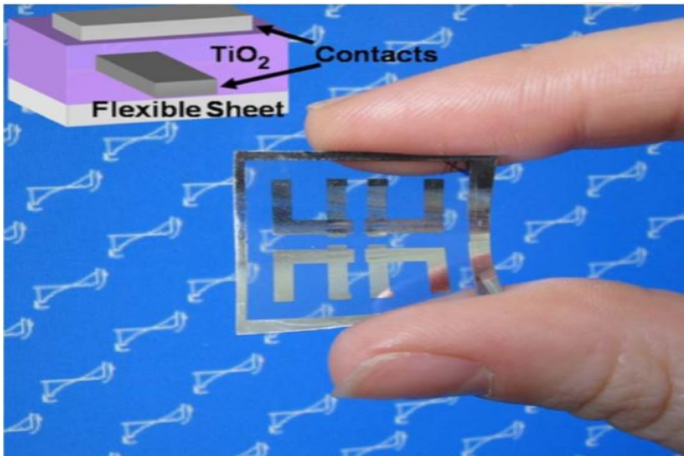

FIGURE 1.2: Flexible polymer sheet [20].

S. Kvatinsky et al. [4] in 2013 presented another model which overwhelm the problems of Simmons barrier model. This model offers a simple expressions rather than a complex equations. This model exhibits identical physical behavior compared to the tunnel barrier model.

S. Kvatinsky et al. [18] in 2015 observed that the computational efficiency and accuracy of VTEAM model lies below 1.5% in terms of relative RMS error. This model is the extension of the TEAM model that couples various benefits of threshold voltage rather than the threshold current. I have used this particular model to characterize and design logic in my thesis.

1.3 Problem Statement

There are various memristor models. Among them, some does not have a threshold, so that the variation in memristance arises for any applied current and voltage. Based on the experimental data, in the practical MD, the existence of threshold voltage instead of the threshold current was found. It is observed that the computational efficiency and accuracy of VTEAM model is less than 1.5% in terms of relative RMS error [18]. This model is the expansion of the TEAM model [4], which couples numerous benefits of threshold voltage rather than the threshold current.

1.4 Objective

The objective of this work is to design one-bit logic gates (AND, OR, NAND, NOR) using VTEAM model, which is the voltage threshold based memristive model. To achieve this work, I have used cadence virtuoso.

1.5 Outline

This thesis started with an introduction of the fundamental circuit element(chapter 1), which consists of a literature survey. Chapter 2 gives the brief information about memristor in this we are discussing memristor properties, different definitions of memristor and switching mechanism occurred in the memristor. Chapter 3 starts with the basic introduction, and it consists of different proposed memristive models and window function. In Chapter 4, we are discussing applications of the memristor. Chapter 5 consists of simulation results which are done in the cadence virtuoso. Chapter 6 consists of conclusion and future work.

Chapter 2

Memristor: At a Glance

2.1 Introduction

In this chapter, we discussed several definitions, switching mechanism and the properties of the memristor are explained.

2.2 Definition of Memristor

Memristor stands for "memory resistor". It is a two-terminal passive device. Magnetic flux is associated with the quantity of charge passed through the device [1]. Since memristor is a passive element, it cannot dissipate or store any energy. Figure 2.1 represents the memristor symbol given by Chua.

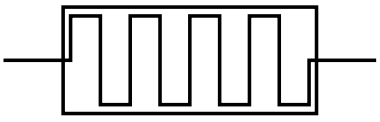

FIGURE 2.1: Memristor symbol

Flux as a function of charge(2.1) illustrate that flux is controlled by charge flow and charge as a function of flux(2.5) means the charge is controlled by flux.

For charge controlled memristor,

$$\Phi = F(q) \tag{2.1}$$

Dividing equation(2.1) we get:

$$\frac{d\Phi}{dt} = \frac{dF(q)}{dq} \cdot \frac{dq}{dt} \tag{2.2}$$

As $V(t) = \frac{d\Phi}{dt}$ and $i(t) = \frac{dq}{dt}$ equation 2.2 can be rewritten as:

$$V(t) = (M(q)) \cdot (i(t)) \tag{2.3}$$

Here M(q),

$$M(q) = \frac{dF(q)}{dq} \tag{2.4}$$

$M(q)$ represents memristance, having the same unit as a resistor(Ω). similarly, we can write flux controlled memristor as,

$$q = F(\Phi) \tag{2.5}$$

Dividing equation(2.5) we get:

$$\frac{dq}{dt} = \left(\frac{dF(\Phi)}{d\Phi}\right) \cdot \left(\frac{d\Phi}{dt}\right) \tag{2.6}$$

As $V(t) = \frac{d\Phi}{dt}$ & $i(t) = \frac{dq}{dt}$ (2.6) can be rewritten as:

$$i(t) = (G(q)) \cdot (V(t)) \tag{2.7}$$

Here,

$$G(\Phi) = \frac{dF(\Phi)}{d\Phi} \tag{2.8}$$

$G(\Phi)$ is known as memductance; it has the units of Siemens similar to conductance.

2.3 Memristance

Memristance illustrates the functional link between magnetic flux & charge [1]. The resistance of the memristor will increment when the charge courses through the memristor one way & diminishes when the flow streams the other way. If there is no power, means there is no input to the device, the memristance freezes. If power gets back ON; the memristance starts precisely from where it was switched OFF.

2.4 Memristor Properties

2.4.1 Relation between Flux and Charge

The relationship between $\Phi - q$ is shown in Figure 1.3. The charge & flux increase monotonically. The slope of this curve represents the memristance. To achieve a passive condition, it is important that resistance has a non-negative value($M(q) \geq 0$). Therefore, the memristance has always a positive value to act as a passive element. The instant power is provided by:

$$P(i) = \{M(q)\} \cdot \{i(t)\}^2 \tag{2.9}$$

As the dissipated power is positive, memristor acts as a passive device and it does not store energy.

2.4.2 Relation between Current and Voltage

The crucial characteristic which makes memristive devices unique is its pinched hysteresis loop. When we are applying sinusoidal current to the memristive devices, the device exhibits a hysteresis curve. As the input voltage reaches zero, the output current also becomes zero. This results in the pinched hysteresis curve passing through the origin. The shape of this curve completely depends on source frequency. If frequency moves towards infinity, the curve shrinks and shows the characteristic of a resistor.

2.4.3 Swithing Mechanism in Memristor

As we apply inputs(current or voltage) to the memristor, dramatic change in memristance occurs. Because of this, the memristor can be use as switch. We assume the voltage to be constant in order to determine the energy dissipation during a signal switching event. Hence the energy dissipation during switching of memristor form R_{OFF} to R_{ON} is given by:

$$E_{switch} = \int P_{switch} = \int \frac{v^2}{R(t)} dt = v^2 \int_{t_{OFF}}^{t_{ON}} \frac{dt}{M(q(t))} \tag{2.10}$$

Putting $dq = idt$, (2.10) can be written as:

$$E_{switch} = v^2 \int_{q_{OFF}}^{q_{ON}} \frac{dq}{I(q)M(q)} \tag{2.11}$$

Inserting $v = i(q)M(q)$ and $\int \frac{dq}{v} = \frac{\Delta q}{v}$ gives:

$$E_{switch} = v^2 \int_{q_{OFF}}^{q_{ON}} \frac{dq}{v(q)} = v.\Delta q \tag{2.12}$$

where $\Delta q = q_{ON} - q_{OFF}$. Δq is the change in charge required to switch a memristor from R_{on} to R_{off}.

As the MIM systems show the resistive switching, these are used as non-volatile memories. The oxides, chalcogenides and organic compounds can be utilized as insulator in the MIM structure. All the metals & the non metals(which are conductor) can be used as a metal for the MIM structure.

Waser & Aono [21] proposed that the switching in MIM based structure can be classified in two types:

- Unipolar: Switching process does not depends on current and voltage polarity.
- Bipolar: Switching process depends on current and voltage polarity. ON and OFF switching occurs on different polarities of current and voltages.

Figure 2.2 shows the unipolar and bipolar switching curves.

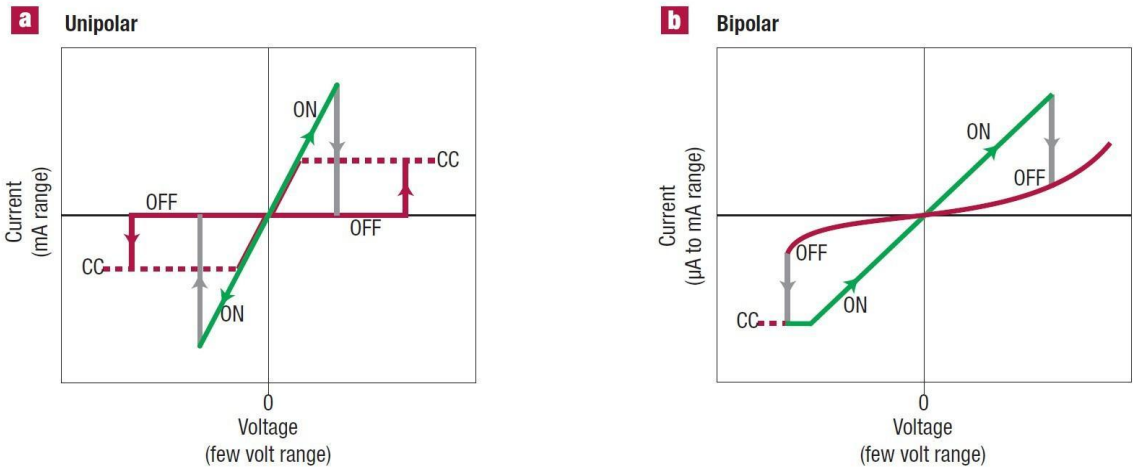

FIGURE 2.2: (a) Unipolar switching (b) bipolar switching curve

2.4.3.1 Thermal Switching

In thermal switching, the material is modified in a discharge filament using Joule heating, and the switching is uni-polar. The fragile conductive filament with regulated resistance is created due to the compliance current. This process of switching is sometimes called the mechanism of fuse-anti-fuse. It is because the filament will thermally disrupt in the reset phase owing to the elevated power density of about $1012W/cm^3$.Titanium dioxide may indicate bipolar switching features, but it may show unipolar switching features if the compliance current is high enough.

2.4.3.2 Electronic Switching

The other method for switching is electronic injection of charge. Charge injection in the structure is exerting through the tunneling process, and the charges are confined in the defective sites. The device gets switched ON when these confined charges scattered over the insulator which causes decrement in device resistance. The movement of ions and redox reaction causes bipolar switching, which is illustrated in detail [21].

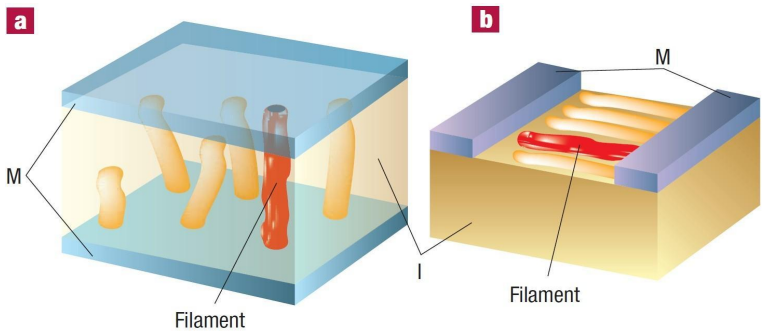

FIGURE 2.3: formation of filament in the switching(a) vertical (b) horizontal

2.4.3.3 Ionic Switching

Ionic switching MIM system depends on reducing metal cations in ionic conductors, because metal atoms have been converted into cathode in conjunction with inactive substances. This illustration is referred to as cation migration. The ON state is accomplished when a filament that leads to anode is produced by the decreased metal cation. This develop a low resistance path between cathode and anode which acts as ON state. If we are changing the bias voltage, the filament boundary is dissolved. In order to anion migration, oxygen vacancies cause oxygen ion defects, which results in bipolar switching in the metal oxide.

2.5 Switching Speed

In case of memristor, OFF switching is slower than ON switching [24]. This is due to distinct currents of diffusion & drift. The diffusion current is triggered by variation in a concentration gradient, or we can say that vacancies flow from TiO_{2-x} to TiO_2 within the device, while drift current is developed due to the internal electric potential. When we are applying positive voltage to the memristor, diffusion and drift occurs in the opposite

direction while in another case (on applying negative supply) diffusion & drift currents are on the same direction.

Chapter 3

Memristor Modeling and Characterization

3.1 Introduction

Memristive system(MS) exhibits the variable resistance characteristic which depends on the internal state variable. MD are non-volatile in nature. The state variable W should show non-linear dependence on the charge to provide non-destructive reading and writing.

To store the boolean logics(0/1), MD should have a high ratio of OFF to ON resistance (i.e, $R_{OFF} >> R_{ON}$). There are several characteristics such as low power consumption, better scalability & compatible with CMOS technology, which are essential for memristor device.

To design and analyse MD based circuit and applications, we require an excellent memristor model. There are different type of memristive models and window functions which are discussed in the later part of this chapter.

3.2 Models

To analyze and simulate the memristor based circuits, we require an excellent model which can satisfy the practical memristive properties. After the discovery of memristor by Strukov et al. in May 2008, several models have been proposed [11]. Different memristor models are explained as follows:

3.2.1 Memristor Linear Ion Drift Model

It was the first memristor model proposed by Strukov et al. in May 2008. This is based on the memristor's physical structure. This model assumes that MD consists of two sections. One section is doped by oxygen vacancies (contains positive oxygen ions) and other remains undoped as in figure 3.1. The net resistance of MD is given by the resistance created by the dopped and undoped region [17]. The undoped segment has large resistance while low resistance is found in the doped region. This model has assumed uniform electric field, ohmic conductance, linear ion drift & oxygen ion having same average ion mobility μ_v. The memristor model created by HP lab in 2008 is shown in Figure 3.1. On applying

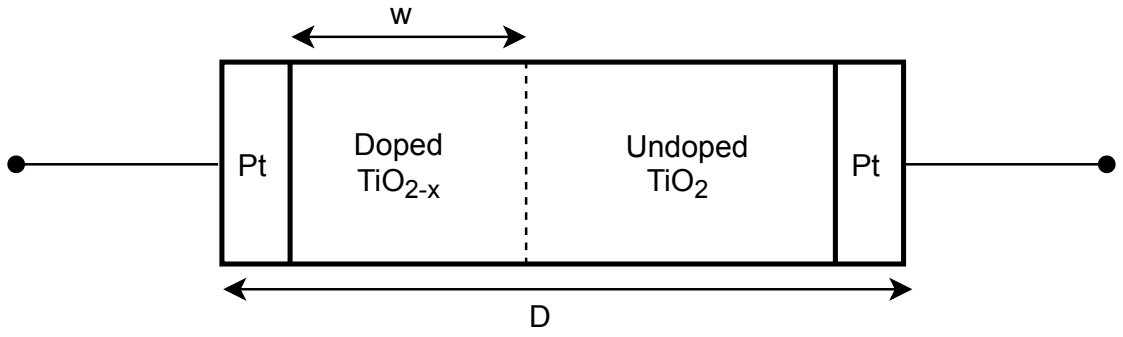

FIGURE 3.1: Equivalent circuit of memristor [2]

supply voltage, the internal state variable moves in between the undoped & doped region [13]. The voltage across the device is given by:

$$V(t) = \left(R_{ON} \cdot \left(\frac{W(t)}{D}\right) + R_{OFF} \cdot \left(1 - \left(\frac{W(t)}{D}\right)\right)\right) \cdot i(t) \tag{3.1}$$

where $W(t)$ is the state variable which depends upon the amount of charge passed through the device in time t. R_{OFF} and R_{ON} are the OFF & ON resistance respectively, and D is the device dimension.

The movement of an state variable $W(t)$ between the doped & undoped region is represented as $\frac{dW(t)}{dt}$.

$$\left(\frac{dW(t)}{dt}\right) = \mu_v \cdot \left(\frac{R_{ON}}{D}\right) \cdot i\,(t) \tag{3.2}$$

On integrating, we get

$$W(t) = \mu_v \cdot \left(\frac{R_{ON}}{D}\right) \cdot q\,(t) \tag{3.3}$$

inserting (3.3) in (3.1), yields the memristance as:

$$M(q) = R_{ON} \cdot \left(\frac{\mu_v R_{ON}}{D^2}\right) \cdot q(t) + R_{OFF} \cdot \left(1 - \left(\frac{\mu_v R_{ON}}{D^2}\right) \cdot q(t)\right) \tag{3.4}$$

As $R_{OFF} >> R_{ON}$. This expression is written as

$$M(q) = R_{OFF} \cdot \left(1 - \left(\frac{\mu_v R_{ON}}{D^2}\right) \cdot q(t)\right) \tag{3.5}$$

Figure 3.2 represents I-V curve using linear ion drift model. It is simulated in cadence by taking model parameters D=10nm, $R_{ON} = 100\Omega$, $R_{OFF} = 16k\Omega$, $\mu_v = 10^{-14} m^2 s^{-1} V^{-1}$,$W_0 = 1 Rad/s$. Figure 3.2(a) represents I-V curve for sinusoidal input.Figure 3.2(b) shows I-V curve for pulse input.

In linear ion drift model, it is contemplated that oxygen vacancies have the autonomy to move along all width of the MD. Research reveals that the drift of oxygen vacancies near the boundary interfaces is not linear.

To render a solution for the above-reported predicament, window functions are introduced.

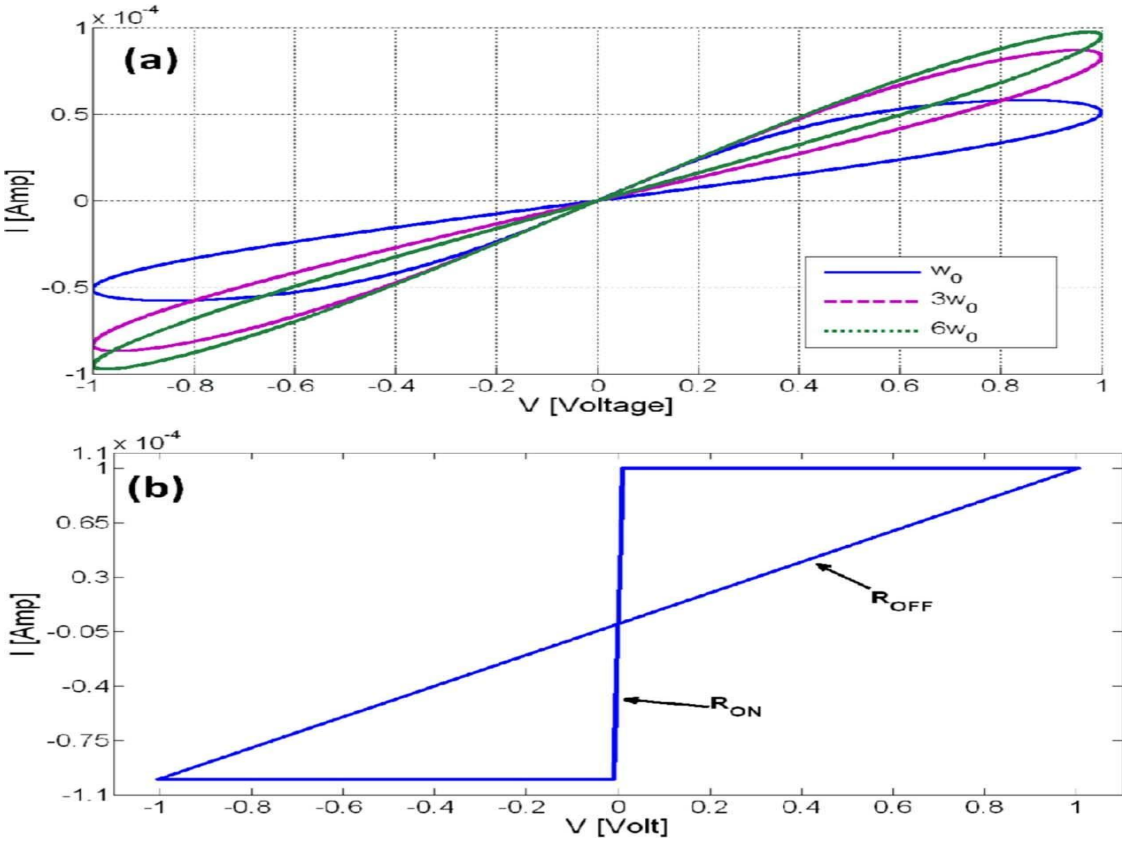

FIGURE 3.2: Linear ion drift I-V curve [2]

3.2.2 Window Function

To render non-linearity to boundary problems, window function is introduced, as shown below:

$$\left(\frac{dW(t)}{dt}\right) = \mu_v \cdot \left(\frac{R_{ON}}{D}\right) \cdot i\,(t) \cdot F\,(W) \tag{3.6}$$

function $F(W)$ represents the window function. An adequate window meets the following prerequisites for modelling of nonlinearity.

- The boundary condition should be taken into account at the bottom & top electrode of the device.
- Across the whole operating area of the device, the function shall provide nonlinear behavior.
- The function involves controlling parameter to establish the model.

3.2.2.1 Joglekar's Window Function

Wolf introduces this window function in 2009 [7]. They attached a fitting parameter 'p' in order to restrain the linearity & nonlinearity of the function $F(W)$.

$$F(W) = \left\{1 - \left(\left(\frac{2W}{D}\right) - 1\right)^{2p}\right\} \tag{3.7}$$

Here p represents the control parameter. p is responsible for the flatness of the curve $F(W)$ around its peak value at $\frac{W}{D} = 0.5$. p is a +ve number. The modified state change

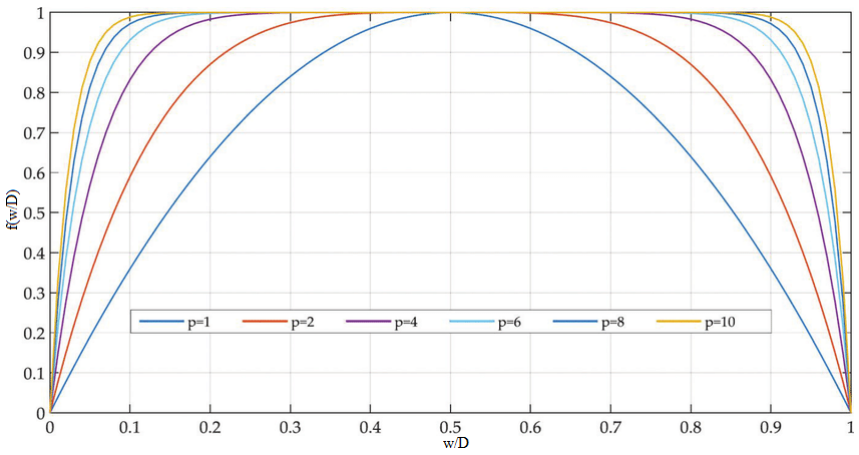

FIGURE 3.3: Joglekar window function for distinct p values [7]

equation is obtained by putting equation 3.7 in equation 3.6.

$$\frac{dW(t)}{dt} = \mu_v \cdot \left(\frac{R_{ON}}{D}\right) \cdot i\,(t)\left[1 - (\frac{2W}{D} - 1)^{2p}\right] \tag{3.8}$$

The real disadvantage of this window function is the stuck state of the state variable 'W' at the boundaries, and it is difficult to alter the window function at the boundaries due to the zero value at both corners.

Nonlinear drift enigma is resolved in this window function, but the border lock is not regarded.

3.2.2.2 Biolek's Window Function

Joglekar's window function manifests a significant difficulty for modeling the practical MD's because the derivative of internal state variable is forced to zero and device status is not changed if it reaches one of it's bounds. Biolek et al. [8], [12] in 2009 revealed another window function which resolves the enigma of Joglekar's window function. To overcome the issue they proposed another function:

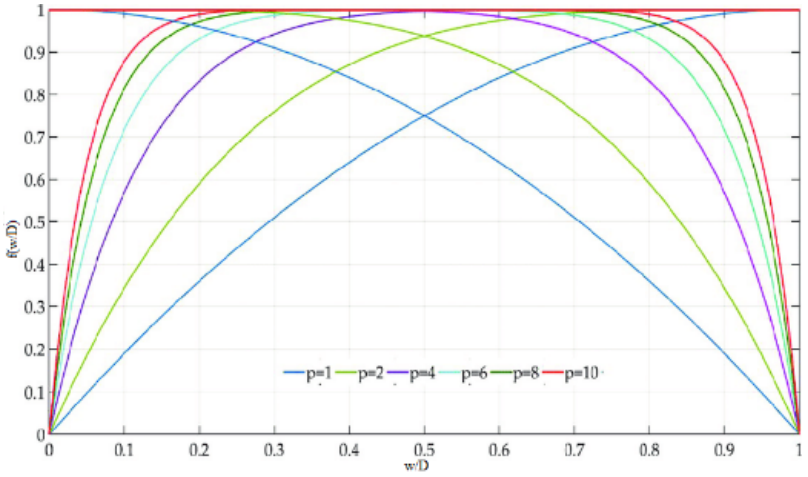

FIGURE 3.4: Biolek's window function for distinct p values [8]

$$F(X) = \left[1 - (X - stp(-i))^{2p}\right] \tag{3.9}$$

$$stp(i) = \begin{cases} 1 & i \geq 0 \\ 0 & i < 0 \end{cases} \tag{3.10}$$

Here, i indicates the memristive current & p is the control parameter. In this, they introduced the step function of memristive current as shown in equation 3.10. Figure 3.6 shows the Biolek's window function for distinct value of p.

This function incorporates the problem of boundary lock. But we can't adjust these window function because they don't have a scale factor, so it's not possible to change the maximum value of the window function to the value below or above one.

3.2.2.3 Prodromakis Window Function

Prodromakis et al. [6], [12] in 2011 gives a new function that can solve the problem that occurs in Biolek's window functions. In this model, they include a new parameter j, which represents control parameter. The function is shown in equation 3.11.

$$F(W) = j\left(1 - \left[\left(\frac{W}{D} - \frac{1}{2}\right)^2 + \frac{3}{4}\right]^p\right) \tag{3.11}$$

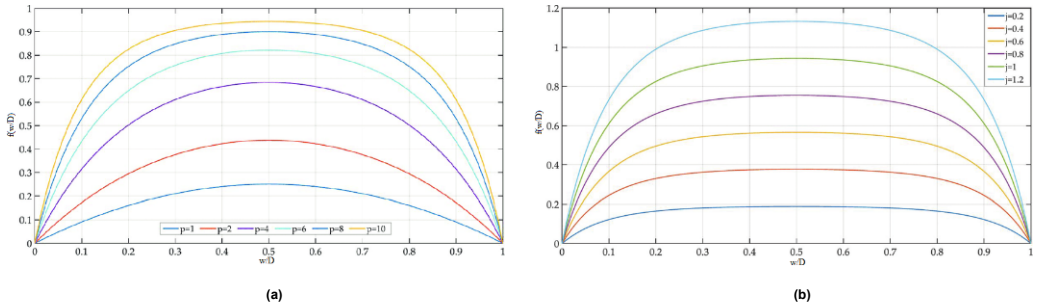

FIGURE 3.5: Prodromakis window function (a for distinct p values,and (b) for different j values. [6]

Figure 3.5 shows Prodromakis window function by fixing j to one and draw the function of different p values. While in figure 3.6, we are setting p=10 and draw the function for different j values.

3.2.3 Nonlinear Ion Drift Model

Linear ion drift meets the basic memristive equation. Researches show that this model slightly strays from the fabricated MD's [16]. Linear ion drift model is not suitable for digital circuits. Thus we require more relevant MD models.

Model is provided in [15] based on the experimental data described in [16]. The relation between voltage and current is

$$i(t) = [W(t)^n \beta \sinh(\alpha V(t))] + \chi\left[e^{\gamma V(t)} - 1\right] \tag{3.12}$$

Here the experimental control parameters are β, α, γ,and χ, and n is a parameter that defines the impact of the state variable W(t) on the current. This model consists of normalized state variable within the interval [0,1]. The state variable is close to one during ON state, and the current equation is governed by the first expression in 3.12, $\beta \sinh(\alpha V(t)$, this phenomenon is called tunneling. The state variable is close to zero during the OFF state and the current equation is governed by the second expression in 3.12, $\chi \left[e^{\gamma V(t)} - 1\right]$, which is equivalent to the equation of the diode.

The dependency of voltage in the state derivative equation is nonlinear shown below:

$$\frac{dW}{dt} = a \cdot \{F(W)\} \cdot \{V(t)\}^m \tag{3.13}$$

Here a and m are the constant to the derivative of the state variable, m represent odd number, and $F(W)$ is the window function.

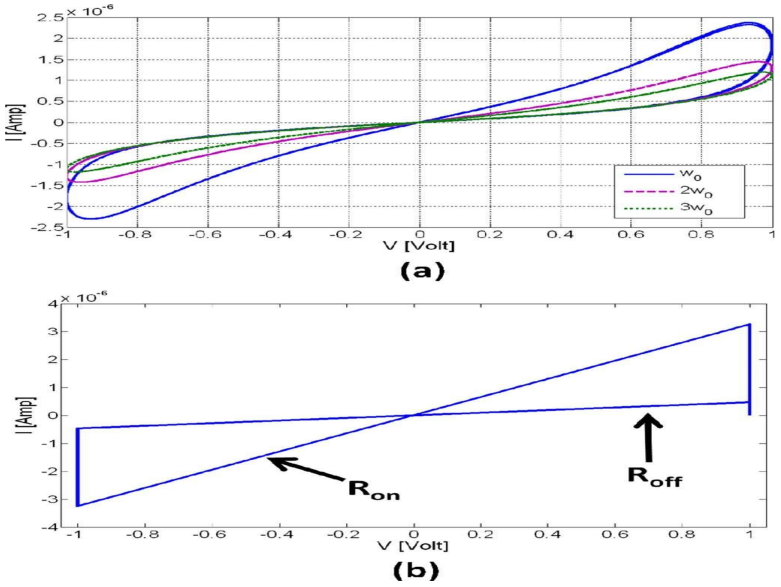

FIGURE 3.6: I-V curve for nonlinear ion drift [4]

The I-V curve for nonlinear ion drift MD's for rectangular and sinusoidal input is demonstrated in figure 3.6, by setting the device parameters $n = 2$, $m = 5$, $a = 1V^{-m}s^{-1}$, $\gamma = 4V^{-1}$, $\beta = 0.9\mu A$, $\alpha = 2V^{-1}$, and $\chi = 10^{-14}$.

3.2.4 Memristor Simmons Tunnel Barrier Model

A more realistic physical model had been proposed by M.D. Pickett et al. [3]. This model considers asymmetric nonlinear switching behavior because the movement of ionized dopants depends on changes in the state variables in an exponential manner. In the earlier model, there were two resistors in series, but in the existing model, there is one resistor in series with an electron tunnel barrier, as shown in Figure 3.7. In this model, x is taken as a state variable.

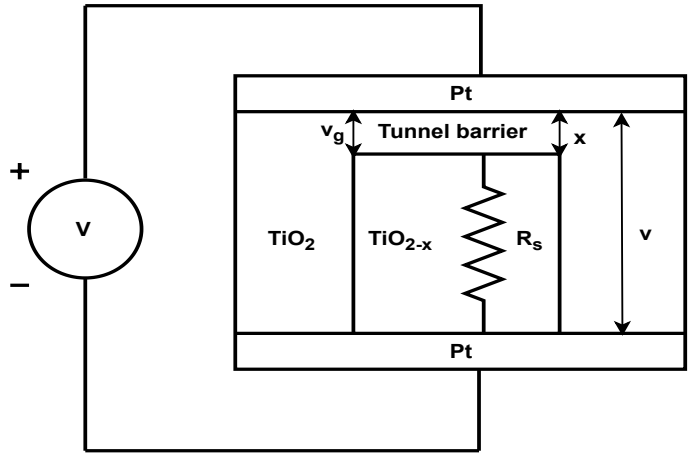

FIGURE 3.7: Physical model of Simmons tunnel barrier model [3]

In this case, the derivative of x indicates the oxygen vacancy drift [13] velocity, which is as follows:

$$\frac{dX(t)}{dt} = \begin{cases} C_{OFF} \cdot \sinh\left\{\frac{i}{i_{OFF}}\right\} \cdot exp\left[-exp\left\{\frac{X-a_{OFF}}{w_c} - \frac{|i|}{b}\right\} - \frac{X}{w_c}\right] & i > 0 \\ C_{ON} \cdot \sinh\left\{\frac{i}{i_{ON}}\right\} \cdot exp\left[-exp\left\{\frac{X-a_{ON}}{w_c} - \frac{|i|}{b}\right\} - \frac{X}{w_c}\right] & i < 0 \end{cases} \tag{3.14}$$

where C_{ON}, i_{OFF}, C_{OFF}, i_{ON}, w_c, a_{ON}, a_{OFF} and b are the adjusting parameters. We are presenting the physical phenomenon in the form of equations in 3.14 as the device size is in the nanometer scale. The electric field and local Joule heating across the platinum electrodes, improving the oxygen vacancies. Due to the diffusion of vacancies (from TiO_{2-x} to TiO_2) in practical MD's and drift of oxygen ion vacancies due to the internal electric

field, the ON switching is speedier than the OFF switching. The drift and diffusion are different for negative and positive voltages.

The parameter C_{ON} and C_{OFF} affect the magnitude of X. The parameter C_{OFF} is lesser than the parameter C_{ON}. The parameter i_{ON} & i_{OFF} represent the current threshold. Below the current threshold, the change in state derivative X is negligible. The parameter a_{ON} and a_{OFF} decides the bounds of the state variable X. In equation 3.14 it has been seen that the derivative of the state variable exponentially depends on $X - a_{ON}$ or $X - a_{OFF}$. Because of that, the state variable is very small in the required range. Hence there is no necessity for window function.

The current and voltage relationship is shown in equation 3.15.

$$\begin{aligned} i(t) = &\left[\tilde{A}(X, V_g\Phi_1(V_g, X)exp(-B(V_g, X)\cdot[\Phi_1(V_g, X)]^{\frac{1}{2}})\right] \\ &- \left[\tilde{A}(X, V_g)(\Phi_1(V_g, X) + e\,|V_g|)\cdot exp(-B(V_g, X)\cdot(\Phi_1(V_g, X) + eV_g)^{\frac{1}{2}})\right] \end{aligned} \tag{3.15}$$

$$V_g = v - i(t)\cdot R_s \tag{3.16}$$

Here v is the internal voltage, which is not equal to the external bias voltage V shown in figure 3.7.

3.2.5 Threshold Adaptive Memristor Model (TEAM)

Tunnel barrier model is the most reliable physical model of the MD. This model is, however, wholly intricate, without a specific relationship between current and voltage. This model fits for specific MD's.

S. Kvatinsky et al. [4] in 2013 presented another model which overwhelm the problems of Simmons barrier model. This model offers a simpler expression sooner than a complex equation. This model exhibits identical physical behavior compared to the tunnel barrier model. This model has several assumptions.

- Below certain threshold current no change in state variable occur.

- Rather than exponential dependence, Polynomial dependence is linked between the internal state drift derivate and memristor current.

The derivative of the state variable is mainly obtained by multiplying two functions. In which, one function depends on the internal state variable and other on depends on memristive voltage independently.

$$\frac{dX(t)}{dt} = \begin{cases} K_{OFF} \cdot \left\{ \frac{i(t)}{i_{OFF}} - 1 \right\}^{\alpha_{OFF}} \cdot F_{OFF}(X) & , 0 < i_{OFF} < i \\ 0 & , i_{ON} < i < i_{OFF} \\ K_{ON} \cdot \left\{ \frac{i(t)}{i_{ON}} - 1 \right\}^{\alpha_{ON}} \cdot F_{ON}(X) & , i < i_{ON} < 0 \end{cases} \tag{3.17}$$

The above equation shows the derivative of the internal state variable. This equation consists of various fitting parameters like K_{off}, K_{on} having positive and negative value, respectively. α_{on} and α_{off} are constant. In the above equation, V_{ON} and V_{OFF} describe that memristor holding bipolar switching mechanism having two threshold voltages of equal magnitude and opposite polarity. Functions $F_{ON}(X)$ and $F_{OFF}(X)$ are the window function which bounds the internal state variable in between W_{ON} and W_{OFF}. The current-voltage relation is given by:

$$V\left(t\right) = \left[R_{ON} + \left\{ \frac{R_{OFF} - R_{ON}}{X_{OFF} - X_{ON}} \right\} \cdot \left\{ X - X_{ON} \right\} \right] \cdot i\left(t\right) \tag{3.18}$$

The change in memristance is exponentially dependent on the state variable [3]. In practical MD's the memristance, depends on the tunneling barrier, as shown in figure 3.7, which is nonlinear. As in (3.15) describe the relationship between current-voltage. The model becomes incompetent in terms of computational time. Therefore, any variation in tunneling barrier width causes the change in memristance. The variation in memristance is assumed to vary exponentially. On this assumption I-V relation, becomes

$$V(t) = \left\{ R_{ON} \right\} \cdot \left\{ e^{(\lambda / X_{OFF} - X_{ON})(X - X_{ON})} \right\} \cdot i(t) \tag{3.19}$$

Here R_{ON} and R_{OFF} are the ON and OFF memristance respectively and λ is the fitting parameter such that

$$\frac{R_{OFF}}{R_{ON}} = e^{\lambda} \tag{3.20}$$

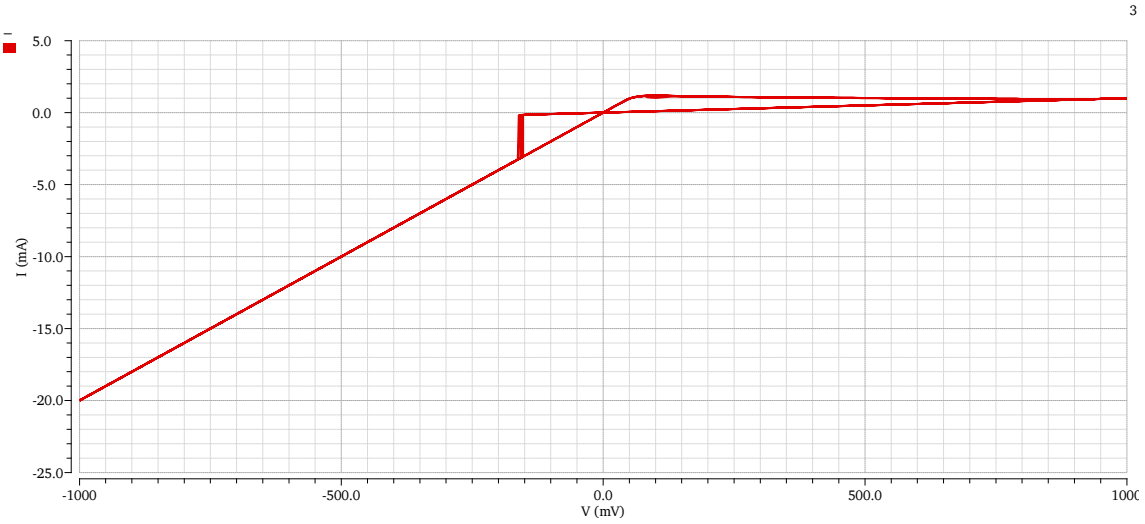

FIGURE 3.8: Hysteresis curve for TEAM model [3]

Fig 3.8 represent the hysteresis characteristics with fitting parameters of $R_{OFF} = 50\Omega$, $R_{ON} = 1k\Omega$, $K_{ON} = -4.68e^{-13}nm/s$, $K_{OFF} = 1.46e{-}9nm/s$, $i_{OFF} = 115e^{-6}A$, $i_{ON} = 8.9e^{-6}A$. Which designate that the OFF switching is slower than ON switching.

3.2.6 Voltage Threshold Adaptive Memristor Model (VTEAM)

Based on the experimental data, in the practical MD, the existence of threshold voltage instead of the threshold current was found. It is observed that the computational efficiency and accuracy of VTEAM model [14] is less than 1.5% in terms of relative RMS error [18]. This model is the expansion of the TEAM model [4], which couples numerous benefits of threshold voltage rather than the threshold current. Two types of equations characterize memristor behavior:

- a state-dependent ohms law, and
- equation defining the internal state variable.

$$\frac{dW}{dt} = F\left(W, V\right) \tag{3.21}$$

$$V\left(t\right) = \left[M\left(q\right)\right].\left[i\left(t\right)\right] \tag{3.22}$$

Where the derivative of the internal state variable is the function of both, applied current or voltage $V(t)$ and internal state variable W, a state-dependent Ohms law depends on memristance $M(q)$.

$$M\left(q\right) = \left[R_{ON} + \left\{\frac{R_{OFF} - R_{ON}}{W_{OFF} - W_{ON}}\right\} \cdot \left\{W - W_{ON}\right\}\right] \tag{3.23}$$

On substituting equation(3.23) in equation(3.22) we get:

$$V\left(t\right) = \left[R_{ON} + \left\{\frac{R_{OFF} - R_{ON}}{W_{OFF} - W_{ON}}\right\} \cdot \left\{W - W_{ON}\right\}\right] \cdot i\left(t\right) \tag{3.24}$$

where memristance $M(q)$ is completely dependent on the bounds(W_{ON} and W_{OFF}) of state variable(defines the movement of oxygen vacancies) and R_{ON} , R_{OFF}. Where R_{ON} , R_{OFF} are the ON and OFF memristance correspond to W_{ON} and W_{OFF}.

The derivative of the state variable is mainly obtained by multiplying two functions. In which, one function depends on the internal state variable and other depends on memristive voltage independently.

$$\frac{dW(t)}{dt} = \begin{cases} K_{OFF} \cdot \left\{\frac{V(t)}{V_{OFF}} - 1\right\}^{\alpha_{off}} \cdot F_{OFF}(W) & ,0 < V_{OFF} < V \\ 0 & ,V_{ON} < V < V_{OFF} \\ K_{ON} \cdot \left\{\frac{V(t)}{V_{ON}} - 1\right\}^{\alpha_{on}} \cdot F_{ON}(W) & ,V < V_{ON} < 0 \end{cases} \tag{3.25}$$

The above equation shows the derivative of the internal state variable. This equation consists of various fitting parameters like K_{OFF}, K_{ON} having positive and negative value, respectively. α_{on} and α_{off} are constant. In the above equation, V_{ON} and V_{OFF} describe that memristor holding bipolar switching mechanism having two threshold voltages of equal magnitude and opposite polarity. Functions $F_{ON}(W)$ and $F_{OFF}(W)$ are the window function which bounds the internal state variable in between W_{ON} and W_{OFF}.

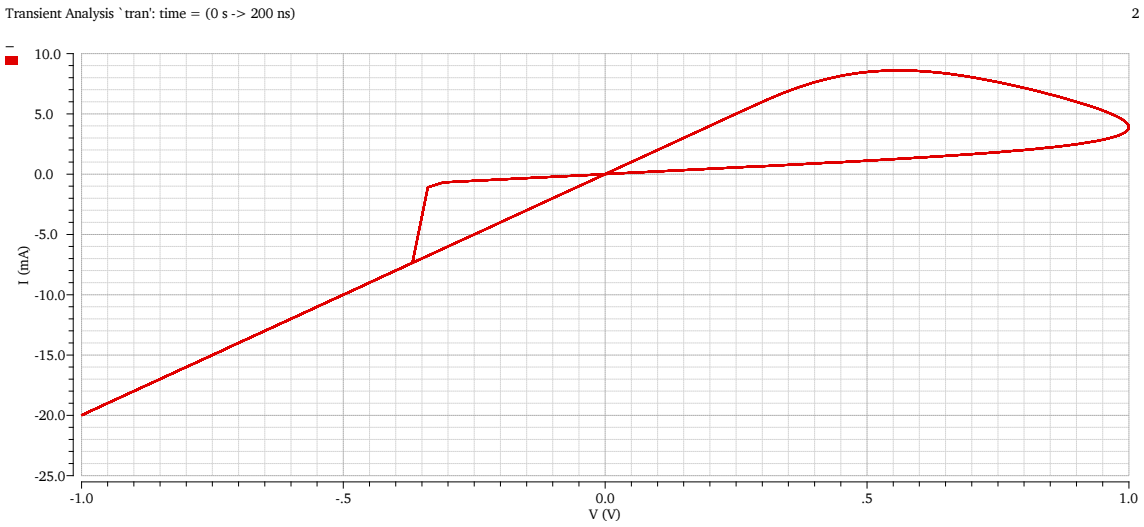

FIGURE 3.9: I-V curve for VTEAM model

Figure 3.9 shows the pinched hysteresis curve between current and voltage. I-V curve is drawn for sinusoidal input having amplitude 1 V and frequency of 50MHz, and the fitting parameters are $D = 3$ nm , $R_{OFF} = 1k\Omega$, $R_{ON} = 50\Omega$, $K_{ON} = -10$ nm/s , $K_{OFF} = 5e^{-4}$ nm/s, $V_{OFF} = 0.3$ V, $V_{ON} = -0.3$ V. Which designate that the ON switching is faster than OFF switching.

Chapter 4

Applications of memristor

4.1 Introduction

Three significant properties of memristor which fascinate the specialists are; (1)nanometer scale (2) memory properties (3) driving abilities. The nanometer scale empowers to construct a high-density chip with very low power utilization. In addition, manufacturing gadgets in nanometer scale is less expensive and simpler contrasting with the CMOS process. Nano-computing techniques will be possible with memristor retention properties.

Mazumder et al. presented an assortment of feasible memristor application, which is shown in the Figure 4.1.

4.1.1 Non-volatile memory

In the near future, memristor will be primarily used as a non-volatile memory device. Memristor holds past state when it is in OFF mode, is the property which makes memristor a decent contender for NVRAMs. Hewlett-Packard Labs manufactured the crossbar memory, which is 10 times slower than DRAMs.

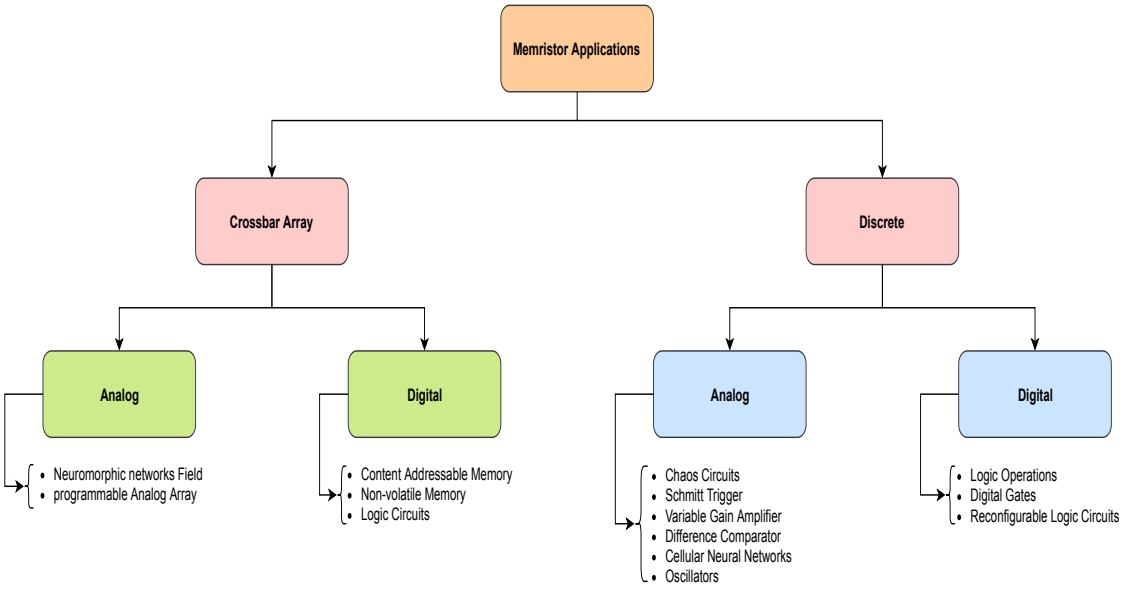

FIGURE 4.1: Assortment of feasible memristor application

4.1.2 Resistive Random Access Memory (ReRAM)

ReRAMs related as memristive memories as per [23] is the research topic in numerous organizations around the globe. Organizations, for example, Unity Semiconductor, Hewlett-Packard, Interuniversitair Micro-Electronica Centrum (IMEC),Fujitsu & Sharp, has given some portion of their exploration to create various kinds of memristive materials. The practical idea of this kind of memory depends on the two logic, "1" and "0" they are related as ON and OFF state respectively [22].

There are two types of switching mechanism present in these materials that are unipolar & bipolar switching. Internal state of the MD is switched by supplying a voltage. For bipolar switching, we require two threshold voltages having equal magnitude and have opposite polarity. In the case of unipolar switching, threshold voltage is lesser than the supply voltage [22].

Table 4.1 contains a correlation of performance parameters of various memory innovations. The burdens in different innovations are slow WRITE/ERASE times & low perseverance for Flash memories, poor versatility for MRAM and FeRAM. Also, voltage scaling in memristors is less complex than its adversaries. Notwithstanding the referenced issues,

	Traditional technologies				Emerging technologies			
	DRAM	**SRAM**	**NOR**	**NAND**	**FeRAM**	**MRAM**	**PCM**	**Memristor**
Knowledge level	mature		advanced		product		advanced	early stage
Cell element	1T1C	6T	1T		1T1C	1T1R	1T1R	1M
Half pitch(F) (nm)	50	65	90	90	180	130	65	3-10
Smallest cell area	6	140	10	5	22	45	16	4
Read time(ns)	<1	<0.3	<10	<50	<45	<20	<60	<50
Write/Erase time(ns)	<0.5	<0.3	10^5	10^6	10	20	60	<250
Retention time(years)	seconds	N/A	>10	>10	>10	>10	>10	>10
Write operational voltage	2.5	1	12	15	0.9-3.3	1.5	3	<3
Read operational voltage	1.8	1	2	2	0.9-3.3	1.5	3	<3
Write endurance	10^{16}	10^{16}	10^5	10^5	10^{14}	10^{16}	10^9	10^{15}
Write energy(fJ/bit)	5	0.7	10	10	30	$1.5x10^5$	$6x10^3$	<50
Density(Gbit/cm^{2}{2})	6.67	0.17	1.23	2.47	0.14	0.13	1.48	250

TABLE 4.1: A correlation of performance parameters of various memory innovations [22].

still, memristors were lower switching speed as compared to DRAMs. In memristor store-to-compose time constant is around 10^3 cycles, whereas in Dynamic RAM cells are 10^6 cycles.

4.2 Crossbar Structure

The crossbar structure is a standout among the most encouraging nanostructures at the architectural level [26]. The crossbar is inherently imperfection tolerant because of the massive number of switches [**?**]. It is a less expensive & straight forward fabrication process. Different points of interest are flexibility, high density & scalability. Crossbar networks can be utilized to play out a lot of calculations.

It comprises of a lattice of nano-wires, where at each crosspoint of the vertical and horizontal wires, a memristor switch exists. In crossbar the size of every junction is around 2-3nm as compared to the size transistor junction being approximately 60nm. NIL is the method for fabricating nanowires, which is basically, high-resolution minimal cost lithography process.

Figure 4.2 shows a picture of the crossbar nano-wires and demonstrating a memristor switch in each crosspoint.

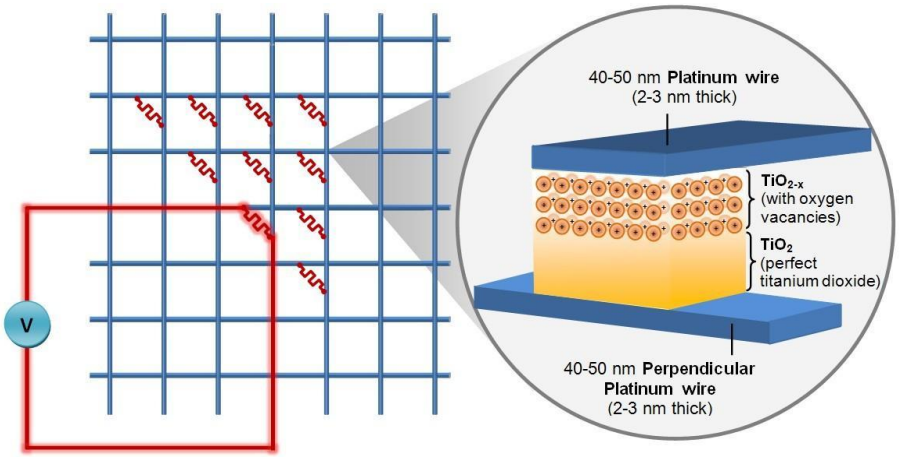

FIGURE 4.2: Schematic of crossbar structure

4.2.1 Hybrid Chip

Hewlett-Packard used crossbar structure that comprised a blend of memristors and transistors in a hybrid chip. A single CMOS layer can efficiently drive a thousand layers of memristor. The entire structure is relatively powerful with respect to energy dissipation, which generates less heat. Because of the very high density of the crossbars, there exist more logics /unit area in the chip. Switching time in ns and the single switch requires energy in picojoule(pJ).

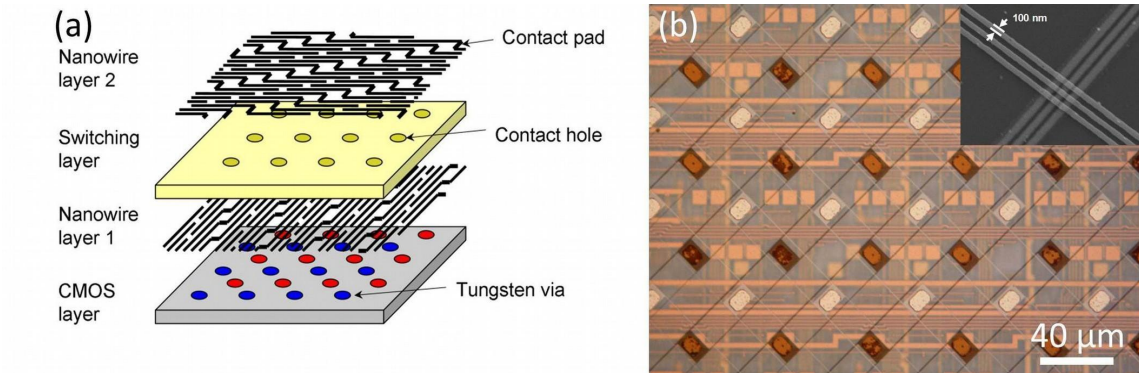

FIGURE 4.3: The first hybrid chip [25] at Hewlett-Packard Labs. (a) Schematic of hybrid circuit having switching layers (b) The hybrid chip

In future, there is no need for scaling down the transistors because of the presence of nanometer size of a memristor. These structure provides high performance while staying aware of Moore's law.

4.2.2 Scaling Potential

As depicted previously, basically it's conceivable to pile a large number of crossbar memories consists of memristors over one another and successfully interface an unlimited number of layers and a confined number of CMOS in a solitary layer. Along these lines, hypothetically, even with one single CMOS layer, it's conceivable to take care a large(thousands) number of memristor layers. To drive the various layers, Strukov [**?**] provided a 4-D address space. Taking into account that piling eight layers appears to be extremely simple, & the way that every crossbar memory layer can posses the bit density of $0.5Tb/cm^2$, results in a large memory of $4Tb/cm^2$. This means that a memristor chip can have a Peta Byte(Pb) memory capacity i.e. enough memory for storing all videos, books, audio clips & pictures available in the library of congress. In this way, with that much of density and scaling potentials of memristors, for all intents and purposes, there will be no requirement for transistors that have half pitch lesser than 30nm.

4.3 Memristor as a Memory Element

In April 2010 HP Labs made 3nm memristor, having a switching time of nanosecond. They additionally discovered that they could stack memristor layers over one another, giving it a density of 2-8 times greater than the flash memory (even 100 times more than flash memory). In this way, having a capacity of roughly $1Pbits/cm^2$ on a solitary chip can bring about revoking hard drive. Envision a camera memory having a size equal to thumb which is store the videos and pictures captured in a 365 days. Memristor innovation can prompt super-little memories which might have an immense measure of use.

4.3.1 Booting Free Computers

The non-volatile nature of memristors raises the concept of booting free computer, where memristive memory can supplant the hard drive & DRAM, and by expelling the battery of Laptop, nothing will be lost. When you restart the gadget, all the data remain intact

as it was previously. Since there is no loss of data, the boot-up time decreases and gives high reliability & flexibility in case of power shutdown in the data centers.

4.4 Programmable Logic

It is demonstrated that memristors can carry out the Implication logic [28]. They [28] are detailed that one can use the memristor in the two ways latch as well as logic. Also, they present a minimum number of memristor required to demonstrate logic functions. Afterwards, Lehtonen et al. [27], utilized a recursive conjunctive form & demonstrated only 2 memristor are required to perform Boolean logic.

Chapter 5

Simulation Results

5.1 Introduction

After the theoretical postulation by Leon Chua in 1971 [1], In 2008, Strukov et al.[2] developed physical memristor model that possessed the same properties that Leon Chua approximated. The proposed HP memristor has thin film TiO_2 sandwiched by 2 electrodes of platinum. They show that pinched hysteresis I-V curve is obtained at the nano-meter scale [17].

They reasoned that memristor has many valuable and exciting circuit properties. In the nano-scale systems [2],memristance emerges naturally. As the device dimension is in nano-meter scale, on applying even a small voltage across MD causes vast electric field which can move the charge species. This movement of charge species causes unexpected variation in device resistance.The electric field and local Joule heating across the platinum electrodes, enhancing the oxygen vacancies. Due to diffusion of vacancies (from TiO_{2-x} to TiO_2) in practical MD and drift of oxygen ion vacancies because of the internal electric field, the OFF switching is slower than the ON switching. The drift and diffusion are different for positive and negative voltages [16]. The resistance of the MD is varied according to the amount of charge passes through it.

5.2 Memristor Modeling and Characterization

5.2.1 Memristor

Strukov et al. [2] in 2008 exhibited the physical model of the memristor. The change in memristance relays on the amount of charge flowing through it. Model proposed in this paper assumed that the MD consists of two regions. One region is doped with oxygen vacancies (contains +ve oxygen ions) and the rest remains undoped [11] as shown in figure 5.1. The total resistance of the device is given by the resistance created by the dopped and undoped region. The doped region is having low resistance while the undoped part has high resistance.

When an ample amount of charge passes through the MD, ions got saturated, and hence they are not able to move further, this causes a device to enter in hysteresis region [3]. This behavior is the principle characteristics of a memristor. The variation in resistance is non-volatile; so, the cell behave as a memory element. For logic application, we are using Voltage Threshold Adaptive Memristor(VTEAM) model. Accuracy of this model is the highest compared with the other memristive model.

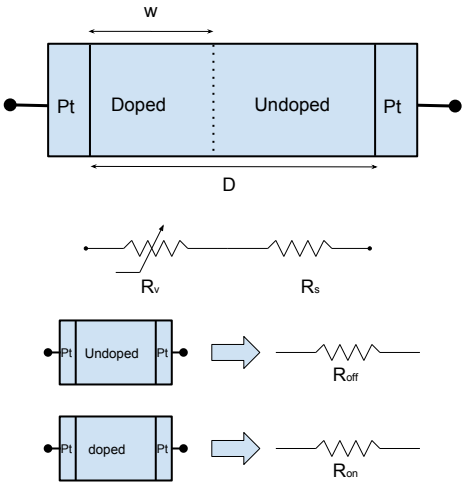

FIGURE 5.1: Simplified equivalent circuit of memristor

5.2.2 Memristor Modelling

Two types of equations characterize memristor behavior: (i) a state-dependent ohms law, and (ii) equation defining the internal state variable.

$$\frac{dW}{dt} = F\left(W, V\right) \tag{5.1}$$

$$V\left(t\right) = M\left(q\right).i\left(t\right) \tag{5.2}$$

Where the derivative of the internal state variable is the function of both applied current or voltage $V(t)$ & internal state variable W, a state-dependent Ohms law depends on memristance $M(q)$.

$$M\left(q\right) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{W_{OFF} - W_{ON}} \cdot \left(W - W_{ON}\right)\right] \tag{5.3}$$

On substituting equation(3.23) in equation(3.22) we get:

$$V\left(t\right) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{W_{OFF} - W_{ON}} \cdot \left(W - W_{ON}\right)\right] \cdot i\left(t\right) \tag{5.4}$$

where memristance $M(q)$ is completely dependent on the bounds(W_{ON} and W_{OFF}) of state variable(defines the movement of oxygen vacancies) and R_{ON} , R_{OFF}. Where R_{ON} , R_{OFF} are the ON and OFF memristance correspond to W_{ON} and W_{OFF}.

The derivative of the state variable is mainly obtained by multiplying two functions. In which one function depends on the internal state variable while other on memristive voltage independently.

$$\frac{dW(t)}{dt} = \begin{cases} K_{OFF}\left(\frac{V(t)}{V_{OFF}} - 1\right)^{\alpha_{off}} \cdot F_{OFF}(W) & ,0 < V_{OFF} < V \\ 0 & ,V_{ON} < V < V_{OFF} \\ K_{ON}\left(\frac{V(t)}{V_{ON}} - 1\right)^{\alpha_{on}} \cdot F_{ON}(W) & ,V < V_{ON} < 0 \end{cases} \tag{5.5}$$

The above equation shows the derivative of the state variable. This equation consists of various fitting parameters like K_{off}, K_{on} having positive and negative value, respectively.

α_{on} and α_{off} are constant. In the above equation, V_{ON} and V_{OFF} describe that memristor holding bipolar switching mechanism having two threshold voltages of equal magnitude and opposite polarity. Functions $F_{ON}(W)$ and $F_{OFF}(W)$ are the window function that bounds the internal state variable in between W_{ON} and W_{OFF}.

5.3 Effect of Frequency on I-V Curve

Memristive devices consist of two regions [2]. One region is doped with oxygen vacancies (contains +ve oxygen ions) & the rest remains undoped as shown in Figure 5.1. When we are applying a sinusoidal signal across the memristor. As the distribution of oxygen vacancies in the TiO_2 varies, the resistance also gets changed. This means that if we apply a positive voltage to the memristive device in OFF state, the device will turn ON. Figure 5.1 shows the simplified equivalent circuit of memristor which indicates that if we apply the positive voltage to the memristor doped with oxygen vacancies, oxygen vacancies get shifted towards the other end which makes low resistance path termed as ON resistance(R_{on}). Similarly, if we apply negative voltage, it shows high resistance termed as OFF resistance(R_{off}).

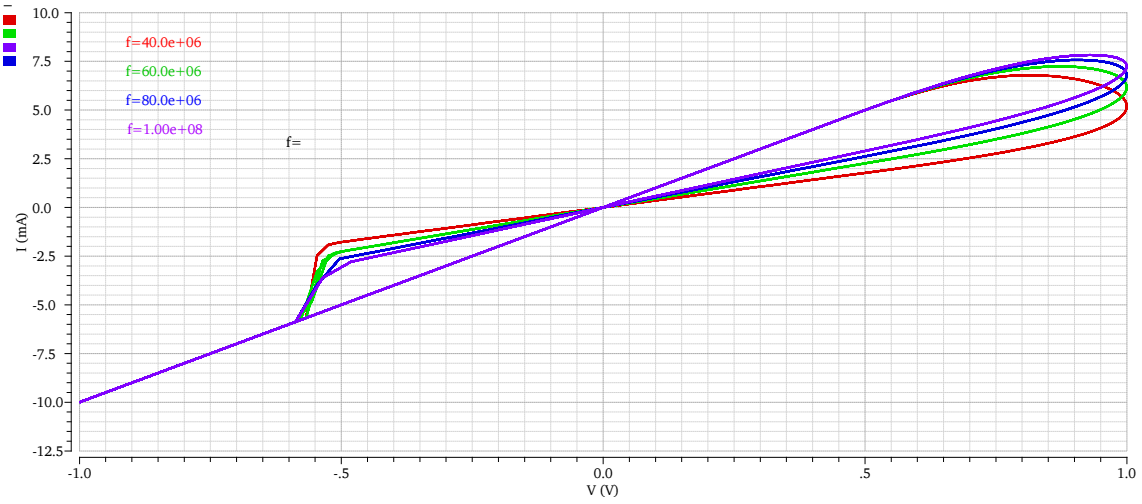

FIGURE 5.2: I-V curve by varying frequency

When a sufficient quantity of charge is passed through the MD, ions remain no longer in motion and become saturated causing the device to move into a hysteresis region shown

in Figure 5.2 as we are increasing the frequency of the input sinusoidal signal. The mobility of oxygen vacancies increases causes the hysteresis loop to shrink. When frequency approaches infinity, the memristive device will behave as a normal resistor.

5.4 Effect of Threshold Voltage on I-V Curve

There are various memristor models. Among these some do not have a threshold, so that the variation in memristance happened for the applied current and voltage. Based on the experimental data, in the practical MD, the existence of threshold voltage in place of the threshold current was found. It is observed that the computational efficiency and accuracy of VTEAM model is less than 1.5% in terms of relative RMS error [18]. This model is the extension of the TEAM model [4] which couples numerous benefits of threshold voltage insted of the threshold current.

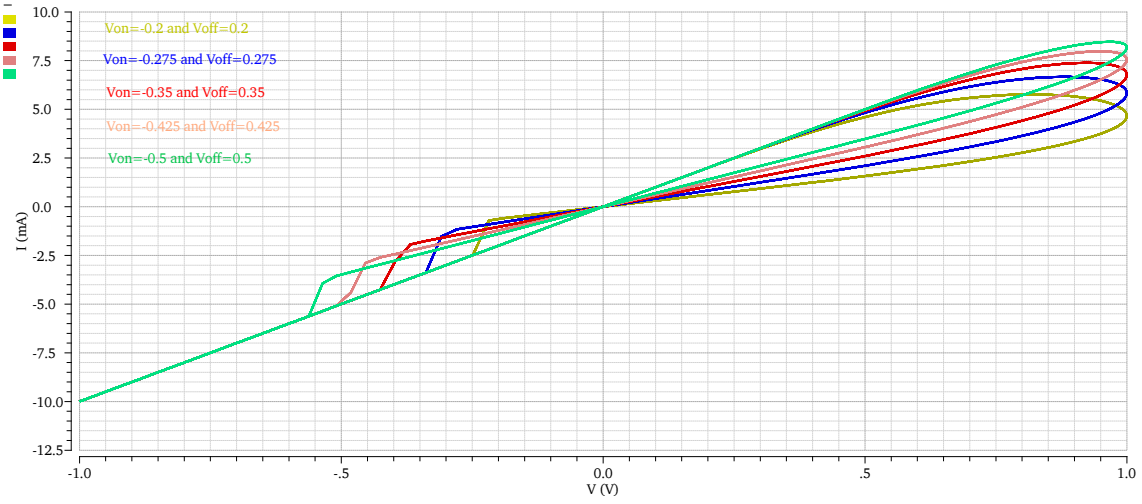

FIGURE 5.3: I-V characteristics by varying threshold voltage

Figure 5.3 shows the I-V characteristic by varying threshold voltages i.e. $V_{ON}$and V_{OFF} and decides how quick the RESET activity is performed. We are varying V_{ON} and V_{OFF} as shown in the figure and comes to know that for threshold voltage of V_{ON}=-0.5V and $V_{OFF} = 0.5V$ have slower reading system than V_{ON}=-0.2V and V_{OFF}=0.2V.

5.5 MeMOS Digital Logic Gates and Circuits

Though memristor is a passive element, it can be used both as the analog and digital storage devices and logic as well. A special feature of this device is that the data stored in a memristor induces variation in the state of another memristor.

5.5.1 AND Gate Implemented by Memristor

Memristor-based AND gate schematic [10] is shown in Figure 5.4. Here A and B are the inputs to the memristor M1 and M2 respectively and OUT as the output terminal [5], [9].

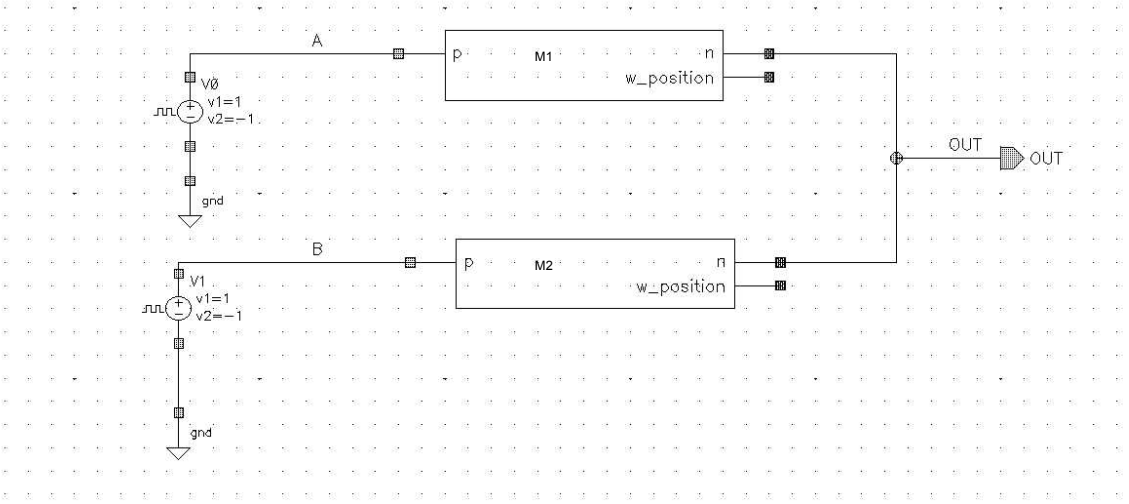

FIGURE 5.4: AND gate schematic

When we apply the -ve voltage on memristor M1 and +ve voltage to memristor M2. Due to the shifting of oxygen vacancies towards the undoped region, a low resistance path has created. This causes a decrease in resistance across M1. Similarly, on the other side, the resistance across M2 is according to voltage divider rule output voltage becomes

$$v_{out} = v_{cc}\frac{R_{on}}{R_{on} + R_{off}} \tag{5.6}$$

where $R_{off} >> R_{on}$ .Due to which logic 0 is obtain at the output node. Figure 5.5 shows the output of memristor-based AND gate using VTEAM model.

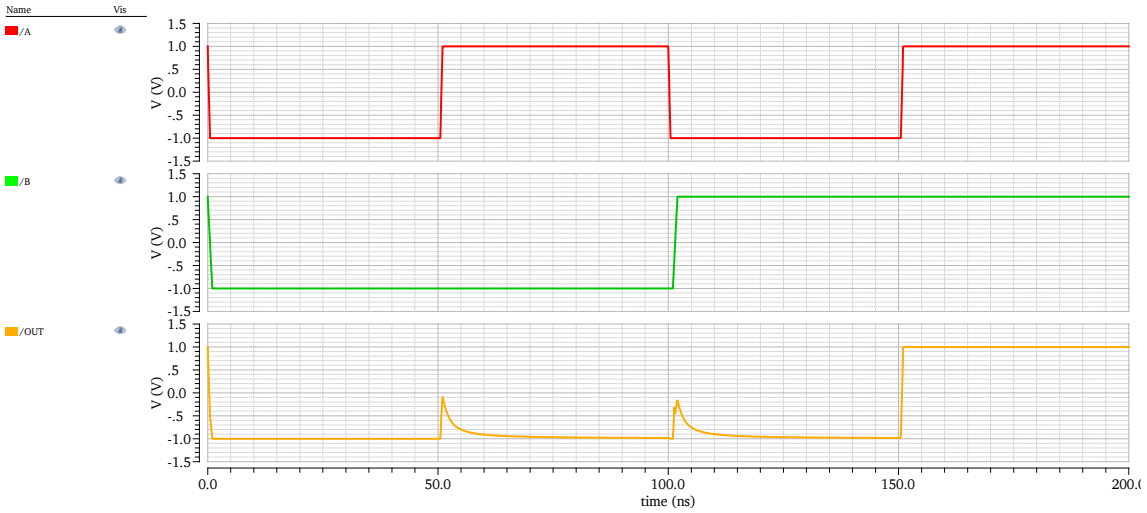

FIGURE 5.5: AND gate result

5.5.2 OR Gate Implemented by Memristor

Memristor-based OR gate schematic is shown in Figure 5.6. Here A and B are the inputs to the memristor M1 and M2 respectively and OUT as the output terminal [9].

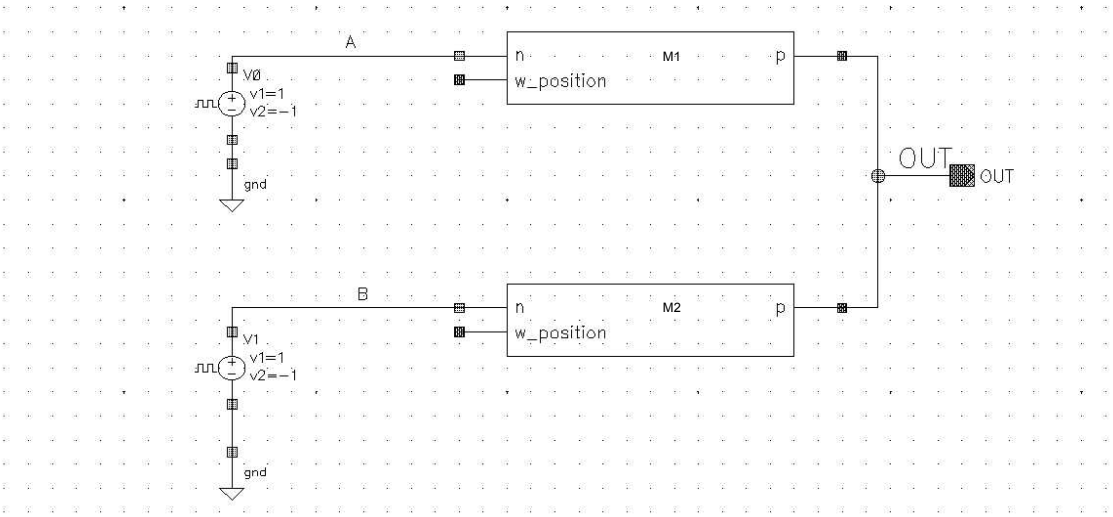

FIGURE 5.6: OR gate schematic

When we are applying the positive voltage (logic 1) on memristor M1 and negative voltage (logic 0) to memristor M2. A low resistance path has been developed due to the shift of oxygen vacancies towards the undoped region. This causes a decrease in resistance across M1. Similarly, on the other side, the resistance across M2 is increasing. The output of

these memristors is connected to the common node. Hence according to voltage divider rule output voltage becomes

$$v_{out} = v_{cc}\frac{R_{off}}{R_{on} + R_{off}} \tag{5.7}$$

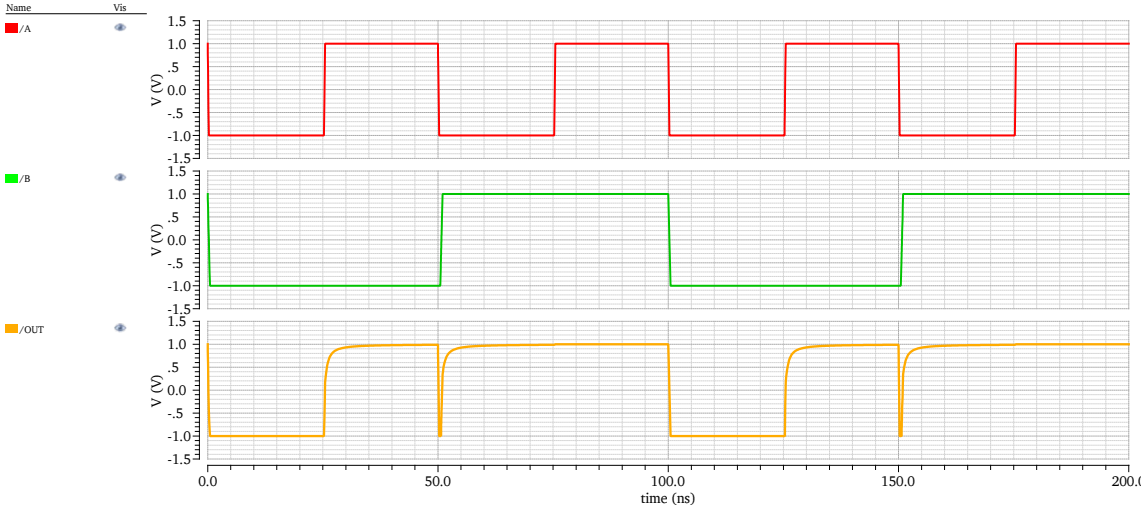

FIGURE 5.7: OR gate result

where $R_{off} >> R_{on}$ .Due to which logic 1 is obtain at the output node. Figure 5.7 represents the output of memristor-based OR gate using VTEAM model.

5.5.3 NAND Gate Implemented by Memristor

MeMOS based schematics of the NAND gate is shown in figure 5.8. Where A, B are inputs to the two different memristor M1 and M2, respectively. Outputs of these memristors are connected to the common node, which is further connected to the MOS based inverter circuit. OUT is the output to the NAND gate.

On applying logic 1, i.e. positive voltage to memristor M1 and logic 0, i.e. negative voltage to M2. The changes in the distribution of oxygen vacancies that consists of positive ions causes the increase in resistance of M1 and decrease the resistance of M2. This results in the output at the common node became logic 0. This logic 0 is applied to inverter circuit made up of NMOS and PMOS. The NMOS become OFF while PMOS is ON. This results the output to be the dc voltage which is treated as logic 1. Figure 5.9 shows the NAND gate simulation result.

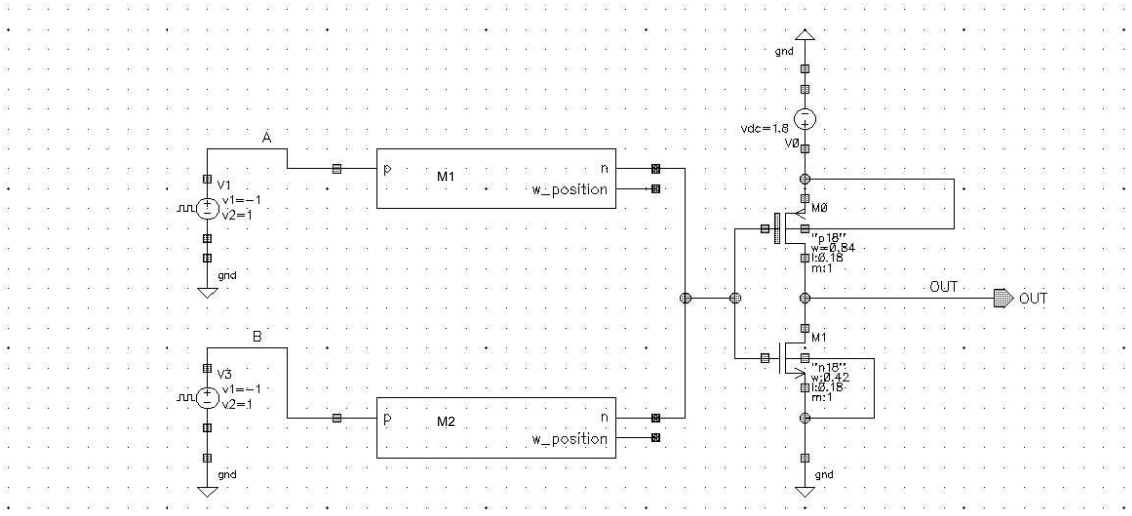

FIGURE 5.8: NAND gate schematics

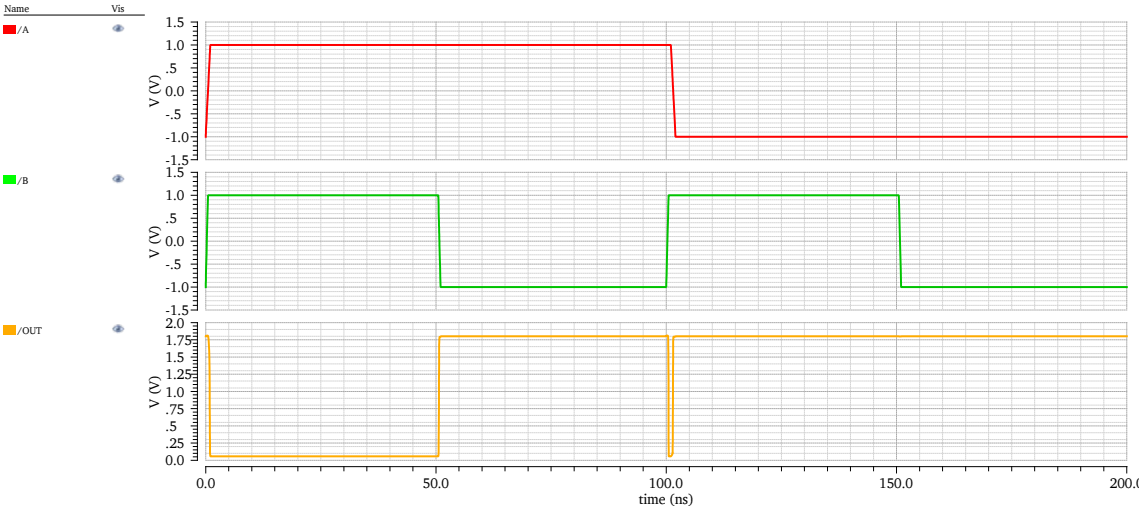

FIGURE 5.9: NAND gate result

5.5.4 NOR Gate Implemented by Memristor

MeMOS based schematics of the NOR gate is shown in Figure 5.10. Where A, B are inputs to the two different memristor M1 and M2, respectively. Outputs of these memristors are connected to the common node, which is further connected to the MOS based inverter circuit. OUT is the output to the NOR gate.

On applying logic 1, i.e. positive voltage to memristor M1 and logic 0, i.e. negative voltage to M2. The changes in the distribution of oxygen vacancies that consists of positive ions

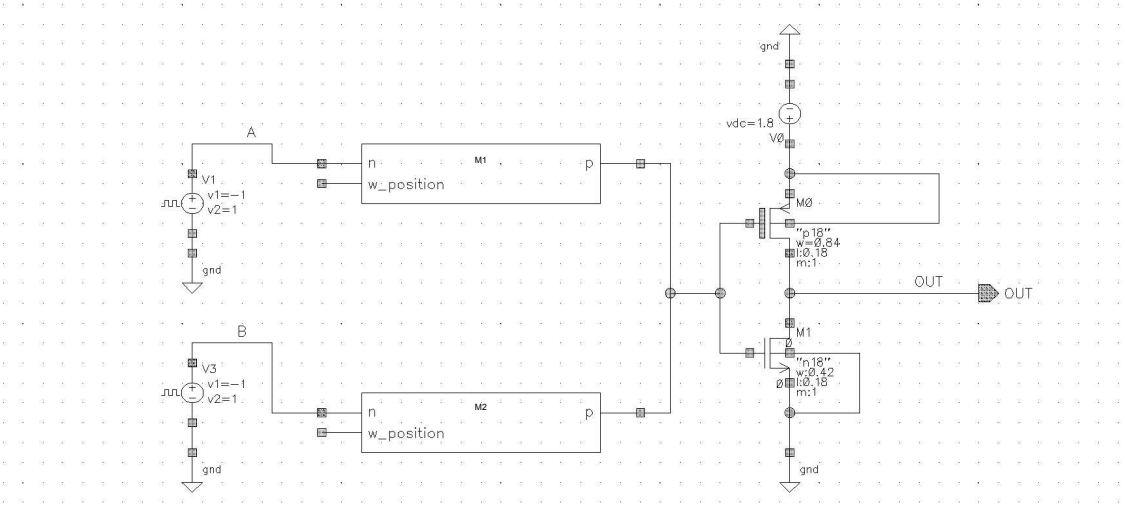

FIGURE 5.10: NOR gate schematics

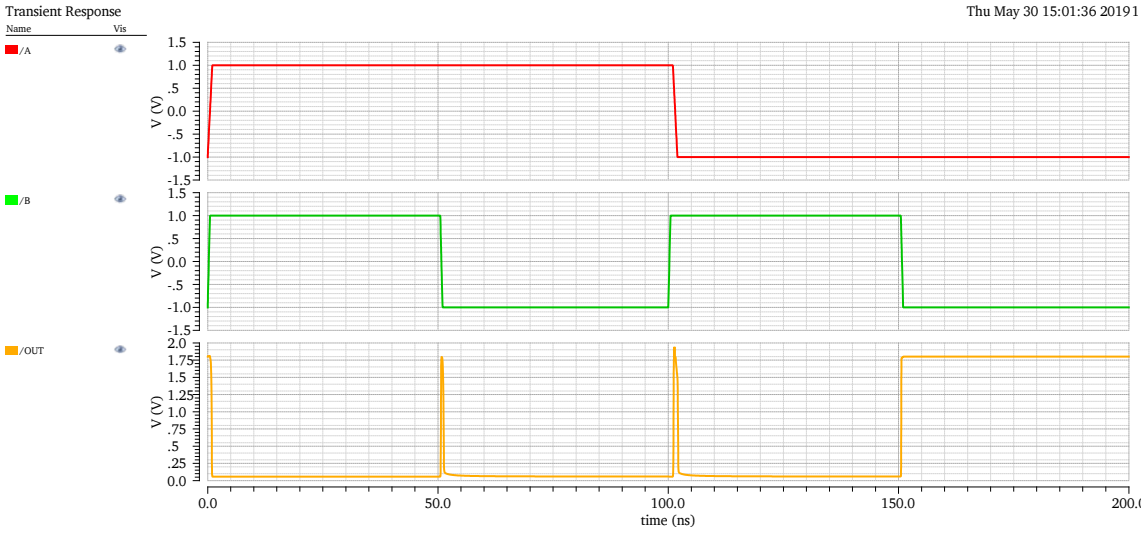

FIGURE 5.11: NOR gate result

causes the decrease in resistance of M1 and increase the resistance of M2. This results in the output at the common node became logic 1. This logic 1 is applied to inverter circuit made up of NMOS and PMOS. The NMOS become ON while PMOS is OFF. This results the output as logic 0. Figure 5.11 shows the NOR gate simulation result.

5.6 Effect on I-V Characteristic by Varying Memristor Width

As shown in Figure 5.12, when we increase the device dimension (D) at constant frequency from 2 nm to 10 nm, the hysteresis curve shrinks and the area below the I-V curve reduces. After watching MD I-V curve, we can conclude that the energy dissipation decreases as the dimension increases.

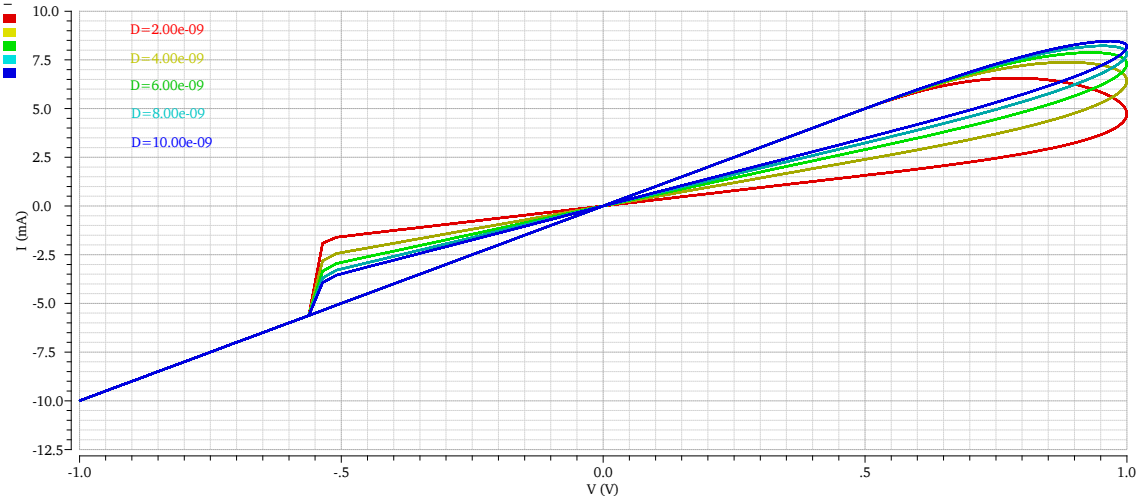

FIGURE 5.12: I-V characteristic by varying D

Chapter 6

Conclusion and Future work

6.1 Conclusion

In this work, we designed basic logic gates, NAND, NOR, AND and OR using VTEAM model in cadence virtuoso. Earlier we were using TEAM, Linear ion drift, Simmons tunnel barrier model; there is a current controlled mechanism in these models. In VTEAM model, we require threshold voltage to describe the characteristics of physical behavior accurately. The accuracy of this model was determined by using Verilog-A model. Its accuracy was further verified by simulating in cadence virtuoso and comparing it with the experimental results. This shows that MeMOS design, implemented using $Pt/TiO_{2-x}/TiO_2/Pt$ nanolayers is a better alternative to achieve low die area and high packing density.

6.2 Future Work

In this work, we are using VTEAM model for designing of logic gates. In future, by making use of these logics, we can redesign different circuits using memristor. By this, we can get a device having low cost & low power consumption.

In future, we can design a booting free computer, flash memory, DRAM and hard drive by using memristor.

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