A

DISSERTATION REPORT

ON

POLARIZATION ENCODED MULTI LOGIC FUNCTIONS USING MACH ZEHNDER MODULATORE WITH DIRECT DETECTION

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by

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Certificate

This is to certify that the dissertation report entitled **Polarization Encoded multi logic functions using Mach Zehnder Modulator with direct detection** submitted by **Saini Jitendra Kumar (2017PEC5485)**, in the partial fulfilment of the Degree Master of Technology in **Electronics And Communication** of Malaviya National Institute of Technology, is the work completed by her under our supervision, and approved for submission during academic session 2018-2019.

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Declaration

I, Saini Jitendra Kumar, declare that this Dissertation titled as "**Polarization Encoded multi logic functions using Mach Zehnder Modulator with direct detection**" and the work presented in it is my own and that, to the best of my knowledge and belief.

I confirm that the major portion of the report except the refereed works, contains no material previously published nor present a material which to be substantial extent has been accepted or the award of any other degree by university or other institute of higher learning. Wherever I used data (Theories, results) from other sources, credit has been made to that source by citing them (to the best of my knowledge). Due care has been taken in writing this thesis, errors and omissions are regretted.

Date : **Saini Jitendra Kumar**

Place : ID : 2017PEC5485

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Abstract

All-optical signal processing techniques are highly desirable in the future To increase the speed of optical network processing with large capacity and to avoid optical electro Optical (O-E-O) conversion. As the basic elements of all-optical Signal processing, optical logic gates are required for optical computing as well as optical networking. Addressing, Switching, Header Recognition, Data Encoding, Regeneration, Parity Checking And network coding. Thus, the implementation of various optical logic gate works In recent years has attracted much interest.

We have proposed a novel scheme for the realization of optical logic circuit using Mach Zehnder Modulators (MZM) with direct detection. Amplitude and phase information of the optical signals has been used for the differentiation of optical signals into four different states that can be represented using two binary inputs, while direct detection has been used for the effective mapping of these states with their respective binary outputs. The realization of 7 logic gates, 2 reversible optical logic gates (Feynman & Double Feynman gates) and half adder & half subtractor in a single optical circuit is achieved successfully. These all logical function is performed by a one set of hardware. High Extinction ratios (ERs) upto 50dB are obtained while keeping the data rate constant at 10 Gbps. Extinction Ration v/s Insertion Loss graphical representation is shown in this dissertation.

List of Abbreviation

2D	-	Two Dimensions
PPLN	-	Periodically Poled Lithium Niobate
NOLM	-	Non-linear Optical Loop Mirror
HNLF	-	Highly Non-Linear Fiber
SOA	-	Semi-conductor Optical Amplifier
MZM	-	Mach Zehnder Modulator
MZI	-	Mach Zehnder Interferometer
ER	-	Extinction Ratio
IL	-	Insertion Loss
CW Laser	-	Continuous Wave Laser
RF	-	Radio Frequency
OEO	-	Optical Electrical Optical Conversion
QPSK	-	Quadrature Phase Shift Keying
NIR	-	Near Infrared
RIMS	-	Resonance Ionization Mass Spectroscopy
GUI	-	Graphical User Interface
OSA	-	Optical Spectrum Analyzer
PRBSG	-	Pseudo-Random Bit Sequence Generator
LPF	-	Low Pass Filter
BER	-	Bit Error Rate
NRZ	-	Non Return to Zero
VLSI	-	Very Large Scale Integration

BCD	-	Binary Coded Decimal
XS-3	-	Excess 3

List of Symbols

f	-	Frequency
c	-	Speed of light
λ	-	Wavelength
$\Delta\lambda$	-	Line width
Δv	-	Frequency change
$\Delta\emptyset$	-	Phase change
$\Delta\eta$	-	Variation in Refrective index
d	-	Distance between electrodes
L	-	Length of Electrode Region
r	-	Electro optic coefficient
η	-	Refrective index
N	-	Refractive Index
nm	-	Nanometer
P_{in}	-	Power at output
P_{off}	-	Power at output for output low or 0
P_{on}	-	Power at output for output high or 1
P_{out}	-	Power at output
P_{out1}	-	Power at out port 1
P_{out2}	-	Power at out port 2
V_{π}	-	Voltage at $\Delta\varphi = \pi$
ω	-	Angular velocity
ψ	-	Sai function
ϕ	-	angle

R	-	Responsivity
I_{ph}	-	Photo current
q	-	Electron charge
η_c	-	Collection efficiency
V_{in}	-	Input voltage
V_{bias}	-	Bias voltage

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Chapter 1. INTRODUCTION

1.1 Introduction

Recently, it has been observed that high-speed performance can be achieved by reconfigurable computing. Next generation computing systems and optical networks rely on using high-speed optical logic gates as key elements for the implementation of signal processing functions [1]. Optical functions like signal processing, data encoding, address recognition, parity checking, counters etc requirement of optical-electrical-optical conversions [2-7].Two schemes based on non-linear optics and modulators are of vital importance [8].When the first type is considered Periodically Poled Lithium Niobate (PPLN) [9], silicon-nanowire [10], Non-linear Optical Loop Mirror (NOLM), Highly Non-Linear Fiber (HNLF) [11] and Semi-conductor Optical Amplifier (SOA) [12] are used. But this type suffers from the drawback of the requirement of high drain current for SOA and its poor speed limit [13-14]. HNLF based logic gates present very high dispersion & nonlinearly chirp noise signal when used with long fiber length [14]. The second type is Mach Zehnder Modulator (MZM) and Mach Zehnder Interferometer (MZI) that focused mainly on intensity information

To achieve the speed limit of electronic devices, demand for high bandwidth has grown rapidly. All-optical signal processing's overall aim is still on the horizon. The prototype of high-grade all-optical logic gates comes from the laboratories nowadays. In this sector, the research is moving forward to make it possible [15]. However, the digital gates are complex in the processing of optical signal and include electro-optical conversion. The development of all-optical technology is critical for the growth of future telecommunication networks, which would implement all node functions in the optical field [9]. Any optical functionality such as packet syncing, multiplexing the add-drop, clock retrieval, signal regeneration and address recognition are essential to stop optoelectronic conversions to the broadband and flexible network bottleneck. On the other side, when it comes to ultra-high bandwidth parallel computing, all-optica signal processing is regarded an alternative [11]. In potential large-capacity optical networks all-optical signal processing methods are useful in improving handling speeds, avoiding inefficient O-E-O [8] transformations. Optical logic gates are fundamental to all-optical signal handling in optical computation as well as optical

connectivity in addressing, changing, header identification, information encoding, recovery, parity monitoring and network coding.

There has been a lot of concern in latest years in implementing distinct optical logic gate features. Optical gates are essential to create the dream come true. Gates are the main components for carrying out all-optical tasks [5]. Therefore, several fundamental models are required to create digital gates in all optical logic gates on the same platform. All-optical logic gates are important components in the implementation of these functions. Some systems of all-optical logic gates [7], which use non-linear impacts in optical fibers, in semiconductor devices or in waveguides are noted in literature. In addition, several attempts were made to show that fresh buildings are suitable for the construction of optical logical gates. Several systems have recently been suggested for the production of optical logic gates. Nonlinearity [6] can be created in many respects, such as nonlinear loop mirror, non-linear fibre, photonic crystal, filter, wave manual, thyristor or semi-inducing optical printer, but HNLF is difficult for photonic inclusion, and PPLN [13] requires accurate temperature control. In addition, the PPLN requires a accurate temperature management. The latter systems include the adoption of different modulators and interferometers, which concentrate mostly on use of data on strength in the past.

1.2 Objective

An optical logic gate is physical component used for implementing Boolean function and performs logical operations on optical inputs. In an all optical system, an optical signal in a logic gate switch to another logic gate or function, a new scheme for reconfigurable logic circuit has been proposed that is based on MZM with a polarization phase shifter. Amplitude, as well as phase polarization of optical signal, has been utilized here along with usage of direct detection [16] at the output port. The function is easily implemented by adjusting the biasing of MZM and the phase shift of the optical signal. The advantage of this methodology is that different optical logic functions are implemented with the same hardware that has high scalability and simple configuration. 3-input 3-output hardware circuit has been proposed with three MZMs, two polarization phase shifters & switches. Extinction ratio [17] of all the logic function is as high as 50 dB has been observed. Eleven logic functions including universal gates, other logical and optical gates like OR, AND, XOR, XNOR, NOT, FEYNMAN, DOUBLE FEYNMAN and logic functions like HALF ADDER and

SUBTRACTOR [18, 19] can be realized using three MZM's and varying their biasing and phase parameters involved at speed of 10Gbps. Increment in number of gates reduce the speed.

This dissertation provides an experimental and simulation study of some new methods of all-optical signal handling for potential optical communication networks. The modulation format transformation, stage discrimination and clock recovery are all-optical methods. The comprehensive techniques in this dissertation are used to manualize signals within the optical domain by the Optical Mach Zehnder Modulator.

1.3 Thesis Organization

This thesis is organized in 6 chapters containing this introduction chapter. Following the introduction chapter, chapter 2 describe the literature survey of proposed work on optical logic gates, reversible Optical gates, half adder and half subtractor using Mach zehnder modulator.

In chapter 3, we have describe a brief introduction of the various component used in proposed design like CW laser, MZM and photodetector. In this chapter we also describe how polarization works which is very important mechanism of proposed design. Component's behaviour and its mathematical equations are explained in detailed.

In chapter 4, simulator tool OPTI-SYSTEM is discussed. How we can design a device through it and how any device is simulated in this simulator all steps are explained in this chapter.

In chapter 5, we have discuss operating principle of proposed design and according to that all the block diagram of all logic gates like NOT, AND, OR, NOR, NAND, XOR, XNOR gates, reversible logic gates like Feynman Gate and Double Feynman Gate, Half adder and Half Subtractor and their mathematical equations and by these equations Optisystem simulation graphs and results is explained.

Finally in chapter 6, conclusion of whole project and future work which can be done after this work is explained.

Chapter 2: LITERATURE SURVEY

The communication of fiber optics is a way of transmission by sending light waves via an optical fiber from one location to another. Fiber optic communication devices were first created in the 1970s, revolutionizing the telecommunications industry and playing a significant part in the emergence of the information age.

Pallavi Singh [20] this paper discusses the all-optical gates and present their condition and models. Different systems are debated and contrasted with and without semiconductor optical amplifiers. The optical gates are categorized by their designs. It is split into two main branches: non-semiconductive optical amplifier gates and optical amplifier-based semiconductor gates.

Sunny G. Lau [21] proposed a work on CW laser. Use of lasers for the selective sectioning of component of interest includes the implementation of RIMS in nuclear forensics. Although existing technologies include pulsed lasers for analysing nuclear detonation debris, the use of continuous wave or CW lasers can also be taken into consideration.

Piyush Singh [22] proposed a work on reversible logic gates. Reversible logical gates decrease the energy by removing energy loss in easy activities during standard logic gates when you lose one piece of information. The primary aim of this article is the comparison between their activities and their apps to provide basic principles for a few reversible logical gates.

Amir Arashlouzadeh[23] proposed a work related to polarization of light. In their thesis, he mainly focus on the multi-band frequency shifting interferometry based on polarization measurement for 3D surface modeling.

Giuseppe Pecere [24] is proposed a work on MZM. Study and assess the efficiency of the technique using an RF test to determine the phase difference and the amplification distinction (dB) of the MZ modulator through both theoretical analytics and program VPI simulations. The Mach-Zehnder Modulator study theoretically and numerically.

Sibastien Agnolini and Philippe Gallion [25] in this paper he propose to use Mach-Zehnder dual electrode modulator for implementing the quantum key distribution protocol of Bennett and Brassard. This application enables for the generation of QPSK signals with separate bases and symbols.

Lorenzo Colace [27] is proposed a work on photodetector. Applied optoelectronics study has spent a great deal in light detection by Near Infrared (NIR). For a variety of applications, the NIR spectral region covers the range of wavelengths from 750 to 2000 nm. Researchers from around the globe have achieved outstanding outcomes in this region, from communication to medicine, including distant sensing in satellite apps, as well as economic and industrial tracking. In particular, optical communications are the workshop for the creation of high-level detection technology.

Xianfeng Tang [8] he introduced a new system to carry out all-optical logic gates with a single I / Q modulator with direct detection is being proposed and investigated. Intensity and phase of the optical signal are used to display the four distinct states of two binary outputs and to match the four states to the appropriate binary output with direct detection. It's a very straightforward and high-speed construction. The two arms of MZM is bias voltages for moving signals and the phase shift can be used to adjust every fundamental logical gate.

G. Berrettini [28] proposed A novel, simple, compact, and integrable scheme of reconfigurable and ultrafast photonic logic gate is demonstrated, based on a single semiconductor optical amplifier (SOA) and able to process ultrafast signals.

Chapter 3. MODULES OF PROPOSED DESIGN

3.1 Continuous Wave (CW) Lasers

The various current researches have shown that the continuous wave laser may be easily tuned RIMS apps to frequencies relevant to various isotopes of a specified component mainly restricted by the time reliance of ionization and the energy and pointing stability laser parameters. The CW laser will offer uninterrupted continuous output energy at the same frequency (f), wavelength (λ) and light velocity (c) associated with:

$$f = \frac{c}{\lambda} \tag{3.1}$$

In fiber optic communications, this kinds of laser is frequently used to convey data thr ough wave amplitude modifications. A CW laser has a distinctively smaller line width ($\Delta\lambda$) and and inversely a higher frequency change (Δv) given by:

$$\Delta\lambda \approx \frac{\lambda^2 \Delta v}{c} \tag{3.2}$$

3.1.1 The properties of Laser

The various Laser features includes its stability and relatively narrow line width at the required wavelength ($\Delta\lambda$), which are being achieved on mode, frequency being stable all the time and tuning dependency of laser. There are broad and variable techniques to control these parameters, but for prediretable RIMS techniques it is essential to control the parameters.

1. **Single Mode Lasing**

As a consequence of constructive transverse interference, lasers will inherently have s everal modes. The lasing single mode assumes a narrow line width beam without being a multimode and keeping it in single mode only. It is a joint exercise between temporal and spatial coherence which leads to one lasting mode. The interaction may be observed or controlled in many ways, and the most common way is by controlling the cavity length. The cavity length has to use gratings and angle adjustment to select only one colour among the polychromatic beam. Method for concurrent time and space controls lead to what is known as a tuneable laser for wavelengths.

2. **Stability of Mode Frequency**

The single mode control will limit of the wavelength to a single wavelength. However, various modes can still be controlled with a medium of gain (see Figure 8). The laser mode frequency can alter with moment because of temperature modifications (heat up) that affect the refractive rate and the cavity velocity. The piezoelectric transducer being used will be regulated through a feedback loop in the required frequency and is an active way of limiting frequency changes. In determining wavelength and shape, mode frequency stability is essential to comprehend.

3.2 Mach-Zehnder Components

The Mach-Zehnder interferometer is the most significant instrument of our measurement scheme. First of all we explain the MZI in terms of its features and transfer function as an optical filter; then we concentrate our attention on the MZI as a modulator with its behaviour and transfer function. The MZI modulator is the tool in our scheme for the acquisition of the modulated RF test signal. It is used as a testing the validity of the suggested characterization technique. The objective to study the signal in these parts before and after its conversion.

3.2.1 Mach-Zehnder Interferometer (MZI)

The fundamental concept of this device is the interferometer impact: the input signal is split between the two arms, each arms changes a phase shift at the signal and the two signals coming from the two arms and joined at the output which can be seen in the Figure 3.1.

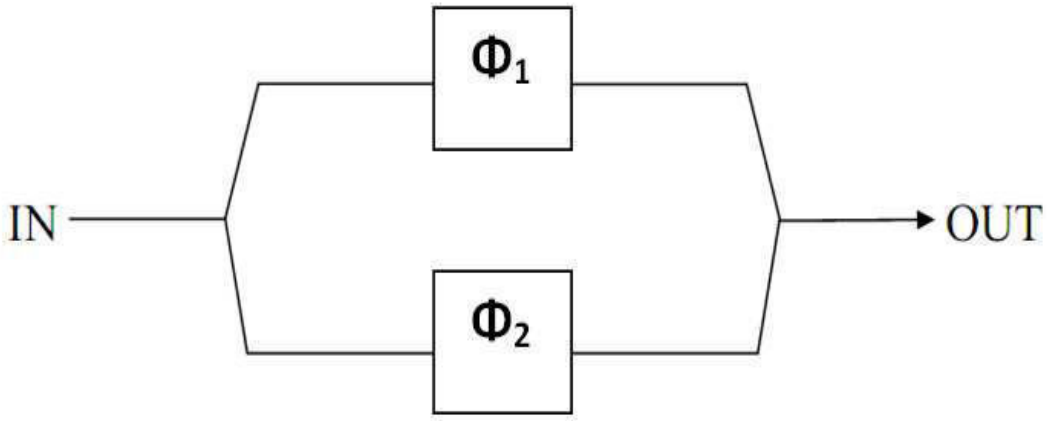


Figure 3.1 Mach Zehnder Interferometer

3.2.2 Mach-Zehnder Modulator

The MZI modulator is now introduced. The input light is divided into two waveguides which has a two conducting electrodes in Mach-Zehnder modulators, as Fig. 3.2 shows. The electro-optical impact induces a modification of the refractive index of every arm of the interferometer and modules the light propagated to that arm by the electric voltage on each electrode. This phase modulation is transformed into intensity modulation by merging the two routes with distinct phase modulations.

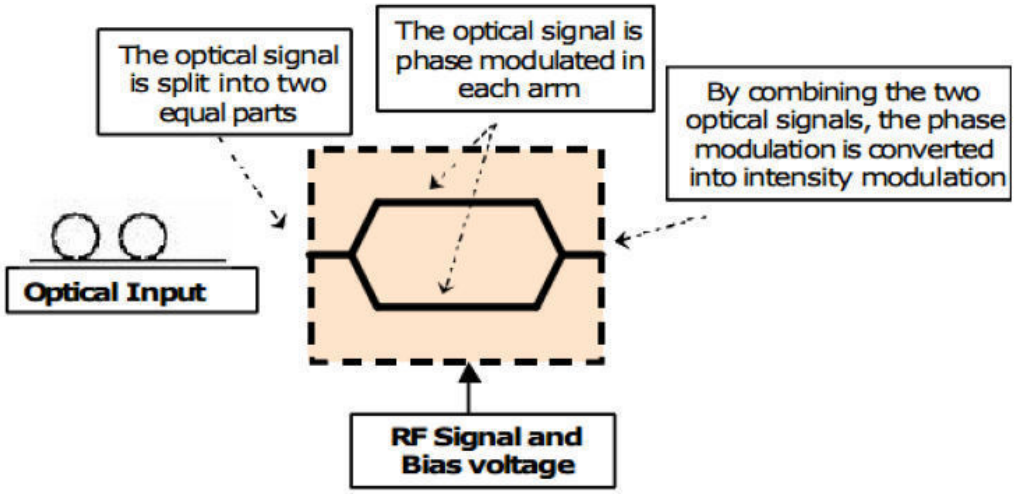


Figure 3.2: schematic diagram of MZM

Basic principle of MZM is phase variation is cause due to applied voltage on optical signal carrying arms and because of electro optic effect refractive index of media change slightly and it creates phase difference.[19] As shown in above figure optical signal is launched from IN port and splits in two equal parts as it passes through 3dB coupler, as both arm are same in length and have same refractive index so no chance of relative phase shift between both. But if we apply some voltage at any one of arm or both arms the refractive index of one or both change due to electro-optic effect according to applied voltage bias and corresponding phase shift occurs.

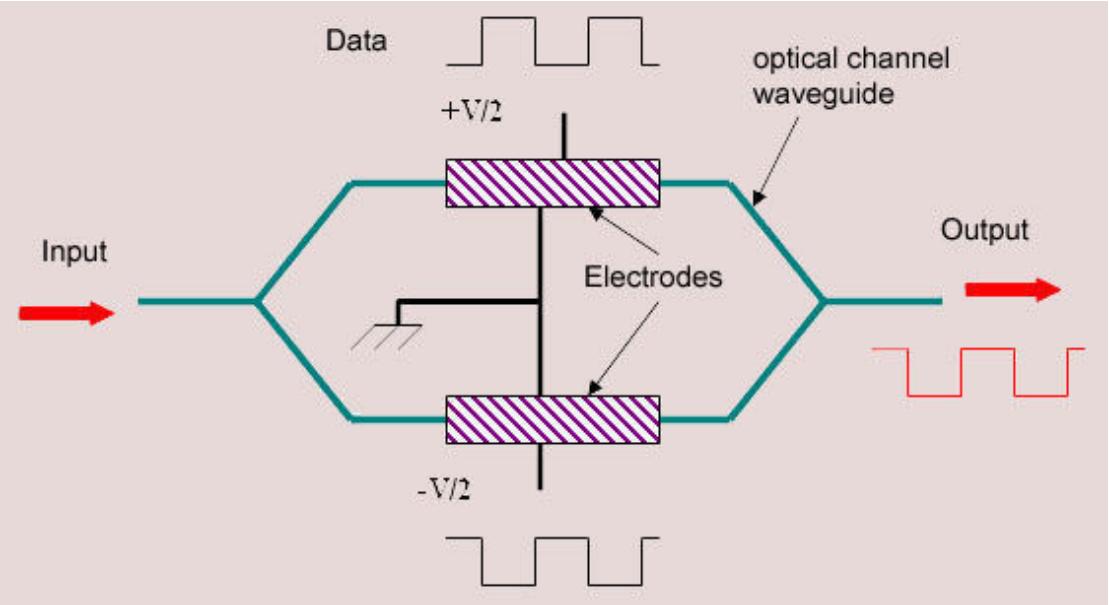


Figure 3.3: MZI Modulator scheme

Sometimes only single arm used to applying electrical signal and sometimes both arm used one for dc biasing and other for electrical signal. Both arm's signal again interacts with each other at next coupler, here both signal interface and phase modulation is converted in to intensity modulation and modulated optical signal emerge from OUT port.

The phase change (ΔØ) equation for the propagation through the interferometric arms can be given as.

$$\Delta\emptyset = \frac{2\pi}{\lambda}\Delta\eta \tag{3.3}$$

The equation for half switching voltage is given as below

$$V_\pi = \frac{\lambda}{\eta^3}\frac{d}{r}\frac{1}{L} \tag{3.4}$$

Where L is the interferometer arm length and $\Delta\eta$ shows the variation in refractive index by the applied electrode voltage. When no voltage is applied to electrodes $\Delta\phi$ is zero, and for a particular applied voltage if $\Delta\eta$ equal to π, then this particular voltage is known as V_π or switching voltage or half wave voltage. Where d explains the distance between electrodes, η is the refractive index of the material and r is the electro-optic coefficient. Normalized power at output ports is given as Pout1 and Pout2. Using P1 and P2 we can calculate extinction ratio and insertion loss.

$$I.L.(dB) = 10log\frac{P_{out1}}{P_{in1}} \tag{3.5}$$

$$Ex.R(dB) = 10log\frac{P_{on}}{P_{off}} \tag{3.6}$$

Here P_{ON} is the output power for input high, or 1 and P_{OFF} is the output power for input low, or 0. In this project, this kind of MZI switch modulator is implemented for the visible light communication at visible wavelengths with reasonable small size.

3.3 Polarization

It is one among the main variables of concern in the dissertation. It explains about the pattern of the electromagnetic waves that are oscillating. Many of the lights is partially polarised. This implies that the Ex and the Ey parts oscillate randomly in the x and axis when light propagates in the-z direction. But the parts swing in one specific direction for a polarized light. The polarization filter have some kind of atoms aligned in order to block unwanted directions of vibration as shown in Fig. 3.4.

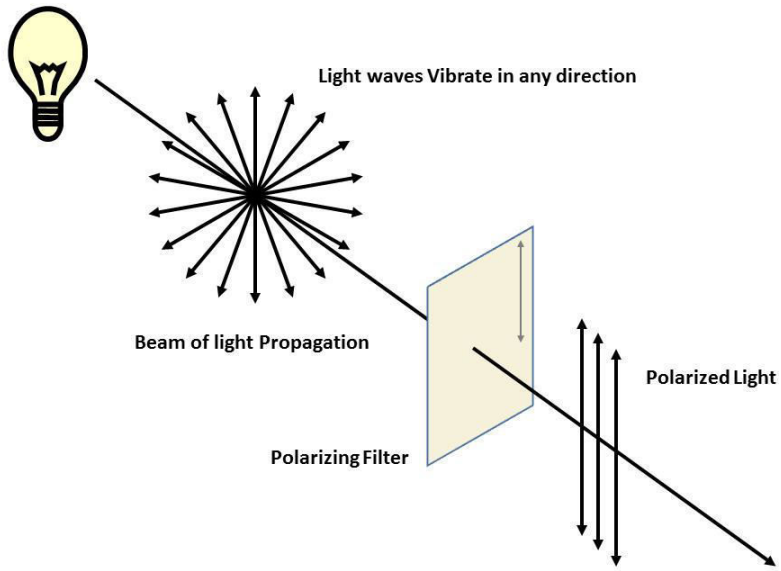


Figure 3.4: Polarization of light

The three different kinds of polarization are linear, circular and elliptical and these are also called as states of polarization. Two orthogonal parts can be represented as an optical plane wave as shown below:

$$Ex = Ax(\omega t - kz + \delta 1) \quad (3.7)$$

$$Ey = Ay(\omega t - kz + \delta 2) \quad (3.8)$$

The wave is linearly polarized if phase difference ($\delta 1$- $\delta 2$) is 0 or π (Figure 3.5)

The phase difference is $\frac{\pi}{2}$ or $-\frac{\pi}{2}$ in the circular polarization. If it is $\frac{\pi}{2}$, then light is anticlockwise circularly polarized and if it is $-\frac{\pi}{2}$ it is clockwise circularly polarized. The amplitude of the input two perpendicular waves must be equal so it is circularly polarized light.

This equation should be satisfied with an elliptically polarized light:

$$\left(\frac{E_x}{A_x}\right)^2 + \left(\frac{E_y}{A_{xy}}\right)^2 - 2\left(\frac{\cos\delta}{A_x A_y}\right) E_x E_y = \sin^2\delta \qquad (3.9)$$

Here δ= δ1-δ2,

This equation shows the geometric representation as shown in Figure 3.5.

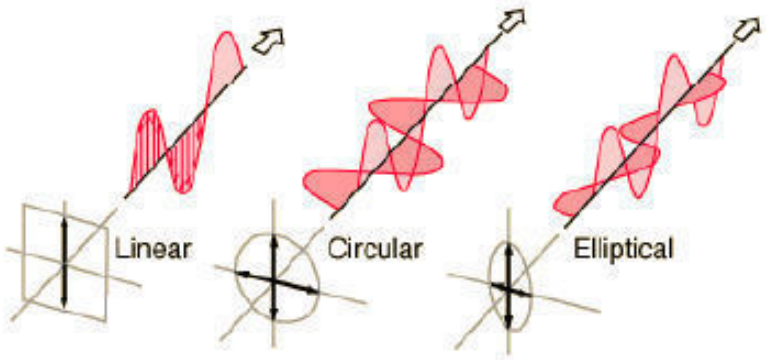


Figure 3.5: Polarization representations of Linear, Circular and Elliptical

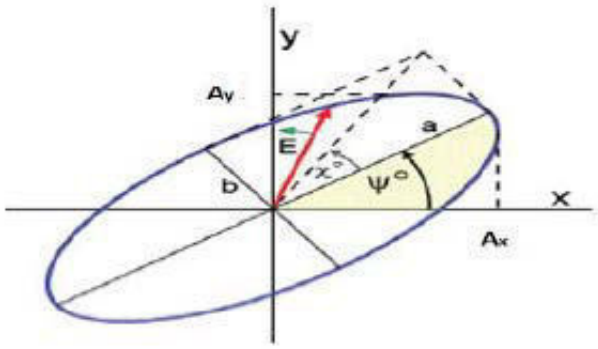


Figure 3.6: Ellipse polarization

According to the above figure we can wright these equations:

$$\psi = \tan^{-1}\frac{A_y}{A_x} \quad ; \qquad 0 \leq \varphi \leq \frac{\pi}{2} \qquad (3.10)$$

If the ellipse is rotated by an angle denoted as ϕ by its origin, then

$$\tan\delta = \frac{\tan^2 x}{\tan^2\phi} \qquad (3.11)$$

We will discuss Poincare values in the following categories:

Several methods have been proposed according to the names of their creator to categorize and apply these polarisation states more efficiently that is parameters of stokes, sphere of Poincare and matrices of Jones. In this dissertation we would like to use the parameters of Stokes that we will discuss as follows:

Stokes parameters:

$$\left.\begin{aligned} S_0 &= {A_x}^2 + {A_y}^2 \\ S_1 &= {A_x}^2 - {A_y}^2 \\ S_2 &= 2A_xA_x\cos\delta \\ S_3 &= 2A_xA_x\sin\delta \end{aligned}\right\} \quad (3.12)$$

The four quantities are shown to be in the equation

$${S_1}^2 + {S_2}^2 + {S_3}^2 \leq {S_0}^2 \quad (3.13)$$

Where S_0, S_1, S_2, S_3 all lies between [-1 to 1].

The sign of equality is true for a completely polarized wave. For each polarization, we can create a vector and this vector is shown as following:-

1. Horizontally linear polarized wave: $\begin{bmatrix}1\\1\\0\\0\end{bmatrix}$
2. Vertically linear polarized wave: $\begin{bmatrix}1\\-1\\0\\0\end{bmatrix}$
3. Linear polarized wave with an 45° angle: $\begin{bmatrix}1\\0\\1\\0\end{bmatrix}$
4. Linear polarized wave with an -45° angle: $\begin{bmatrix}1\\0\\-1\\0\end{bmatrix}$
5. Left-handed circularly polarized wave: $\begin{bmatrix}1\\0\\0\\1\end{bmatrix}$
6. Right-handed circularly polarized wave: $\begin{bmatrix}1\\0\\0\\-1\end{bmatrix}$

3.4 Photodetectors

The inner photoelectric effect is the fundamental principle of photodetection. In a bandgap (E_g), semiconductor material illuminated by a wavelength optical beam, if the energy of the incident photons E_{ph}= hc/λ (here c represent the speed of light and h represent the plank constant) exceeds the material's energy bandgap, one electron is

move to the conduction band after each photon absorbed. Every time an electron-hole couple is generated and an external electric field can be used to collect the photo carriers in an external circuit and convert the optical signal into electrical signal. The figure of merit showing how effectively light is converted into photocurrent. Responsivity (R), the ratio between the photocurrent (I_{ph}) versus the incident optical power (P_{in}) is shown below:

$$R = \frac{I_{ph}}{P_{in}} \tag{3.14}$$

The incident light power and photocurrent can be represented as the photocarrier generation rate G and the photon flux ϕ:

$$R = \frac{Gq}{\phi_{in} h\nu} = \frac{Gq\lambda}{\phi_{in} hc} = \eta \frac{\lambda}{1.24} \tag{3.15}$$

Where q is the electron charge, v = $\frac{hc}{\lambda}$ the frequency of the light, η the quantum efficiency; λ is expressed in micrometers. The quantum efficiency is an important parameter representing the capability of the photodetector to convert a photon in an electron-hole pair; if η is 1, every single photon generates a carrier pair. If we consider a photoconductor of thickness d, neglecting reactions at the interface, the quantum efficiency can be expressed in function of the absorption coefficient α as:

$$\eta = \eta_c(1 - e^{-\alpha d}) \tag{3.16}$$

where η_c is the collection efficiency, i.e. the percentage of carriers generated and contributing to the photocurrent.

3.4.1 Junction Photodetectors

In this section I introduce junction photodetectors. The simplest junction photodetector shown in Fig. 3.7 consists of a p-n diode whose internal electric field is used to collect the photocarriers generated by light. The photocurrent is associated to two fundamental mechanisms: drift and diffusion.

The main contribution is the drift current associated to the carriers generated in the space-charge region. There the generated electrons and holes are swept and transported by the electric field to the neutral regions where they recombine with majority carriers from the electrodes. As the drift current depends on the generation in the depletion area, applying a reverse bias to the diode helps to increase both the absorption efficiency and the collection efficiency. By consequence the photocurrent in the drift regime increases with reverse voltage.

Photons absorbed in the neutral regions generate photocarriers that partially con- tribute to the photocurrent. In fact, the absence of electric field allows the generated carriers to recombine without affecting the charge neutrality. Only the photocarriers generated in the proximity of the space charging region can lead to the photocurrent. Defining the diffusion length L_n, L_p as the average distance covered by an electron (hole) before recombining, if the photocarrier is generated within a diffusion length from the space charge region it can reach it by diffusion and collected by the electric field. This current represents the diffusion contribution to the photocurrent and, as it is not affected by the electric field, it is constant with the reverse bias. The different absorption regions and the associated collection mechanisms (drift and diffusion) are pointed out in Figure 3.7.

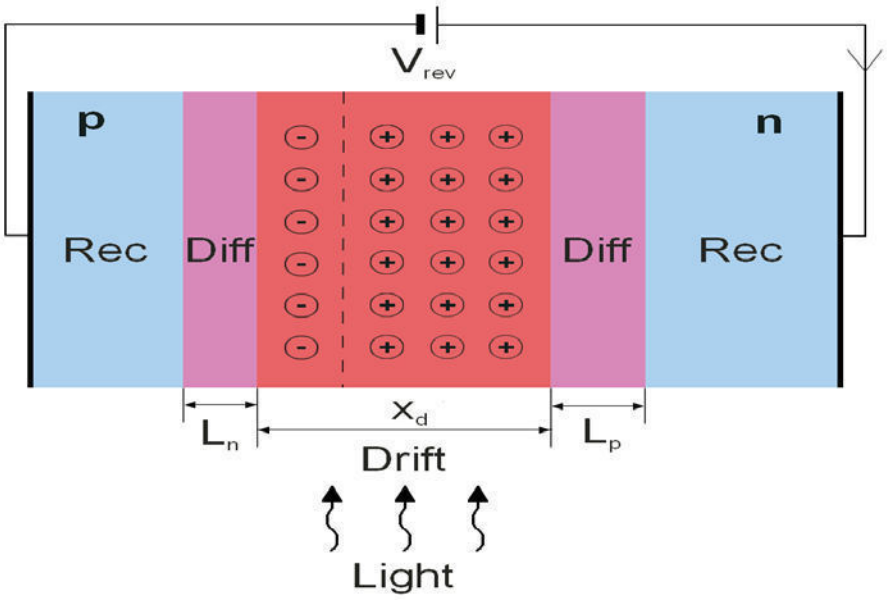


Figure 3.7: p-n junction

Absorption regions in a p-n photodiode. Only photocarriers generated in the depletion region (X_d) and within a diffusion length (L_n;L_p) contribute to the total photocurrent While transit and diffusion time rule the intrinsic time response of these devices, it is important to point out that the bandwidth is also limited by the parasitic components determining the extrinsic response.

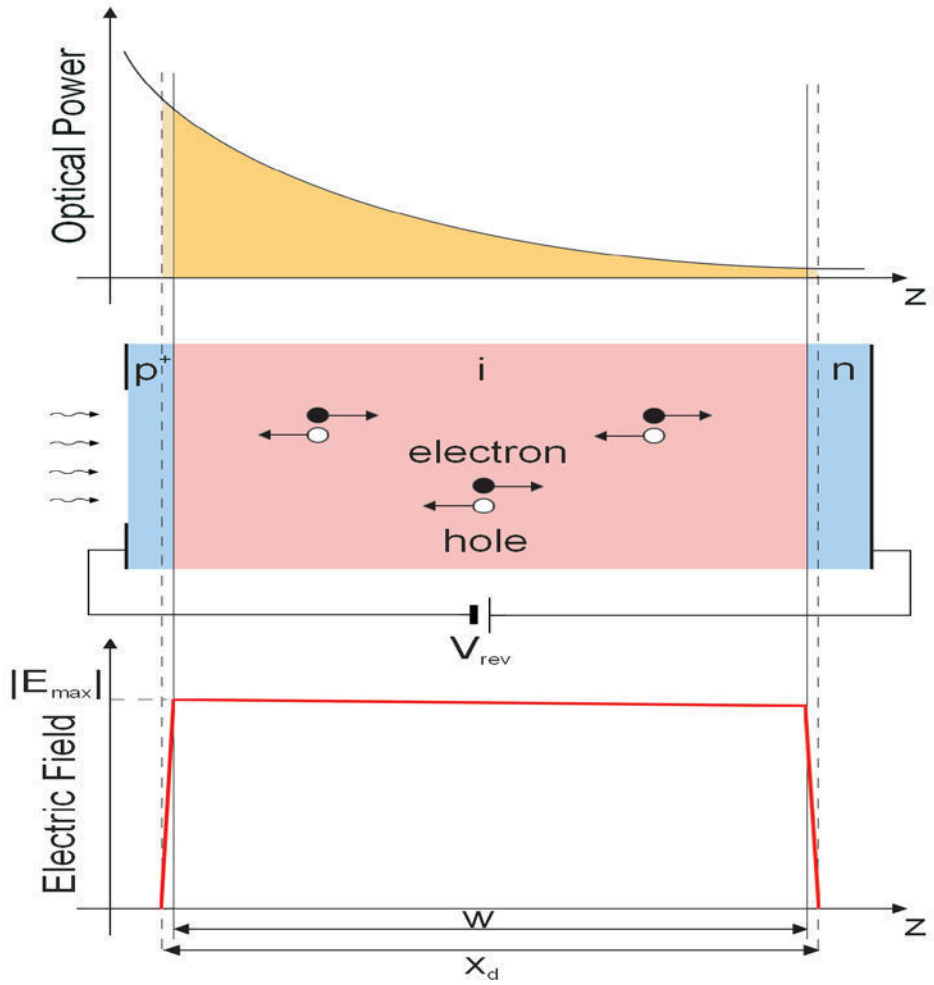


Figure 3.8: p-i-n junction - Illustration of a p-i-n device with optical power and the electric field distribution. Acting on the intrinsic layer width it is possible to optimize the optical absorption and the time response.

PIN photodiodes exhibit better performance with respect to the p-n ones. In fact in p-n photo detectors it is very important to properly tune the doping levels to achieve a better trade-off between neutral region resistivity and depletion region width. In p-i-n photodiodes this is less crucial because it is possible to act on p and n doping without affecting the depletion region restricted to the i -layer width.

Before we have dealt with the optimization of the photodiode structure in terms of temporal response without being concerned by the responsivity. Let us consider a normal incidence p-i-n photodiode as in Fig. 3.8. We have to minimize w in order to optimize the overall bandwidth; however, if the material absorption at the incident wavelength is not high enough, we could have a fast photodiode with a very low responsivity.

Unfortunately, this is unavoidable when photodetectors operate near the absorption cut off wavelength. In such conditions it would be crucial to treat the photon absorption and the photocarrier collection independently. The solution is represented by distributed absorption in guiding structures where photocarriers are collected normally to the propagation direction. Let us consider a p-i-n structure forming a ridge waveguide with the junction plane parallel to the propagation direction, as in fig. 3.8; unfortunately, this is unavoidable when photodetectors operate near the absorption cut off wavelength. In such conditions it would be crucial to treat the photon absorption and the photocarrier collection independently. The solution is represented by distributed absorption in guiding structures where photocarriers are collected normally to the propagation direction. Let us consider a p-i-n structure forming a ridge waveguide with the junction plane parallel to the propagation direction, as in Fig. 3.9;

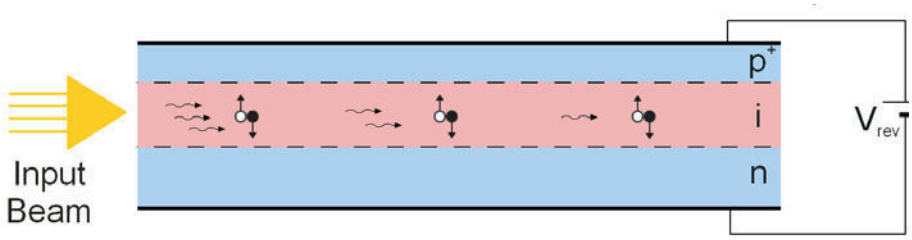


Figure 3.9: P-I-N Waveguide Photodetector.

Chapter 4. OPTISYSTEM TOOL

4.1 Introduction

Optical communication systems design and analysis, which usually include nonlinear equipment and non-Gaussian sources of noise, are very time-consuming and highly complicated so we use new software which is more effective.

OptiSystem is an advanced simulation package for optical communication scheme, designed, tested or optimized the physical layer which has wide variety of optical systems by nearly any optical link type. It's a simulator based on fiber-optic communication systems realistically modelling. According to the user parts, its capabilities is expanded readily and effortlessly interfaced with a large range of component. A Graphical User Interface (GUI) controls the optical component design and net list, display graphics and component models. The comprehensive library of active and passive components includes wavelength-dependent parameters and realistic elements.

4.2 Features of software

- **Component Library**

  Based on the chosen precision and effectiveness, component modules should be replicate the actual performance of the actual system and definite effects.

- **Mixed signal representation**

  OptiSystem combined signal arrangements in Component Library for both electrical signals and optical signals.

- **Measured components**

  You can enter factors which is measured from actual components using the OptiSystem Component Library. This is integrated into testing and measuring facilities from distinct providers.

- **Integration with Optiwave Software Tools**

  The OptiSystem enables the use of certain Optiwave component instruments, including OptiAmplifier, OptiGrating, OptiBPM, OptiFiber and WDM Phaser for embedded fiber and optic applications.

- **Advanced visualization tools**

  OSA's spectrum, visual charts, constellation charts, polarization state, signal chirp and many other advanced visualization tools are available.

- **Data monitors**

  After the simulation ends, you can select component ports for data storage or attach the monitor. At a time many visualizers can be connected at the same port to monitor signals.

- **Multiple layouts**

  Using the same project file, you can generate many designs that allow you to easily and effectively generate and change your designs. A different design version can be contained with every project file.

- **Report page**

  With a fully customizable report page, you can show any set of parameters and outcomes in the design. The reports produced are organized in 2D and 3D graphs and resizable and moveable spreadsheet.

- **Parameter sweeps and optimizations**

  If parameters changes in same layout so for changing this parameter Sweep iteration is used. To achieve accurate results, parameters can be maximize or minimize through optimization in the Optisystem simulation. Combinations of different parametric sweeps along with different optimization.

- **Bill of materials**

  OptiSystem offers system design, system, layout or component cost assessment table for the system being built, organized.

4.3 Quick Start

Now we'll learn how to load a model, simulate, customize local parameters and global parameters, and get outcomes.

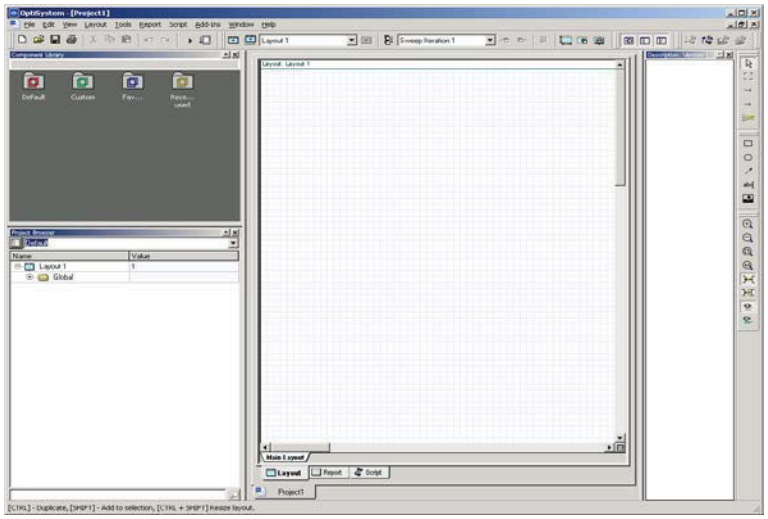


Figure 4.1: Graphical user interface (GUI) in OptiSystem

- **Main Feature of the GUI (1 of 3)**

1. **Project layout :-**

   This window shows in Figure 4.2 is the work area where element is inserted and edit their parameters of the component.

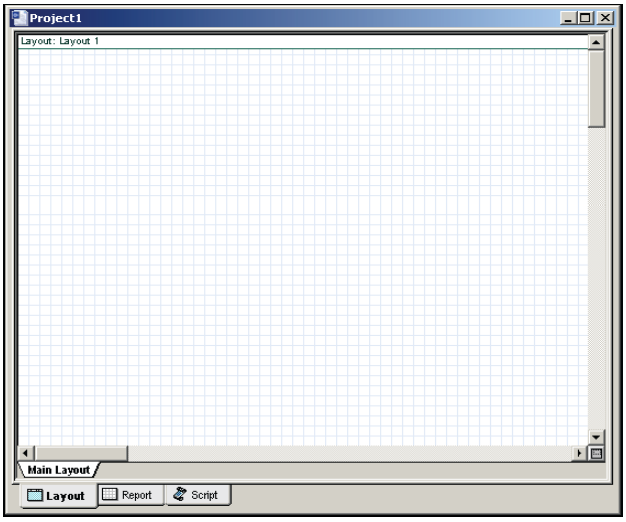


Figure 4.2: project layout window

2. **Dockers :-**

   To show the active (present) project data. Component Library, Access elements for designing the system. Project Browser is formatting the

project to obtain outcomes further effectively. Displaying in Figure 4.3 is the detailed project details of that layout.

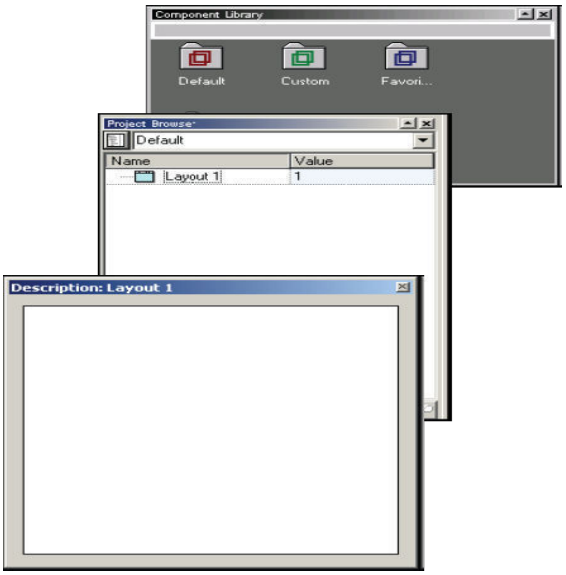


Figure 4.3 Docker layout window

3. **Status Bar :-**

Display the project advance calculation data for using OptiSystem and other assists. This window shows in Figure 4.4 is display in the layout's bottom.

Figure 4.4 Status bar window

- **Direct Modulation sample file:-**

i. Pseudo-Random Bit Sequence Generator (PRBSG):- it generates the bit sequence and transmit to the NRZ Pulse Generator.

ii. MZM is used for modulate the signal and it modulate the optical signal according to the electrical signal.

iii. Signal can be received by the PIN photodetector and it convert the optical signal into electrical signal.

iv. LPF filter is used to reconstruct the message signal.

v. Optical Time Domain Visualizer is display a response of optical signal in time domain.

vi. Oscilloscope Visualizer is display a response of optical signal in frequency domain.

vii. BER Analyzer is show the response of the signal and compare before and after propagation response.

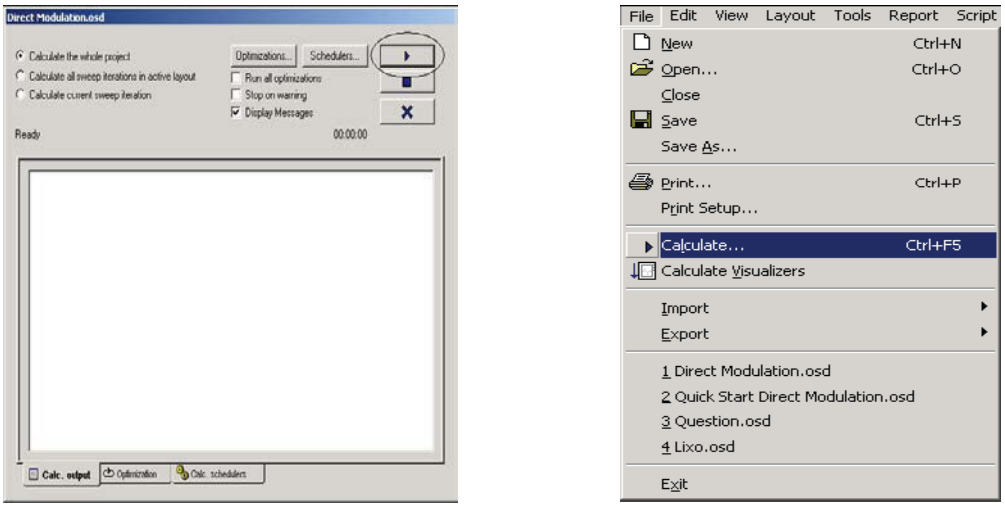


Figure 4.5 OptiSystem Calculations dialog box and calculate from File menu

- **Using the Layout Editor**

The following layout will be modified: the laser modulation system will be changed from direct to external modulation

- The Laser Measured component can be deleted and Edit by double click on the component.
- In Component Library add Default and then chose Transmitter Library and select optical Source.
- In Project layout add CW Laser
- Autoconnect links components in the Project design automatically.

- **CW Laser added to Optical Layout**

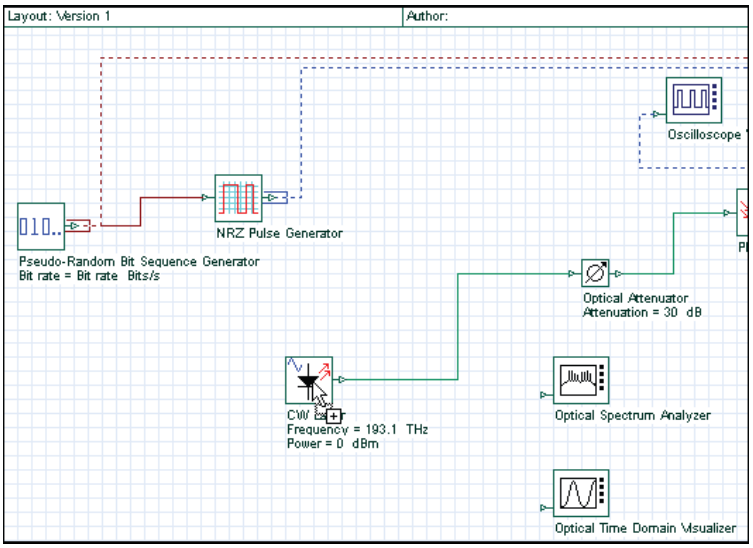


Figure 4.6: CW Laser added to Optical Layout

- **Mach Zehnder Modulator**
  - Select Default and choose Transmitters Library and select Optical Modulators from Component Library
  - Select Mach Zehnder Modulator and add in Project Layout
  - The output port of the NRZ Pulse Generator is linked to the Mach Zehnder modulator input port.
  - The CW Laser output channel is linked to the Mach Zehnder Modulator input port of the Carrier.
  - The output port of Mach Zehnder Modulator is linked to the Optical Attenuator input port.
  - Connect the output port of the MZM to the optical spectrum Analyzer input port and to the Optical Time Domain visualizer.

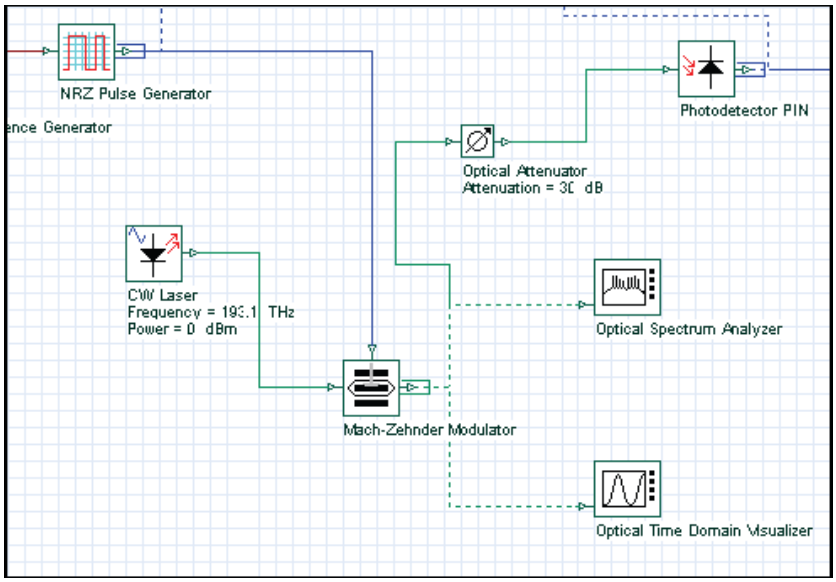


Figure 4.7: Mach Zehnder Modulator is connected to visualizers

- **How to select Calculate in the File menu and the dialog box for designs of the OptiSystem appears.**

- Select Run button.
- Outcomes are shown in the Output Design window.
- Double-click visualizers to view the graphs and results.

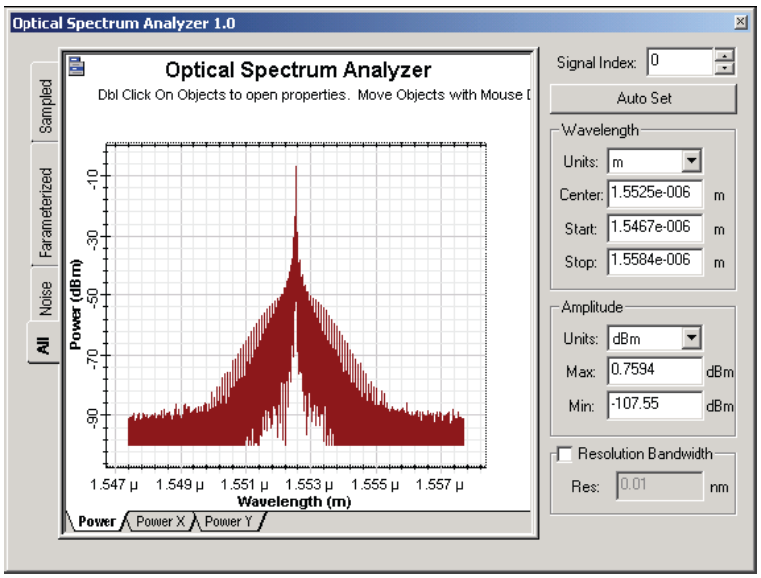


Figure 4.8: Visualizer results and OSA example

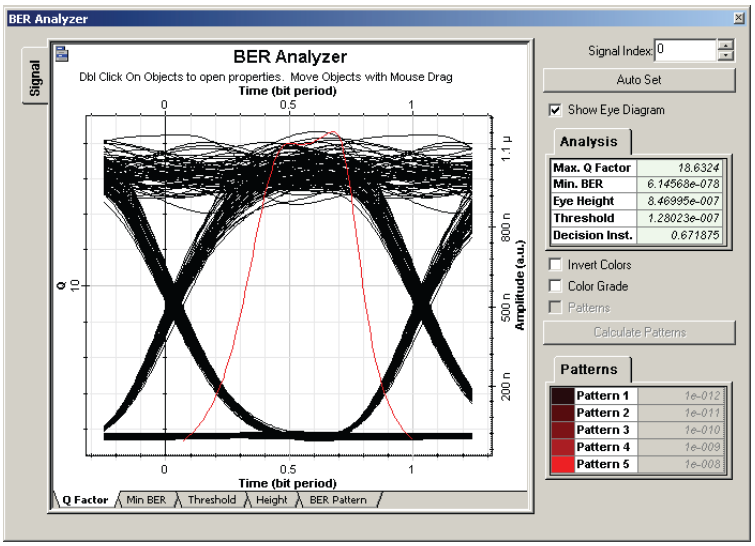


Figure 4.9: Visualizer results and BER example

Chapter 5. RESULTS AND ANALYSIS

5.1 OPERATING PRINCIPLE

The circuit schematic as shown in Fig. 1 comprising of the Continuous Wave laser (CW laser), three MZM's driven by three binary data input sequences which are connected in parallel, three photodetectors, two polarization phase shifters, and two switches. 3 input 3 output ports are designed for different optical logic functions and adjustment of input signal amplitude and phase gets used for the selection of the logic function of interest. The basic formula for an output of MZM is shown below:

$$|E| = \frac{1}{10^{\frac{I}{20}}}\{\cos[\frac{\pi}{2V_\pi}(V_{in}(t) - V_{bias})]e^{j\frac{\pi V_{bias}}{2V_\pi}}\}\begin{pmatrix} a_x \\ b_y e^{j\theta} \end{pmatrix} e^{j\varphi} \qquad (5.1)$$

Where I is the insertion loss of MZM, V_π is the half wave voltage, $V_{in}(t)$ shows input signal voltage & V_{bias} shows biasing voltage of MZM.

For a typical 3x3 logic circuit we can arrange input & output ports according to the requirement of that particular logic circuit. As show in Fig. 1 Port 1, Port 2, Port 3 are input Ports. Port 4, Port 5, Port6 are output ports. The 2x1 logic gate performs mapping of all the 4 combinations of the 2 binary inputs [(0,0), (0,1) (1,0), (1,1)] to their desired/respective output state (0 or 1). The key factor behind this is vector addition.

CW laser with 10dBm power, 100 kHz line width and 193.1THz operating frequency has been employed at the input of the experimental setup as shown in Fig. 5.1. The three MZM's in parallel driven by input binary data of amplitude 2 a.u. gets biased and polarized accordingly based on the input binary data for the realization of different logic gates and functions, the details of which has been summarized in Table.1. The input signal of 10Gbps is generated using the input bit sequence and the eye diagram detection and wave form recording has been done by the use of an oscilloscope.

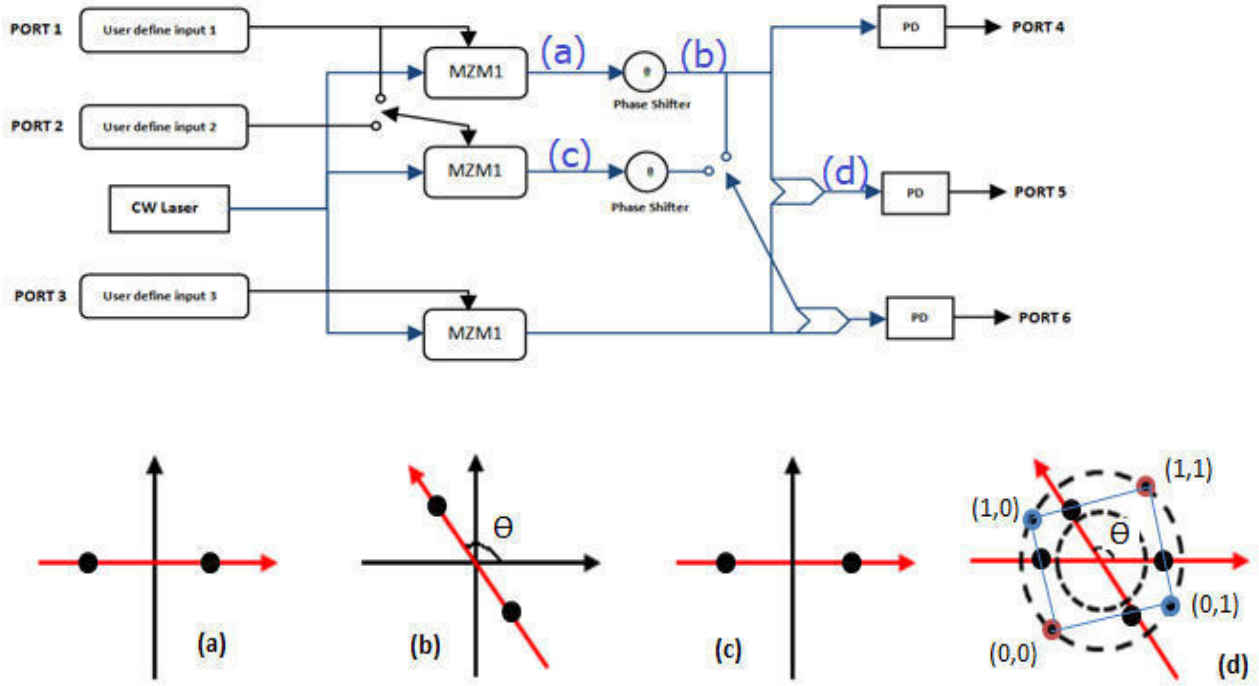


Figure 5.1: Schematic diagram for logic gate implantation using MZM's describing operating principle of logical OR gate (a).constellation at MZM 1 output. (b). constellation at phase shifter output. (c). constellation at MZM 3 output. (d). constellation after vector addition.

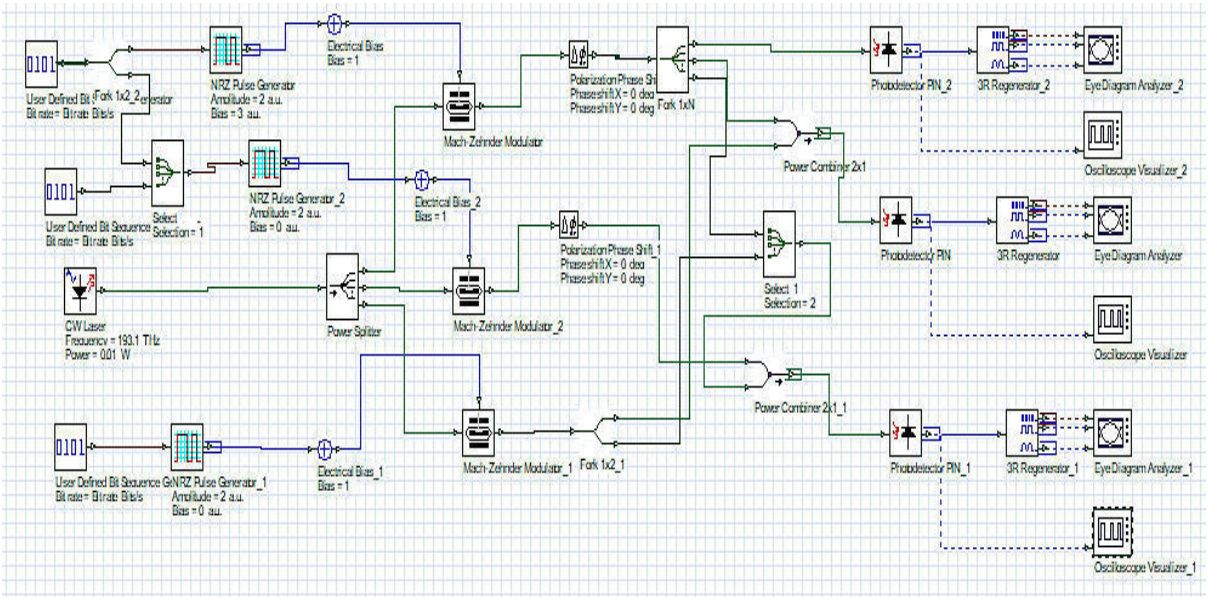


Figure 5.2: optisystem layout of design

Input bits used in proposed design:-

Here Port 1, Port 2, Port 3 are Input ports. In port 1 the input bits are 10101010, in Port 2 the input bits are 11110000 and in Port 3 the input bits are 11001100. These combinations of input bits are used for all eleven logic function which is shows in table 5.1.

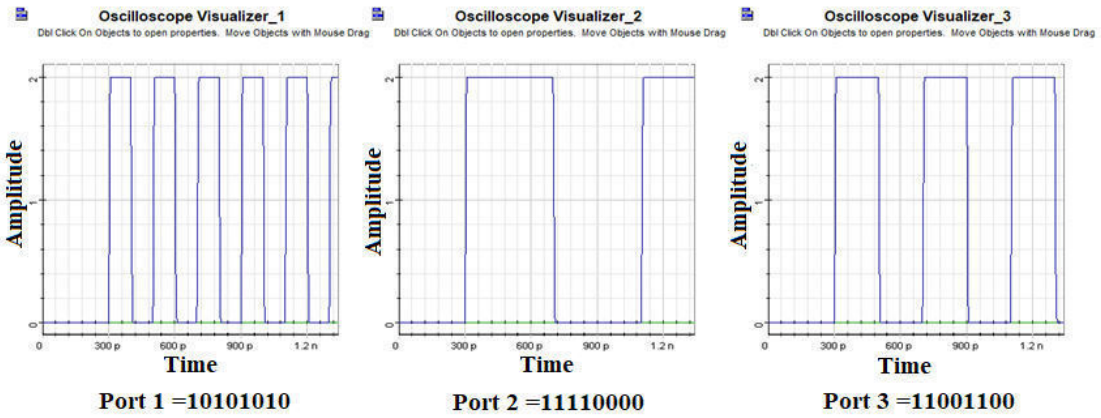


Figure 5.3: Input signals of proposed design

Table 5.1: Configuration of eleven Optical logic circuits

Sr. No.	CIRCUIT	BIASING			POLARIZATION PHASE SHIFT	
		MZM(1)	MZM(2)	MZM(3)	Phase shift (1)	Phase shift (2)
1	NOT	+Quad point	Zero Point	Zero Point	0	0
2	OR	Zero Point	Zero Point	Zero Point	120	120
3	AND	Zero Point	Zero Point	Zero Point	45	45
4	NOR	+Quad Point	+Quad Point	+Quad Point	15	15
5	NAND	+Quad Point	+Quad Point	+Quad Point	120	120
6	X-OR	Zero Point	Zero Point	Zero Point	180	180
7	X-NOR	Zero Point	Zero Point	+Quad Point	180	180
8	FEYNMAN	Zero Point	Zero Point	Zero Point	180	180
9	DOUBLE FEYNMAN	Zero Point	Zero Point	Zero Point	180	0
10	HALF ADDER	Zero Point	Zero Point	Zero Point	180	45
11	HALF SUBTRACTOR	Zero Point	+Quad Point	Zero Point	180	45

5.2 Optical Logic Gates

In the past years, all-optical signal processing in high-speed optical networks and in optical computing has received increasing attention. All optical systems can improve operating speed to GB / s and significantly decrease system energy usage in comparison to standard O-E-O signal handling systems. So all digital gates function are design in optical domain to increase operating speed and no need to perform optical electrical optical conversion.

5.2.1 OR Gate

An OR gate has two or maybe more input, but only one output is produced. OR gate generates a logic 0 state output if its output is in logic 0 state and also generates logic1 state output even if it has any input logic in 1 state. The output can then be displayed as Z = X + Y if the input is X and Y. The OR gate can also be defined as a device, whose output is 1, even if it has an input 1.

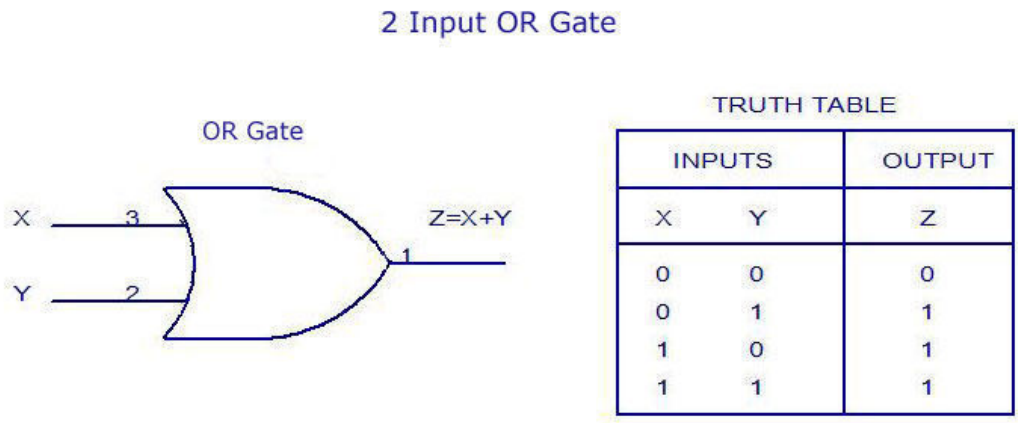


Figure 5.4: Symbol and truth table of OR Gate

Taking OR Gate, for example, all MZMs are at the null point. Here we use port-1 and port-3 for the input signal and port 5/6 for the output signal. So MZM1 & MZM3 are driven by two different signals with the same voltages. As shown in Fig.1(a) and (c), after passing the two input signals through both the MZMs they undergo same polarization phase, so the 1st signal is passed through the polarization phase shifter and it gets rotated by 120° (Fig. 1(b)). The purple and blue dots in Fig.1(d) representing the constellation of combined signal denote all the four input combinations of the binary inputs. The 2 combinations of these four signals are detected in the electrical domain by photodetector thus OR gate is realized.

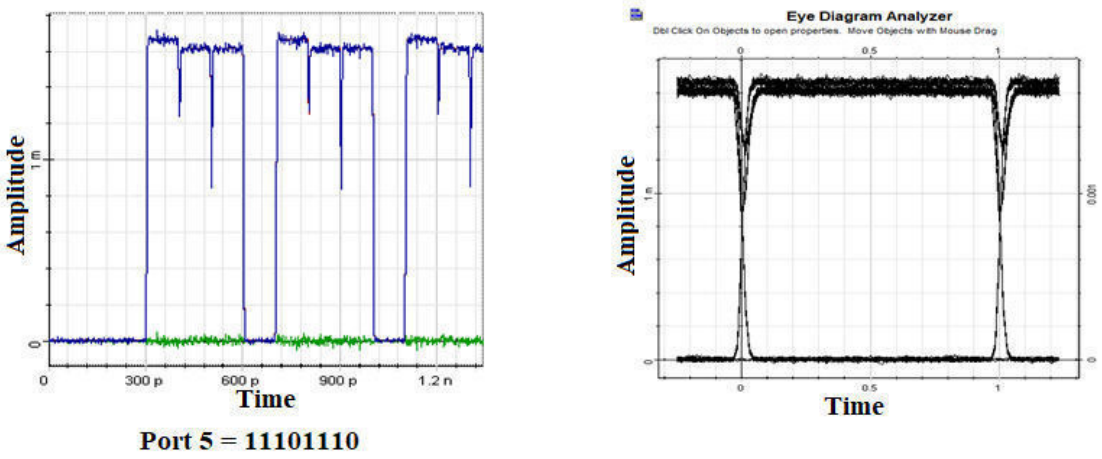


Figure 5.5: Output and Eye diagram of OR Gate

5.2.2 NOT Gate

NOT gate is known as an inverter because it switches input to another. Only one input and one output are available for NOT gate. The output is always a compliment for the input received. This means that the knot gate logic produces 1 state output when the logic 0 states are entered and logic1 state output is also generated when logic1 is entered. Here we use port 4 for the input signal and port 4 for output signal in Fig. The logic symbols and truth tables are given below:

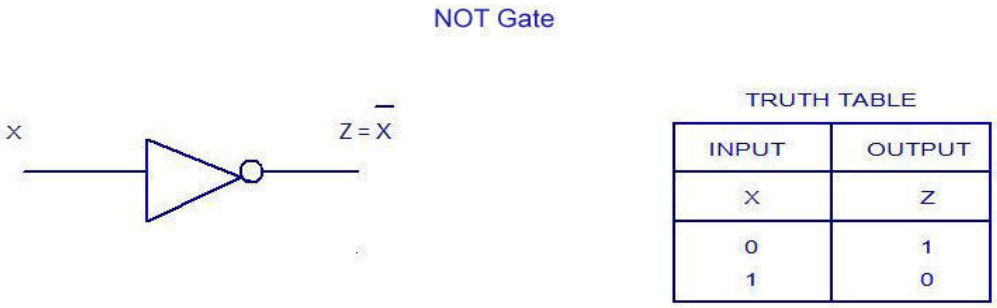


Figure 5.6: Symbol and truth table of NOT Gate

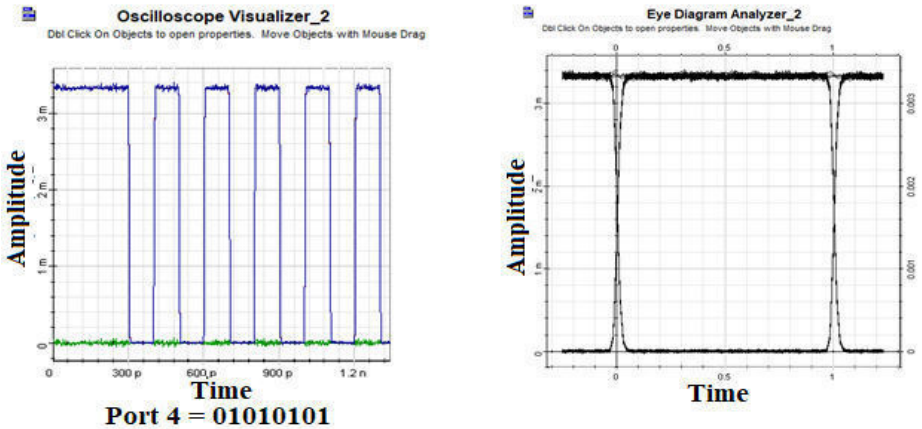


Figure 5.7: Output and Eye diagram of NOT Gate

5.2.3 AND Gate

Another gate requires two or more inputs and the same output is produced. AND gate logic generates 1 status output when each input logic is at 1 status and logic 0 status output also occurs when it has an input logic at 0 status. The result can be shown as Z = XY, if the input is X and Y. It is known as a gate or all or nothing. Here we use port-1 and port-3 for the input signal and ports 5/6 for output signal in Fig. 1. Two-input and Gates logic symbol and truth table are given below.

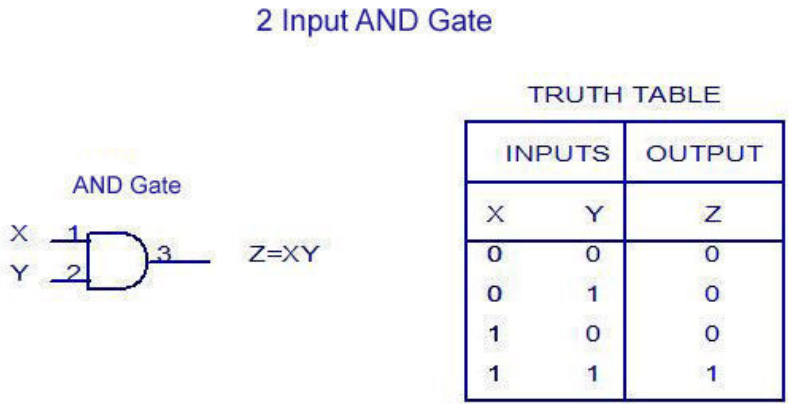


Figure 5.8: Symbol and truth table of AND Gate

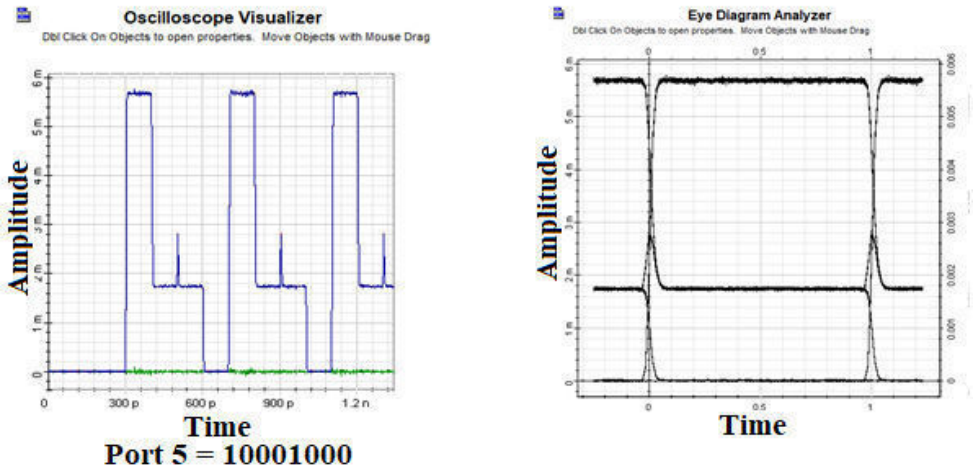


Figure 5.9: Output and Eye diagram of AND Gate

5.2.4 NAND Gate

The universal door is NAND and NOR gateways. Each of these doors can understand the logic circuit single-handedly. The basic logical features of the gate, such as AND, OR and NOR, can be made by NAND and NOR gate. NAND gate is an AND gate and not gate combination. Only when each input considers an argument 1 level, the output log of the NAND gate is 0. Here we use port-1 and port-3 for the input signal

and port 5/6 for the output signal in Fig. 1. The truth table of two-input NAND gate is given below:

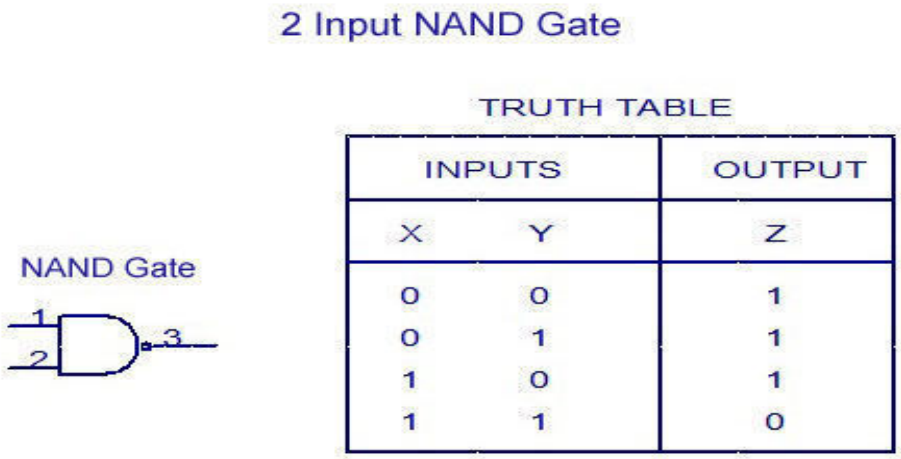


Figure 5.10: Symbol and truth table of NAND Gate

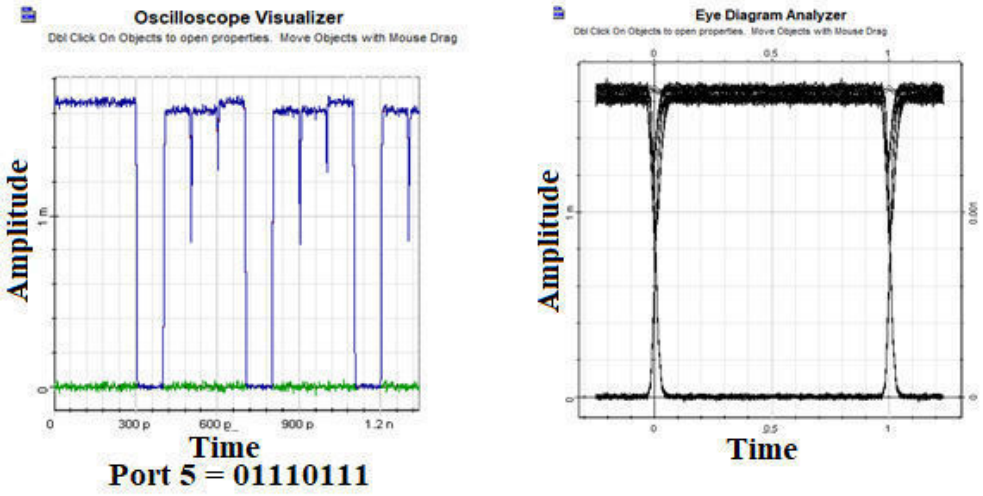


Figure 5.11: Output and Eye diagram of NAND Gate

5.2.5 NOR Gate

NOR indicates NOT-OR, that means that the NOR gate is a combination of the gate and not gate. The product is only a level of logic 1 if the logic in each of its input is considered to be level 0 and the output logic is the level of 0 for any other combination of input. Here we use port-1 and port-3 for the input signal and port 5/6 for the output signal in Fig. 1. The truth table of two-input NOR gate is given below:

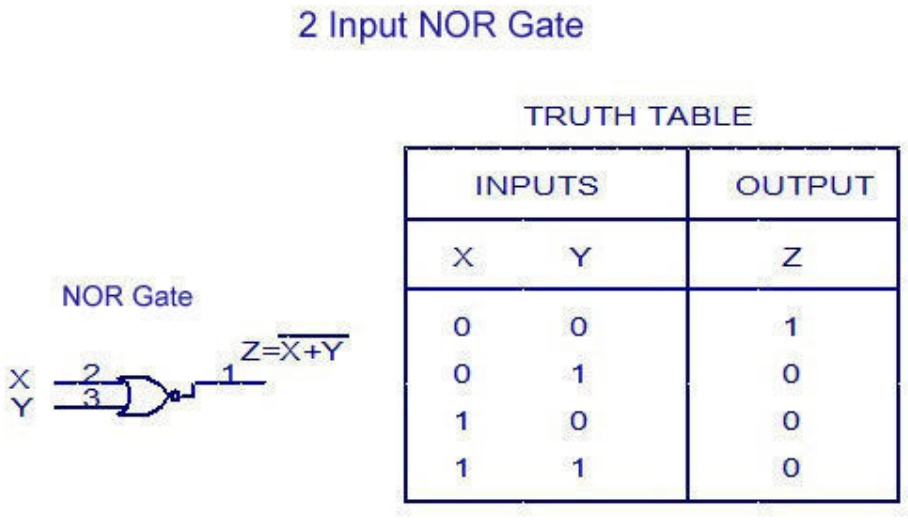


Figure 5.12: Symbol and truth table of NOR Gate

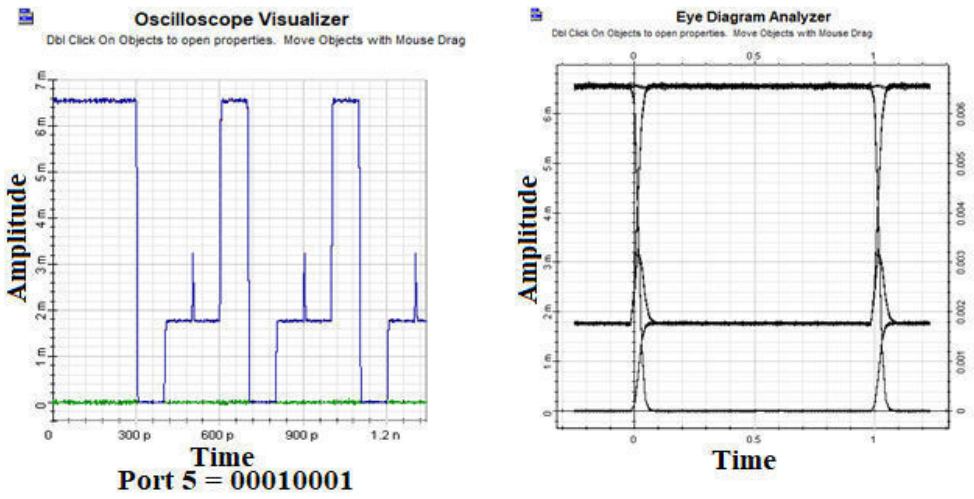
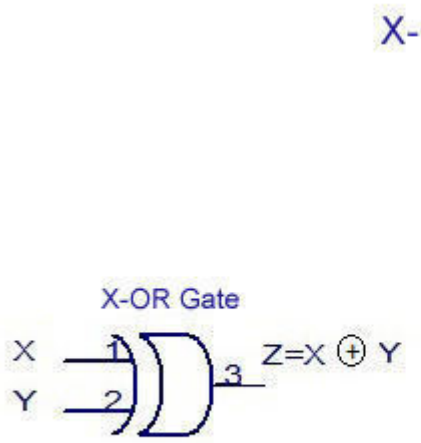


Figure 5.13: Output and Eye diagram of NOR Gate

5.2.6 Exclusive-OR (X-OR) Gate

The X-OR gate is a circuit with two inputs, one output logic. The X-OR gate recognizes the state of logic when one of its two inputs regards the position of the argument. 1. If both values assume the position of the input logic or the values of the logic are considered both the input, then the value of the output logic assumes the

position. The X-OR gate output is the sum of the input modulo yoga. X-OR gate is also known as inequality detector or coincident gate. The X-OR gate can also be used as an inverter, one of the two input terminals can be connected to logic 1 and the inverted sequence can be input on the second terminal. Here we use port-1 and port-3 for the input signal and port 5/6 for the output signal in Fig. 1.



X-OR Gate

TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

Figure 5.14: Symbol and truth table of X-OR Gate

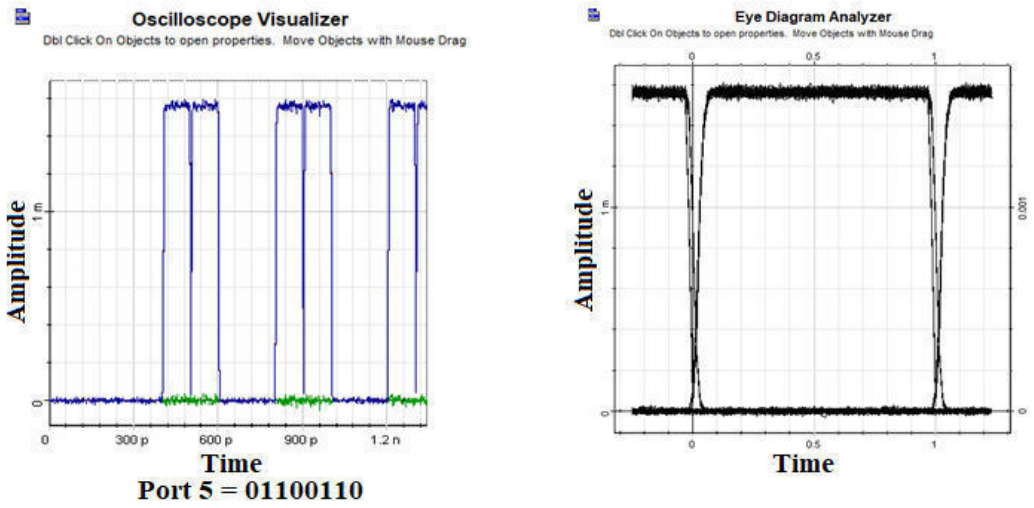


Figure 5.15: Output and Eye diagram of X-OR Gate

5.2.7 Exclusive-NOR (X-NOR) Gate

The X-NOR gate connects the X-OR gate with no gate. The X-NOR gate is also a design for two inputs, one output. When both inputs are assumed to be 0 positions or 1 position, then X-NOR gate output logic will be logic 1. If one takes one of these

inputs and the other 1 status, the output logic of the X-NOR gate will be 0. The combination is also referred to as the gate because the output is only 1 if the input is coincident. The X-NOR gate can also be used as an inverter, by connecting one of two input terminals to the argument 0 and input the reverse order on the output terminal. Here we use port-1 and port-3 for the input signal and port 5/6 for the output signal in Fig. 1.

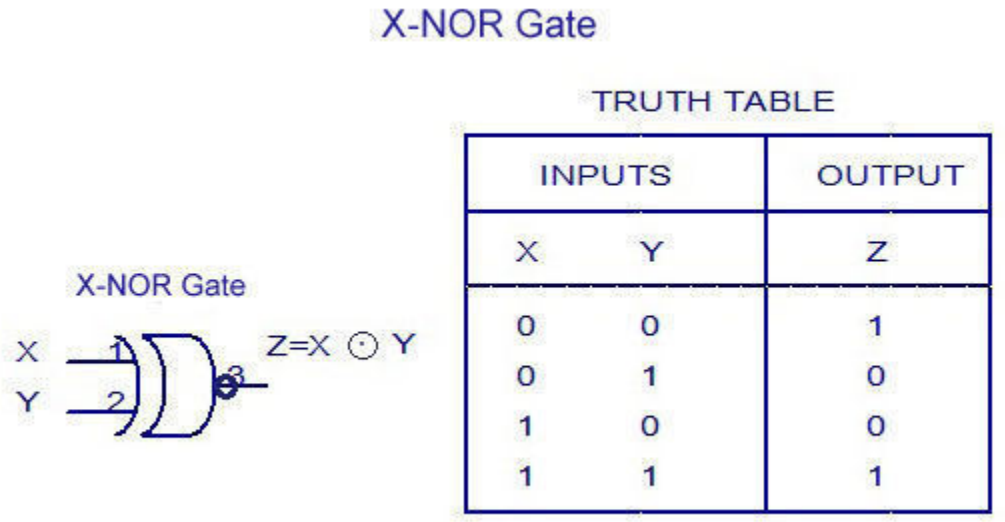


Figure 5.16: Symbol and truth table of X-NOR Gate

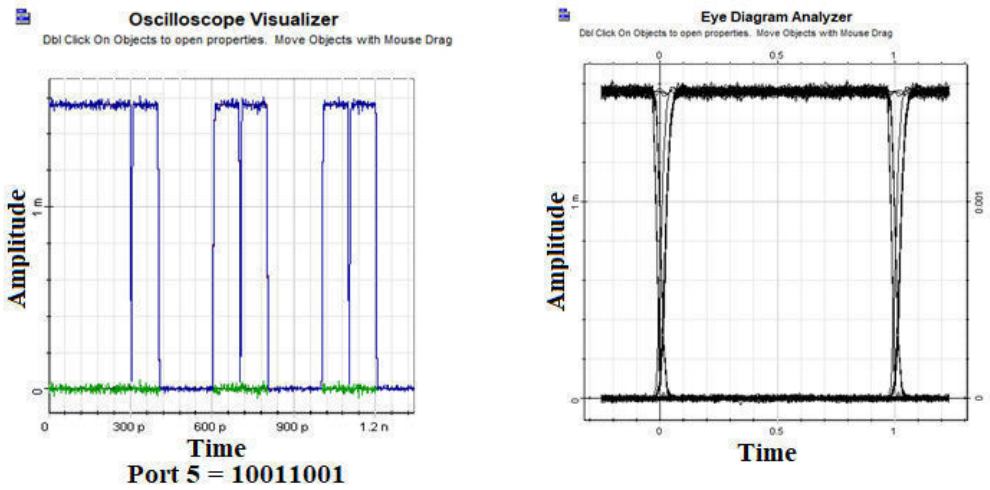


Figure 5.17: Output and Eye diagram of X-NOR Gate

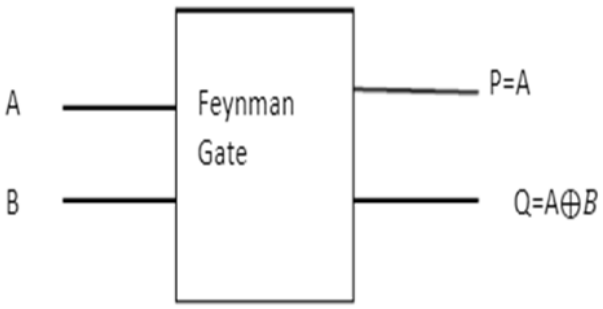
5.3 Reversible Logic Gates

A reverse logic gate is in great demand for future computing systems because they are known to produce zero power dissipation in optimal conditions. In the advanced computing technologies such as Low Power VLSI, Quantum Computing,

Nanotechnology, Optical Computing, etc., there is a promise of reversible circuits. Reversible gates require continuous input to reconstruct gate functions and garbage output which help to maintain reversal. It is necessary to reduce the parameters like continuous and waste bits, quantum cost and delay in designing reversible circuits.

5.3.1 Feynmam Gate

The Feynman gate is 2*2 gate. It is a controlled NOT Gate. As show in fig the inputs (A, B) are produce output signal P=A, Q=A □ B. Feynman gate uses port 1 = A and port 3 = B as input ports and outputs are taken at port 4 = P and port 5 = Q as shown in Fig.



Inputs		Outputs	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 5.18: Symbol and truth table of Feynman Gate

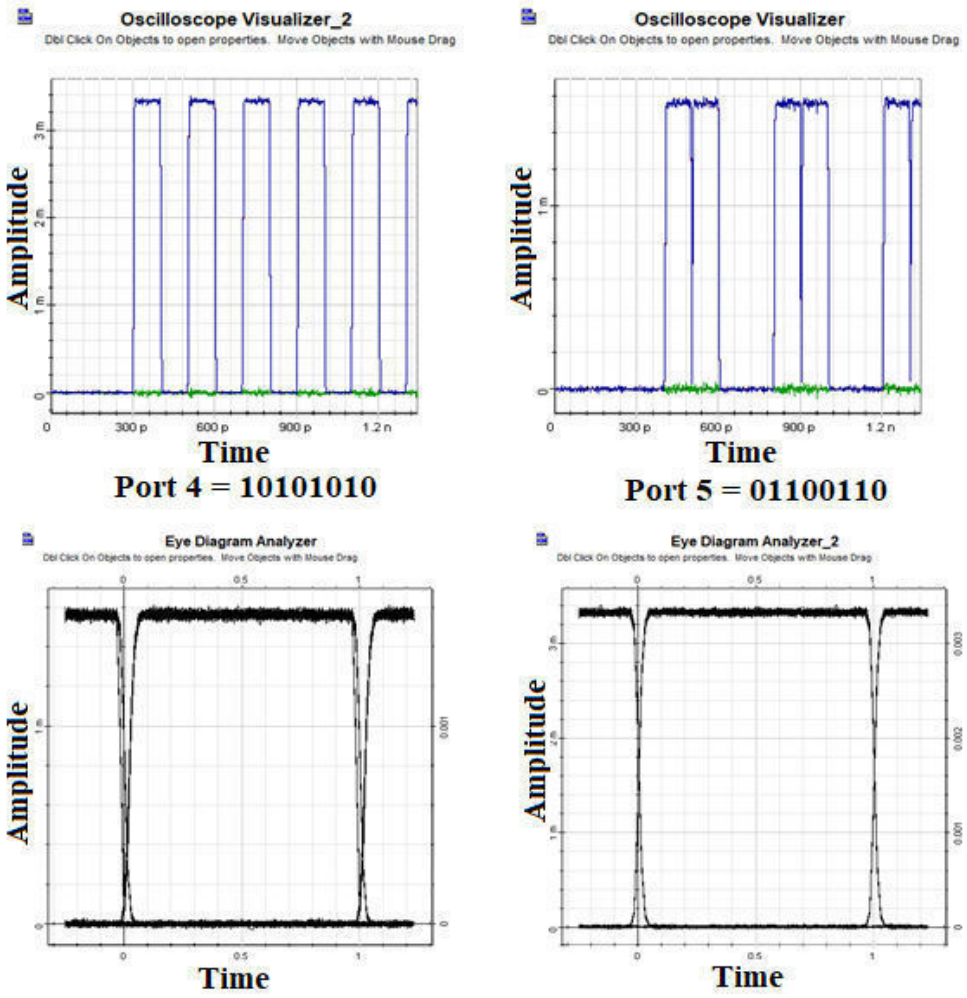
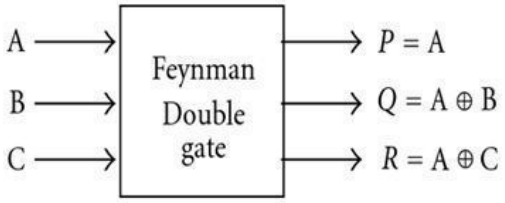


Figure 5.19: Output and Eye diagram of Feynman Gate

5.3.2 Double Feynman Gate

Double Feynman gate is advanced version of Feynman gate which have 3input and 3 output ports. This reversible logic gate has A, B, C as input Signal and X, Y, Z as output port. Double Feynman gate all input and output ports are taken. Port 1 = A, Port 2 = B, Port 3 = C are used as a input Ports and Port 4 = X, Port 5 = Y, Port 6 = Z are use as output Ports. For Double Feynman gate the key is positioned to port-2. For Double Feynman gate the key is positioned to port-2 in Fig 1. The block diagram of Double Feynman gate is shown and truth table are shown below:



Input			Output		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Figure 5.20: Symbol and truth table of Double Feynman Gate

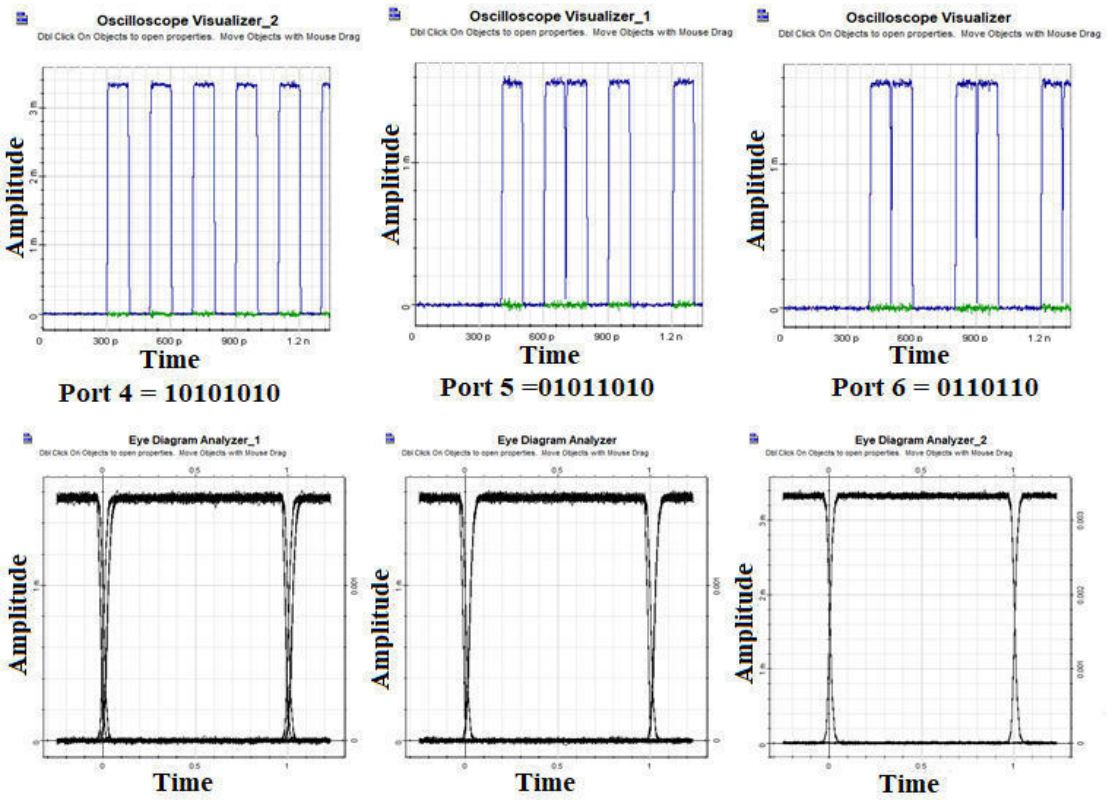


Figure 5.21: Output and Eye diagram of Double Feynman Gate

5.4 Half Adder Circuit

You must first know what a connector to understand what half additives is. Radar is a composite digital circuit that is used to add two numbers. The adapter circuit produces a single bit (designated as S) and a carry bit (designated as C) as an output signal. Orders are usually made to add binary numbers, but can also be made to connect other formats such as BCD, XS3, etc. The adapter circuit can also be used in many other digital electronic applications like Table Index calculation, Address decoding, etc.

Half adder is a combination arithmetic circuit that adds two numbers and generates a sum bit (S) and the carry bit (c) as the output signal. When the input bits are A and B then the sum bit (S) is the A X-OR B, and the carry bit (C) is the A AND B. It is clear from this that a half adder circuit can simply be built with one X-OR gate and one AND gate. Half adder is the simplest adder circuit. Here port-1 & port-3 are used as the input ports and port-5 & port-6 are used as output ports for both Half Adder. port-4 works as a sum port & port6 as a carry port in Fig. 1. The truth table, schematic representation and XOR//AND realization of a half adder is shown in the figure below:

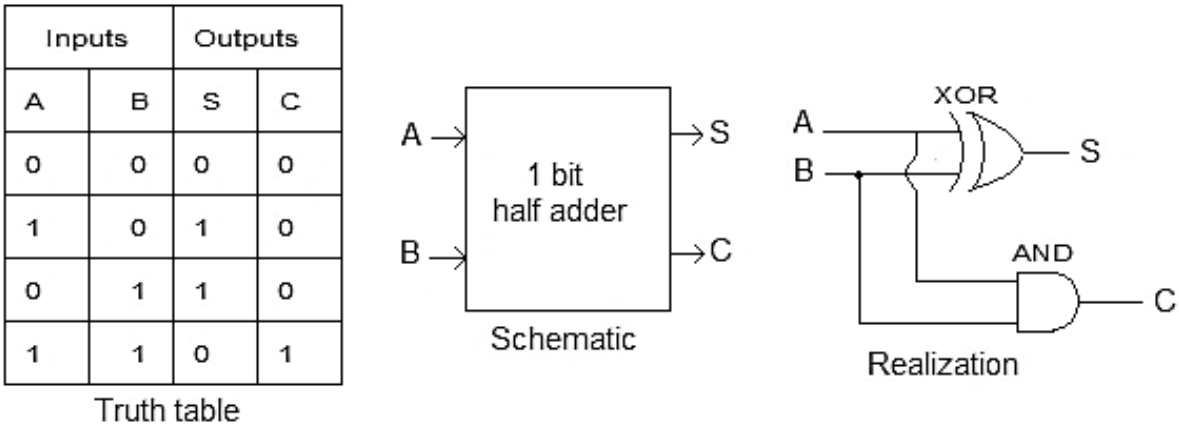


Figure 5.22: truth table, schematic and realization diagram of half adder

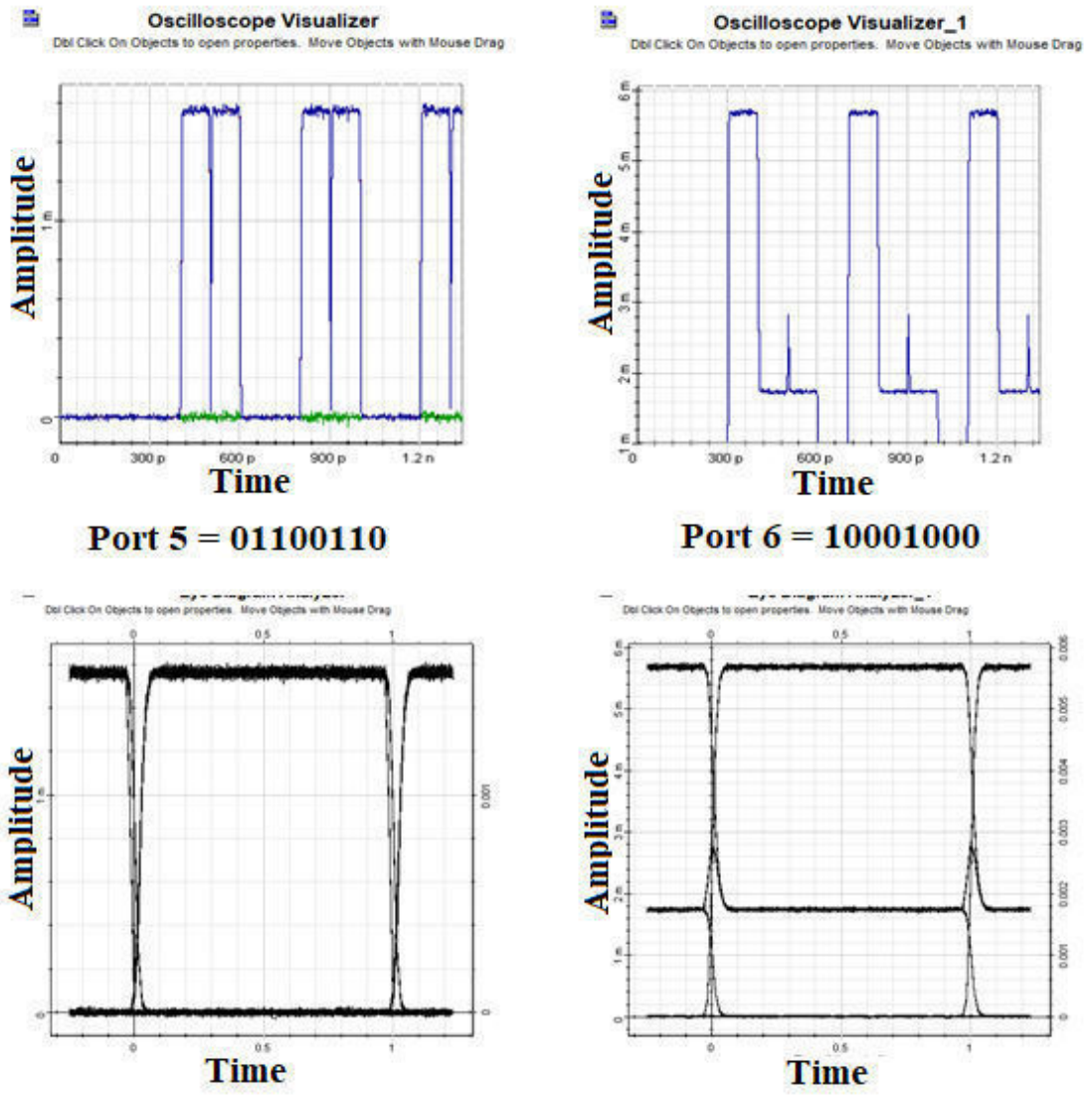


Figure 5.23: Output and Eye diagram of Half Adder

5.5 Half Subtractor

Half subtractor is one of the most significant combination circuits used in digital electronics. Half subtractor is essentially electronic devices. The logical circuits performing two binary digits subtraction. Like the addition of 2 binary digits producing SUM bit and CARRY bit, the subtraction has two outputs called difference and borrowing. The simplest possible 2-bit binary digit subtraction is made up of four possible operations, 0-0, 0-1, 1-0 and 1-1. The 0-0, 1-0 and 1-1 operations produce a 1-bit output subtraction while the 0-1 operation generates a 2-bit output. They are called the difference and the borrow respectively. For the subtraction of the next higher pair bit, this borrow bit is used. So, we can describe half-subtractor as a combinational circuit that is known as a half-subtractor that is capable of subtracting

2-bit binary digits. The binary digit from which the other digit is subtracted is referred to as minuend, and the binary digit to be subtracted is referred to as subtracting Here port-1 & port-3 are used as the input ports and port-5 & port-6 are used as output ports for Half Subtractor. port-5 works as a difference port & port-6 as a borrow port. For half subtractor key-1 is switched to position1 in Fig. 1. so MZM-2 performs NOT operation, now A and $\bar{A}$ both are present and XOR & AND operation are operated by shifting key-2 to position 2.

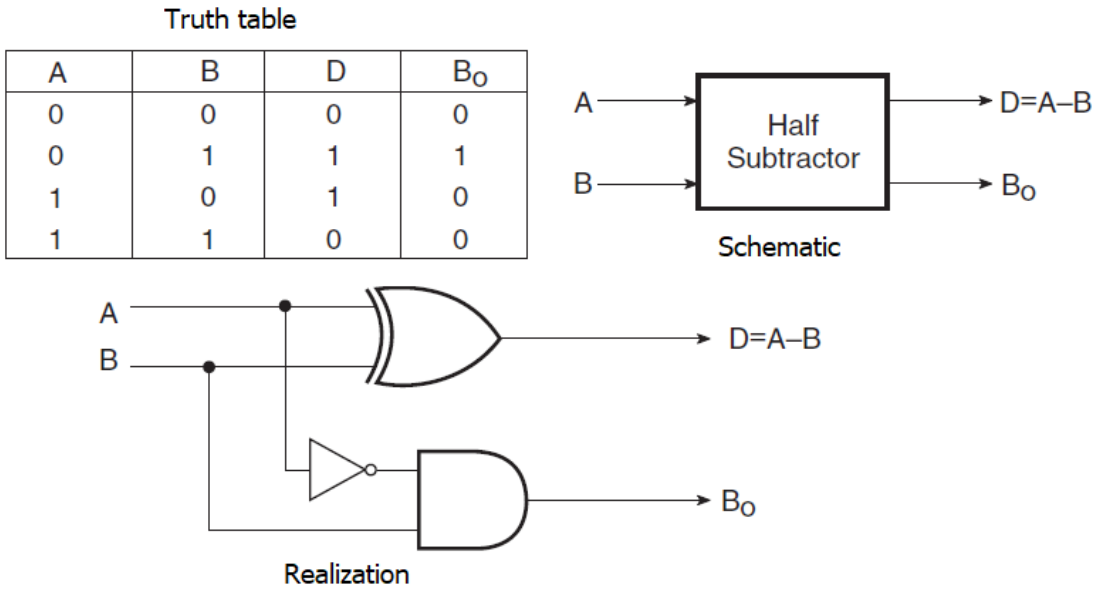


Figure 5.24: truth table, schematic and realization diagram of half Subtractor

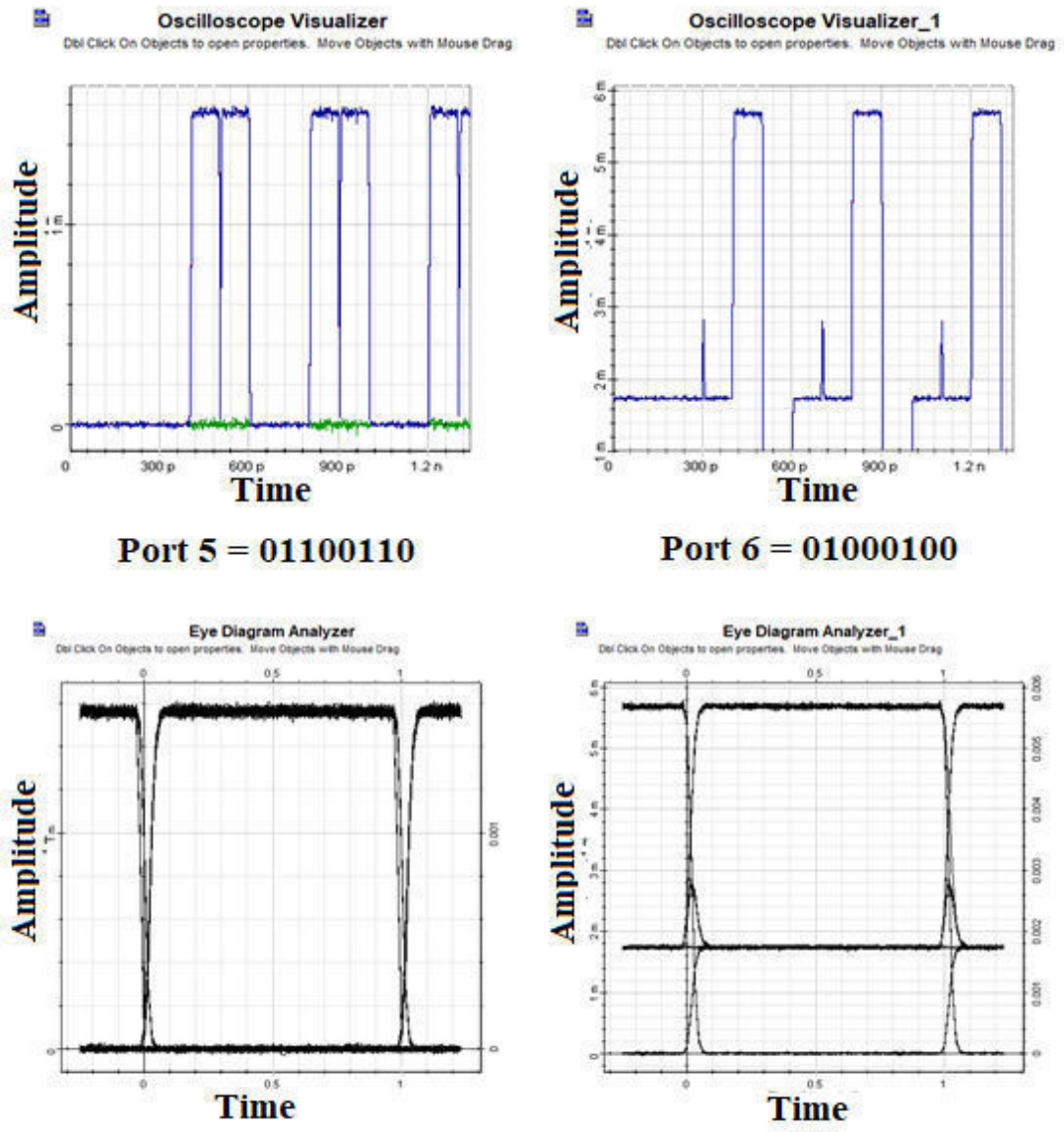


Figure 5.25: Output and Eye diagram of Half Subtractor

5.6 EXTINCTION RATIO

When used to define the efficiency of an optical transmitter used as a digital communications, the extinction ratio is actually the energy ratio (power) used to transmit a level of logic' 1' to the energy used to transmit a level of logic'0.' The eye diagram is generally used for a graphical description as shown in Fig 5.26.

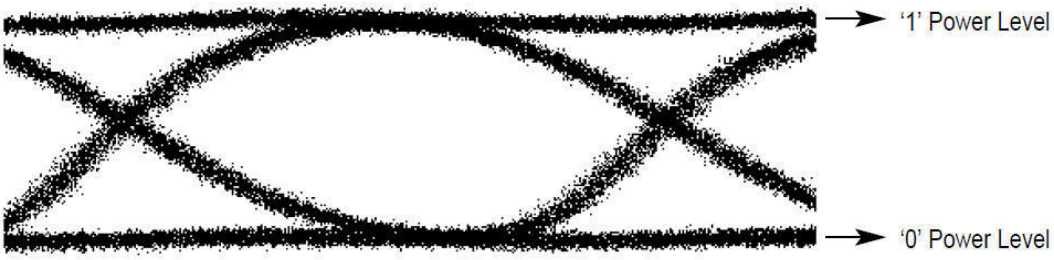


Figure 5.26: Representation of Extinction ratio

It is possible to determine the extinction ratio from the eye diagram, as a linear ratio, in decibels, or as a percentage as shown below:

$$\text{Extinction ratio} = \frac{\text{'1' power level}}{\text{'0' power level}} \tag{5.2}$$

$$\text{Extinction ratio(dB)} = \log_{10} \frac{\text{'1' power level}}{\text{'0' power level}} \tag{5.3}$$

$$\text{Extinction ratio \%} = \frac{\text{'1' power level}}{\text{'0' power level}} \text{ x } 100 \tag{5.4}$$

There are several factors that can possibly degrade the measurement of the extinction ratio. It is possible to group these variables into the following categories:

- Offset / spurious signals produced by the instrumentation
- Waveform distortion induced by the instrumentation
- Instrument accuracy in the measurement of waveform amplitudes

The following approach should be introduced to minimize measurement degradation:

- Use a histogram-based measurement method that is robust even when circumstances of error arise
- Understand the mechanisms of waveform distortion and use instrumentation that produces high waveform fidelity
- Understand and remain within in the instrument's measurement limitations where applicable.

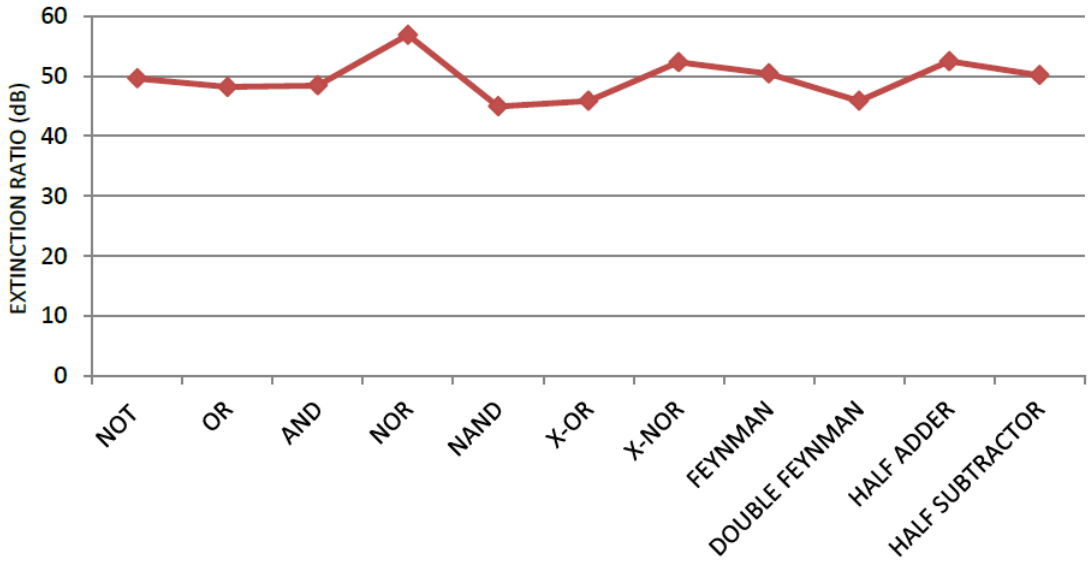


Figure 5.27: Graphical representation of Extinction ratio of all logic functions

As shown in fig. 4 ERs of different logic functions have been obtained by formula as shown below.

$$ER = 10\log(\frac{P_{ON}}{P_{OFF}}) \quad (5.5)$$

We consider 10 dBm for ON power and -100 dBm for OFF power of the laser. As the difference between P_{ON} and P_{OFF} widens the receiver can easily distinguish between level '0' and level '1'. Thus a high value of ER is always desirable. The below given table 5.2 and Fig 5.28 and Fig 5.29 shows the Extinction ratio and Insertion loss with the respective power given at input as per my proposed design for X-OR gate.

Table 5.2: Extinction ratio and insertion loss of X-OR Gate

Extinction Ratio (dB)	Insertion Loss (dB)	Power(dBm)
29.877	44.019	2
33.874	42.022	4
37.872	40.024	6
41.871	38.025	8
45.871	36.025	10
49.871	34.025	12
53.871	32.025	14
57.871	30.025	16
61.871	28.025	18
65.871	26.026	20

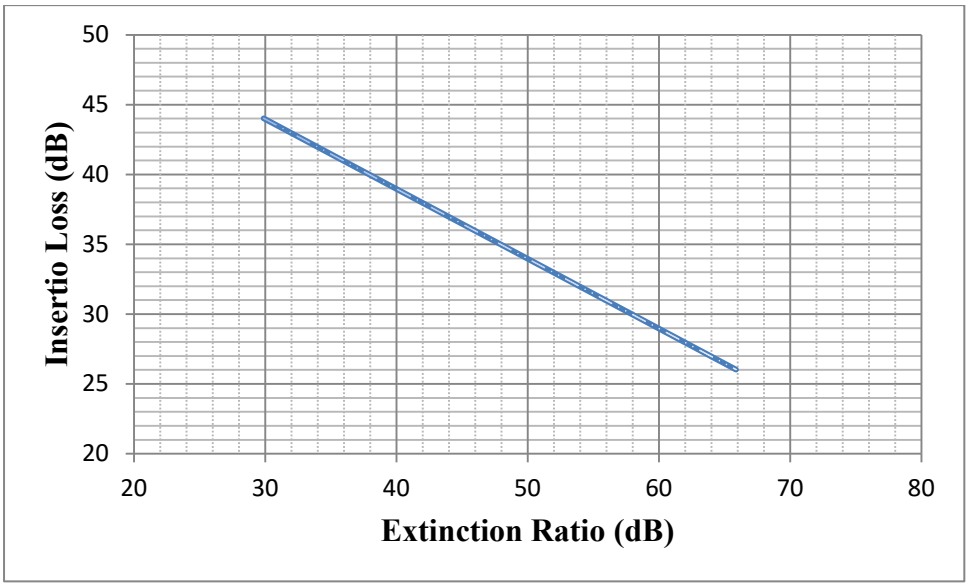


Figure 5.28: Extinction Ration v/s Insertion Loss of X-OR Gate

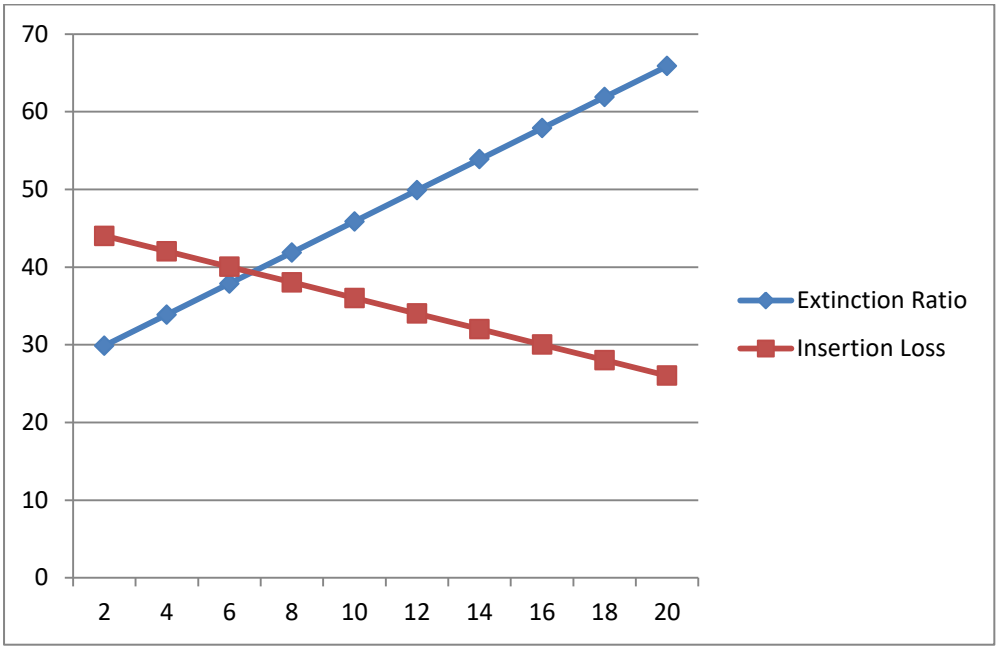


Figure 5.29: Extinction Ratio And Insertion Loss Analysis of X-OR Gate

CHAPTER 6: CONCLUSION AND FUTURE ASPECTS

6.1 Conclusion

This dissertation proposes a new scheme to realize different kinds of optical logic functions and combination circuits based on three MZM modulators. As a result of this circuit the realization of 7 logic gates, 2 reversible optical logic gates (Feynman & Double Feynman gates) and half adder & half subtractor in a single optical circuit is achieved successfully and its complexity is reduced to manifold. Both phase & intensity of the optical signal are employed to create the four combinations of the input signal. pin diode photo detector is used to directly detect the output states of the circuit. Large ERs of the value 50 dB is calculated that is higher than reported in [8]. Extinction Ration v/s Insertion Loss of X-OR Gate graphical representation in Fig 5.28 which shows if insertion loss decreases extinction ratio is increase. They are inversely proportional to each other. The values of ER are obtained theoretically as shown in table 6.1 which is better than the previous work reported in [8].

Table 6.1: Extinction ratio of all logic function

Sr. No.	Optical Logic Function	Extinction Ratio
1	NOT	49.64
2	OR	48.21
3	AND	48..45
4	NOR	56.9
5	NAND	44.98
6	X-OR	45.89
7	X-NOR	52.35
8	FEYNMAN	50.43
9	DOUBLE FEYNMAN	45.88
10	HALF ADDER	52.5
11	HALF SUBTRACTOR	50.16

6.2 Future Aspects

In future, more improvement can be made in the optical logic gates, Optical revesible gate, half adder and half subtractor designs. More combinational and sequential circuits will be added in proposed design. Future work can be done on following parameters of these modulator designs-

- Bias Voltage: By reducing the switching voltage more power efficient designs can be made, reduction in switching voltage will result in a decrement of switching voltage length product parameter of MZI structure which is desirable.
- Insertion Loss: lower value of insertion loss for any device is desirable, by working on these designs one can reduce the value of insertion loss more than three digits after decimal point.
- Extinction Ratio: higher value of ER is desirable. So, working on these designs one can increase the value of Extinction Ratio.

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LIST OF PUBLICATION

1. Jitendra Kumar Saini, A. Saharia, T.Ismail, I. S. Fahim, M. Tiwari and Ghanshyam Singh, "Polarization Encoded multi logic functions with direct detection" International Conference on Optical and Wireless Technologies (OWT 2019), Springer, Jaipur, India, March 2019.

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