A

Dissertation Report

on

Simulation and Performance Investigation of Double Gate Junctionless Transistor for Ultra-low Power Applications

Submitted in

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Master of Technology in VLSI Design

by

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DECLARATION

I hereby declare that the work presented in this thesis entitled **Simulation and Performance Investigation of Double Gate Junctionless Transistor for Ultra-low Power Applications** in partial fulfillment for the award of Master of Technology in VLSI Engineering, Malaviya National Institute of Technology, Jaipur, India is a record of my own investigation carried under the supervision of Dr. Chitrakant Sahu, Assistant Professor, Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur. I have not submitted the matter presented in this dissertation anywhere else for the award of any other degree.

Place: Jaipur **Shashank Sharma**

Date:..... **2016PEV5392**

CERTIFICATE

This is to certify that the thesis report entitled **Simulation and Performance Investigation of Double Gate Junctionless Transistor for Ultra-low Power Applications** submitted by **Shashank Sharma**, bearing roll number 2016PEV5392 in partial fulfillment of the requirements for the award of **Master of Technology in VLSI Engineering** with specialization in **Electronics and Communications** during session 2016-2019 at Malviya National Institute of Technology, Jaipur is an authentic work carried out by him under my supervision and guidance.

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Date:.....
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Abbreviations

JLT Junctionless Transistor

DIBL Drain Induced Barrier Lowering

SCE Short Channel Effect

ULP Ultra Low Power

DGMOS Double Gate Metal Oxide Semiconductor Field Effect Tansistor

Abstract

The current-voltage characteristics and sensitivity with respect to various device parameters of junctionless (JL) MOS transistors for ultra low power (ULP) subthreshold logic applications has been studied in this dissertation. The double gate (DG) JL devices, which do not require any process for source or drain extension, can perform significantly better than conventional inversion mode devices for ULP applications.

The drain current model of JLT shows the approximate similar result with the mathematical model of the JLT. Sensitivity analysis shows that for all device parameters, JL devices have the minimum sensitivity values to gate length in comparison to inversion mode MOSFETs. The results also generate the need of the alternative materials and architectures which could be used to further use the JL device purposedly.

Acknowledgment

Firstly I would like to express my sincere thanks and gratitude to my supervisor and mentor Dr. Chitrakant Sahu for his guidance and advices for this thesis. He always shares his knowledge and experience with me. We have shared a very nice teacher-student relationship. He always guided me whenever I have doubts and in trouble in understanding the concepts or getting the results. His teachings in his core areas provide motivation and encouraged me to take the device level research. Eventualy, I have developed interest in the topic. I am greatly indebted to him and his kind directions at the time of encouragement and support. An excellent academician, a gentleman, a devoted teacher with helping mind, a tireless researcher himself Dr. Sahu had imbibed the virtue of enthusiasm in me.

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Chapter 1

Introduction

1.1 Overview

The technology has a very crucial role in the lives of people in present times. When it comes to research in space, manufacturing, defence, automobile, travel, household, economy or any other field, it has its own advantages. The number of researchers are engaged in the work through which the boons of technology can be extracted. In the same context, the various physicists and scholars have given their theories of how the electronics plays an important role in advancement of technology. As the time flies, it requires more advanced and noval inventions which directly affects the living of mankind by improving its performance. At the same time, it has some limitations.

For the device level research, the downscaling of transistors is a major driving force for performance advancement as the Moore's law is to be followed with the time. In order to justify the law, the miniaturization of the transistors is the need of the hour, but due to the Short Channel Effects SCEs, the subthreshold characteristics (characteristics which the transistors exhibits at low or very low bias conditions) of transistors degrades. The phenomena of sensitivity for the change of various device parameters impose some limitations on the device to work in subthreshold region. These reasons prevent the use of transistor for ULP operation. The low power applications includes cellular phones, personal assistants, medical electronics and other portable computing devices where the low power consumption is the primary criteria instead of high speed operation. The study of any device in its subthreshold region provides the idea about how it behaves when a very low voltage is applied to it. Although the current drive obtained in this region is low so the analysis is being done for low voltages. The various number of architectures of transistors have been studied globally to accomplish the use of the applications which require low power consumption and to minimise the SCEs but

still there is a scope with which the more significant results can be achieved.

The multigate architecture in silicon-on-insulator technology with minimised SCEs which enables to scale the MOSFETs into the nanoscale regime.
Junctionless FET is one of those new architectures proposed which is having no junctions. It is a single silicon nanowire which have high doping. It has advantages over the abrupt S/D junction MOSFET as it has a much easier fabrication process, minimised SCEs and high current drive. It also shows better performance characteristics than abrupt S/D junction MOSFETs.

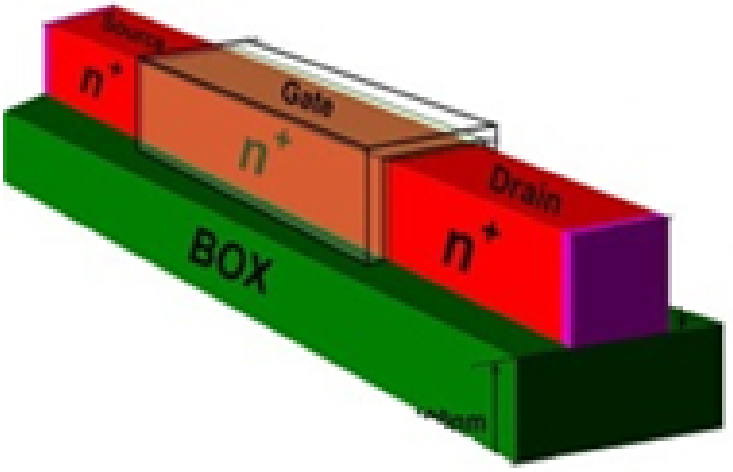

Figure 1.1: Cross sectional view of silicon nanowire junctionless transistor [3]

The junctionless transistor (JLT) is a multigate FET with no PN junctions. The device is basically a resistor (a nanowire) in which the mobile charge carrier density can be modulated by the gate as it will create the potential with the help of work function difference between gate and substrate material. This potential will help to generate an electric field vertically which moves the charge carriers accordingly, hence generating the body current. The JLT can be operated either in the positive or negative gate bias. Normally, the JLT remains in the off state at the zero gate voltage provided that the silicon nanowire thickness is such that the depletion region formed due to work function difference will cover the entire body of the substrate, thus restricting the charge carriers to flow through the nanowire. It is driven into the on state by means of a positive gate voltage for n-channel FET. The doping of silicon nanowire in JLT is high in order to achieve the suitable current drive.

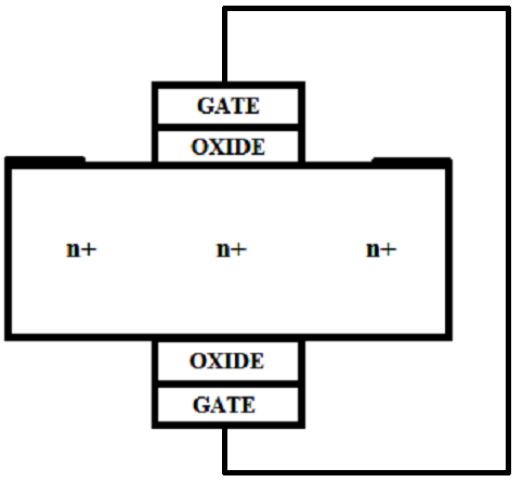

Figure 1.2: Silicon nanowire junctionless transistor with both the gates short [1]

The performance characteristics of JLT FET have their importance in a way that by studying and pondering on these characteristics provide the significance of the device. It is also useful in order to compare the superiority of the device with any other particular device which can be used for the same application. These characteristics include subthreshold slope (S-Slope), ON-OFF current ratio (I_{on}/I_{off}), Gate Capacitance (C_{gg}) and Intrinsic Delay (τ).

The sensitivity of the subthreshold parameters of JLT FET is another entity by which the performance of JLT MOSFET can be compared with abrupt S/D MOSFET. It is mostly evaluated when the transistor is meant to operate at low voltages beacause at low voltages small change in the parameter can impact the device performance upto a significant extent. The sensitivity analysis of JLT MOSFET can be done by calculating the per unit change of performance metric with respect to per unit change in parameter.

S (Parameter) = ((Metric)/Metric)/((Parameter)/Parameter)

In this work, the JL nanowire is simulated using 2-D simulator ATLAS for uniformly doped silicon nanowire of silicon nanowire thickness (t_{si}) varying from $6nm$ to $8nm$, oxide layer thickness (tox) varying from $1.0nm$ to $1.7nm$, gate length (L_g) of $20nm$, channel doping (N_d) varying from 1 x$10^{19}cm^{-3}$ to 3 x 10^{19} cm^{-3}. Since the focus is to extract the characteristics of device for ULP applications, it is evaluated at low drain bias $Vds = 0.4V$. The results obtained for the JLT FET is compared with the DG MOSFET which is also simulated for the same device parameters and bias conditions except the doping of substrate which is 1x$10^{15}cm^{-3}$. The results are plotted by using

Tonyplot and various conclusions have been derived.

1.2 Motivation

The following points are mentioned which motivated and arouses the need to study JLT in the subthreshold region:
1. The gadgets and electronic devices which are operating presently requires very low power consumption besides high speed operations. The gadgets and other application meant to work for long duration with power constraints. The answer lies in the statement that the present devices need to be evaluated in the subthreshold region so that the unwanted OFF-current power losses could be restricted upto a considerable extent.
2. The sensitivity of the device with respect to the change in different parameters of the device as to how the device would react to the change is to be worked upon so that the device can be used for a number of applications with greater margin of usage.
3. The fabrication complexity which is encountered to fabricate various devices and are meant to operate in nano regime is such that it would ultimately lead to increase in the cost.
4. Short channel effects which degrades the device characteristics and restrict to further downscale the channel length shall be taken into account which directs to find the alternatives to address the same issue.
5. The earlier literatures on the JL devices proves that it could be a promising device for fulfilling the needs of next generation applications.

1.3 Outline

The work in the thesis is organised in six chapters.

Chapter 1 presents the basic introduction of the JLT explaining its architecture and normal working phenomenon. It also comprises of the brief explanation on how the work in the thesis is done.
Chapter 2 presents the various literatures available which have been explored and used. It also includes the concept and characteristics of each device on which it is operating and how it can be used in various applications. The results of such works and the limitations of all those devices are also discussed in this chapter.
Chapter 3 describe the methodology to determine the drain current current characteris-

tics using the simulator. It includes models, methods and mesh defining methods which are used to determine the same. Sub-threshold Logic parameters in AC analysis are also discussed.

Chapter 4 describe the proposed work about the drain current characteristics of JLT FET with respect to different thickness of oxide layer, silicon layer and N_d. In this chapter subthreshold sensitivity has been explained with graph analysis.

Chapter 5 shows the results of proposed work and discussed all the graph briefly.

Chapter 6 conclude all the results and future scope of the above proposed work.

Chapter 2

Literatures

2.1 Conventional MOSFET

The very first architecture which constitute the basics of all devices and were researched the most is the conventional MOSFET. A conventional MOSFET is having four terminals namely source, drain, gate and substrate or body. For an NMOSFET, substrate is of p-type and source and drain is of same n-type impurity. Generally the type of gate material is P^+ and N^+ polysilicon for NMOSFET and PMOSFET respectively. The workfunction for substrate is same as that of drain and source. There is a layer between channel and gate called oxide and mostly common material is used for oxide is SiO_2. Normally, source should be connected at lowest potential and high k material is used to prevent from leakage current [4].

For the purpose of comparing the performances of two different devices, the conventional MOSFET is simulated for the double-gate architecture enabling it to have the more precise control over the conduction is channel region though the channel formed here is of inversion type.

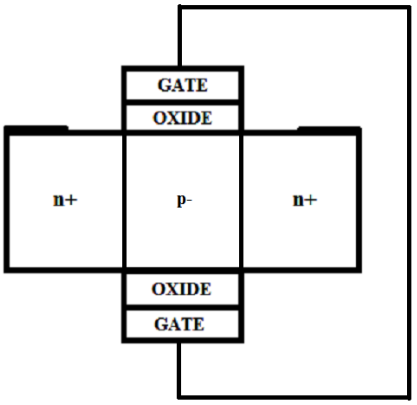

Figure 2.1: Cross scetional view of double gate MOSFET [1]

When $V_{gs} = Negative$ and $V_{ds} = 0$, holes will be accumulate at the surface of substrate region, called accumulation mode. When no baising is done to gate terminal, V_{gs} is zero in that case there is no charge carrier and holes will disappear from the surface region. This is called flat band condition and this V_{gs} is known as flat band voltage. By increasing V_{gs}, the channel gets pinched off and an inverted channel is formed near the gate in the substrate. The electron flow will increase from source to drain and channel is called inverted channel and when gate voltage is continuously increasing with drain voltage then channel goes under strongly inversion mode.

2.2 Short Channel Effects in Conventional MOSFET

The concept discussed in the previous section is valid till the channel length is not reduced to such an extent which will create some unwanted effects and hinderances in flow of charge carriers. As channel length is reduced, there are several effects which occur and affects the overall performance of the device in not so positive way. These effects are due to the increasing drain bias, degradation in the mobility values of charge carriers, increase in the subthreshold current etc. These effects are called Short Channel Effects SCEs which arise as a result of a two-dimensional potential distribution and high electric fields in the channel region.

When the channel length L_g is reduced to provide a high speed operation and to increase the number of components per chip, then short channel effects arises. (SCE makes it hard to accurately predict device performance). Attributes of short channel effects are limitation in the electron drift characteristics of the channel and change or modification in threshold voltage due to reduced channel length.

For a given channel doping concentration, as the channel length is reduced, the depletion

layer widths of source and drain junctions become comparable to channel length. The potential distribution in the channel now depends on both the tranverse field Ex(controlled by the gate voltage and back-surface bias) and the longitudinal field Ey(controlled by the drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e. E_x ¿¿ E_y) is no longer valid. This two dimensional potential results in the degradation of the threshold behaviour, dependence of threshold voltage on the channel length and biasing voltages and failure of the current saturation [5].

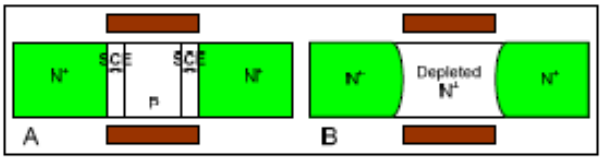

Figure 2.2: Illustration of SCE origin in Junctioned and Junctionless Transistors [2]

2.2.1 Mobiliy Degradation

The mobility can be described for the charge carriers viz. electrons and holes which both constitute the current in the device. The mobility degradation in the short channel devices can be explained by considering the electric fields on both the axes.

Lateral Field Effect: In case of short channels, as the lateral field is increased, the channel mobility becomes field-dependent and eventually velocity saturation occurs. This results in current saturation.

Vertical Field Effect: As the vertical electric field also increases on shrinking the channel lengths, it results in scattering of carriers near the surface. Hence the surface mobility reduces.

Hence for short channel, mobility degradation occurs due to velocity saturation and scattering of carriers.

2.2.2 Drain Induced Barrier Lowering effect

The source and drain depletion regions can intrude into the channel even without bias, as these junctions are brought closer together in short channel devices. This effect is called charge sharing since the source and drain in effect take part of the channel charge, which would otherwise be controlled by the gate. As the drain depletion region continues to increase with the bias, it can actually interact with the source to channel junction and hence lowers the potential barrier. This problem is known as Drain Induced Barrier

Lowering (DIBL). When the source junction barrier is reduced, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current [4].

Here when depletion region surrounding the drain extend to the source, so that these two depletion layer merge and $X_{dS} + X_{dD} = L$, punchthrough occurs. If gate to source bias (V_{gs}<V_T) is less than the threshold voltage then there will be a potential barrier that will block the flow. Increasing the gate voltage will reduce the potential barrier and allow the carrier to flow due to electric field. In small-Geometry MOSFET the potential barrier is controlled by both V_{gs} and V_{ds} if drain voltage increased, potential barrier will be reduced, this lead to DIBL the reduction in potential barrier allow the carrier flow between source and drain even if V_{gs} is less than the threshold voltage (V_{gs}<V_T). The current flow under this condition called sub-threshold current.

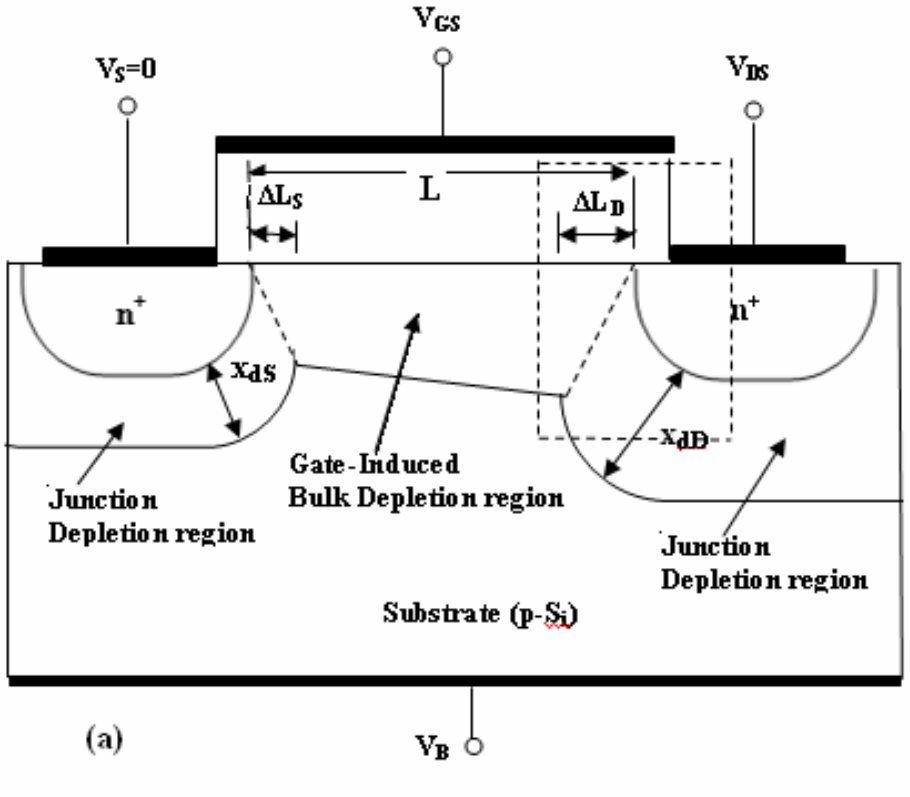

Figure 2.3: DIBL effect in MOSFET

Hence SCE make it hard to accurately predict the device performance. So it can be minimized by the proposed solution Multi-gate Junctionless Field Effect Transistor (JLT FET) with higher channel controllability such as Triple-gate Fin-FET [6], depleted silicon-on-insulator MOSFET [7], Silicon nanowire MOSFET [8].

2.3 Double Gate Junctionless Transistor

A junctionless transistor is normally an accumulation mode device, in which the device doping concentration in channel is equal throughout the source and drain. These devices have better short-channel electrical characteristics than conventional inversion mode devices. For the channel which is doped with n-type materials, and in n-channel junctionless device, the gate material with a high work function, for example P+ polycrystalline silicon or platinum is used in order to achieve a suitable threshold value. It is well known that the use of a metal as gate material is preferable for gate resistance reduction purposes.

If the channel of device is small enough, then gate can deplete the heavily doped channel entirely, which results in off-state of the transistor. The subthreshold slope is improved for junctionless transistor, and device is working in low power operation. This shows the potential of junctionless transistor for extremely short-channel applications. Here the off current is defined by the electrostatic control of the gate all over the channel and not by the leakage current of a reverse-biased diode. This determines the less sensitive device to contamination which reduces carrier lifetime and temperature, it also enables to minimize leakage current if a low-bandgap semiconductor such as Ge is used.

The different geometries have been studied in the published works viz. Single Gate, Double Gate, Triple Gate and All-around Gate. [9]

Since the double gate structure is expored here, the phenomenon on which it is working is described in the next section. The corresponding results of simulation of the JLT have been compared with that of the DGMOS FET.

2.3.1 Working of JLT FET

The working of the JLT depends on the fact that the workfunction difference between the gate and substrate materials will deplete the channel and hence it can be act as a switch. The turn-on capabilities of this type of switch depends on the OFF current which is flowing through it when no gate bias is applied. These capabilities of the switch is studied in the subthrehold region of the transistor where the transition from OFF to ON is occured at very low drain bias [10].

The workfunction of any material is defined as the energy required to take the electron from its fermi energy level to the vacuum energy level.

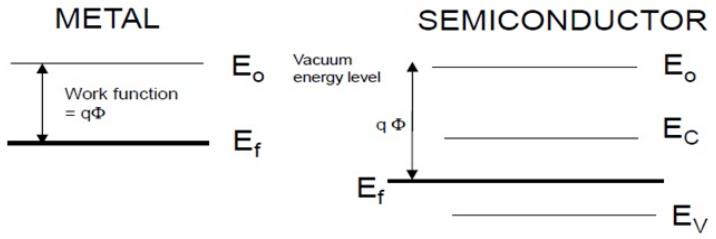

Figure 2.4: Metal and Semiconductor energy band diagrams showing their workfunctions

JLT FET has an initial depletion region inside the substrate because of the workfunction function difference between the metal gate and doped silicon substrate. The workfunction difference creates potential difference in the device which can act as a bias for the device instead of applying zero gate voltage to the gate. [11]
The thickness of the silicon nanowire and oxide layer between the channel and the gate is selected in such a manner that at zero gate bias the channel is fully depleted and hence no drain current can flow through it. The device is optimised for the various values of these parameters as well as for the different gate materials (to get the differnet workfunction values).
The potential difference which is created vertically between the gates enables the charge carriers to move and hence will deplete the channel from the surface towards the center of the silicon nanowire. Hence, JLT constitutes the body current.
The one of the condition which arises when a suitable t_{si} and t_{ox} is selected, the depletion layer from both the gates would penetrate into the body upto the extent of t_{si}/2. This condition is known as pinch-off condition. [12]

The workfunction difference can be calculated by the following equation:

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - (\chi + \frac{E_c - E_i}{q} + \Phi_F) \tag{2.1}$$

Where Φ_M is the workfunction of metal
Φ_S is the workfunction of doped semiconductor
χ is the electron affinity of silicon

Φ_F is the bulk potential which is equal to :

$$\Phi_F = V_t \log_e \frac{n}{n_i} \qquad \text{(....for n-type SC)}$$

$$\Phi_F = - V_t \log_e \frac{p}{n_i} \qquad \text{(....for p-type SC)}$$

2.3.2 Depletion Width Calculation

The depletion width which is created due to the workfunction difference between gate and substrate can be calculated mathematically with the help of the equation below. Since the depletion layer is created at the zero gate bias, hence gate voltage can be equated by the sum of the flatband voltage, voltage drop acroos the silicon substrate and the voltage drop across the oxide is given by below equation [13]

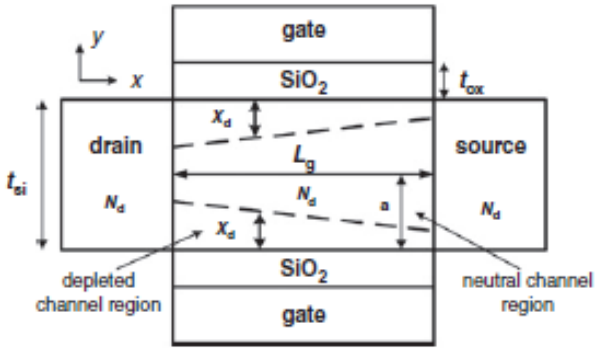

Figure 2.5: Depletion region in the substrate of JLT [13]

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} - \frac{qN_dX_d^2}{2\epsilon_s} - \frac{qN_dX_dt_{ox}}{\epsilon_{ox}} \qquad (2.2)$$

Hence, the depletion width can be calculated by below equation [13]

$$X_d = -\frac{\epsilon_s t_{ox}}{\epsilon_{ox}} + \sqrt{\left(\frac{\epsilon_s t_{ox}}{\epsilon_{ox}}\right)^2 + \frac{2\epsilon_s(V_{fb} - V_g)}{qN_d}} \qquad (2.3)$$

The pinch off voltage can be calculated by the following equation which is derived from the equation of X_d:

$$V_p = V_{fb} - \frac{qN_dt_{si}^2}{8\epsilon_s} - \frac{qN_dt_{si}t_{ox}}{2\epsilon_{ox}} \qquad (2.4)$$

2.3.3 Subthresold Parameter Sensitivity Analysis of JLT

Sensitivity analysis is done for the device to know as how its working changes for the change of different parameters of JLT. These parameters include channel length, silicon nanowire thickness, oxide thickness and doping. The variation in the parameter of workfunction of the material also contributes to the change in the working of the device in subthreshold region but this parameter change is not evaluated in this thesis [14].
The subtheshold sensitivity is calculated by below equation [1]

$$S(Parameter) = \frac{\frac{\Delta Metric}{Metric}}{\frac{\Delta Parameter}{Parameter}} \tag{2.5}$$

Chapter 3

Methodology for Subthreshold Logic Parameters Determination

The device 2-D structure is simulated on Silvaco ATLAS tool. The characteristic of the device basically depend on the mesh defined area, so proper meshing should be provided before applying the voltages for parameter extraction.

3.1 Mesh Defining

Meshing for electrical characterization in ATLAS is one of the biggest challenges that a user faces. Poor meshing in ATLAS can lead to simulation failures. Poor meshing can be the reason for inaccurate electrical results. An optimum mesh will consider sufficient number of points for accuracy but still it will not have an excessive number of points as this will increase the simulation time.

For a 2-D structure command **go atlas** is used directly within DeckBuild. In this command mode simulating these structures allows device engineers to examine spread and corner characteristics of devices. The mesh can also be directly modified using the relax and refine boxes. High quality prisms or tetrahedras created using refinement criteria while reducing the elements in the area which do not have useful details. A 2-D structure defined in the atlas for the JLT is shown here and it shows the defined mesh through the channel.

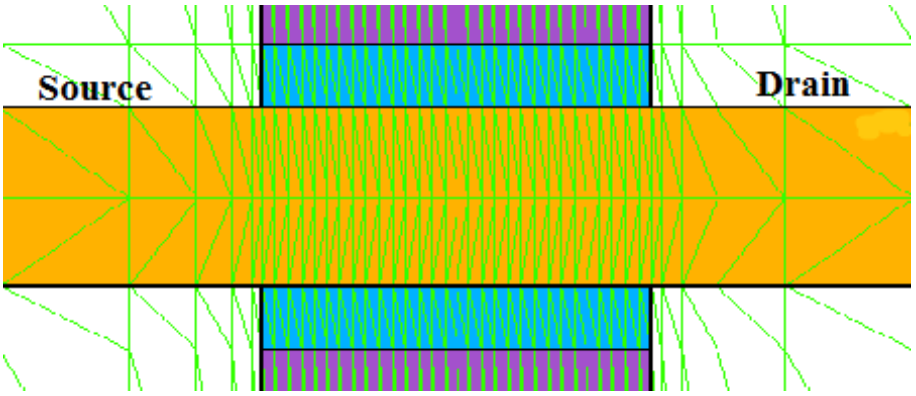

Figure 3.1: mesh defined throughout the channel and oxide in JLSNW MOSFET

Here uniform doping is used all over the channel. In the DG MOSFET three different concentrations with uniform doping is used. For the purpose of oxide, insulator SiO_2 is used. For any semiconductor region which is defined as an electrode is considered to be a conductor region such polysilicon gate electrodes. If the file contains unknown materials, these regions will become insulators. Polysilicon is treated differently depending on how it is used. In cases where its defined as an electrode, its treated as a conductor. It can also be used as a semiconductor such as in a polysilicon emitter bipolars. Here in the JLT FET it is used as an electrode.

3.2 Models and Methods

The ”models” syntex is define the physical mechanism, models and other parameters like temperature etc. for the simulation process. Here in this simulation quantum mechanical models are used to describe the carrier behavior in the formation of N channel MOSFETs inversion layer. The quantum mechanical model is given by Hansch [15] is used for accurate simulation of the effects of quantum mechanical confinement near the gate oxide interface in the MOSFET. To specify this model ”HANSCHQM” model statement should used [16]. The process is non local and specify the profile of energy bands or the separation of the electron generated in the conduction band from holes generated in the valance band. ”SRH” model is used for recombination effect. This model simulate the current due to thermal generation called leakage current. At silicon/oxide interface traps are present,to simulate them ”AUGER” model is used. Both these parameters are used for the purpose of mobility statement. For most of the materials, to specify materials parameters ”PRINT” model is used.

To solve convergence criteria and iterations, some non-linear solution method are specified in Method statement. Th solutions are specified using these method statement NEWTON, GUMMEL, or BLOCK. Newton method is solved the each iteration by the

linearized version of the entire non-linear algebraic system. This method is default for the drift diffusion calculations. It used automatic bias step reduction with a good initial guess. Each iteration of Gummels method solves a sequence of relatively small linear subproblems. The subproblems are obtained by linearizing one equation of the set with respect to its primary solution variable, while holding other variables at their most recently computed values. Solving this linear subsystem provides corrections for one solution variable. One step of Gummel iteration is completed when the procedure has been performed for each independent variable. Gummel iteration typically converges relatively slowly, but the method will often tolerate relatively poor initial guesses. The Gummel algorithm cannot be used with lumped elements or current boundary conditions [16].

3.3 AC Analysis

AC analysis or frequency domain perturbation analysis can be used for the small-signal and large signal characteristics. AC analysis can be done using the frequency statement in the SOLVE statement. SOLVE statement is used for the DC analysis of the device. Frequency, fstep, and nfsteps determine the frequency range for which solutions are obtained. To calculate the small signal parameters of this 3-D device proper voltage is provided at the gate and source terminals and provide a valid frequency for AC analysis [17]. In this thesis provided frequency range is in 100GHz.

3.4 Extract Commands

The Extract commands are used namely "Curve VT Extraction" and "Curve Subvt Extraction". These commands are used to evaluate the Subthreshold Slope and Threshold Voltage of the device opertaing in subthreshold region [18]. Subthresold slope can be mathematically evaluated by the following equation:

$$\text{SS} = \text{d}V_g/\log(I_d) = \log(10)(1 + C_s/C_o x)\text{kT/q}$$

Chapter 4

Proposed Work

4.1 Drain Current characteristics of JLT FET

The drain current characteristics of JLT FET is the most important study to know how the device would work in different bias conditions.
In this thesis, since the device is studied in subthreshold region, the I_d-V_gs characteristics is evaluated in that region only. The comparison of all the results of JLT FET is being done with DG MOSFET so that a comparative study can be done between both the devices and various merits and demerits of the devices can be figured out. The devices is simulated bias conditions at very low drain voltage.
This is also helpful in knowing whether that particular device is used for a particular application or not depending upon the requirements of that application. [19]

The devices are biased at very low drain voltage of V_{ds} = 0.4V so as to analyse for ultra low power consumption. Thickness of silicon and oxide layer is varied from 6nm to 8nm and 1nm to 1.7nm respectively. The silicon nanowire in JLT FET is highly doped having the doping density of 10^{19} /cm^{-3} to 3X10^{19} /cm^{-3}. In case of DG MOSFET the substrate is doped by p-type material with doping density of 10^{15} /cm^{-3} and S/D regions are doped with n-type material with doping density of 10^{19} /cm^{-3}. The devices are evaluated for these values of parameters and optimised for a particular set of values of parameters so that the further analysis on the device can be done for low drain bias.

4.2 Capacitance Voltage Characteristics

The knowledge of various capacitance values of the nano devices is important in the sense that by using these characteristics only, the ON-OFF characteristics can be decided for a particular device. It also enables to find out how fast the particular device is switching on or off. [20]
In the subthreshold region, this analysis shows how sensititive the device is when operated in that region as it is analysed in that region only purposedly. The C_{gg}-V_{gs} graph is plotted and the analysis is being done [21].

4.3 Subthreshold Sensitivity Analysis

As described in Chapter 3, sensitivity analysis is being done for the performance metrices which includes S-Slope, C_{gg} and intrinsic delay. This analysis is being done for a change in device parameters which consists of t_{si}, t_{ox}, L_g and N_d and it is important to know as to how the device will react for a certain change in any of the parameters. The results are obtained and analysed as for what values of device parameters the operation of JLT FET can be optimised for the particular application of ultra low power consumption [22].

Chapter 5

Results and Discussion

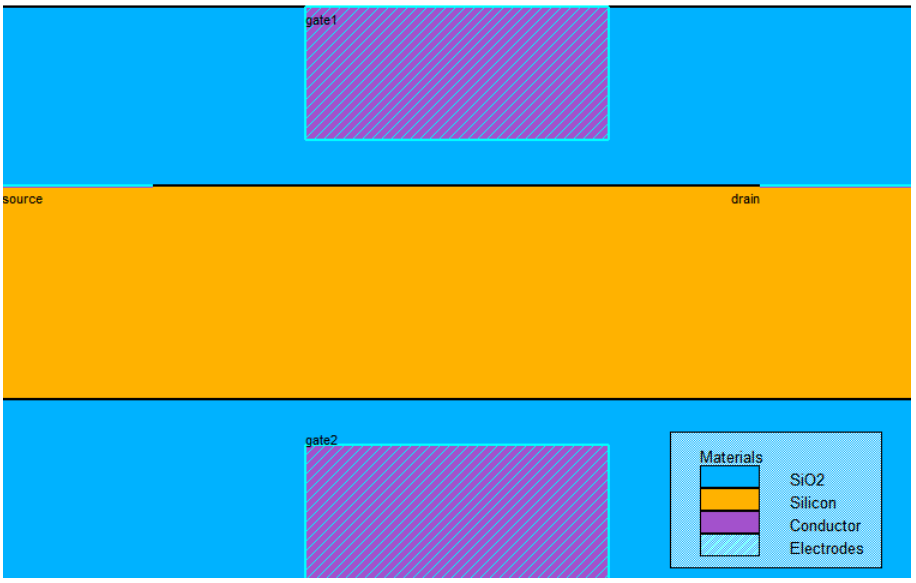

Figure 5.1: Cross Section view of the simulated Junctionless Transistor

In figure 5.1, the simulated figure of Junctionless tranisitor has been shown. The simulation has been done for $t_{si} = 8nm$, $t_{ox} = 1.7nm$, $N_d = 1\text{x } 10^{19}$ and $V_{ds} = 0.4V$, $I_{off} = 10^{-5}\ uA/um$

The gate material used here is p-type polysilicon. It is clearly shown here that the double gate architecture has been simulated here. It is also shown here that a single silicon nanowire having two gates on both the sides. Unlike DG MOSFET, there is no depletion region formed due to the diffusion. The drift current only flows from the substrate.

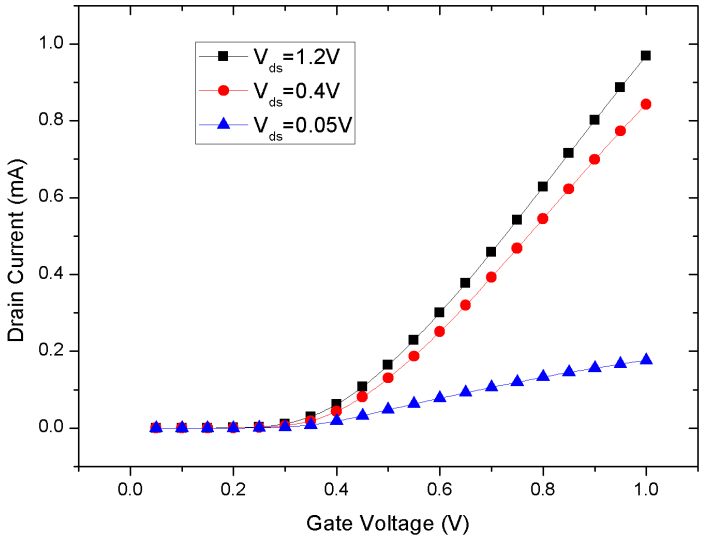

Figure 5.2: $I_d - V_{gs}$ characteristics of JLT MOSFET for different V_{ds}

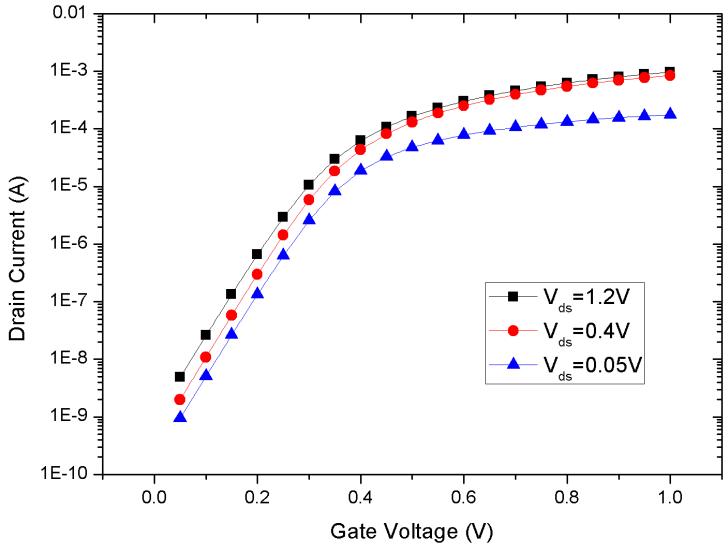

Figure 5.3: $I_d - V_{gs}$ characteristics of JLT MOSFET for different V_{ds} on semilog scale

In figure 5.2 and figure 5.3, the drain current is plotted with respect to gate voltage in linear and semilog scale respectively. The gate voltage is applied as a common on both the gates for different V_{ds}. It shows that by increasing drain-to-source voltage, drain current increases which shows the direct dependence of drain current on drain-to-source voltage. The on-current which is generated by increasing the gate-to-source voltage is higher as the voltage increases. On the other hand, it can also be implied from figure 5.3 that off-current also increases by increasing the voltage. Hence, there is

a trade-off between the on and off currents. The gate voltage, thus selected to optimise the use of device in subthreshold region.

It also corresponds that by increasing the drain-to-source voltage, it reduces the potential difference near the drain side. Hence, the depletion layer will have the more depth in the substrate near the source side.

The following equation can be used as to understand the above explaination mathematically.

$$X_d = -\frac{\epsilon_s t_{ox}}{\epsilon_{ox}} + \sqrt{\left(\frac{\epsilon_s t_{ox}}{\epsilon_{ox}}\right)^2 + \frac{2\epsilon_s(V_{fb} - V_g)}{qN_d}} \tag{5.1}$$

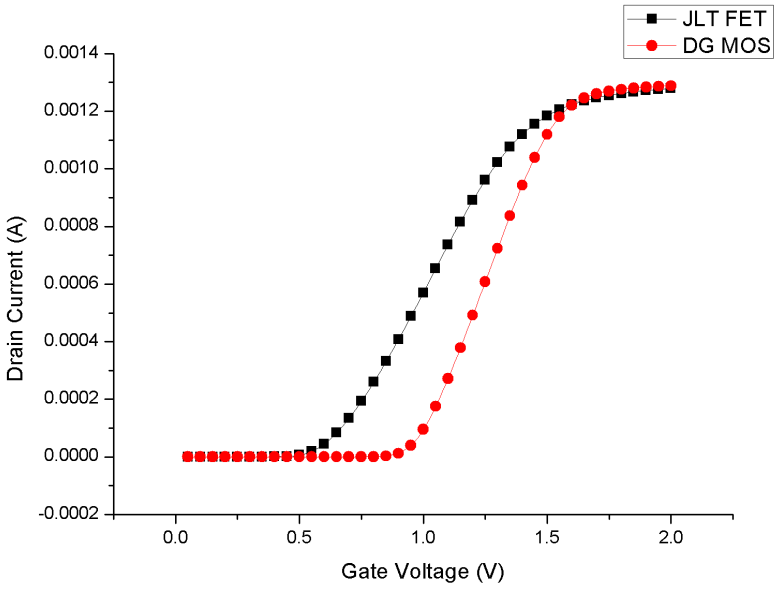

Figure 5.4: Comparison of $I_d - V_{gs}$ characteristics of JLT and DG MOSFETs

Figure 5.4 directly provide the sense that how JLT MOSFET has the better performance than DG MOSFET. The figure shows that at zero gate bias, DG MOSFET is normally-OFF device and by applying some positive voltage, it gets ON which enables the charge carriers to flow through it. On the other hand, JLT MOSFET shows the flow of current at a bias which is lower than that is applied on gate of DG MOSFET. It also shows that the change from ON state to OFF state in JLT FET is slow than that in DG MOSFET. It shows that in subthreshold region, JLT FET shows better subthreshold slope as compared to DG MOSFET. This also enables to select and vary the thickness of silicon

nanowire upto such extent at which the device becomes OFF at zero gate bias. This can be explained by the fact that there is already a depletion layer formed in the silicon nanowire due to the workfunction difference between silicon and gate material.

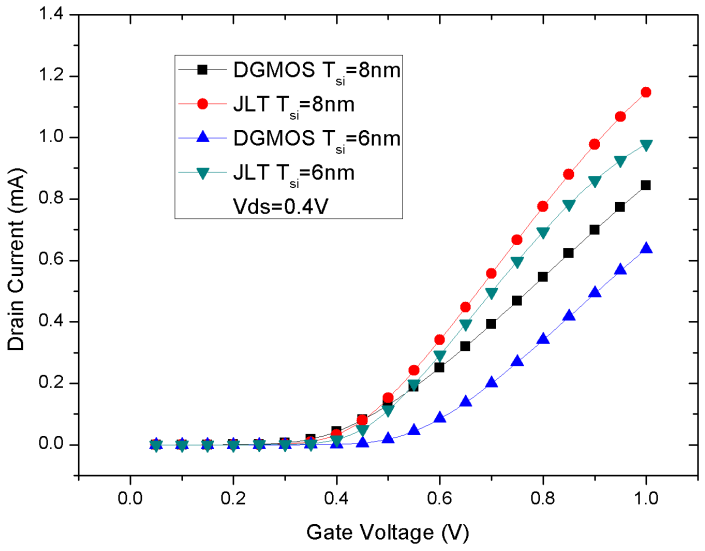

Figure 5.5: $I_d{-}V_{gs}$ characteristics of JLT MOSFET for different t_{si}

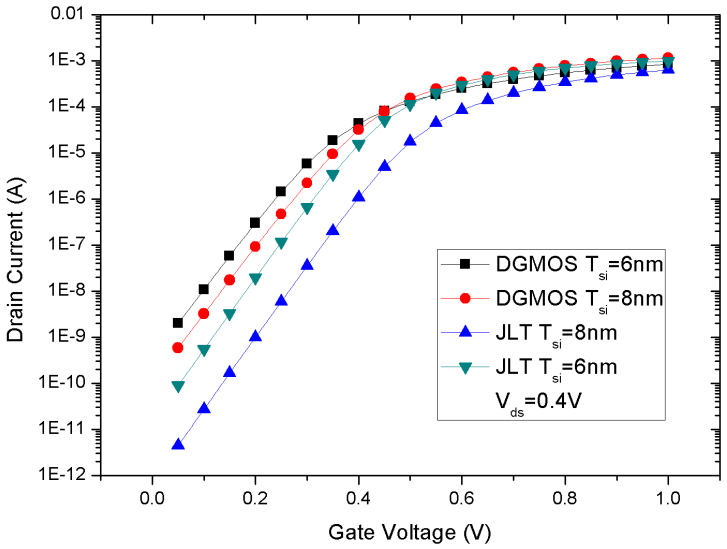

Figure 5.6: $I_d{-}V_{gs}$ characteristics of JLT MOSFET for different t_{si} on semilog scale

Figure 5.5 and Figure 5.6 shows the change of drain current with respect to change in gate voltage for different t_{si}. This will create an understanding of the earlier quoted point that how the channel thickness can affect the drain current. The more the thickness of silicon nanowire the less the channel will be depleted by work function difference of

silicon and gate material. Since the current starts increasing from a lesser value of V_{gs} which means that it requires a less voltage to make the channel undepleted. It can also be understood by the fact that as the thickness of silicon nanowire increases, the more depth of depletion region is required. The off-current can be justified by the fact that as the threshold voltage is same for both the devices the decrease in current is faster in JLT FET than in DG MOSFET.

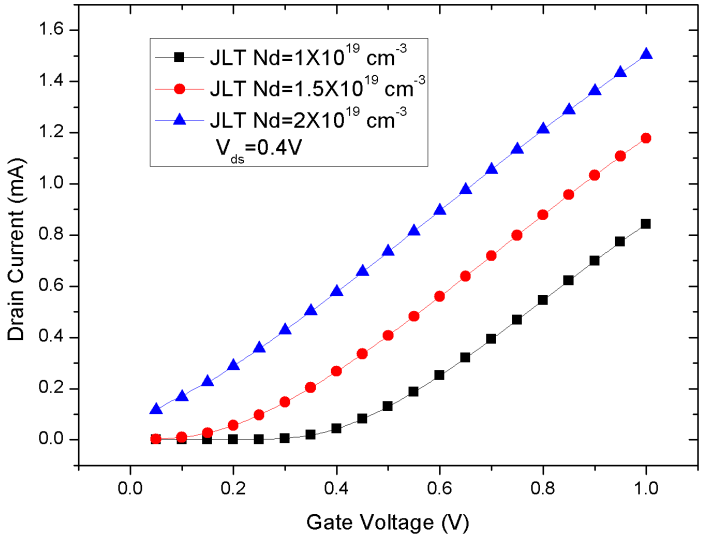

Figure 5.7: $I_d - V_{gs}$ characteristics of JLT MOSFET for different N_d

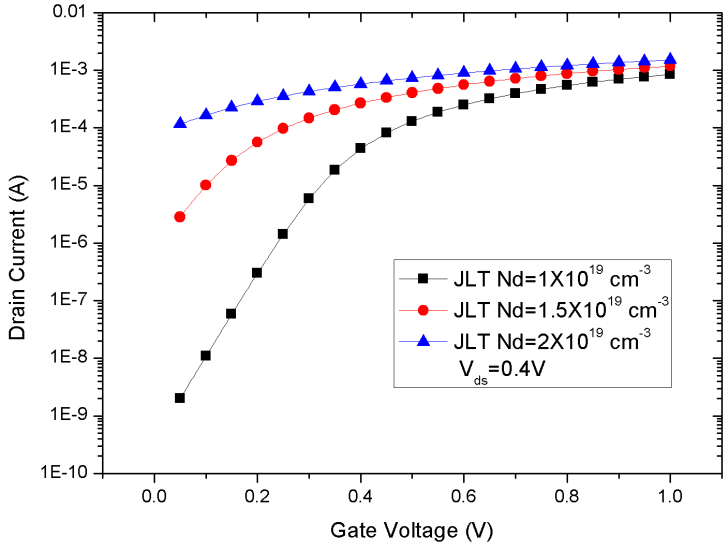

Figure 5.8: $I_d - V_{gs}$ characteristics of JLT MOSFET for different N_d

Figure 5.7 and figure 5.8 shows the change of drain current with respect to change in gate voltage for different N_d. It can be shown from the figures that N_d increases, drain current increases which means that the drain current have directly proportional relation with doping of substrate. Secondly, as the doping increases the device becomes ON at very lesser gate bias then that of with the configuration of previously doped device. It shows that if the substrate has high number of charge carriers, it will directly affects the turn-on capabilities of the device.

Further, with the increase in doping of the substrate, there comes a situation that the workfunction difference between the gate and substrate materials is unable to deplete the substrate at zero gate bias and there is a significant drain current which can flow through it at zero bias. From figure 5.8, it can also be implied that for higher doping the device is unable to get off and there is a significant current at V_{gs}=0V.

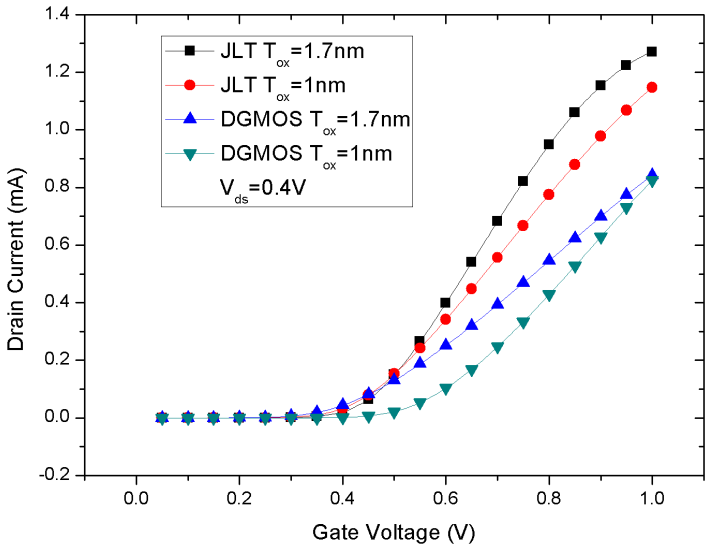

Figure 5.9: $I_d - V_{gs}$ characteristics of JLT MOSFET for different t_{ox}

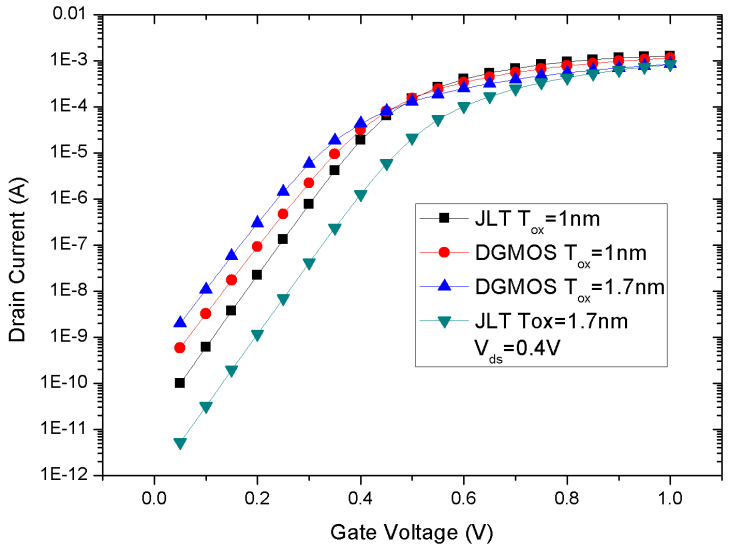

Figure 5.10: $I_d - V_{gs}$ characteristics of JLT MOSFET for different t_{ox} on semilog scale

Figure 5.9 and figure 5.10 shows the change of drain current variation with respect to change in gate voltage for different t_{ox}. As t_{ox} increases, drain current increases. From the figure, it can be shown that as the thickness of the oxide increases, the electrostatic control of gate over the channel reduces and hence, it can be shown from the figure also that as the t_{ox} increases drom 1nmm to 1.7 nm the drain current starts flowing in the channel at a lesser value of gate voltage. Moreover, the turn-on capabilities of the device also degrades as the oxide thickness increases. For the same threshold volage of two different devices, it is observed that JLT FET has lesser off-current than DG MOSFET. Hence, the leakage current is less in JLT which can be useful for ultra low power appliactions as there is low static power consumption in the device.

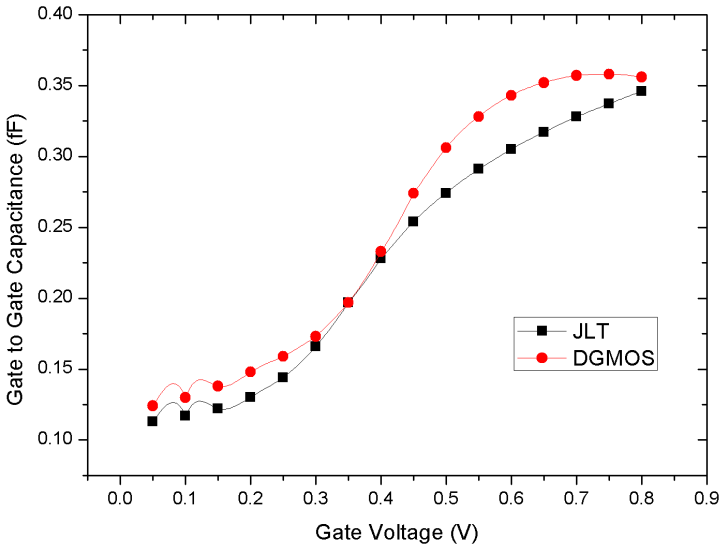

Figure 5.11: $C_{gg}-V_{gs}$ characteristics of JLT MOSFET

Figure 5.11 shows the variation of gate-to-gate capacitance with respect to gate voltage. As the graph suggests that there is a non-linear increase in values of C_{gg} with respect to increase in gate voltage. It is also observed that C_{gg} for JLT FET is less as compared to DG MOSFET. This is due to the parasitic capacitance contribution only in JLT FET. [23]

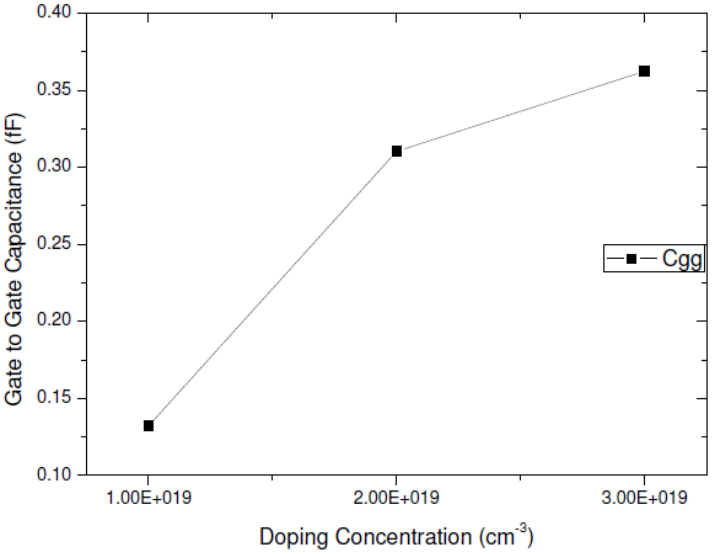

Figure 5.12: C_{gg} characteristics of JLT MOSFET for different N_d

Figure 5.12 shows the variation of gate-to-gate capacitance with respect to three different doping level. As the graph suggests that the C_{gg} increases as the doping level in

the substrate increases. As the doping increases, the number of charge carriers in the substrate increases. It increases the C_{dep} and hence contributes in the increase of C_{gg}.

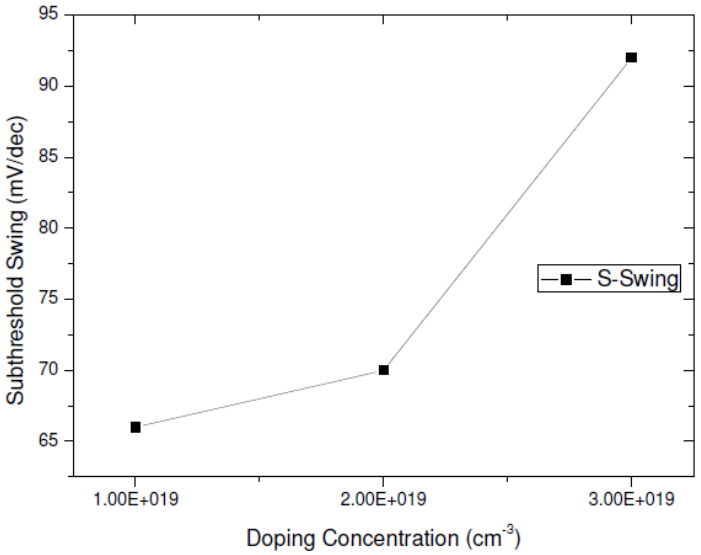

Figure 5.13: Subthreshold Slope characteristics of JLT MOSFET for different N_d

Figure 5.13 shows the variation of subthreshold slope with respect to three different doping densities of the substrate. The graph shows that with the increase in doping density, the subthreshold characteristics of the device degrades. Since, for the low power applications, the speed of the device is secondary, hence the S-Slope which is near to the ideal S-Slope which is 60 mV/decade proves to be significant and useful for such applications.

Device Parameters		JLT FET		DG MOSFET	
		SS (mV/dec)	Sensisitivity	SS (mV/dec)	Sensisitivity
Tsi	8 nm	66.1757	0.142	75.1979	0.119
	6 nm	63.1775		72.7222	
Tox	1.7 nm	66.1757	0.072	75.1979	0.061
	1 nm	63.0121		72.5138	
Nd	1.00E+19	66.1757	0.546	75.1979	NA
	2.00E+19	102.274			
Lg	20 nm	66.1757	-0.005	75.1979	-0.026
	40 nm	60.8874		81.6523	

Figure 5.14: Table showing different values of sensitivity of S-swing for JLT FET and DG MOSFET

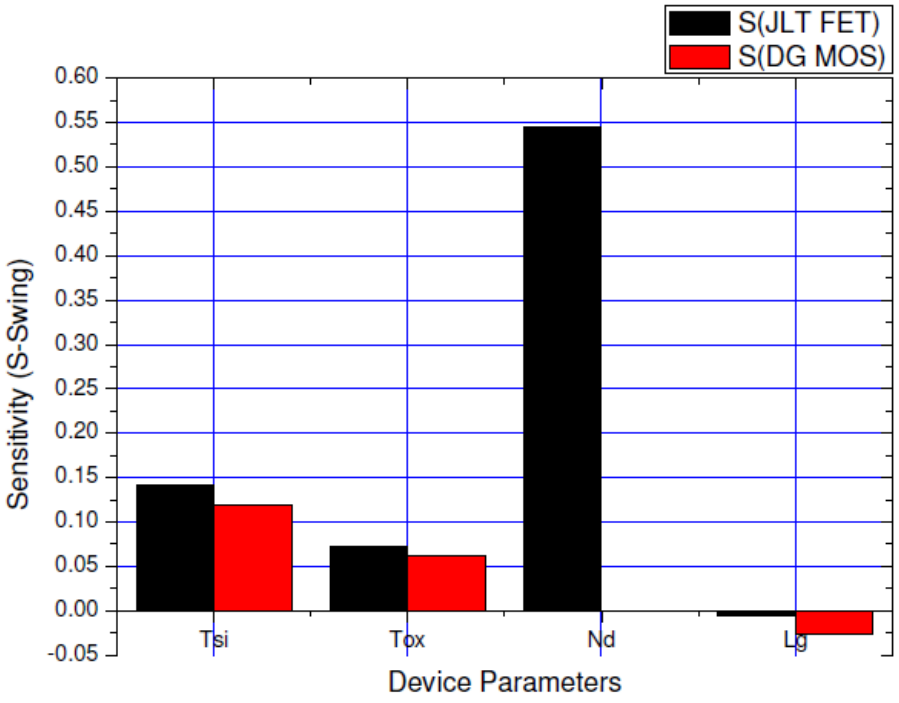

Figure 5.15: Sensitivity of subthreshold swing of JLT FET and DG MOSFET with respect to device parameters

Figure 5.14 and figure 5.15 shows the different values of sensitivity of S-Swing with respect to change in device parameters of the devices. From the bar chart it is concluded that JLT FET exhibits high sensitivity of S-Swing with respect to all parameters except gate length. Hence, JLT can be used at very less gate length also as per the requirement of a particular application.

Device Parameters		JLT FET		DG MOSFET	
		Cgg (fF/m)	Sensisitivity	Cgg(fF/m)	Sensisitivity
Tsi	8 nm	0.13	1.005	0.11	0.699
	6 nm	0.097		0.0894	
Tox	1.7 nm	0.13	0.158	0.11	0.033
	1 nm	0.117		0.108	
Nd	1.00E+19	0.13	1.152	0.11	NA
	2.00E+19	0.31			
Lg	20 nm	0.13	-0.009	0.11	-0.192
	40 nm	0.129		0.101	

Figure 5.16: Table showing different values of sensitivity of C_{gg} for JLT FET and DG MOSFET

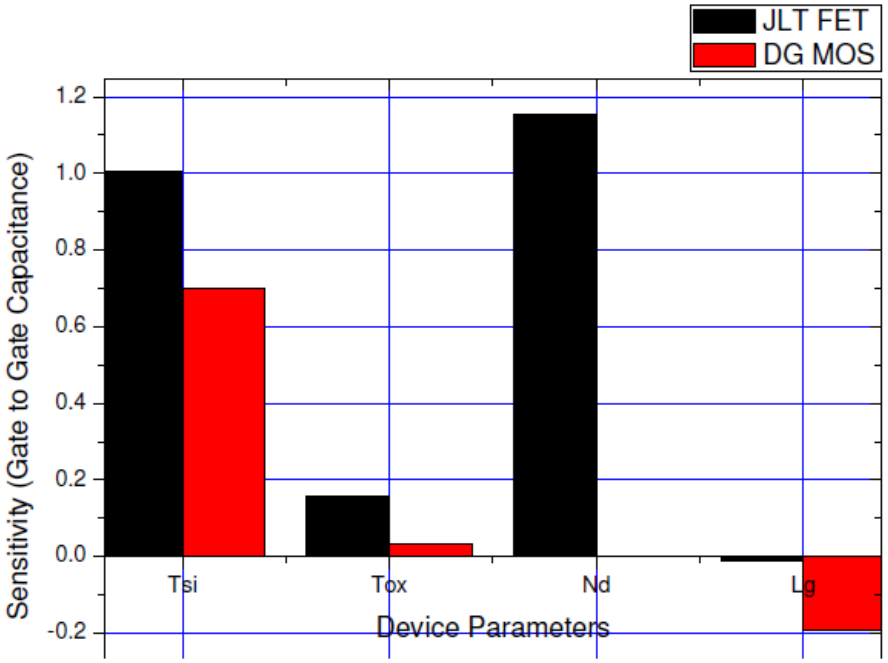

Figure 5.17: Sensitivity of gate-to-gate capacitance of JLT FET and DG MOSFET with respect to device parameters

Figure 5.16 and figure 5.17 shows the different values of sensitivity of C_{gg} with respect to change in device parameters of the devices. From the bar chart it is concluded that JLT FET exhibits comparatively high sensitivity of C_{gg} with respect to all parameters except gate length. So, again it can be said that JLT FET is useful for the short channel devices.

Device Parameters		JLT FET		DG MOSFET	
		τ(ps)	Sensisitivity	τ(ps)	Sensisitivity
Tsi	8 nm	1.642	-2.1876	1.019	-2.91
	6 nm	2.54		33.26	
Tox	1.7 nm	1.4785	-0.142	1.019	-1.38
	1 nm	1.642		33.92	
Nd	1.00E+19	1.642	-1.429	1.109	NA
	2.00E+19	0.213			
Lg	20 nm	1.642	20.638	1.109	87.145
	40 nm	22.28		88.254	

Figure 5.18: Table showing different values of sensitivity of intrinsic delay for JLT FET and DG MOSFET

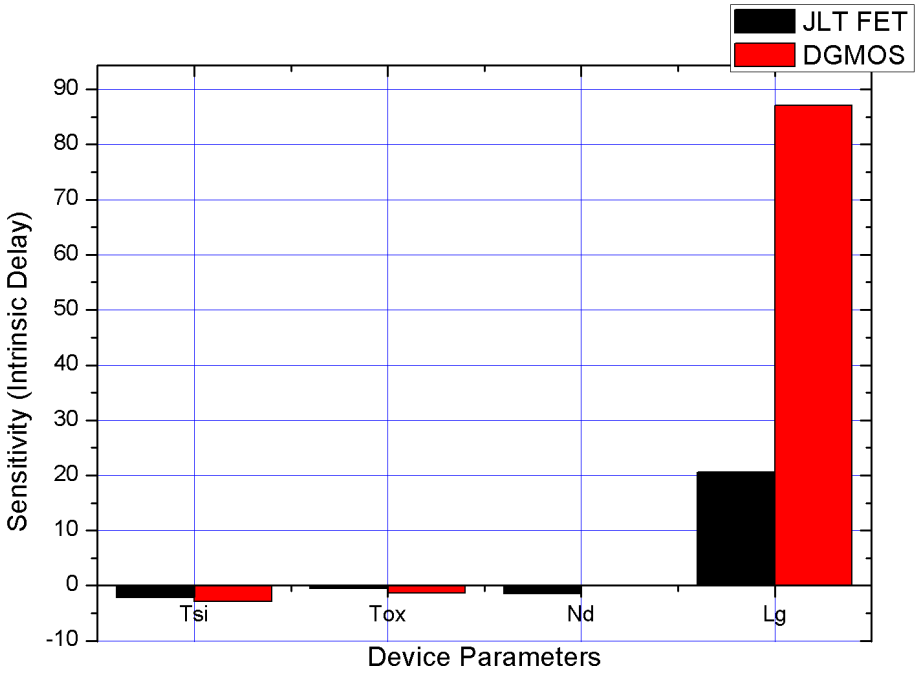

Figure 5.19: Sensitivity of intrinsic delay of JLT FET and DG MOSFET with respect to device parameters

Figure 5.18 and figure 5.19 shows the different values of sensitivity of intrinsic delay with respect to change in device parameters of the devices. From the bar chart it is concluded that JLT FET and DG MOSFET exhibits almost same sensitivity values of intrinsic delay with respect to all parameters except gate length. For the gate length, DG MOSFET exhibit a higher value of sensitivity hence slowing the device.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

The Junctionless field effect transistor is analysed for low drain bias in subthreshold region. The results are comapred with that of the conventional Double Gate MOSFET in the same region. The results clearly predicts several points. The OFF current is much negligible in JLT which adds an advantage to the device. Secondly, the device channel width modulation in JLT is quite simpler than that of the counterpart.

It is also observed that the performance of JLT FET varies by varying thickness of silicon and oxide and doping but for the channel length the performance has a negligible effect due to no SCEs in JLT provided that the optimum values for thickness of oxide and silicon and doping are selected. The performance of JLT FET is determined in subthreshold region and it is concluded that it shows better results with that of the DG MOSFET.

It is also observed that the SCEs in case of JLT FET has not much affect on drain current characteristics and hence it can be scaled further to answer the needs of minitiarisation. As no SCEs are there in JLT FET, the scaling of transistor to much less extent than other devices is possible.

The same can be concluded by the anaysis of Sensitivity of performance metrices of both the devices. As the primary concern is to how to decrease the channel length without affecting the performance of the device, can be best understood with the help of JLT FET. Although, it has a limitation in the form that it shows comparatively high sensitivity values for some parameters but JLT has the least sensitivity when it comes to changing channel length.

The results also concludes that the JLT has low I_{off} as compared to other devices, hence the static power consumption is very less. This point has more significance in order to

work the device in subthreshold region when low voltage is applied.
The results also predicts that JLT has the optimum value of subthreshold slope which is added feature for lower power consumption as well as turn on capabilities.

6.2 Future Scope

Based on the research which is already done on JLT FETs and this work, it is suggested that the different geometries could be explored to get the better results. The devices other than the JLT FETs can also be explored to compare the results of those devices with that of JLT FET.
The research on material physics can also be done over JLT FET so as to find out the different alternative materials which show the similar properties as that of silicon, germanium or other semiconductor materials. Oxide materials also can be explored at the same time.

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