A DISSERTATION REPORT

ON

SoC APPLICATION DESIGN: ON-CHIP LOW DROP OUT VOLTAGE REGULATOR

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VLSI DESIGN

to the

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by

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JAIPUR (RAJASTHAN) – 302017

Certificate

This is to certify that the dissertation report entitled **SoC Application Design : On-Chip Low Drop Out Voltage Regulator** submitted by **Tinku Kumar(2017Pev5208)**, in the partial fulfilment of the Degree Master of Technology in **VLSI Engineering** of Malaviya National Institute of Technology, is the work completed by him under our supervision, and approved for submission during academic session 2018-2019.

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Abstract

The Integrated Electronics (Intel) needs no introduction to a technologist, academician or a layman on what services it has unveiled to mankind. Of course, the dimension of research and hard work with pure and conscientious discharge of a number of intellectual human brains has made Intel achieve the position it holds today in the global market. Being in analog domain regulators are the essential part of any electrical powered system, which includes the growing family of applications of portable battery operated products. As a result low dropout regulators are always in high demand.

In this dissertation, A CMOS On-chip Low Drop-out Regulator with Improved PSRR is proposed. The proposed circuit is developed using error amplifier and PMOS as pass device. For the improvement of dc PSRR, the two stage error amplifier with PMOS input differential pair followed by NMOS common source stage and PMOS pass device topology is used. With the help of Miller Compensation technique, stability of the LDO is achieved.

The LDO is designed in CMOS 10nm process technology. The importance of the obtained results is to maintain stability for a wide range output capacitance and output current while keeping a reasonable regulation performance and good transient response with the help of frequency compensation technique.

Capacitor-less solutions are very attractive as compared to LDO's with external capacitor. The external compensated LDO's huge output capacitor helps the regulator in suppressing output voltage variations in case of fast and high power load currents. Because of the huge output capacitance, a series resistance may cause increment in voltage spike while LDO load transient. In case of capacitor-less LDO's due to the small output capacitance with zero series resistance the voltage spikes are very large. But, these voltage spikes are minimized by improving bandwidth of the LDO. There is no need of special compensation techniques as like external capacitor LDO.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The demand for Low Drop-out (LDO) regulators has been driven with the aid of the portable electronics marketplace as well as industrial and automobile applications [2]. Most recently, the High speed serial I/O, Display and memory applications are demanding for lower operating voltages. Furthermore, the improvement in battery lifetime can be achieved by higher current efficiencies. The ground current or quiescent current and overall load current both together will determine the life of the battery. This chapter discusses the role and necessity of Low Drop-out regulators in today's High speed I/O and Display applications. The objective of the thesis is then identified and described in step with the needs that drive regulator design into the future.

1.2 DEFINITION

Low Drop-out (LDO) voltage regulator is kind of series regulator which will provide stable DC output voltage without any ripples in the output voltage [1]. Low drop-out means the upper swing limit for the output voltage closed to supply levels and the load current should be more than zero. Since the V_{drop} out voltage is described as the margin between o/p voltage which is regulated and input supplied. Conceptual implementation of linear regulator is given in following Fig.1.1.

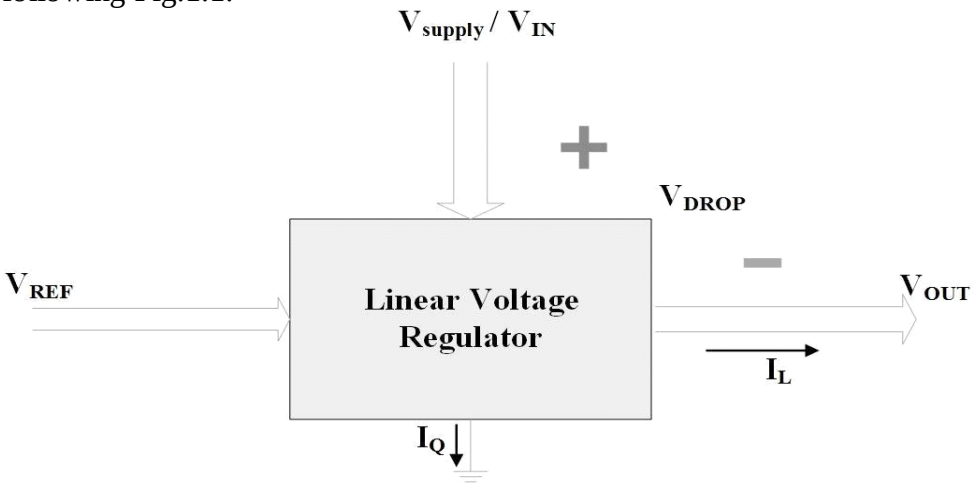

Fig.1.1 Top Level module for Linear Voltage Regulator

For the voltage regulator, output resistance should be as low as possible. Because of the low output resistance, voltage regulators are acts as a voltage controlled voltage source. With the help of the shunt feedback, minimization of output resistance is achieved. As shown in Fig.1.1, the reference voltage (V_{REF}) generated from resistor ladder or from bandgap reference voltage will help to produce output voltage (V_{OUT}) which is independent of supply voltage. Addition of Load current (I_L) and current which is quiescent (I_Q) is the current which is consumed by the circuit. Hence, the total input and output power is given by,

$$P_{IN} = V_{supply}(I_L + I_Q) \quad (1.1)$$
$$P_{OUT} = V_{OUT} I_L \quad (1.2)$$

Efficiency of regulator is given by,

$$\eta = \frac{Pout}{Pin} = \frac{VoutIl}{Vsupply(Il+Iq)} = \frac{Vout}{Vout + Vdrop} \frac{Il}{Il+Iq} \quad (1.3)$$

In the equation 1.3, the efficiency of LDO is improved by minimizing the drop-out voltage that is V_{DROP}. I_Q is the Quiescent current or Ground current that is composed of the current required for biasing of error amplifier and current flowing through pass device when LDO is operating at low load ideally load current of 0mA.Therefore, the higher current efficiency is achieved by minimizing the overall I_Q. A good specified as well as DC o/p voltage V_{OUT} which is stable & is obtained by error signal which is feeded back by amplified version of the same which will control the I_L of the output stage that is pass device. This type of linear regulator specified by characteristics:

1.Magnitude of output voltage is lesser than the respective input voltage.
2.Output resistance is as low as possible in order to improve the regulator performance.

Depending upon the application the Low Drop-out (LDO) voltage regulator are characterized as low power and high power. Furthermore, the power is defined by the current handling capability of LDO. For serdes application it is always less than 1A and for industrial application it is greater than 1A.

1.3 MARKET DEMAND

1.3.1 High current efficiency, Low voltage and Low drop-out

In the present day scenario, most of the portable devices are mainly focused on battery operated. In the High speed serial I/O application or in display application, power dissipation is the most important factor. Most of the power in this applications is consumed by its transmitter driver only. So, it is important to make this drivers will be operated at low voltages.In case of Mobile Industry Processor Interface (MIPI) application, the transmitter driver needs to be operated at 400mV supply but the other blocks in transmitter IPs are operating at different voltage levels. It is important for the IP to derive the 400mV voltage from the main supply line without any ripples present in the output voltage. For this, LDO need to perform the stepdown operation with very less biasing current or ground current to provide stable and ripple free output voltage. As the supply levels are very low for the present IPs, noise is important parameter which is mainly focused while operating these IP's. Present market demand mainly focused on high current efficient LDO's with better ripple rejection ability [5]. Also, chip area will play an important role while focusing on portable applications. Hence, the LDO's with on chip capacitors has to provide better transient response as compared to off chip capacitors LDO's. Minimization of drop-out voltages in a low voltage surroundings is also important to maximise dynamic range. This is due to the fact the signal-to-noise ratio decreases because the electricity deliver voltages decrease even as noise typically stays consistent.

1.3.2 Alternative: Switching Regulators/ Buck Converters

Another option for Linear Drop-out (LDO) voltage regulators are buck converters or switching regulators. The buck converters provides excellent power efficiency as compared to LDO [23].The basic idea behind buck converter is energize the capacitor or inductor and delivered the stored charge to the load. Fig.1.2 shown the block level diagram for buck converter.

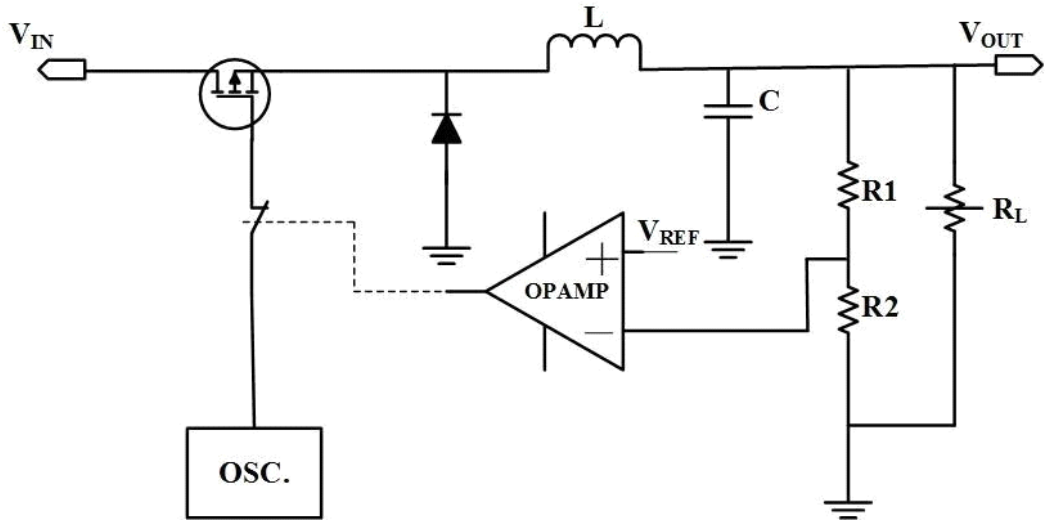

Fig.1.2 Block Diagram of Buck Converter

Both LDO and buck converters requires reference voltage (V_{REF}) that will be generated from bandgap reference voltage or resistive ladder voltage reference. The principle of switching regulator is to energize the capacitor or inductor and delivered the energy from them to the load. But the problem is how to energize the capacitor or inductor? Therefore, a series element which is nothing but the switch is used to provide supply to the energy storing elements as shown in Fig.1.2. Here the gate voltage of the MOSFET is switched, switch is used to control the gate voltage therefore it is called as switching regulator. When the switch is ON, then inductor gets energized and RL gets energy from the source. In second case, when the switch is open, R_L gets stored energy from inductor (L) as circuit is completed by diode. When the inductor (L) is dropped that is current storage capability came down, it will again switch on the regulator or gate voltage which charges inductor (L). So, this open close switch action will be continued always. Because of this switching activity, there are ripples present in the output voltage of the buck converter. For the regulator point of view, response of the regulator is considered to be the important factor, as the buck converter consists of more number of components which defines the response time is very poor as compared to fewer components LDO. The number of components are more in case of buck converter gives limitation on the bandwidth of the regulator. For the switching regulator, regulator bandwidth must fall below the switching frequency by a decade. And, increasing switching frequency is not an option since regulator may face switching losses which causes battery to dissipate more power and reduces the lifetime of the battery. IoT devices are connected to battery driven supply, so LDO's are the better options. In some of the applications LDO's can be used along with buck converters.

1.4 MOTIVATION AND PROBLEM STATEMENT

The study for power stability an management techniques has monotonically increased to the vast increase of portable, handheld . Management of power will seek to further improve the device power efficiency and operating time of the device.. Especially in surprisingly complicated gadget-on chip designs, a huge range of those simple regulators are required alongside the interfaces of the diverse sub-circuits. In spite of this huge demand, No work exists for the same to implement and optimize this kind of low value, low complexity regulator circuit. The project will address then by presenting a current efficient power low, on-chip LDO voltage regulator which is below then 1V regulated o/p voltage with the proposition of quick response (QR) ckt and high PSRR to improve the transience response of the load and further maximize the battery life.

1.4.1 Objective

The objective of this venture is to layout On-chip Low Drop-out Voltage (LDO) Regulator to generate the regulated output voltage for under 1V this is zero.4V to 0.6V with the drop-out voltage of minimal 0.4V.The principal objective of this venure might be to design and broaden a on-chip low energy completely CMOS LDO which is primarily based to quick reaction (QR) circuit and further used to enhance the load transience reaction which then trap on the spot of load fluctuation from the condition which is low power and then to improve excessive PSRR to acquire good battery existence. Furthermore, this proposed circuitry will provide a strong output voltage irrespective of how rapid the load changes. In this work, a zero.4V to 0.6V, 2mA-10mA LDO load contemporary with the proposed brief response circuit has been designed and applied in a 10nm AMS CMOS era using Intel's unique tool for schematic seize. In the assignment, several design options and architectures are explored for overall performance alternate-off analysis.

1.4.2 Work Scope

The reason for this project undertaking is to design a low drop-out voltage, small output hunch, aggressive load regulation and small silicon area LDO without making use of a massive capacitor. The proposed circuit consists of circuit which voltage referenced, error amplifier circuit, rate and circuit discharge , and skip element. In primary the objective of the project then is to observe finally and understand the Low Drop-out Voltage Regulator and its utility. There are few key considerations which could define the scope of the work.

a. Conceptual layout on systems degree (pinnacle down design of block diagrams).
b. Smaller subsystems generation from breakdown of systems.
c. Devices which are realizable in the foundry from bottom to top down design.
d. Design of the Error amplifier for the defined specifications and maintain the stability.
e. Checking up whether the LDO specifications are matching with the Error Amplifier.
f. Design of the Pass transistor for the drop-out voltage of minimum 0.4V with 10mA of maximum load current.
g. Finally checking of the LDO stability for the different loading conditions.

The organization of thesis is as follows:

CHAPTER 1: The chapter involves the discussion for the motivation ,contributions and thesis organization .

CHAPTER 2: In this chapter, the various literature reviews based on different topologies of low drop-out regulators such as on-chip and off-chip capacitor LDO's are discussed. This chapter also deals with stability issues in design of LDO's and available compensation techniques.

CHAPTER 2: This chapter involves the discussion of LDO block diagram in detailed structure along specified with various specifications

CHAPTER 4: Discussion for the proposed design of Low Drop-out (LDO) regulator and the design characteristics in detail.

CHAPTER 5: The chapter discusses Simulation results of the proposed LDO design.

CHAPTER 6: Summary of the proposed design.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

Low drop-out regulators (LDO) are broadly made use in electronic products because of their precision output voltage and less prone to noise. In designing of LDO's, stability as well as area is an important issue. In most common topologies external capacitors are used to achieve stability of LDO's. These topologies are termed as low drop-out regulators with off-chip capacitor. Use of off-chip external capacitors provides a good stability on the cost of portability of device. The stability of this type of LDO's can be achieved by some special compensation techniques that is making an output pole as dominant. LDO's without any obligation of external capacitors are termed as capacitor free low drop-out regulators or on-chip LDO's. Main cause of instability in LDO's is due to pass devices. In CMOS low drop-out regulators, usually common-source PMOS pass elements are used, which have high output impedance. Due to their more o/p impedance ,the o/p location of the pole will be changed with the variation in load and in turns low circuit stability. So, there is requirement of some compensation techniques to improve the stability of LDO's. The chapter is organized as follows. Section 2.2 discusses the various topologies and operations of LDO's available in the literature. The compensation techniques used in the designing of LDO's are discussed in the Section 2.3.

2.2 DIFFERENT TOPOLOGIES OF LOW DROP-OUT REGULATORS

In power management system, LDO's are special class of linear regulators. Different topologies of low drop-out regulators discussed in [10-22]. These topologies are broadly classified on the basis of requirement of external capacitors as LDO's with capacitor [10-16] and capacitor-free LDO's [17-22].

2.2.1 Low Drop-Out Regulators with Capacitor

Oh *et al.* [12] presents a Low drop out voltage regulator with CFA as shown in Fig.2.1. This LDO provides high slew rate and fast response with class-AB operation.

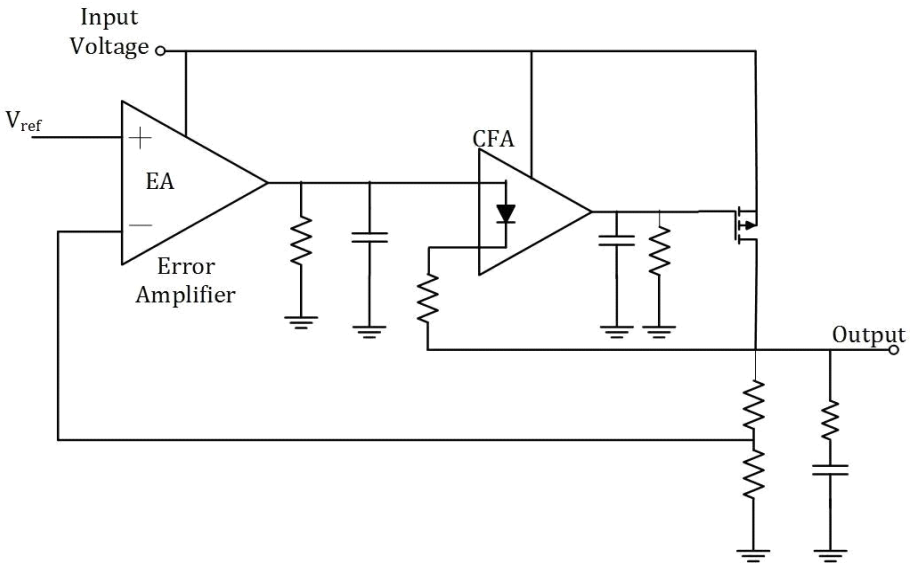

Fig.2.1 LDO structure using CFA based buffer amplifier [12].

CMOS LDO has major problem of high impedance feedback path which has been removed in the suggested structure. This structure affords a low ac impedance remarks direction to attain speedy reaction whilst retaining low quiescent strength consumption. The low ac impedance remarks path is designed using a CFA based second-stage buffer. CFA's are well-known for presenting rapid brief reaction with minimum slew-rate proscribing. It makes use of global voltage mode comments for steady nation accuracy.

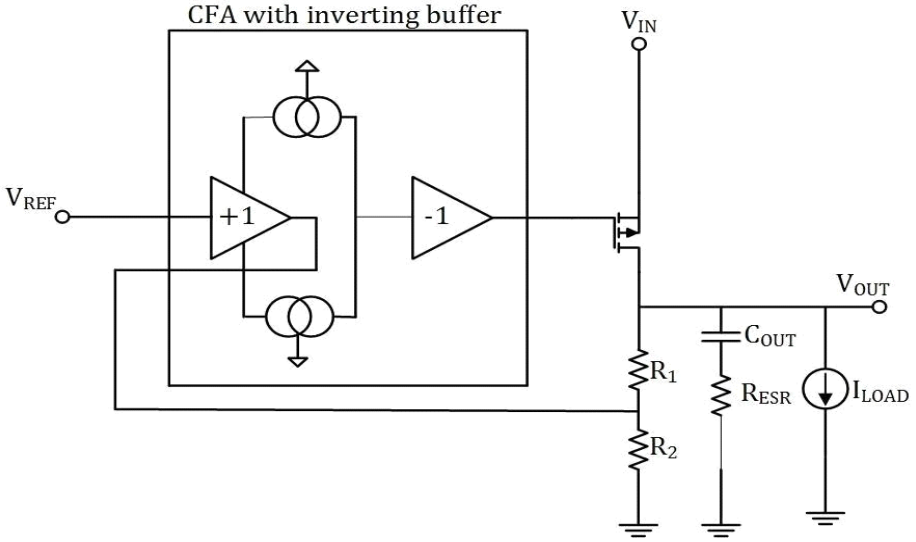

Fig.2.2 LDO architecture based on CFA with inverting output buffer [14].

Chava et al. [16] proposed a low drop-out voltage regulator with low equivalent series resistance (ESR) capacitive loads as shown in Fig.2.3.

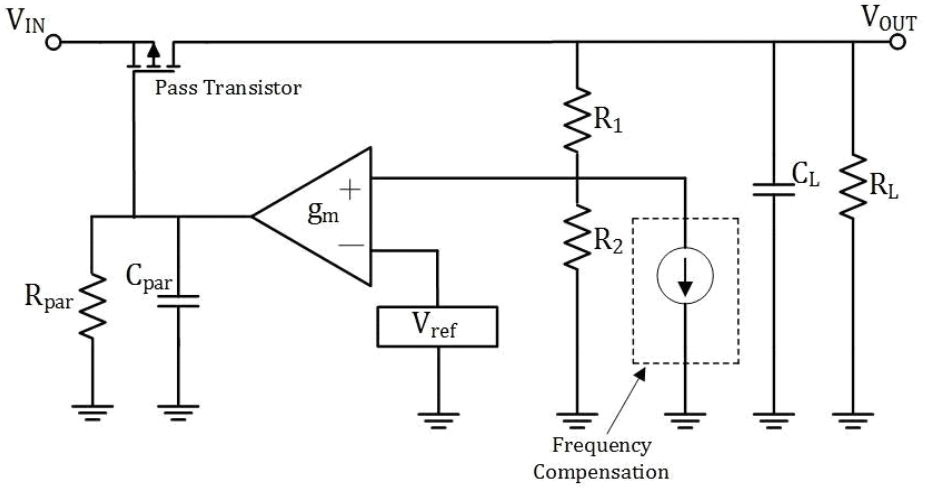

Fig.2.3 LDO with frequency compensation technique [16]

In this approach a zero is generated internally by using frequency compensation technique. Due to generation of internal zero there is less dependency on ESR for stability. In frequency compensation approach, this structure utilizes the concept of capacitive feedback. The capacitive feedback introduces a zero in left side of the s-plane. This introduced zero in the feedback loop is used to eliminate the requirement of ESR. It also minimizes the overshoot as it has less requirement of ESR. This structure does not consume significantly higher ground current or chip area compared to conventional low drop-out regulator. The authors have also suggested that the charge pump as voltage booster is an alternative of ESR. The charge pump

voltage booster generates a voltage better than supply voltage and the mistake amplifier makes use of that voltage for riding a pass device. This structure provides low output impedance, which in return provides stability. This structure has some disadvantage of requirement of additional circuitry.

Table 2.1 Comparison of various specifications of existing LDO Regulators w/ capacitor.

Parameters	Unit	[10]	[12]	[13]	[14]	[15]
Year		2003	2007	2007	2008	2012
CMOS Process	µm	0.6	0.25	0.35	0.35	0.35
Drop-out Voltage	mV	200	-	54	-	99.8
CL	µF	10	0.05	1	1	1
ESR	Ω	1	0.1	N.A.	0.016	-
Ground Current(IQ)	mA	-	0.1	0.02	6	59-189
PSRR	dB	-60 at 10Hz	>43at 30KHz	-	-	>56at100MHz
Current Efficiency	%	-	99.8	99.8	-	99.8
Line Regulation	mV/V	-	-	2	18	13.5

Load Regulation	mV/mA	-	-	0.17	0.28	0.025
Area	mm^2	0.31	0.23	0.264	4.48	-

2.2.2 Capacitor Free Low Drop-Out Regulators

The LDO shape with a capacitor-multiplier frequency repayment method described in [18] is shown in Fig.2.4. This approach gets rid of the cascade structure or buffer stage, due to which suggested LDO facilitates low voltage operation.

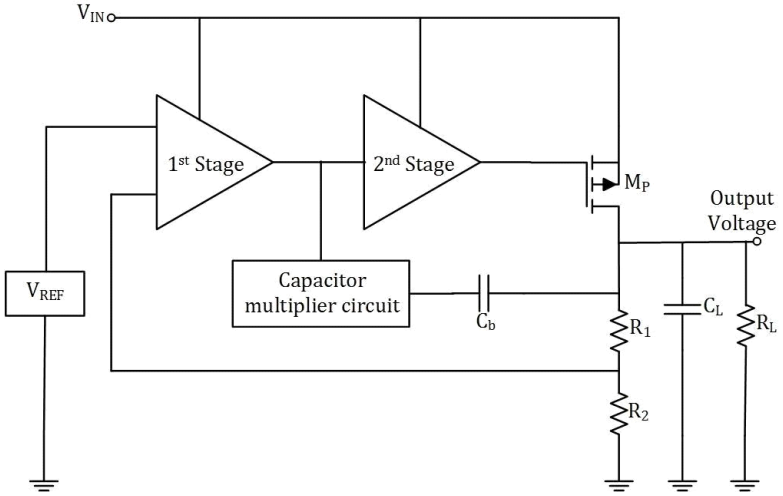

Fig.2.4 LDO with capacitor-multiplier frequency compensation [18].

Shiyang et al. [19] has reported a LDO the use of Damping-thing-control (DFC) block at the side of miller compensation shown in Fig .2.5.

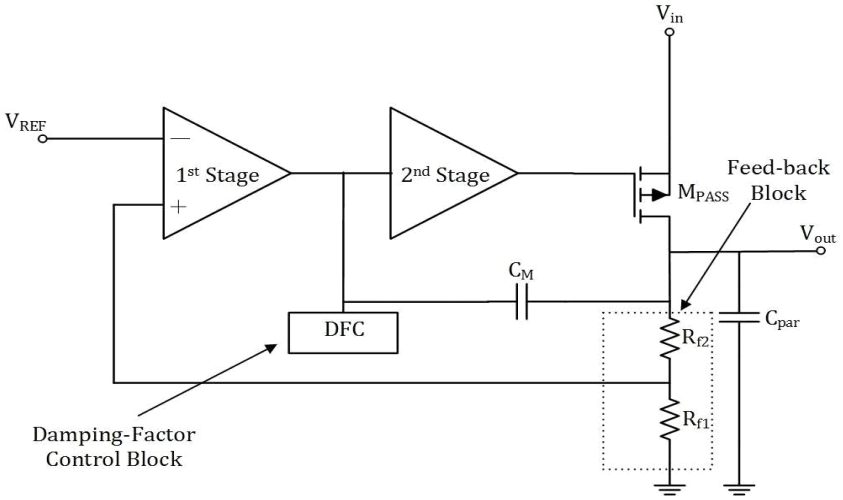

Fig.2.5 LDO Str. With DFC Block[19]

With the help of Miller compensation, a low frequency dominant pole, configured by DFC block is at higher frequencies than the unity gain frequency (UGF). Kamal et al. [21] proposed a topology in which an external capacitor isn't always required for the stability.

Table 2.2 Performance parameters of existing capacitor free Low Drop-out Regulators available in literature.

Parameters	Unit	[13]	[14]	[15]	[19]
Year		2005	2008	2009	2011
CMOS Process	µm	0.09	0.18	0.25	0.35
Drop-out Voltage	mV	90	160	50	110
Ground Current(IQ)	mA	6	0.2	0.04	0.05
PSRR	dB	-	70 at 10KHz	-80 at 1KHz	>50 at 3KHz
Current Efficiency	%	94.3	99.99	-	-
Line Regulation	mV/V	-	1.27	-	0.012
Load Regulation	mV/mA	-	0.002	-	0.005
Area	mm^2	0.008	-	-	0.056

From table 3.2, it is observed that there is no need of External capacitor for that stability of LDO's while maintaining its specifications.

2.3 ANALYSIS OF VARIOUS LDO'S COMPENSATIONS TECHNIQUES

In low drop-out regulators, common-source PMOS pass elements are used. Due to the high output impedance of common source pass elements the output pole location changes with the variation in load and the stability of the circuit decreases. Therefore some compensation schemes are required to increase the stability. The various compensation schemes reported in literature [6] are as follows:

2.3.1 Compensation of LDO's Using Equivalent Series Resistance (ESR)

The compensation technique shown in Fig.2.6, the output capacitor is used by the LDO's to improve the stability [6]. The output capacitor has inherent characteristics of ESR.

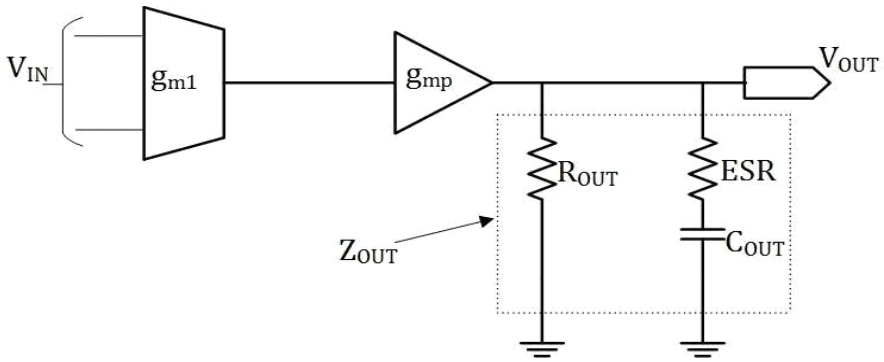

Fig.2.6 Compensation of LDO with ESR

Equivalent output impedance (Z_{OUT}) is defined as,

$$Zout = Rout \,||\, \frac{1}{sCout} + ESR \qquad (2.1)$$

From equation (2.2), it can be seen that the output impedance contains zero introduced by ESR. The zero introduced by ESR is used to reduce excess negative phase shift. The ESR zero frequency is inversely proportional to the output capacitor C_{out}

In this technique, the LDO normally require the output capacitor of appropriate value to assure regulator stability and avoid oscillation [1, 6].

2.3.2 Compensation of LDO's using capacitive Feedback for Frequency Compensation

The basic idea for capacitive feedback is to reduce the requirements of ESR compensation by generating the internal left hand side pole zero to compensate the LDO. It is common approach to compensate two stage operational amplifier compensation. The Fig.2.7 shows thetwo-stage operational amplifier with capacitive feedback compensation technique.

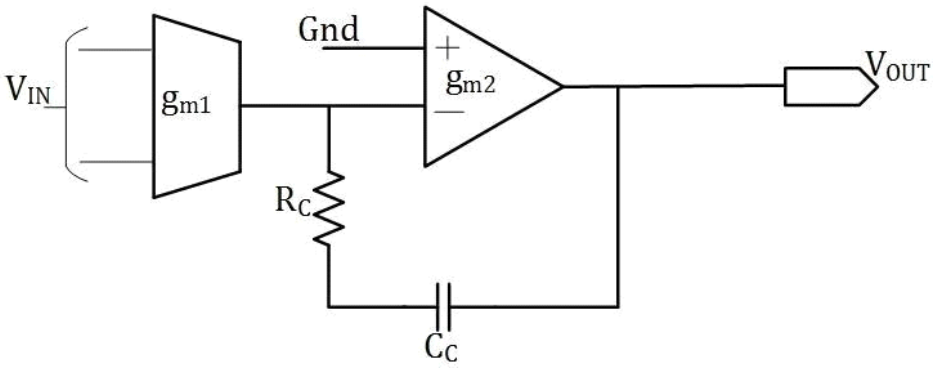

Fig.2.7 Two-stage op-amp block w/ capacitive feedback [27]

From Fig.2.7, the resultant zero location without zero resistance ,

$$f_Z = \frac{g_{m2}}{2\pi C_C} \tag{2.4}$$

The zero location with Rc in feedback is given by ,

$$f_Z = \frac{1}{2\pi C_C\left(\frac{1}{g_{m2}} - R_C\right)} \tag{2.5}$$

CHAPTER 3

METHODOLOGY

3.1 INTRODUCTION

LDO's are important blocks in Industrial as well as Automotive applications. LDO basically consist of error amplifier, pass device, feedback network and voltage reference block. This chapter is organized as follows. The basic idea behind the linear regulators is discussed in section 3.2. The block level description and LDO characteristics are discussed in section 3.3.Specifications of the LDO and Stability of the LDO are described in section 3.5 and 3.5.Selection of the devices for LDO according to applications stated in section 3.6. Different methods of generating voltage references and their limitations discussed in section 3.7.

3.2 LINEAR REGULATOR: BASIC IDEA

Linear regulators concept is derived from the following Fig.3.1 which is simple resistor divider having one controlling resistor Rc.

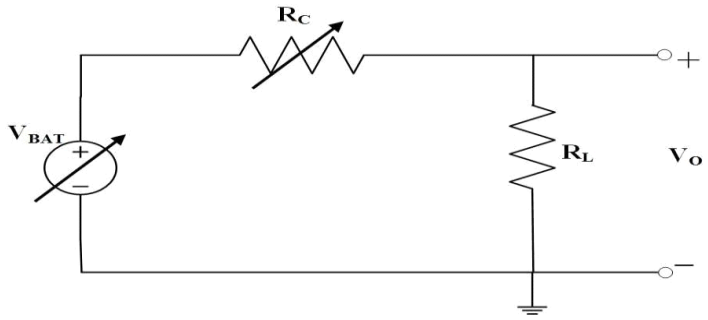

Fig.3.1 Concept of Linear Regulator

VBAT is battery voltage which is function of time which defines VO given by,

$$Vo = Rl/(Rl + Rc)\, Vbat \tag{3.1}$$

In order to maintain const. output voltage ,the value of controlling resistor Rc is given by,

$$Rc = Rl\left(\frac{Vbat}{V0} - 1\right) = Rl\frac{(Vbat - V0)}{V0} = Rl\left(\frac{Vdrop}{V0}\right) \tag{3.2}$$

So, Rc should be properly set such that VO is equal desired regulated output voltage. For the circuit to acts as a voltage regulator Rc should be very small as compared to RL that regulator should be Voltage Controlled Voltage source. The Proper value of RC obtained by taking feedback from the output as shown in following Fig.3.2. Hence, the LDO will provide proper

value of RC which is placed in between input supply and output load with voltage drop VDROP across it to provide stable regulated output voltage. The implementation of the Low drop-out voltage regulator is shown in following Fig.3.2.

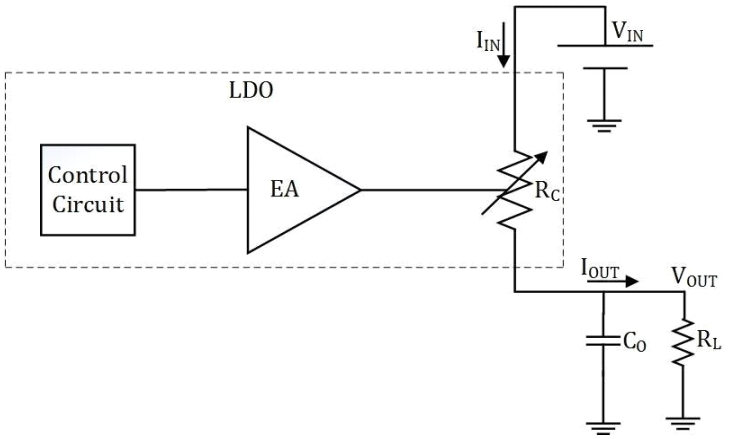

Fig.3.2 Implementation of Low Drop-out Voltage Regulator

3.3 CHARACTERISTICS

3.3.1 Block Level Description

As discussed is chapter 1, LDO's are basically a Linear Drop-out (LDO) voltage regulators but what does the drop-out means?, it means that the device can regulate the output voltage even when the input voltage is very close to output voltage. Fig.3.2 shown the closer look of the LDO operation in relation to the drop-out voltage (V_{DROP}). Fig.3.3 shows the basic block level description of the LDO with the PMOS or NMOS pass device as output stage.

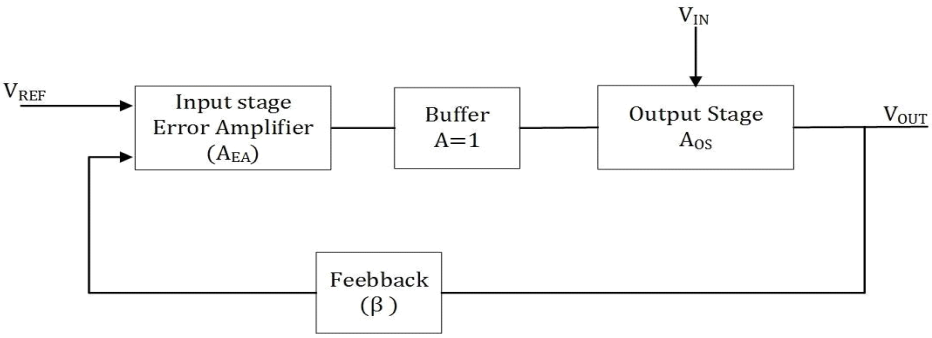

Fig.3.3 Block Level Description of the LDO

Output Voltage VOUT from the Fig.3.3 can be derived as,

$$Vout = \frac{Vref(AeaAos)}{1+\beta(AeaAos)} + \frac{Vin}{\beta(AeaAos)} \approx \frac{Vref}{\beta} + \frac{Vin}{\beta(AeaAos)} \quad (3.3)$$

Where A_{EA} is the gain of the input stage error amplifier, A_{OS} is the gain of the output stage and β is the feedback ratio. As it can be seen from the equation 3.3, if open loop gain ($A_{EA}A_{OS}$) is

much higher, then output voltage V_{OUT} is independent of line variations and output will be function of the reference voltage and feedback network. For PMOS skip device, MOSFET source is connected to V_{IN}. To alter the output voltage, the error amplifier controls the PMOS gate voltage with admire V_{IN}, thereby controlling the MOSFET conduction stage. The LDO needs positive amount of enter to output voltage distinction for law. When the difference between input and output voltage becomes smaller, the MOSFET operation shifts in the direction of the MOSFET ohmic location. In the ohmic location, MOSFET acts as a resistor and mistakes amplifier pull the gate of the MOSFET to floor level. At that factor, the output voltage can not be regulated anymore. LDO drop-out voltage is described as the voltage drop across the regulator wherein the tool can not alter the output voltage. Reference voltage VREF for the LDO is generated from the Bandgap Reference Voltage or Resistive Ladder Voltage reference generator. In the proposed design Resistive Ladder voltage reference generator is used to generate one-of-a-kind voltage tiers.

3.3.2 Drop-out Voltage

Drop-out curves is shown in Fig.3.4 which is function of output current I_L and temperature. Fig.3.5 shows Input-output behavior of LDO. To guarantee regulation,

$$V_{IN} > V_O + V_{DROP}$$

It would be nice to have V_{OUT} to be at a fixed value regardless of the input voltage V_{IN} but most practical LDO's requires some minimum amount of V_{IN} in order to regulate the output voltage V_{OUT} for desired value. Hence, the drop-out voltage (V_{DROP}) is defined as the difference between V_{IN} and V_{OUT} at which V_{OUT} is no longer regulated. This could be in the range of 0.1V to 0.6V range depends upon the application. Clearly, the exact value of drop-out voltage (V_{DROP}) depends upon the kind of pass device used and how much load current is passing. Ideally it should be as low as possible.

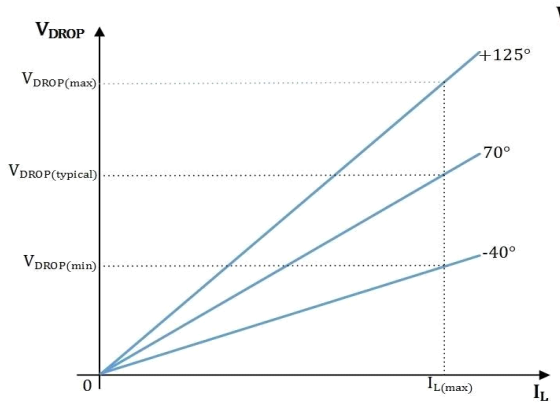

Fig.3.4 Drop-out curve function of temperature

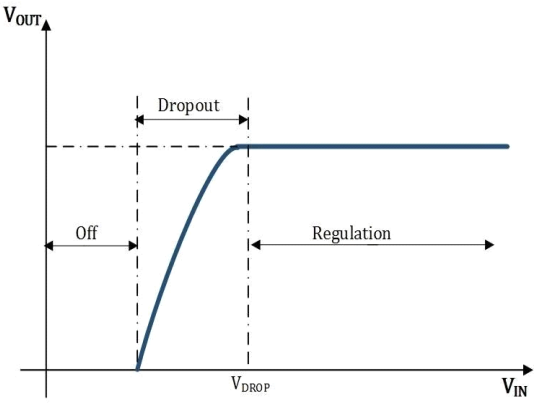

Fig.3.5 Input-output behavior of LDO

3.3.3 Quiescent Current

As LDO consists of error amplifier, reference generator and feedback network which needs some biasing current for their operation. So, this quiescent current (I_Q) is bias current consumed in all these building blocks. Here as the MOSFET is pass the pass device, the gate current is ideally zero therefore the quiescent current (IQ) is independent of the load current (I_L) or output current (I_{OUT}). If BJT is used as a pass device then base current is function of load current, so the quiescent current (I_Q) varies with the load current (I_L). The current efficiency (η) is given by the following equations,

$$\eta 1 = \frac{Iout}{Iin} \times 100$$

$$\eta 2 = \frac{Iout}{Iout + Iq} \times 100$$

To analyze the LDO output voltage and its specifications, LDO is represented in its signal flow graph. Using Mason's gain formula, output of LDO due to input voltage and reference voltage is derived. Following Fig.3.6 shows the signal flow representation of the LDO to analyze the LDO specifications.

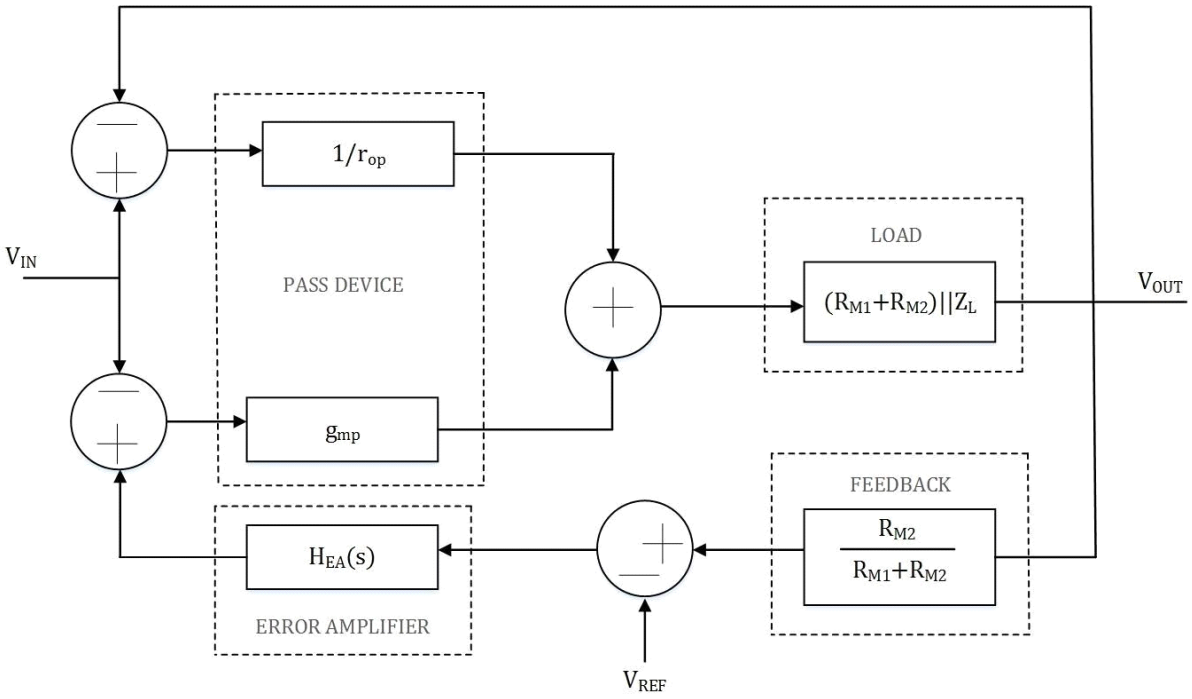

Fig.3.6 Signal flow representation of LDO

3.3.4 Output voltage

Output voltage from Fig.3.6 is function of V_{REF} and V_{IN} and it is calculated in following section and equations .

a. Due to V_{REF}:

At DC,

$$Z_L = R_L \ , \ H_{EA}(s) = A_{OEA}, \ (R_{M1}||R_{M2})||R_L = R_O \ , \ \beta = \frac{R_{M2}}{R_{M1} + R_{M2}}$$

$$\frac{V_{OUT}}{V_{REF}} = \frac{A_{OEA} g_{mp} R_O}{1 + A_{OEA} g_{mp} R_O \beta + R_O / r_{op}}$$

$$\frac{V_{OUT}}{V_{REF}} = \frac{A_{OEA} g_{mp} r_{op}}{1 + A_{OEA} g_{mp} r_{op} \beta + r_{Op} / R_O}$$

$$\frac{V_{OUT}}{V_{REF}} \approx \frac{1}{\beta} \ if \ A_{OEA} g_{mp} r_{op} \beta \gg 1$$

b. Due to Vin :

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{mp} R_O + {}^{1}/_{r_{op}} R_O}{1 + A_{OEA} g_{mp} R_O \beta \, {}^{R_O}/_{r_{op}}}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + g_{mp} r_{op}}{1 + A_{OEA} g_{mp} r_{op} \beta + {}^{r_{op}}/_{R_O}}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{A_{OEA} \beta} \ \ if \ g_{mp} r_{op} \gg 1$$

So, overall LDO output voltage is given by considering equations 3.6 and 3.7,

$$\Delta Vout = \frac{\Delta Vin}{\beta Aoea} + \frac{\Delta Vref}{\beta}$$

(3.8)

Where A_{OEA} is DC gain of error amplifier, gmp is the transconductance of pass device, r_{op} is

output resistance of pass device and β is feedback network.

3.4 SPECIFICATIONS OF LDO

LDO specifications are defined in the different operating modes of LDO given as,

a. *Static state or Steady state Specifications*:

When output is at its steady state value by that time what the fluctuation is or significant deviation occurs at output due to change in input supply voltage or load current.

1. Line Regulation
2. Load Regulation
3. Temperature Coefficient

b. *Dynamic state Specifications:*

This will occurs at transient moment. When a current state as given from zero to maximum value by that time what is the change occurs during transient period.

1. Load Transient
2. Line Transient

c. *High Frequency Specifications:*

When LDO is operating at its higher frequency this specifications are defined,

1. Power Supply Rejection Ratio (PSRR)
2. Regulator Output Noise

Some of the important specifications from above are explained in detail as follows,

3.4.1 Line Regulation

It is the ability of LDO which specifies how much change is observed in the output voltage when there is change in LDO input voltage and it is given by,

$$L_R = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{\beta A_{OEA}} \tag{3.9}$$

To have excellent Line Regulation, error amplifier has to be built with very high DC gain that is A_{OEA} should be very high. Therefore, LDO can easily suppress changes in input voltage. Line regulation can also be considered as PSRR at DC or one particular frequency.

3.4.2 Load Regulation

It is the ability of the LDO which specifies any changes in the output voltage due to change in load current. Following Fig.3.7 is used to define the Load regulation,

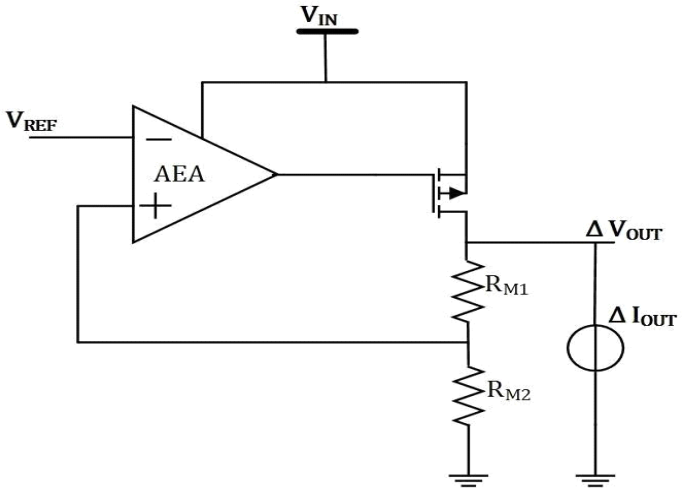

Fig.3.7 Setup for Load Regulation

Load regulation is given by the ratio of changes in the output voltage (V_{OUT}) with respect to changes in the load current (I_L).

Hence, for the LDO voltage regulator, output impedance is minimized by loop gain. To have better load regulation, the output impedance should be as low as possible but lower output impedance may increase leakage current, so there is tradeoff between these specifications.

3.4.3 Temperature Coefficient

Output voltage (V_{OUT}) of the LDO is function of temperature dependence reference voltage. So, maximum 5% variation is allowed for the reference voltage while designing reference voltage block for all the PVT variations. Temperature dependence is given by,

$$Tc = \frac{1}{Vout}\frac{\partial Vout}{\partial TEMP} \tag{3.12}$$

3.4.4 Load Transient

For the LDO, if load current (I_L) steps out by a large value, it takes time for the gate voltage of the pass transistor to change because it has a very high capacitance and it has to be charge so

that it can change transconductance. Furthermore, error amplifier response is limited by quiescent current (I_Q) .It means that the moment I_L stepped out to a high value, output resistance doesn't change immediately as the feedback will take time. LDO transient response is shown in Fig.3.8.

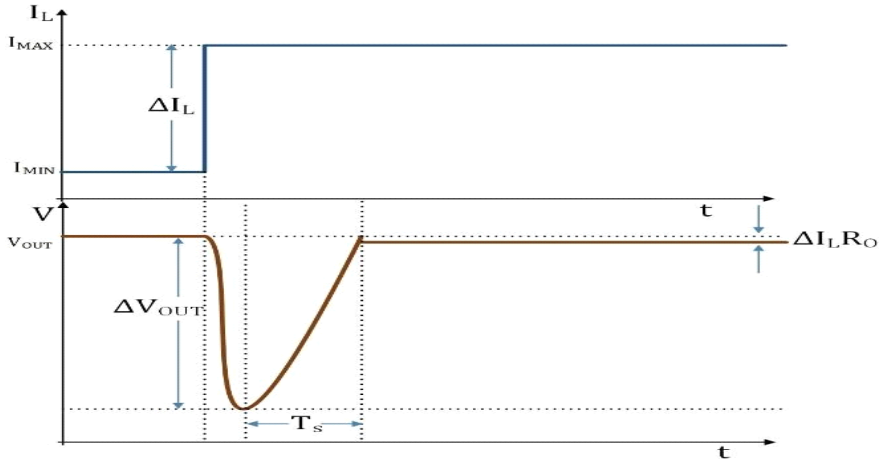

Fig.3.8 Load Transient response of the LDO

If the load current (I_L) steps to high value, then output of the LDO have large capacitor (C_o) so in steady state output capacitor (C_O) will charge to output voltage (V_{OUT}) and when current step occurs, then current will be drawn from capacitor C_O and it maintains minimum voltage droop ΔV_{OUT}. Voltage droop ΔV_{OUT} is given by,

$$\Delta Vout = \frac{Il}{Co}\left(\frac{1}{BW} + Tsr\right) \tag{3.12}$$

Where ΔVOUT is the transient droop voltage, BW is open loop bandwidth of the LDO, tsr time due to slew rate limitation of the LDO. Further tsr can be derived as,

$$Tsr = Cgate\frac{\Delta Vg}{Ib} \tag{3.13}$$

Where Cgate is the gate capacitance of the pass device, Δvg is the change in gate voltage of the pass device, I_b is the bias current of the second stage. Bandwidth of the LDO will decide the settling time for the LDO which is nothing but time required for the LDO to reach regulated value after the transient. Thus summary is voltage droop can be minimized by either increasing the output capacitor or increase the bandwidth of the LDO.

3.4.5 Power Supply Rejection Ratio (PSRR)

PSRR is the small signal high frequency parameter of the LDO which is nothing but the capability of rejection of power supply noise at all frequency and it is given by,

$$PSRRin\ db = 20log\frac{Vout, ripple}{Vi, ripple}$$

PSRR and Line regulation is considered as same but for line regulation defined at only one particular frequency whereas for PSRR whole spectrum is considered [7]. PSRR can be increased by increasing the loop gain as it will increase the amplitude at lower frequencies which gives very high ripple rejection at lower frequency. In case of MIPI application, the power supply is coming from the battery which gives very clean supply. If the supply is coming from the battery, PSRR for the LDO is required maintain at high value for lower frequencies only.

There are many paths from input supply to output voltage of the LDO are given by,

1. Error Amplifier
2. Reference Voltage Circuit
3. Pass transistor

Following Fig.3.9 shows signal flow representation of the LDO for PSRR calculation,

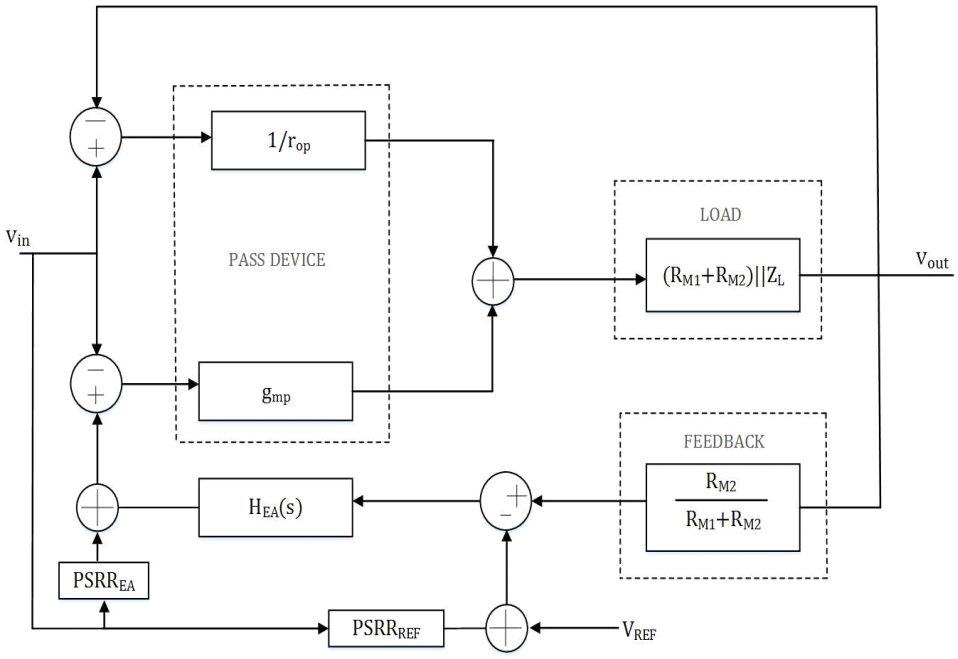

Fig.3.9 Signal flow representation of LDO for PSRR

3.5 STABILITY OF THE LOW DROP-OUT VOLTAGE REGULATOR

LDO is using feedback technique to maintain constant output voltage and consists of multiple loops, stability becomes an important factor for the LDO.LDO loop gain defines the stability of the LDO that means phase margin should be a positive number. In practical, Phase Margin of 50° is considered as good number for stability as it gives very less damping. LDO consists of multiple poles defined as output of LDO and poles given by error amplifier and also some parasitic poles. As a result, the main focus is to find out the dominant and non-dominant poles

to make them widely apart in order to achieve better phase margin [3]. To achieve the LDO stability, LDO requires some frequency compensation techniques which are as follows,

1. Pole Zero Cancellation
2. Pole Splitting

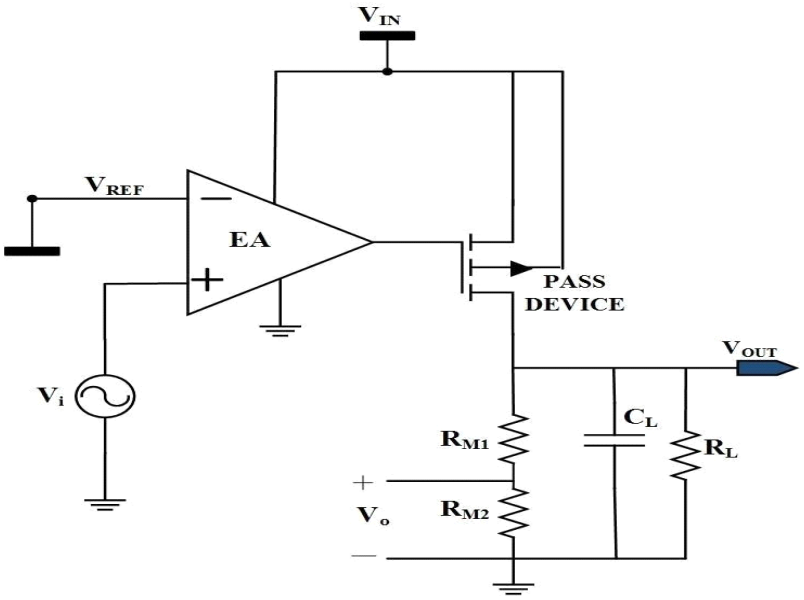

Fig.3.10 LDO model for loop gain calculation

For On-chip LDO, the output pole is not a dominant pole because there is limitation on output capacitor value. So, on chip LDO uses Miller Compensation technique to achieve the stability. Following Fig.3.10 shows model to calculate loop gain,

Loop gain GH(s) from the above figure is defined as,

$$GH(s) = \frac{V_o}{V_i} = A_{OEA}(s) g_{mp} \left(r_{op} || R_{M1} + R_{M2} || R_L\right) \beta \tag{3.15}$$

DC loop gain, $GH(0) = A_{OEA} g_{mp} r_{op}$ (3.16)

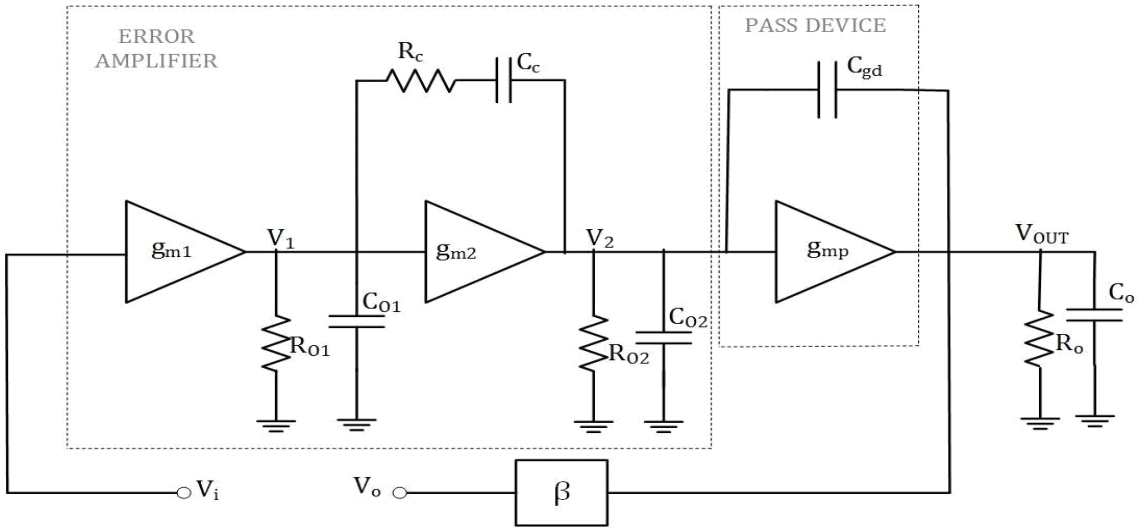

Fig.3.11 Small signal model for LDO

Transfer function for the above small signal model is calculated by applying KVL and KCL at nodes V_1, V_2 and V_{OUT}, is given by,

$$\frac{V_i}{V_o} = \frac{-g_{m1}R_{o1}g_{m2}R_{o2}\beta g_{mp}R_o\left(1+s\left(R_C-{}^1/_{g_{m2}}\right)C_C\right)\left(1-s\left({}^{C_{gd}}/_{g_{mp}}\right)\right)}{\left(1+sR_{O1}(C_{O1}+g_{m2}R_{O2}C_C)\right)\left(1+sR_{O2}\left(C_{O2}+g_{mp}R_OC_{gd}\right)\right)(1+sR_oC_O)}$$

(3.17)

The transfer function of the LDO in equation 3.20 shows there are three main poles and two zeros. The dominant pole p1 is observed at the output of the error amplifier, second dominant pole p2 is slightly less than error amplifier output pole is given by first stage of error amplifier. For the On-chip LDO, output capacitor (CO) value is very less and LDO output resistance (R_O) is also less so the third pole p3 is far away from other two poles.

The Poles and zeros locations from the transfer function is given by,

$$p_1 = \frac{1}{R_{01}(C_{O1}+g_{m2}R_{O2}C_C)} \quad , \quad p_2 = \frac{1}{R_{O2}(C_{O2}+g_{mp}R_OC_{gd})} \quad , \quad p_3 = \frac{1}{R_OC_O}$$

$$z_1 = \frac{1}{\left(R_C-{}^1/_{g_{m2}}\right)C_C} \quad , \quad z_2 = \frac{g_{mp}}{C_{gd}}$$

There are two zeros in the transfer function equation because of presence of the Miller capacitance between input and output. The stability of the LDO is explained with the help of Fig.3.12 and Fig.3.13 with compensation network and without compensation respectively.

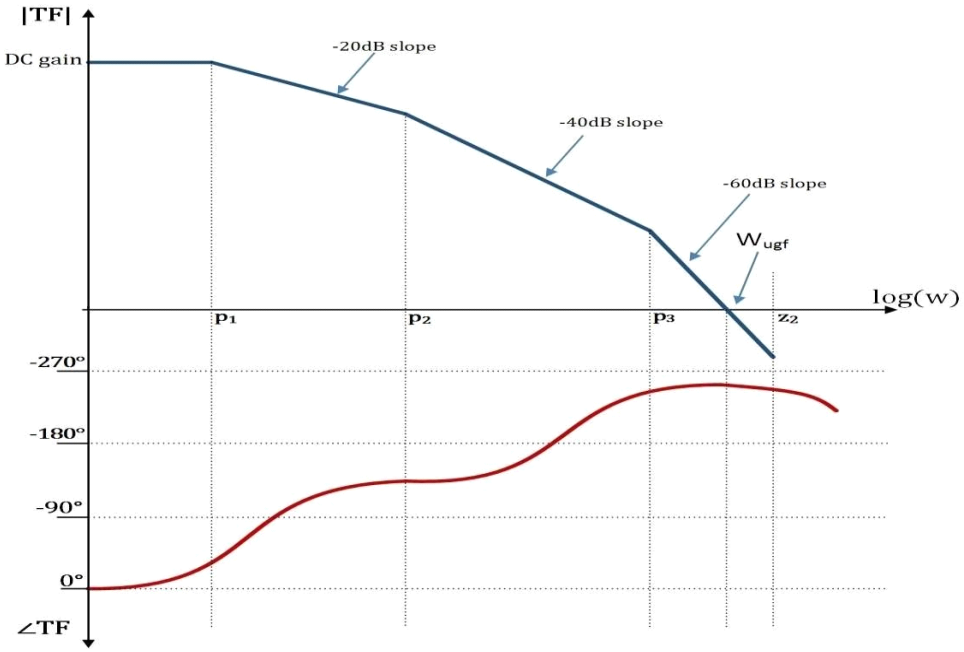

Fig.3.12 Frequency response of LDO without frequency compensation

Fig.3.12 shows the bode plot for LDO without any frequency compensation, as seen in Fig.3.12 three poles coming under the UGB which causes LDO to be unstable. Phase margin for the above bode plot is negative as ∠TF across the UGB is around -250° because the Phase margin for any open loop system is given by,

$$\text{Phase Margin} = 180 + \angle TF \tag{3.21}$$

Fig.3.13 shows the bode plot for LDO with frequency compensation with the help of Miller compensation technique. With the help of miller capacitance for the second stage of the amplifier, the pole p1 is made dominant which is at the output of the first stage. Furthermore, Miller compensation causes second pole p2 to move higher frequencybecause of pole splitting as gm2 is dominating than Ro2. By placing resistor in series with miller capacitor (CC), extra zero will be added. Location of the zero is decided by the resistance Rc, if Rc is made exactly equal to $1/g_{m2}$ then p_2 will move to infinity. If R_c is made larger than $1/g_{m2}$, then p_2 will move to left hand side which helps to improve stability as shown in bode plot Fig.3.13. Furthermore, if R_c is made less than $1/g_{m2}$, then right hand zero will be created which will degrade the stability.

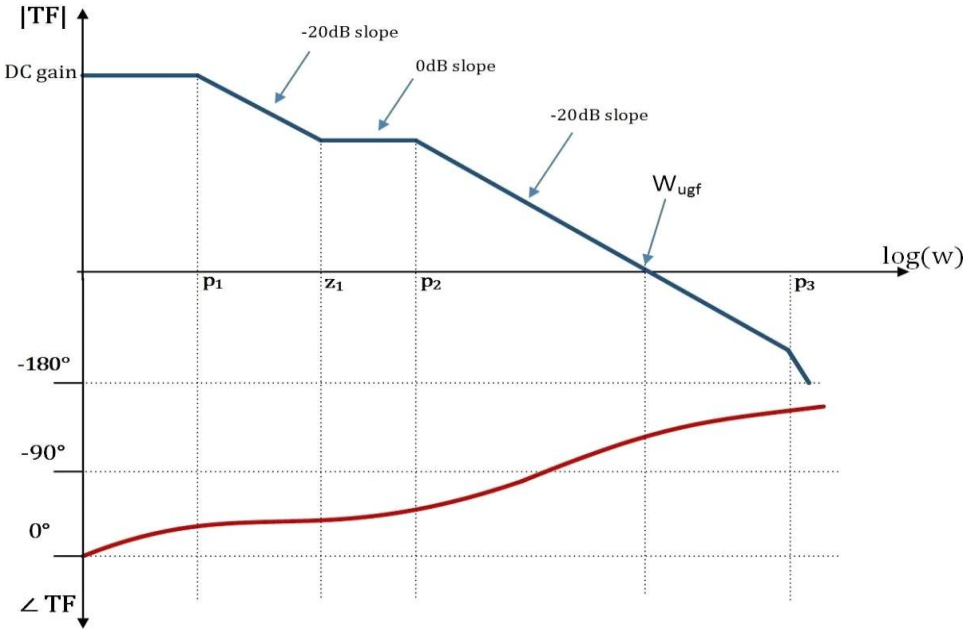

Fig.3.13 Frequency Response of LDO with Miller compensation

Bandwidth of the LDO will decide the settling time for the LDO as settling time is inversely proportional to bandwidth for any system. Settling time is one of the important specification for any linear regulator as it will define how quick the regulator will response to the transients which is discussed in section 3.3.4.

3.6 SELECTION OF DEVICES FOR LDO APPLICATION

3.6.4 N Channel or P Channel input stage

1. DC advantage is essentially unaffected with the aid of the selection seeing that both the designs have one or greater n-channel riding transistors and one level with one or greater p-channel riding transistors [9].

2. For a given bias current having p-channel input pair stage maximizes the slew rate. Slew rate improvement can be one of the most important consideration while designing an amplifier.

3. Having p-channel enter first stage implies that the second degree has n channel riding transistor. This association maximizes the Trans conductance of the pressure transistor of 2nd degree, which is important while excessive frequency operation is important.

4. P channel Tr has less 1/f noise than N channel Tr.

3.6.2 NMOS vs. PMOS Pass Transistor

1. NMOS pass FET LDO calls for the VDD rail to be higher than supply enter, whilst a PMOS does not. To try this, a charge pump is typically required with accompanying dangers of higher quiescent modern and additional price pump noise [7].

2. Power Supply Rejection (PSR) is better with PMOS.

CHAPTER 4

PROPOSED DESIGN OF THE LDO

4.1 INTRODUCTION

This chapter proposes On-chip CMOS Low Drop-out Voltage regulator with improved transient performance and wider bandwidth PSRR for MIPI driver. Most of the power is consumed by driver part of transmitter, so it's necessary to minimize power consumption due to drivers. Proposed LDO will provide supply voltage of 0.4V for transmitter driver. This chapter is organized as follows. Section 4.2 explains top level representation of proposed circuit. In section 4.3, design specifications for proposed LDO is specified. Design flow for proposed LDO is discussed in section 4.4.Section 4.5, section 4.6 and section 4.7 discusses the design of error amplifier, pass device and feedback network respectively.

4.2 TOP LEVEL REPRESENTATION OF PROPOSED CIRCUIT

The proposed on-chip Low Drop-out (LDO) voltage regulator is designed to improve transient performance which will minimize the transient voltage droop and provide high power supply rejection over wide bandwidth. In the conventional on-chip LDO topology, voltage droop is minimized by increasing the slew rate of the LDO without considering the power dissipation since the slew rate improvement is done by increasing the bias current of second stage of error amplifier. In the proposed circuit transient & PSRR performance is improved by focusing on bandwidth. Fig.4.1 shows the top level representation of proposed circuit .

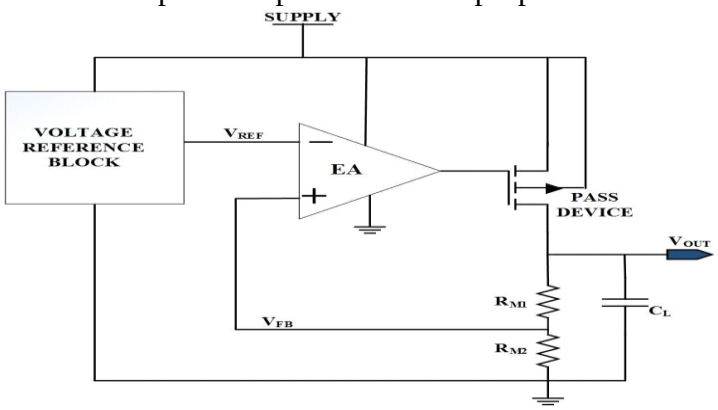

Fig.4.1 Top level representation of proposed circuit

The circuit diagram of proposed CMOS On-chip Low drop-out voltage regulator with improved transient and PSRR performance is shown in the Fig.4.2 .The transistors Q1 - Q8 are used to form the Error amplifier. The transistors Q1 and Q2 forms the 1st stage of error amplifier which is PMOS input differential pair. The transistors Q6 and Q7 gives 2nd stage gain for error amplifier which is NMOS common source amplifier. The output of error amplifier V_{EA} is connected to gate of the pass device. Bias current of 2nd stage and input gate capacitance of the pass device will determine the slew rate of the LDO. Q_P is the pass transistor, resistors R_{m1} and R_{m2} used to form the feedback network which will provide feedback voltage to the error amplifier.

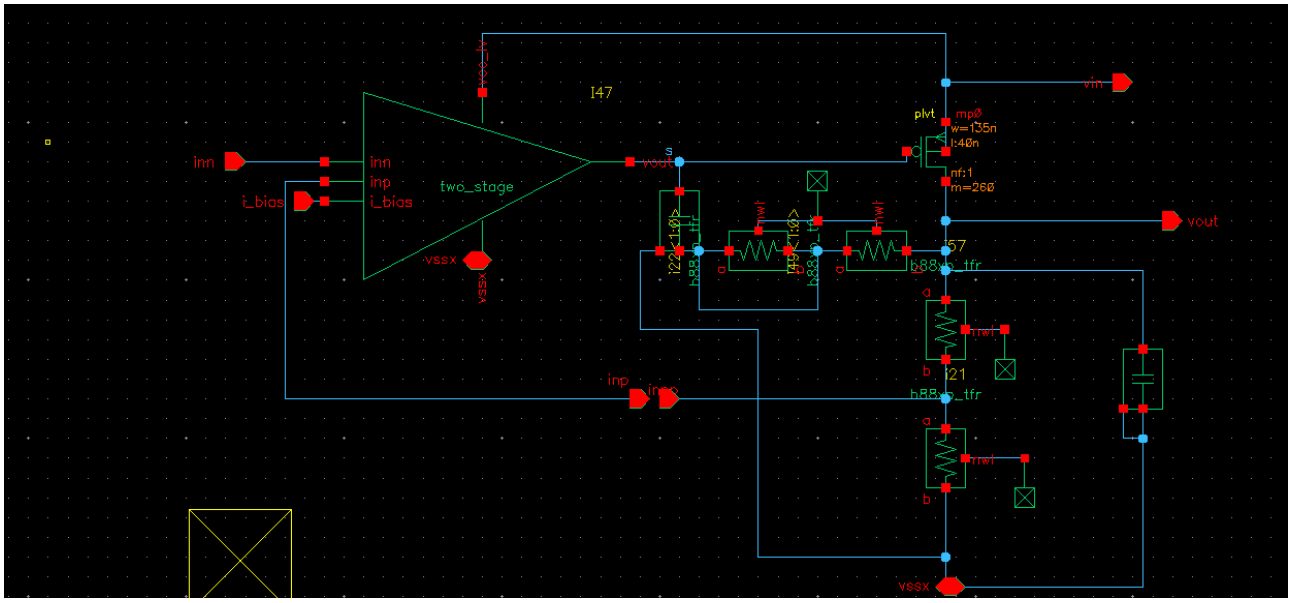

Fig: Schematic of the block diagram of proposed LDO

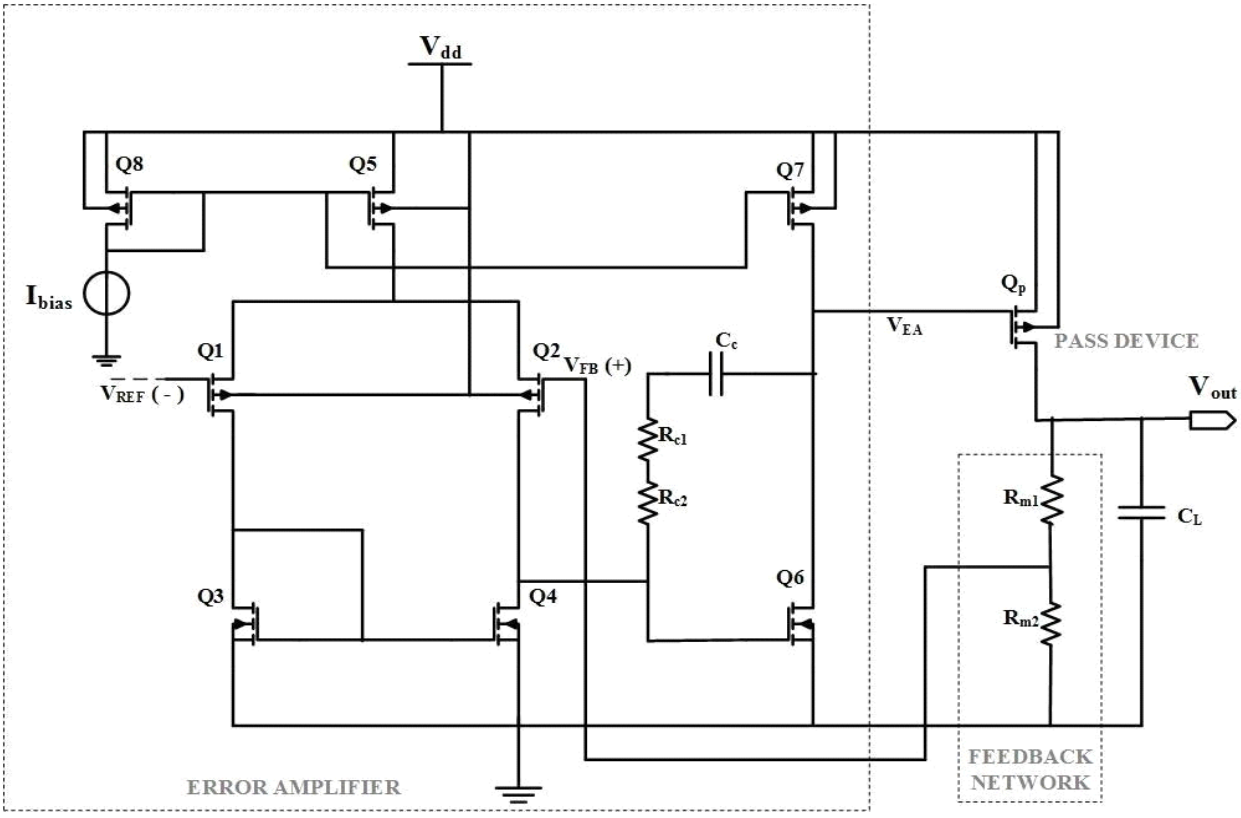

Fig.4.2 Circuit diagram of proposed on-chip LDO regulator

The RC compensation network, which is formed by R_{C1}, R_{C2} and metal finger capacitor C_C to provide LDO stability. R_{C1}, R_{C2} and C_C are the metal resistors and metal figure capacitor respectively having some fixed value which will be varying according to temperature, process.

4.3 DESIGN SPECIFICATIONS FOR PROPOSED LDO

LDO specifications are derived from the application to which LDO is driving. The proposed LDO is driving MIPI driver, so LDO specifications are derived from MIPI driver. Table 4.1 shows the design specification for proposed LDO.

Table 4.1 Specifications for Proposed LDO

Circuit Parameters	Specifications
Process	AMS CMOS 10nm
Power Supply	1V
Output Voltage	0.4V to 0.6V
Load Current	2mA to 10mA
Input voltage range	0.1V to 0.6V
Gain	> 40dB
Phase Margin	>50°
Unity gain Bandwidth	1GHz
Power Supply Rejection Ratio	-35dB at 1MHz
Power Dissipation at Low Load	1mw
Settling time Ts	100ns

4.4 DESIGN FLOW FOR THE LOW DROPOUT VOLTAGE REGULATOR

LDO voltage regulator is designed according to application which is going to be driven by LDO. Proposed designed LDO is used to drive the MIPI transmitter driver. In the proposed On-chip LDO design, output load capacitor value is given by capacitance seen from supply end for display driver which is typically around 600fF.For MIPI case in display transmitter, 0.4V is the supply required for driver therefore the output of LDO has given to transmitter driver. Following flow chart in Fig.4.3 specifies about design flow of LDO,

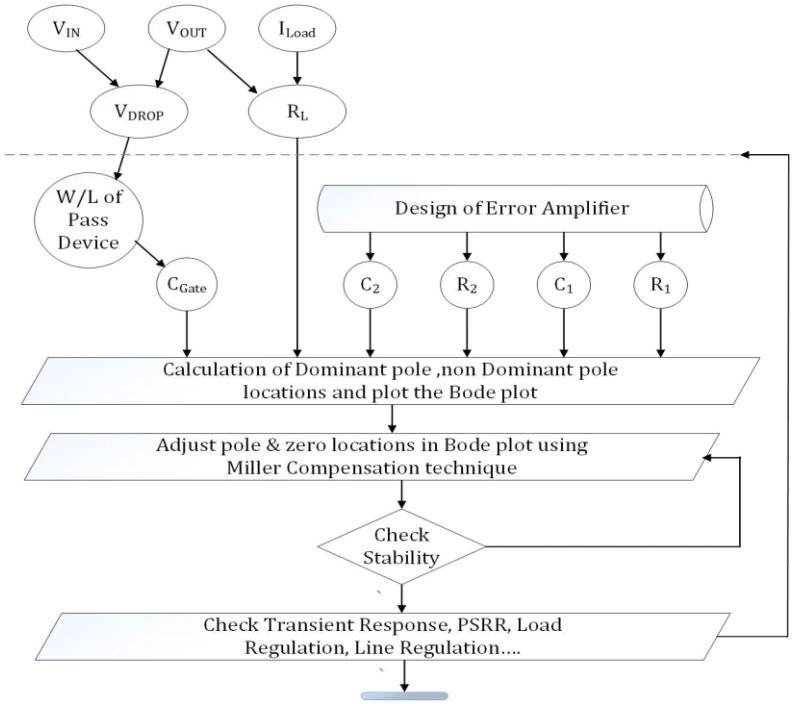

Fig.4.3 Design flow for Proposed LDO

4.5 DESIGN OF ERROR AMPLIFIER

Different topologies are used to implement error amplifier depending upon the application. For high PSRR of error amplifier PMOS input differential pair with NMOS 2nd stage is preferred. The output of the error amplifier has given to the gate of the pass device which will control the current flow at the output. Proposed LDO has worst case gain of 40dBthat is composed of the gain given by error amplifier and pass device. Hence, the error amplifier has to give the gain of 30dB in worst case corner. Design specifications for error amplifier in AMS 10nm CMOS technology are listed below in table 4.2.

Table 4.2 Specifications for error amplifier

Circuit Parameters	Specifications
DC Gain	40dB
Unity Gain Bandwidth	1GHz
Phase Margin	50°
Bias Current	30µA
Load Capacitor	100fF
Input Common mode Range	0.1V to 0.5V (400mV Range)

An opamp topology for two stage error amplifier is shown in Fig.4.4.The circuit consists of PMOS input differential pair driven by NMOS common source amplifier.

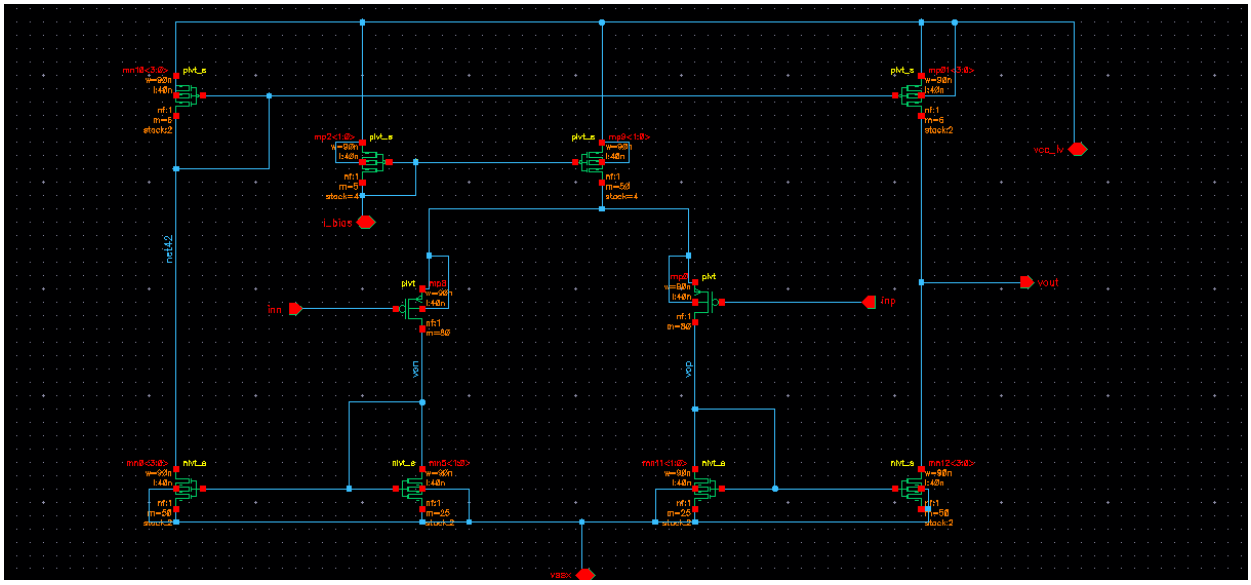

Fig: Schematic Design of Error Ampllifier

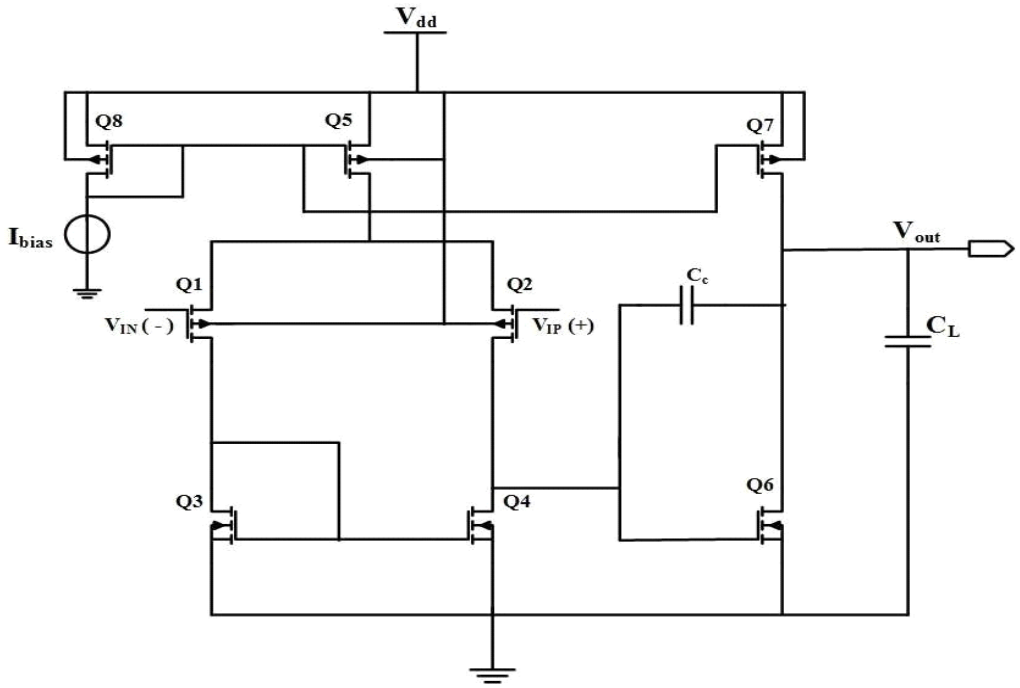

Fig.4.4 Circuit diagram for two stage Error Amplifier

As seen from the Fig.4.4, the two stage opamp composed of the first gain stage differential input single ended output, second gain stage is normally a common source gain stage that has an active load. The capacitor CC is used to provide the stability using Miller compensation technique when opamp is used in feedback. The sizing of the transistors are derived from the given specifications in table 4.2.

4.5.1 Design of Transistors Q1 & Q2:

The two stage opamp is designed for UGB of 1 GHz .Furthermore, the UGB will specify the transconductance of transistor Q1 & Q2 that is given by,

$$UGB(in\ radians) = \frac{Gm1,2}{Cc} \tag{4.1}$$

From the transcoductance gm12, the W/L ratio for Q1 and Q2 is given by,

$$\frac{Gm1,2}{2uCoxId1,2} = \left(\frac{w}{l}\right)1,2 \tag{4.2}$$

4.5.2 Design of Transistors Q3 & Q5:

Input common mode range for proposed two stage error amplifier is given by,

$$V_{ds3} - |V_{thp}| < V_{icm} < V_{dd} - V_{sd5} - V_{sg1} \tag{4.3}$$

From the lower limit of common mode range, the sizing of Q3 is derived, that is given by,

$$V_{icm} > V_{gs3} - |V_{thp}| \tag{4.4}$$

Where Vgs3 is gate to source voltage of transistor Q3 and it is given by,

$$V_{gs3} = \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}(W/L)_3}} + V_{thn} \tag{4.5}$$

From the upper limit of common mode range, the sizing of Q5 is derived that is given by,

$$V_{icm} < V_{dd} - V_{sd5} - V_{sg} \tag{4.6}$$

Here Vsd5 is saturation voltage across the transistor Q5.Upper limit of common mode range is increased by maintaining minimum saturation voltage across transistor Q5 that is Vsd5 approximately close to 100mV.From Vsd5 ,the sizing for transistor Q5 is given by,

$$(W/L)_{5,6} = \frac{2I_{D5}}{\mu_p C_{ox} {V_{sd5}}^2} \tag{4.7}$$

4.5.3 Design of Transistors Q6 & Q7:

Transistor Q7 is providing biasing current for second stage, therefore transistor Q7 will mirror the current from transistor Q5 with mirror ratio unity. Hence, sizing of transistor Q7 will be same as transistor Q5.While designing an opamp it is necessary to maintain no input offset voltage, the condition for no input offset voltage is given by

$$\frac{(W/L)_5}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5} \tag{4.8}$$

4.6 DESIGN OF PASS DEVICE

The proposed Low drop-out (LDO) voltage regulator has to support output load current (IL) up to 10mA.Therefore, the bigger size pass device is required to support required output load current. In the 10nm CMOS process technology, the RV limit for the one device is up to 30uA.Furthermore, the sizing of pass device is derived from VDROP and IL.

$$\left(\frac{w}{l}\right) Qp = \frac{Maximum\ Load\ current}{Maximum\ Current\ supported\ by\ one\ device} \tag{4.9}$$

4.7 FEEDBACK NETWORK

Once the error amplifier has designed, the input common mode range for the proposed amplifier is found to be 0.1V to 0.35V by simulation. Feedback ratio is decided to be 0.5 for VREF of 0.2V and 0.3V for regulated output of 0.4V and 0.6v respectively. Resistance Rm1 and Rm2 values should be as low as possible to maintain minimum output impedance considering leakage power into the account.

Once the sizing of the all transistors are fixed, LDO need to be analyzed for stability test. Stability of the LDO normally depends upon the locations of poles and zeros. The proposed LDO will give three main poles as discussed in chapter 2. According to locations of poles, stability analysis is performed by adjusting values of compensation capacitor or by adding extra zeros to cancel the extra poles. For phase margin of 50°, miller compensation capacitor value is 300fF and one zero is added by adding 6KΩ resistance templates to cancel extra pole.

4.8 VOLTAGE REFERENCE GENERATOR DESIGN

LDO requires reference voltage to generate the regulated output voltage. There are basically two methods of generating reference voltage.

a. Bandgap Reference voltage circuit
b. Voltage reference generator using resistive ladder

In the proposed design reference, voltage is generated using the resistive ladder. Standard bandgap reference circuit will give reference voltage of 1.2V with the help of CTAT (Complementary to absolute temperature) and PTAT (Proportional to absolute temperature) blocks. Bipolar junction transistors (BJT) are required to design these blocks. In present 10nm AMS library, it is easy to fabricate resistance than larger size BJT's. Fig.4.5 shows the top level block diagram of proposed voltage reference circuit design.

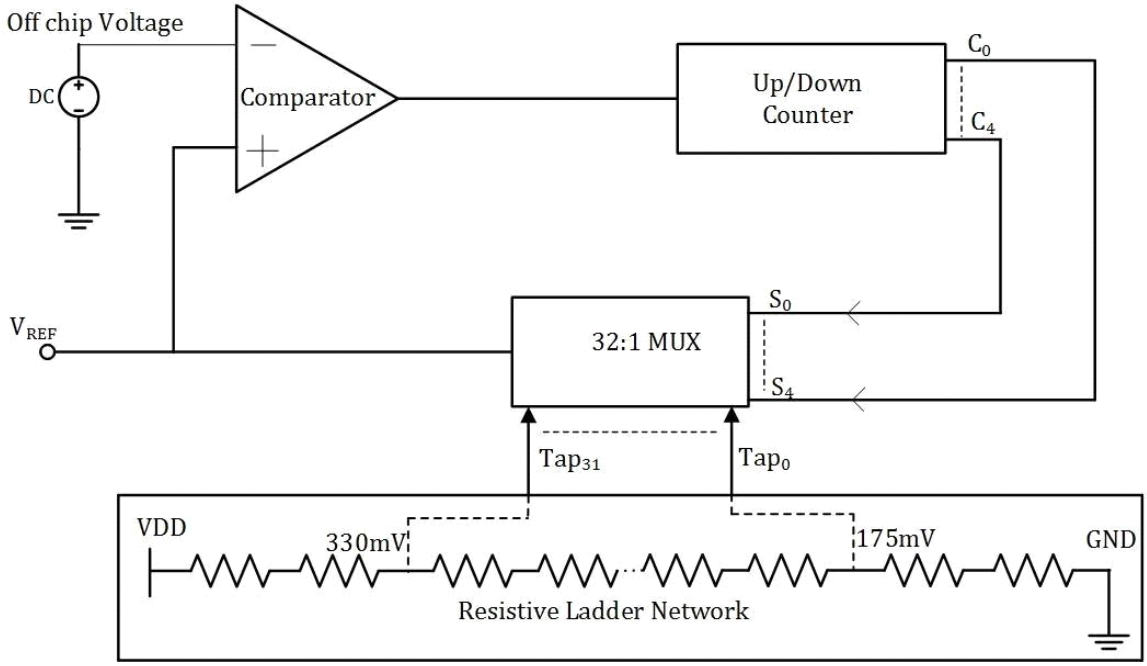

Fig.4.5 Top level view of Voltage Reference block

In the Fig.4.5, the resistive ladder network is created with the help of metal resistor available in the library. The 32 taps have selected from 175mV to 330mV with 5mV of difference between them. To get 5mV of difference for 50µA of ladder current, the resistance value required will be 100Ω.Hence, 32 templates of 100Ω resistors are used to form the ladder. These 32 taps are given to the input of 32:1 mux and can be selected by 5 select lines which are controlled by UP/DOWN counter. The static comparator will compare the output of mux with off chip external voltage and generate an enable signal which decides the counting operation. Once the code is locked, the comparator will not come into picture and final output of the mux will be the reference voltage to the input of error amplifier in LDO.

CHAPTER 5

RESULT ANALYSIS

5.1 INTRODUCTION

The proposed On-ship CMOS Low Drop-out voltage regulator has designed in Cadence Virtuoso Schematic. The results for the proposed LDO is obtained with the help of cadence Spectre simulator. This chapter is organized as follows. Section 5.2 discusses the results for the stability analysis, transient performance and PSRR for the proposed design. In the section 5.3, summary of the results for 0.4V and 0.6V regulated output voltage for all the PVT skews and corners is discussed.

5.2 SIMULATION RESULTS OF THE PROPOSED CMOS LDO

The Low Drop-out Voltage regulator as shown in Fig.4.2 has been simulated using Cadence Spectre simulator for CMOS 10nm AMS technology. The Dimensions for the transistors and devices are given in following tables,

Table 5.1 Dimensions of the transistors for proposed LDO

Transistor	**Size** (W/L)	**Bias Current**
Q1,Q2	14	15µA
Q3 Q4	14	15µA
Q5,Q8	20	30µA
Q6	28	30µA
Q7	20	30µA
QP	1230	10mA

Table 5.2 Dimensions of the other devices for proposed LDO

Devices	**Size**
R_{m1} , R_{m2}	375Ω
C_O	> 600fF
R_{C1} , R_{C2}	3KΩ
C_C	400fF

5.2.1 Frequency Response of the LDO:

Fig.5.1 shows the gain vs frequency and phase vs frequency plots for the proposed uncompensated LDO regulator. In the Fig.5.1, it is observe that phase margin for the uncompensated LDO is very poor. For the stable LDO regulator Phase margin should be minimum 50°.To achieve this 50° phase margin, LDO needs to be compensated.

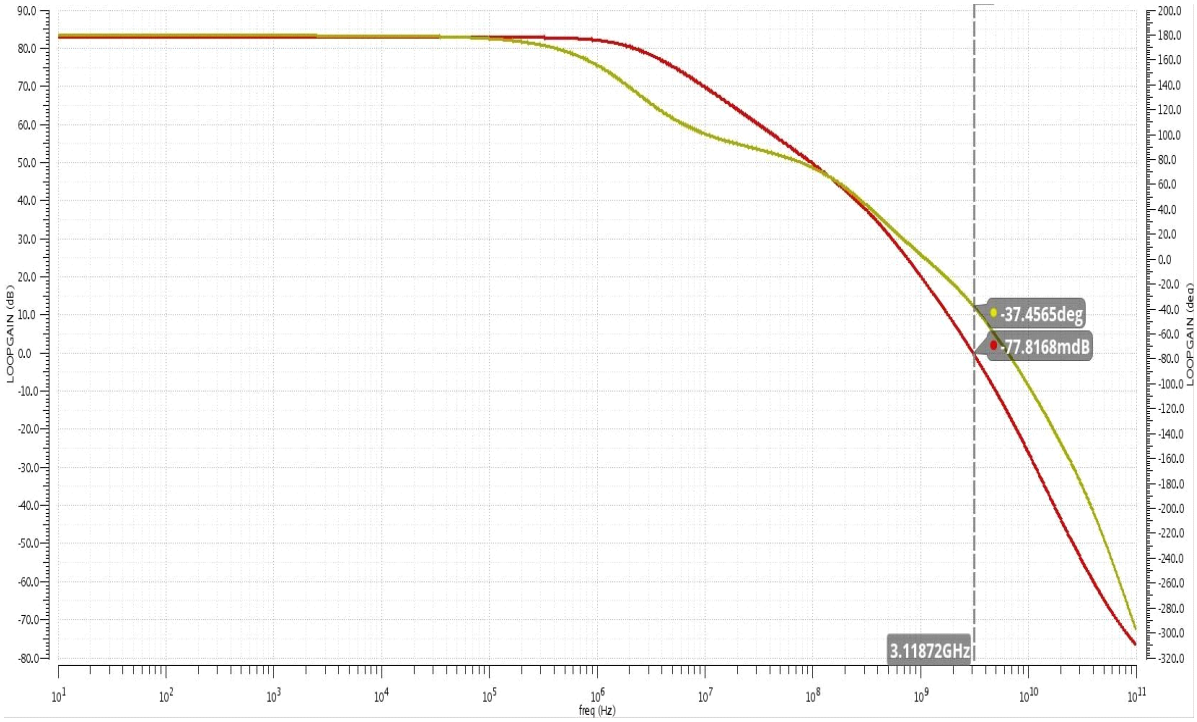

Fig.5.1 Frequency response of proposed LDO without compensation

From the Fig.5.1, Phase margin for uncompensated LDO is -37.45°, which is very poor. LDO simulation has performed for all the PVT skews and corner. Fig.5.2 and Fig.5.3 shows the frequency compensated proposed LDO for fast corner and slow corner respectively.

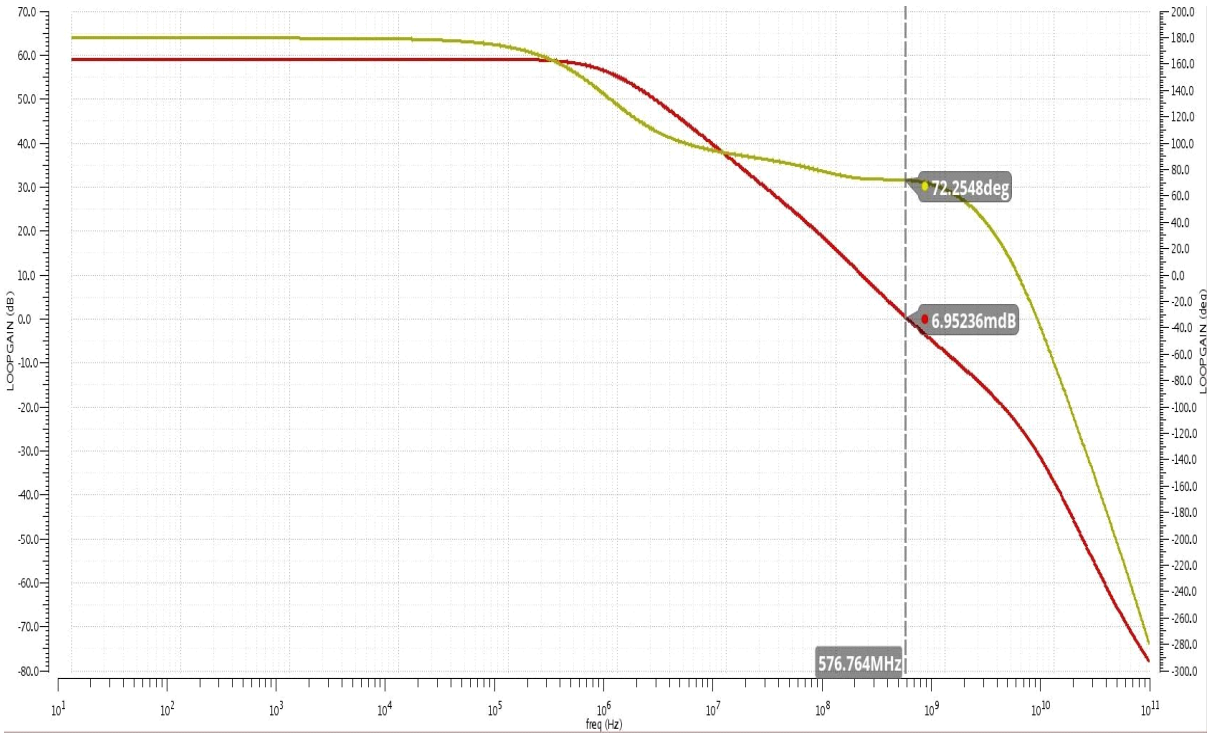

Fig.5.2 Frequency response of proposed LDO with compensation for FAST corner

As seen in Fig.5.1, frequency response has plotted for fast corner by keeping supply voltage level to 1.1V, temperature set to 125° and process is fast. Generally, in the fast corner, gain of the LDO dropped as compared to that of slow corner as shown in Fig.5.2 because resistance offered by devices in the fast corner is very less as compared to devices in slow corners. Furthermore, the bandwidth also decreased for fast corner as compared to slow corner frequency response as shown in Fig.5.1 & Fig.5.2. The LDO is designed for typical 1 GHz bandwidth but the variation observed because of different PVT variation conditions. Both Fig. and Fig.5.3 plotted for load current of 10mA that is full load condition for the LDO. Fig.5.3 shows the frequency response of LDO for slow corner by keeping supply voltage level to 0.9V, temperature to -40°and process is slow.

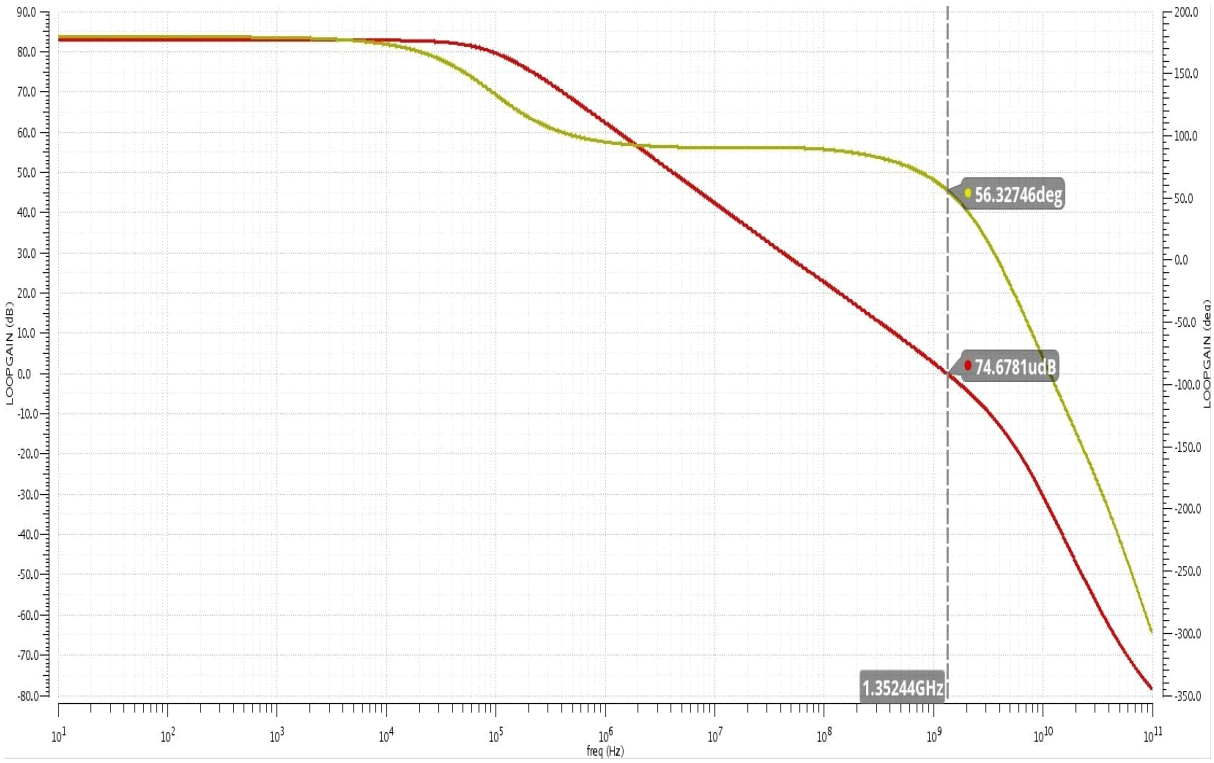

Fig.5.3 Frequency response of proposed LDO with compensation for SLOW corner

5.2.2 Load Transient Response of the LDO:

As discussed in section 3.4.4, the load transient occur due to large step occur in the output load current. The transient response for proposed LDO has shown in Fig.5.4. LDO transient response depends upon the output load capacitor, slew rate of the LDO, bandwidth of the LDO and also depends upon how quickly the current is changing as discussed in 3.4.4. The proposed LDO is driving the Mobile Industry Processor Interface (MIPI) transmitter driver, the capacitance seen from the supply terminal of the driver is approximately 600fF. Hence, load capacitor of 600fF is kept at the output of the LDO to observe the load transient response. The maximum voltage droop of 37.71mV for undershoot is observed for the worst case slow corner and 49.24mV for overshoot is observed for current change of 2mA to 10mA in 20nsec as shown in Fig.5.4.

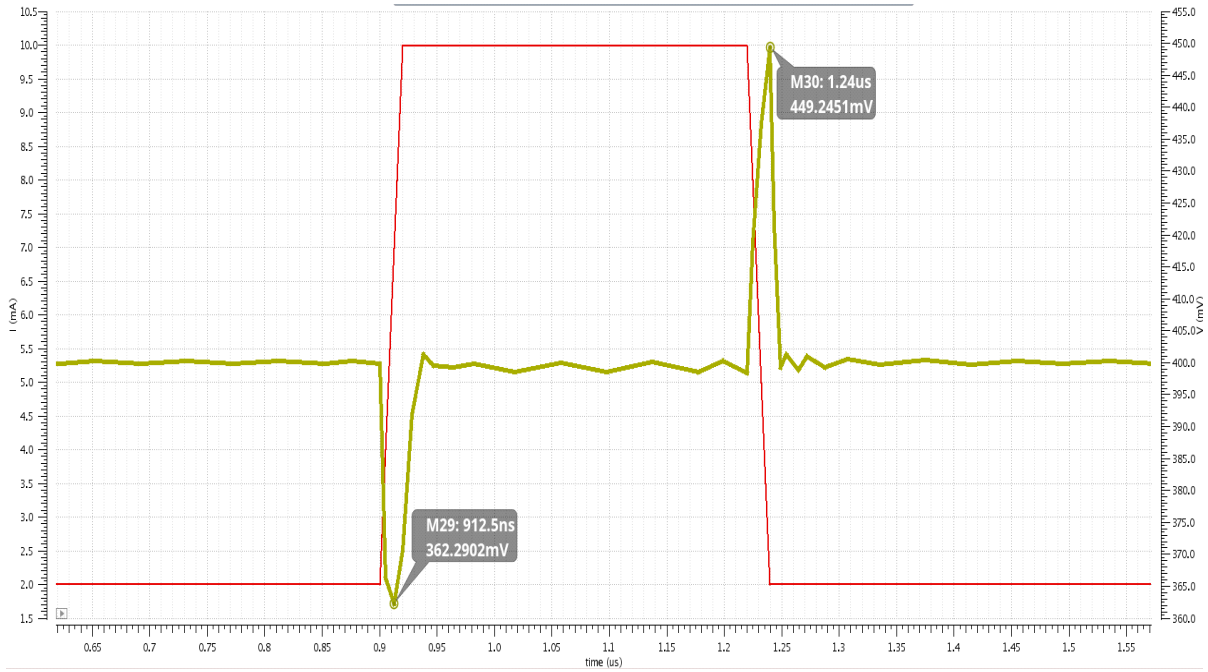

Fig.5.4 Load transient response of proposed LDO

The voltage droop as shown in Fig.5.4 should be as minimum as possible for better performance. For the proposed LDO, 30mV is the desired specification which is not achieved in the Fig.5.4.The reason for that is current step change is assumed to 20nsec that is for the ideal load but in practical while driving the transmitter driver, it may not be that much sudden change. So, it's possible to obtain the 30mV voltage droop with practical load.

5.2.3 PSRR Performance of the LDO:

In the theory of PSRR in section 3.4.5, it defines ability of LDO to reject the ripples from supply voltage. As the supply input is coming from the battery which gives very clean voltage, there is no high frequency variation in the supply input to the LDO. If supply input is coming from the buck converter, then PSRR need to check at high frequency. For the proposed LDO, PSRR of -32.21dB is observed at 1MHz.If the bandwidth of the LDO is very high, then PSRR can be better at wider frequencies. PSRR for the proposed LDO at 10mA is shown in Fig.5.5.

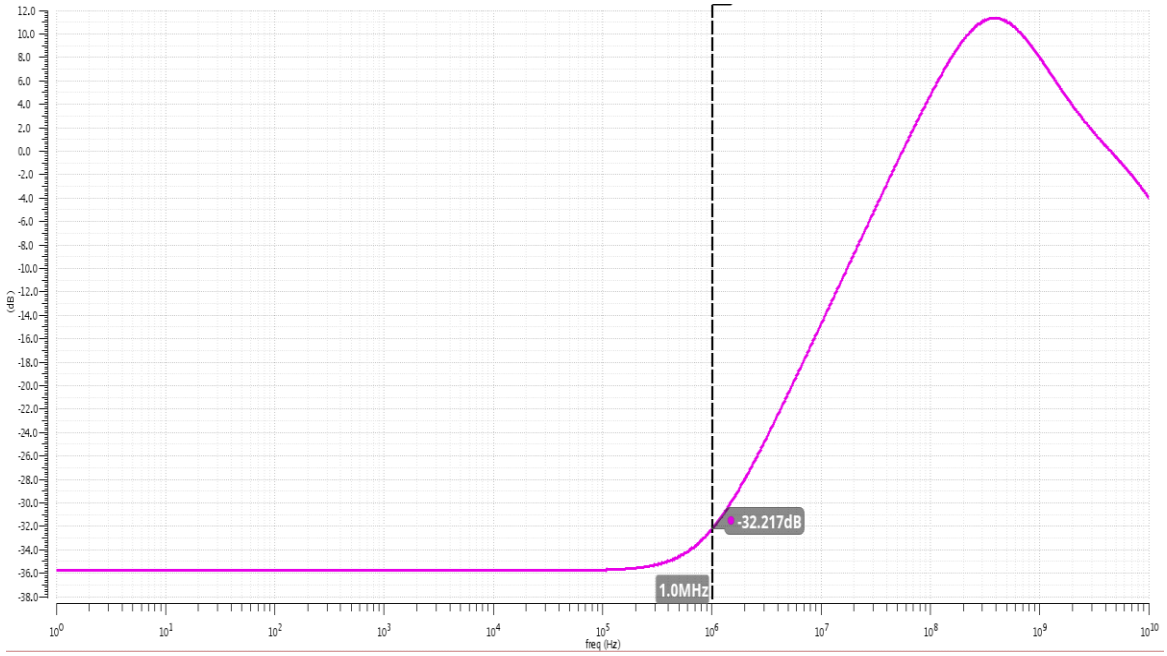

Fig.5.5 PSRR performance of proposed LDO

Fig.5.6 shows the plot of LDO output voltage variation with respect to temperature. From the Fig.5.6, it is observed that LDO output is stable over wide range of temperature variation.

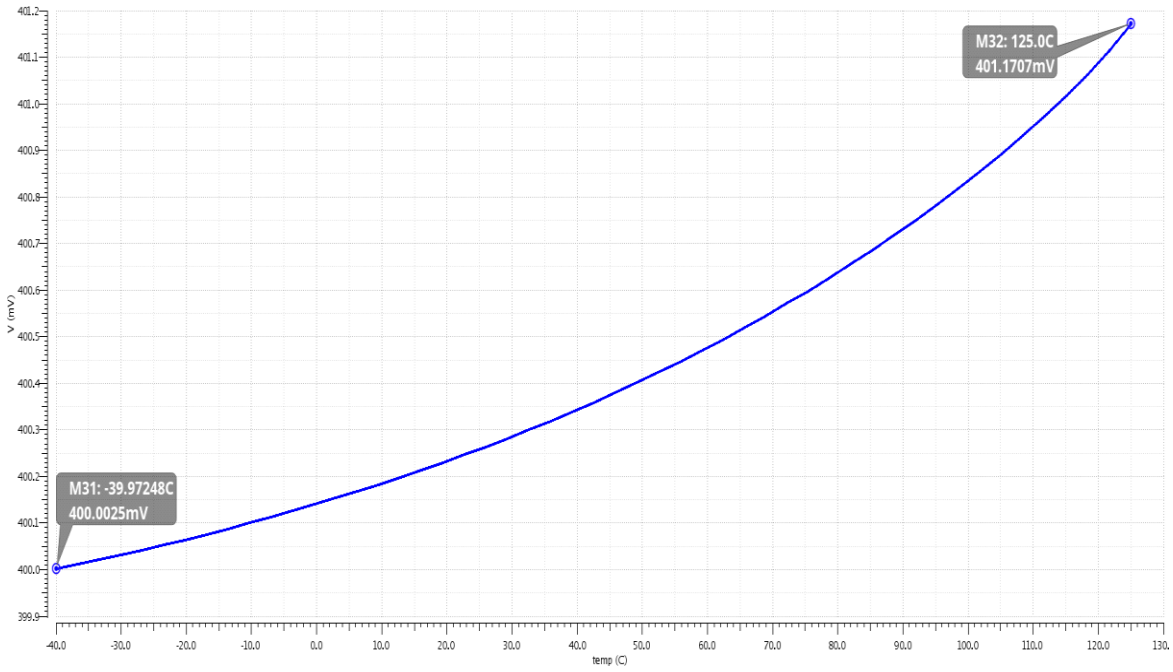

Fig.5.6 LDO output voltage with respect to temperature

Fig.5.7 shows the proposed LDO output voltage variation with respect to load current (I_L) which defines the Load regulation of the LDO.

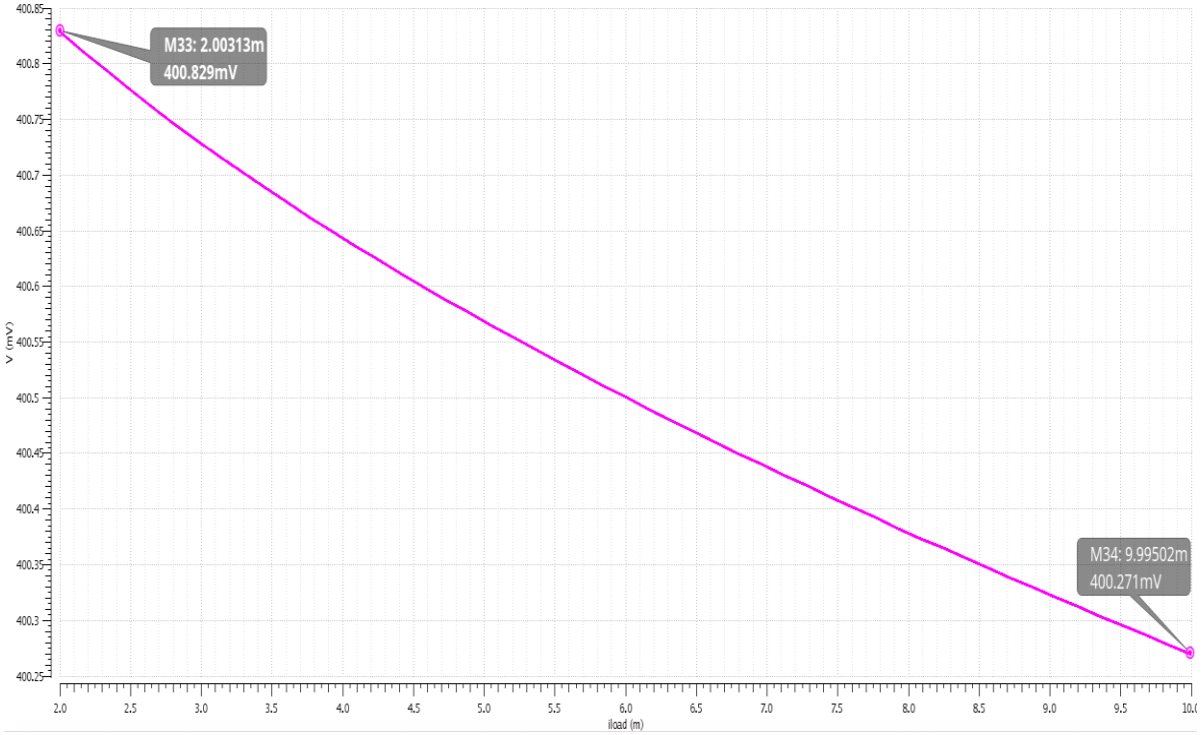

Fig.5.7 LDO output voltage function of Load current (I_L)

5.3 SUMMARY OF THE RESULTS

Table 5.2 shows the summary of the results that is the results obtained 0.4V output for all the PVT variation conditions for best case as well as worst case.

Table 5.3 Summary of the results for 0.4V output voltage

Circuit Parameters	Desired results	Obtained results			
		I_L= 2mA		I_L=10mA	
		Worst case	Best case	Worst case	Best case
Output Voltage	0.4V	0.410V	0.401V	0.407V	0.402V
Gain	40dB	57.22dB	88.66dB	52.82dB	84.18dB
Phase Margin	50°	48.69°	70.3°	51.99°	74.49°

Table 5.3 (contd.)

UGB	1GHz	409.9MHz	1.307GHz	502.8MHz	1.534GHz
PSRR at 1MHz	-40dB	-30.74dB	-38.65dB	-30.48dB	-38.46dB
Settling Time	100ns	Worst case		Best case	
		90.4ns		48.28ns	

As shown in table 5.2, there are deviations in the obtained results from desired results. This is due to device characteristics changes according to skews and corners. The table 5.3 shows the results obtained for 0.6V for all PVT.

Table 5.3 Summary of the results for 0.6V output voltage

Circuit Parameters	Desired results	Obtained results			
		IL=2mA		IL=10mA	
		Worst case	Best case	Worst case	Best case
Output Voltage	0.6V	0.608V	0.600V	0.605V	0.601V
Gain	40dB	52.19dB	87.96dB	52.87dB	87.99dB
Phase Margin	50°	49.02°	74.42°	53.17°	85.34°
UGB	1GHz	381.2MHz	1.237GHz	362.8MHz	1.445GHz
PSRR at 1MHz	-40dB	-30.49dB	-38.14dB	-29.73dB	-37.79dB
Settling Time	100ns	Worst case		Best case	
		78.4ns		44.31ns	

CHAPTER 6

6.1 WORK CONCLUSION

Many applications required low noise power supply. These application includes High Speed Serial I/O applications, Display transmitter, Memory applications, powering signal chain and many others. To address these needs, this thesis worked towards meeting demands for low noise MIPI display transmitter application. A proposed Low drop-out voltage regulator provides stable output voltage over wide range of Load current and input voltage for all the PVT variations. Stability is an important phenomena while designing on-chip Low drop-out voltage regulator, which can be achieved by Miller Compensation technique. In case of transient response of LDO, output load capacitor is providing the required charge at the time of load transient. But for scalability point of view that is for on-chip power management, the load capacitor will be within the chip so it will be lesser in value. Hence, it is unable to provide required current. Transient performance for the present LDO is improved by focusing on bandwidth of the LDO and slew rate of the LDO.

In this work, PSRR of the LDO is developed over wide range of frequencies. The proposed circuit is designed with PMOS input 1st stage followed by NMOS common source error amplifier. This topology helped to improve supply variation from error amplifier. PMOS pass device used in common source configuration which helps to improve PSRR as compared to NMOS source follower stage. Proposed LDO has simulated using Intel 10nm CMOS technology process and simulation results have presented. The proposed circuit provides adjustable output voltage of 0.4V to 0.6V with the load current of 10mA. The proposed design have compared with the previous designs listed in literature review. Proposed design have better PSRR bandwidth as compared to other designs presented in literature. 47

6.2 FUTURE SCOPE OF THE WORK

To improve the LDO power efficiency, switching regulators can be cascaded with LDO that is Hybrid DC-DC converter. In this concept, cascaded stage and LDO stage will work as parallel. LDO can be used as a post regulator. Hence, multiple LDO's can be combined with the switching regulator to achieve better power efficiency.

When it comes to powering sensitive and analog RF applications, LDO's are preferred over their switching counterparts. However, these applications have reached their capabilities and sensitivities that are testing the limits of the conventional low noise LDO's. With combination of ultra-low noise and ultra-high PSRR, LDO's can be directly power some of the noise sensitives applications while post regulating the output of switching regulator. Programmable output voltage as well as programmable current limit designs can be implemented for multiple applications.

In applications that need to run from a small battery cell for longer periods, need to make application average power consumption as low as possible. These application will often run in sleep mode most of time and are only active for short periods. To minimize power consumptions in sleep mode, need to select part of LDO's which are working on very low quiescent current. This helps to improve life time of battery.

REFERENCES

1. G. Alfonso and R. Mora, "Analog IC design with low-dropout regulators*," McGraw Hill New York*, 2009.

2. H. Armani and **H. Cordonnier,** "Power and battery management ICs for low-cost portable Electronics", *Annales Telecommun*ications Juilet/Aout, vol.59, pp. 974-983, Jul. 2004.

3. C. Simpson, "A User's Guide to Compensating Low-Dropout Regulators", *National Semiconductor*, 1997.

4. G. A. R.-Mora and **P. E. Allen,** "Optimized Frequency-Shaping Circuit Topologies for LDO's," in *IEEE Transactions on Circuits and Systems—ii: Analog and Digital Signal Processing*, vol. 45, pp.703-707, June 1998.

5. Gabriel A. Rincon-Mora and **Phillip E. Allen,** "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," *IEEE Journal of Solid-State Circuits*, Vol. 33, pp. 36-43, Jan. 1998.

6. G. A. Rincon-Mora, "Current efficient, low voltage, low drop-out regulators," Ph.D. dissertation, Elect. Comp. Eng. Dept., Georgia Inst. of Technology, Atlanta, 1996.

7. Texas Instruments, "Fundamental Theory of PMOS Low Drop-out Voltage Regulators," Application Report, Apr. 1997.

8. Jerome Patoux, "Low Drop-out Regulators," *Analog Dialogue*, May 2007.

9. P. Phillip, E. Allen and **D. R. Holberg,** "CMOS Analog Circuit Design," 2nd Ed., Oxford University Press, pp. 246-301, 2002.

10. K. N. Leung and **P. K. T. Mok,** "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1691–1702, Oct. 2003.

11. X. Lai, J. Guo, Z. Sun and **J. Xie,** "A 3-A CMOS low-dropout regulator with adaptive Miller compensation," *Analog Integrated Circuit Sig. Process*, vol. 49, pp. 5-10, Oct. 2006.

12. W. Oh and **B. Bakkaloglu,** "A CMOS Low-Dropout Regulator with Current-Mode Feedback Buffer Amplifier," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 54, pp. 922-926, Oct. 2007.

13. M. Al-Shyoukh, H. Lee and **R. Perez,** "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1732-1742, Aug. 2007.

14. T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok and **M. Chan,** "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 55, pp. 1392-1401, June 2008.

15. A. Saberkari, E. Alarco and **S. B. Shokouhi,** "Fast transient current-steering CMOS LDO regulator based on current feedback amplifier," *Integration, the VLSI Journal*, vol. 46, pp. 165-171, Mar. 2013.

16. C. K. Chava and **J. Silva-Martinez,** "A Frequency Compensation Scheme for LDO Voltage Regulators," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 51, pp. 1041-1050, June 2004.

17. P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan and **S. Borkar,** "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 933-940, Apr. 2005.

18. Z. Yan, L. Shen, Y. Zhao and **S. Yue,** "A Low-Voltage CMOS Low-Dropout Regulator with Novel Capacitor-Multiplier Frequency Compensation," *IEEE International symposium on Circuits and Systems*, pp. 2685-2688, May 2008.

19. Y. Shiyang, Z. Xuecheng, Z. Zhige and **C. Xiaofei**, "A Loop-Improved Capacitor-less Low-dropout Regulator for SoC Power Management Application*," IEEE Asia-pacific Conference on Power and Energy Engineering*, vol. 10, pp. 1-4, Mar. 2009.

20. J. Hu, W. Liu and M. Ismail, "Sleep-mode ready, area efficient capacitor-free low-drop-out regulator with input current-differencing," *Analog Integrated Circuit Sig. Process*, vol. 63, pp.107-112, Jan. 2010.

21. Z. Kamal, Q. Hassan and **Z. Mouhcine,** "Full On-Chip Capacitance PMOS Low Dropout Voltage Regulator," *IEEE International Conference on Multimedia Computing and systems in Morocco*, vol. 54, pp. 1-4, Apr. 2011.

22. D. Camacho, P. Gui and **P. Moreira,** "Fully on-chip switched capacitor NMOS low Drop-out voltage Regulator," *Analog Integrated Circuit Sig. Process*, vol.65, pp.141–149, Jan.2010.

23. Intel internal Documents.