PART A: Design and Simulation of a ZnO based Thin Film Transistor

PART B: Design and Verification of Bridges Based on AXI, APB, and OCP using System Verilog

by

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Certificate

This is to certify that this dissertation report entitled "**PART A design and simulation of ZnO based TFT** and **PART B Design and Verification of Bridges Based on AXI, APB, and OCP using System Verilog**" by Divya Goswami has been completed under our supervision and guidance, hence approved for submission in partial fulfillment for the award of degree of Master of Technology in VLSI Design to the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur during the academic session 2015-2017.

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Divya Goswami
(2015PEV5206)

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Abstract

This thesis work is divided into two parts. In part A Zinc oxide based thin film transistor is designed and its electrical characteristics are studied. Looking at previously fabricated zinc osxide based thin film transistors one would realize that their main application is in display electronics, in flat panel displays as switch for individual pixel.

In this work in part A I have proposed a zinc oxide based thin film transistor with high drain to source current ratio, high field effect mobility and low threshold voltage which makes it suitable for high speed display application. Dielectric material and substrate are selected according to application requirement of thin film transistor.

In part B I have designed bridges for bus communication in system on chip. With increasing complexities and size of Soc IP reusability is very important different IPs are designed around w different communication protocols at interface. Communication is required between them those IPs in a system therefore bridges are required to convert one protocol specification into another so that IPs can communicate without any error.

Failure in functionality of bridge to convert the information accurately can result in failure of complete system.

PART A: Design and Simulation of a ZnO based Thin Film Transistor

Chapter 1

Introduction

1.1Motivation

thin film transistors (TFTs) using ZnO as active layer have been widely incorporated in display electronics, because of their properties which makes them superior in comparison to existing semiconductor material which are used in display electronics, that include large band gap, high transparency, and large value of field-effect mobility. Problems like low value of field effect mobility, less pixel brightness, undesirable off state leakage current and opacity are present in conventional Silicon based TFTs which limits their application to high-resolution electronic display devices.

To overcome the problems associated with conventional silicon based TFTs various advancement and research work is performed to develop the new generation active channel layer material. ZnO is of the suitable candidate as it can be grown well oriented at relatively low temperature on various substrates. Several researches have been made for the use ZnO based TFTs in active matrix liquid crystal display (AMLCD) to increase the performance of device.

Properties of ZnO like optical transparency to near infrared and visible region makes ZnO based TFTs devices less sensitive to visible light spectra and results in optimization of fabrication process. The important parameters which are considered as figure of merit that can be used for comparison between performances of different TFTs are drain current on/off ratio and field effect mobility.

A large value of channel mobility produces large drive current density and results in faster switching speed of a TFT. Therefore many device structures for ZnO based TFTs are explored in order to improve device performance. There are various technological challenges which are still needed to resolve to make commercially viable TFTs. The various components like gate material. Dielectric material plays a very crucial role in the performance of TFTs. A not so good quality of dielectric can produce large leakage current and affect device performance. A high value of interface trap density between Semiconductor and dielectric can results in large threshold voltage value, which limits the TFT operation to large voltage thereby reduces its application.

Solution to the above problem is high K dielectric materials such as Ta_2o_5, orgainic polymer mixed with inorganic material like tio_2, Hfo_2, SiN, Al_2o_3 can be used instead of Sio_2 to reduce the leakage current and threshold voltage.

However there are still various practical challenges faced in fabrication of these gate insulators due to the surface roughness and difficulty of manufacturing procedure. Therefore despite of the drawbacks in conventional dielectric material they are still popular in fabrication processes

1.2 literature review

Existing publications relevant to the ZnO based TFTs were examined and only after the survey this design is proposed. In the below table 1.1 important parameters which are consider before selecting any material for fabrication are considered and compared, from the table 1.1 it can be seen that selecting oxide based material for channel is good choice both in terms of cost, ease of fabrication, reliability and performance.

Table 1.1 comparison chart between present technologies

TFT properties	Organic semiconductors	Amorphous Si	Oxide semiconductors
Carrier mobility [cm2 V−1 s−1]	0.1-10	1 max	1 to 100
Leakage current [A]	~10−12	~10−12	10−13
Manufacturing cost	low	Low	low
Long term TFT reliability	Low in air	Low	High
Process temperature [°C]	RT	~250	RT to 350

Shaivalini Singh proposed and fabricated the thin film transistors (TFTs) using Zinc oxide semiconductor as active layer which was deposited by using radio frequency magnetron sputtering technique. A bottom gate TFT was designed and SiO_2 is used as dielectric layer. The X-

ray diffraction pattern showed that the zinc oxide films are orientate in the (002) plane with c – axis perpendicular to the substrate. TFT which was fabricated by this method has saturation mobility of 0.6134 cm^2/Vs, an off current 20×10^{-7} A and ratio of drain current on to off is 10^2. Simulation is performed using ATLAS™ from Silvaco-International [18].

Yasemin Caglar proposed and fabricated bottom gate zinc oxide TFT using SiO_2 as a dielectric on p type silicon substrate, zinc oxide active channel layer of different thickness was deposited by using sol gel spin coating technique and electrical characteristics of TFTs were compared for different active layer thickness. The effect of active layer thickness on morphological and structural properties of ZnO was examined. The value of field effect mobility significantly improves by increasing the thickness of channel layer highest value obtained was $1.09cm^2/Vs$ for the thickness of 140 nm layer but the value of off current increases as the channel thickness increased [21].

Soo Chang Kim fabricated and study the property of a InGaZnO based TFT with short channel (W/L = 12/3) length. The field effect mobility is found to be 6 cm^2/Vs, threshold voltage around 3.32V and current on to off ratio < 10^9.high threshold voltage was one of the drawbacks of this design [23].

FF Vidor fabricated a low cost and low temperature integration process for zinc oxide nanoparticle based thin film transistor by spray coating technique. They developed a inverted coplanner structure with high k dielectric layer filled with TiO_2 nanoparticle to increase the dielectric constant. Field effect mobility observed 0.1 cm2/Vs and drain current on to off ratio was found 105 with negative threshold voltage of -3.5V.

C. J. Chiu fabricated an amorphous indium gallium ZnO based thin film transistor with a high- k dielectric on glass substrate. It's deposited in the room temperature. Ta_2o_5 is used as a dielectric the electrical characteristics were observed, darin current on to off ratio was 10^5, a threshold voltage swing of 0.61V/decade and field effect mobility was around $61.5cm^2/v$ which is very high. These features make this TFT suitable for switching transistor and low power applications [25].

Fabrizio Torricelli fabricated and studied the properties of zinc oxide based thin film transistor. The zinc oxide active layer was deposited by spray pyrolysis. He investigated the transport properties in detail over a wide range of temperatures, for different channel length and electrical conditions for example subthreshold and above subthreshold, saturation and linear region. Zinc oxide deposited by using spray pyrolisis technique is in nanocrystalline form. Its field effect mobility increases with the carrier concentration and affected by temperature. On the basis of the above analyisis he proposed a multi-trapping- release transport mechanism model to describe the charge transport in zinc oxide and performed numerical simulation to validate this model. The value of field effect mobility observed was $0.5cm^2/Vs$ and ratio of drain on to off current is 10^5 [24].

1.3 Thesis Outline

The thesis is organized as follows:

Chapter2 discusses the theory behind TFTs about the device operation, properties of zinc oxide, role of dielectric material and figure of merit for measuring performance of TFTs.

Chapter 3 is about the different topologies present for designing transistor.

Chapter 4 is dedicated to design and simulation of the device.it includes detail description abt the design parameters and material used for simulation.

Chapter 5, this chapter includes result and conclusion of the above simulation results.it contain the result produced using ATLAS too of silvaco international and conclusion derived from those results.

Chapter 2

Theory

2.1 device operation

Transistors are the basic building blocks in modern electronic systems. They are the very essential part of integrated circuits, which can be found in nonvolatile memories, as switches in display applications and micro-processors. A transistor can be used as an amplifier and a non mechanical switch reason is that it is possible to control the electrical resistance between the two terminals drain and source by applying voltage to the gate terminal which is the third terminal.

In present scenario most commonly used transistor functionality is based on field effect. In 1925 field effect was discovered and Lilienfeld filed the first patent on the use of this principle [12]. In 1960 kahng and Atalla fabricated the first fully functional field effect transistor this was the first fully functional transistor [13]. It is known as metal oxide semiconductor field effect transistor because of the material used in its construction (Si/SiO_2). Nowadays it is most popular type. The thin film transistor was first presented in RCA laboratories by Weimer in 1962 [3]. Cadmiumsulfide was the semiconductor which was used thin film of it was deposited by evaporation. In the following section working principle of a field effect transistor is presented.

Normally transistor is called a three terminal device. There are three terminals in a transistor source, drain and gate name are assigned to the terminal according to their functionality. Semiconductor is connected with source and drain electrodes, semiconductor is insulated from gate terminal by a dielectric layer. There various suitable dielectric materials like SiO_2, Ta_2O_5 polyemers with mixed with inorganic materials like TiO_2. Most commonly inverted staggered structure is used as shown in Fig. 2.1. Opening and closing of channel between the two terminals is controlled by gate terminal. The gate electrode and insulating dielectric layer are coupled capacitively with the active channel layer.

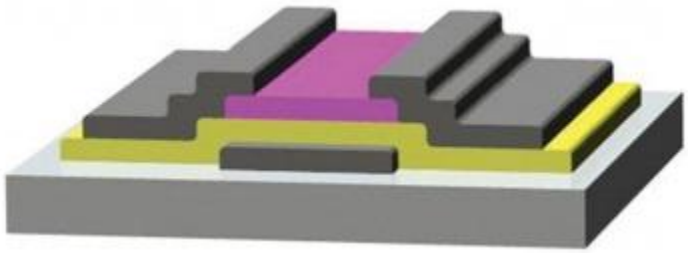

Fig 2.1 most commonly used architecture of TFT

Electric field is generated between source and drain terminal by applying a voltage V_{GS} between source and gate terminal of transistor. This results in accumulation of minority charge carrier between the dielectric and semiconductor interface and up to a width known as depletion region width. In n type transistor accumulation of electrons take place at the interface by applying positive voltage to the gate terminal as depicted in figure 2.2. The accumulated charges along with the initial charge carrier type and it's concentration in the active channel contributes towards the drain to source current flow in the channel [14]. Thus current I_D can be calculated from the drain to source voltage and voltage applied between gates to source electrode.

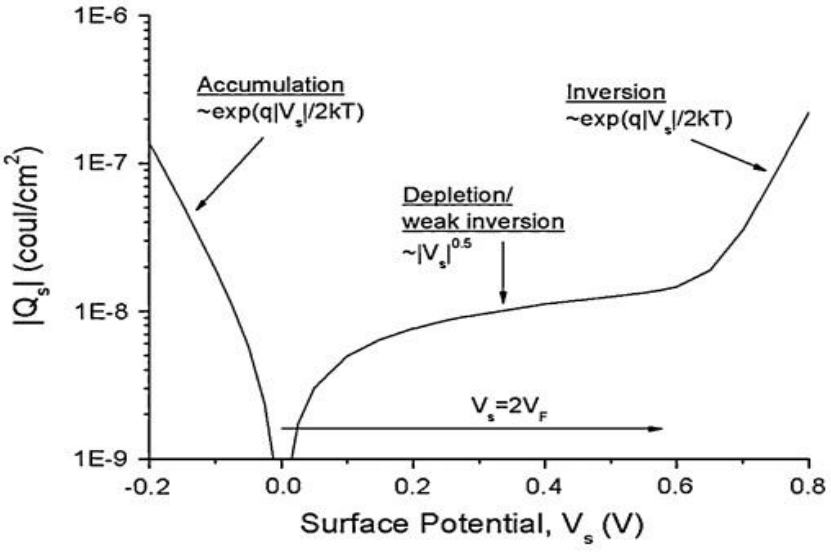

Fig 2.2 variation of surface charge density with surface potential

There is certain voltage called as threshold voltage after which charge carrier starts flowing between drain to source terminal electrode. There two operation region in transistor one is linear region in which value of V_{DS} is very low and other region is saturation region in which current remain constant for a constant value of V_{GS}. For linear region $V_{DS} << V_{GS}- V_{TH}$ and for saturation region this condition is reversed. I_D can be obtained from equation 2.1:

$$I_D = u_{lin} c_i \frac{W}{L} (V_{gs} - V_{th}) V_{ds} \qquad \text{eq. 2.1}$$

In equation 2.1 W is channel width, L is channel length, C_i is gate dielectric intrinsic capacitance and μ_{lin} is linear charge carrier mobility Gate dielectric intrinsic capacitance per unit area C_i is calculated by the equation 2.2.

$$C_i = \frac{C}{A} = \frac{\varepsilon_o \varepsilon_r}{d} \qquad \text{eq.2.2}$$

In equation 2.2 thickness of the dielectric layer is d, ε_r is the relative dielectric constant and ε_0 is the permeability. To achieve a high capacitance thickness of the dielectric layer should be less and relative permeability should be very high.SiO2 though popular but it's ε_r value less therefore dielectric material like HfO_2, AlO_x and TiO_2 are preferred materials in order to achieve high dielectric capacitance [15]. Advantage of larage capacitance is high value of drain current at lower voltage level. Large value of drain to source voltage results in decrease in charge near the drain region because strength of electric field is decreased at the drain junction. This condition of depletion of charge near drain region is known as pinch off. After this condition drain current becomes independent of drain source voltage. There is no enhancement in drain current with drain to source voltage. As shown in the equation 2.3

$$I_D = u_{sat} c_i \frac{W}{L} (V_{gs} - V_{th}) V_{ds} \qquad \text{eq. 2.3}$$

μsat stand for saturation field-effect mobility.

In figure 2.3 output characteristic is shown in this graph transition between the two regions, linear and saturation region can be seen. For a constant V_{GS} relation between drain voltage and drain current has been shown. Operation condition of the transistor can be determined from the output characteristics

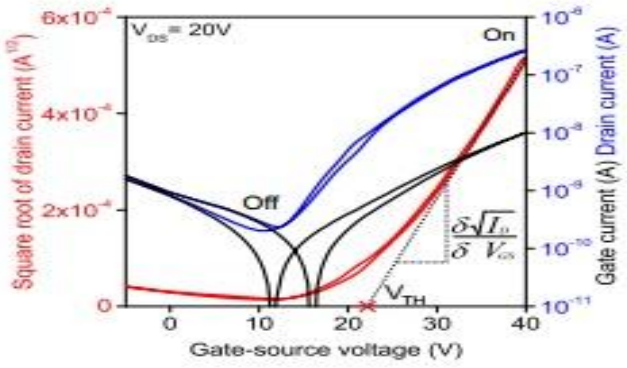

Fig 2.3 shows drain current as a function of gate bias

Field effect mobility is the figure of merit that's used to compare the different transistor configuration performance. It is indicates the active channel's, which is made up semiconductor, efficiency in transporting charge carrier through it. Its impact is not only on the draun current but also on the frequency of operation of device. It also indicates the quality of dielectric and semiconductor interface along with quality of material as mobility is affected the impurities of crystal and grain boundary this phenomenon is called as scattering [5]. Field effect mobility is given in equation 2.4

$$\mu_{EF} = \frac{g_m}{C_i \frac{W}{L} V_D} \qquad eq\ 2.4$$

Another factor which is considered as figure of merit is V_{on} or V_{th} i.e. threshold voltage, which can be obtained from the transfer characteristics of the curve. Basically most of the studies V_{th} is not used a parameter instead of V_{th} V_{on} is used. This is also obtained from the transfer characteristic graph by taking log of drain current, Von is the value at which log of drain current becomes non zero for the applied gate voltage [17].

Third important parameter is drain off to on current ratio. It is basically the ration maximum darin current to the leakage current of transistor. Maximum drain current is dependent on various factor like applied gate voltage and electric filed generated by that gate voltage, contact resistance and the properties of channel material. Whereas leakage current or off current is dependent on doping, both intrinsic and extrinsic doping of semiconductor material, charge present in the semiconductor or produced by the thermal excitation. A ratio larger than the 10^6 is required in most of the application of transistor.

Though the operation of thin film transistor is similar to the MOSFETs, there are few important differences between this two. First is substrate and semiconductor are made up of Si in MOSFETs where this is not the case in TFTs. Second is in single crystalline semiconductor performance of charge carrier transport improves. Furthermore, the modulation of the channel resistance in a MOSFET is caused by a charge carrier inversion at the interface, allowing e.g. the formation of an n-type conductive layer in a p-type silicon substrate in thin-film transistors, insulating substrates are used and the required semiconducting and dielectric layers are deposited as thin films. Further, the channel modulation is achieved by charge carrier accumulation and depletion, respectively.

2.2 Properties of ZnO

Zinc oxide is used from decades in many products like rubber, cosmetics, paints etc. interest is renewed in the material from past one decade. Reason of this renewed interest is possibility of producing thin layer at low temperature and superior quality nano crystalline structures can be fabricated form zinc oxide material. Applications of zinc oxide material are many like in field effect transistors, solar cells etc. in this section properties of zinc oxide are explained in detail[1,2,3].

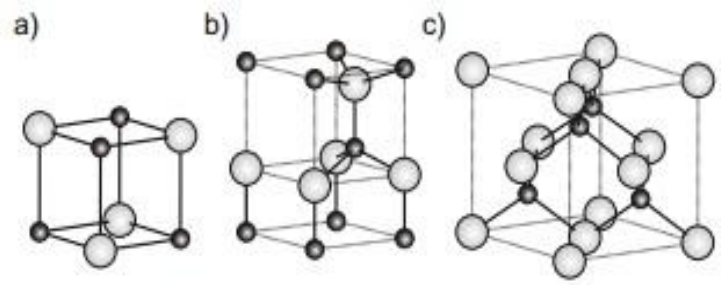

Fig 2.4 Crystal structure unit cells of zinc oxide. From left to right: a) cubic rocksalt, b) hexagonal wurtzite and c) cubic zincblende. The zinc atoms are depicted in light gray color.

ZnO is a brittle powder like material which is non toxic. One of its interesting properties is thermochronic behavior which is basically ability to revert the change in color from white to yellow on heating. Property that makes is it suitable for sensor application is piezoelectricity. It is insoluble in water and decomposes at 1975◦C.

Hexagonal wurtzite structure is thermodynamically favorable crystal structure under ambient temperature and pressure [4]. In this structure configuration, oxygen ions tetrahedrally surround each zinc ion. Zinc and oxygen bounds have strong ionic characteristics even though zinc and oxygen bounds are covalent bounds with sp^3 hybridization [5]. Therefore it can be classified as both ionic and covalent compound. The lattice constants of the hexagonal unit cell are a=3.2 Åand c=5.2 Å. Other phass in which zinc oxide can be found are rocksalt form and zincblende form [6, 7]. The figure 2.1 shows crystalline structure.

Zinc oxide is a compound semiconductor made from group second and fourth. It is direct band gap material with large band gap of 3.4 eV and its excitation binding energy is very large 60meV. Therefore it is ideal candidate for optical devices. Zinc oxide conduction band is formed from 4s orbital. In oxygen atom valance band is formed from 2p orbital. S orbital has large radii and spherical structure. Distance between the zinc atoms determines the formation of conduction band not the spatial orientation bands. This is the reason that in both crystalline and amorphous forms has effective charge transport. This is the reason material is not affected by the disturbance

in the bulk material. If compared with silicon, the mobility in amorphous form is 2 times less than its crystalline form. In silicon there are unsaturated bounds with bound angles tilting highly because of the high order disorder in silicon amorphous form as result mobility decreases. Fig 2.5 shows the difference between zinc and silicon oxide structures in amorphous and crystalline form

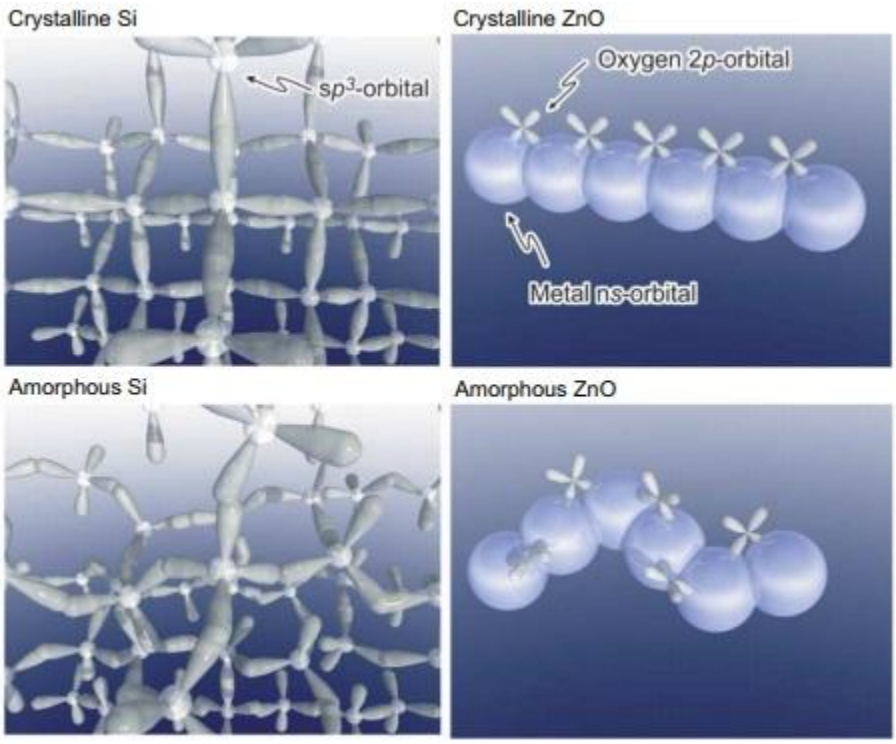

Fig 2.5 difference in structure of zinc oxide and silicon oxide

Zinc oxide is an n type semiconductor without any doping. Due to the property of large band gap thermal generated charge carrier are not able to contribute in charge transport. It can be doped with n type impurities like In, Ga, and Al which are the third group elements or there is one more method oxygen atom are replaced by fluorine and chlorine atom also known as halogen ides. This kind of doping is called as intentional doping [4,10].

As zinc oxide is intrinsically n type in nature therefore to introduce p- type doping is very difficult due to the presence of large number of donor atoms p type acceptor atom are compensated by them. P type impurities are mostly alkali metals like Na and Li or fifth group elements like As, N, P etc. Özgür *et al* has studied the different materials of various group for doping zinc oxide [4].

Zinc oxide can have a very large electron mobility value up to 200 cm^2/Vs at room temperature for a single crystal but varies vastly with fabrication method[]. But the value of hole mobility is very low in comparison to electron mobility it varies in the range of 5 cm^2/Vs to 30 cm^2/vs [11].

at low temperatures hopping mechanism dominates as charge transfer occurs only between defect state of band gap. Tunneling and thermionic emission dominates in case of nano crystalline material as there are large numbers of grain boundaries.

This high mobility, low leakage current, long term reliability, high yield, low processing temperature and less manufacturing cost of ZnO based thin film transistors are the main reason behind increased attention for using ZnO material for transistor application.

2.3 Role of Dielectric Material

Transistor design seeks to maximize the response of the gate-induced charge in the semiconductor channel. The ability to modulate semiconductor charge is ultimately limited by the electronic properties of the gate-dielectric ideally; it is desirable to have gate-dielectrics with high permittivity, low loss and high breakdown fields. For example, materials which are good insulators (i.e. large band gaps) tend to have low dielectric constants (Figure 1.1, page 2). Furthermore, defect formation is unavoidable, leading to additional conduction pathways that enhance losses. Consequently, gate-dielectric optimization is a sensitive component of transistor design. Historically, aggressive scaling of physical dimensions of transistors has necessitated the use of high-permittivity (i.e. "high-k") dielectrics in high-performance electronics in order to lower operating voltages and increase current density. Properties of dielectric material play a very crucial role in deciding the characteristics of thin film transistor. In this project I have used two different type of dielectric material to base on different advantages they have. First one is High-*k* resist the high-epsilon resist, based on hydrolyzed and second is Ta2O5. In below section detail description and advantage of using these dielectric materials is explained. The high dielectric constant leads to a better gate control over the driving current, resulting in a good sub threshold swing (SS), less threshold voltage (VT) [17].

2.3.1 High-*k* resist (K = 12)

For decade silicon dioxide is used a gate dielectric, insulating gate from channel material in transistor. With advancement in technology result in shrinking of transistor size which requires decrease in thickness of dielectric layer so that capacitance can be increased which further results in increase in drain to source current for high performance of device large drain current is required. In case silicon dioxide as the thickness decreased less than 2 nanometers tunneling effect increases which result in high leakage current resulting power wastage and decreases the drain current on to off ratio. Therefore the need arise to replace the silicon dioxide with high materials having large value of dielectric [17].

High-k resist are high-epsilon resist, where K indicates the dielectric constant of the dielectric material. These are basically based on hydrolyzed and partially condensed ethyl silicates that can be deposited at processing temperature below 80°C. The value of dielectric constant can be

varied by adding inorganic components. Hence it offer mechanically flexible and a high dielectric insulating material.

2.3.2 Ta_2O_5

It is known as Tantalum pentoxide, other name is tantalum (V) oxide, and this is an inorganic compound. It is an inert material and has very high refractive index and low absorption or insensitive towards light which make it a potential candidate for display application based TFTs. It is insoluble in water. Due to its high dielectric constant value it provides a large capacitance. This results in large current, and a high current on to off ratio. To solve the gate dielectric reliability problem various high dielectric materials are suggested but the major issue faced is defect formation near the gate and dielectric interface boundary Chyuan-Haur Kao conducted a study in which RF sputtering is used to deposit Ta2O5 on polycrystalline silicon and used post RTA annealing to mitigate defect formation [22].

2.4 Important parameter for calculating the performance of transistor

The most important TFT static characteristics are extracted from the input/output and transfer characteristic graphs. These characteristics are $I_{On/off}$ ratio, mobility, V_{on}/V_T. These parameters are used to measure the performance of transistor.

$I_{On/off}$ ratio: It is the ratio of maximum drain to source current to minimum drain to source current (leakage current). The minimum value of drain to source current is dependent upon gate leakage current (I_G), while the maximum I_D depends upon the semiconductor material properties and the effectiveness of capacitive injection by the field effect. On to off ratio of current above 10^6 is required for their successful usage as electronic switches. Lower value of leakage current is mostly desired because maximum values are mostly in the range of 106 - 10^3 ampere [20].

V_{ON}/V_T: Threshold voltage is that gate voltage at which sufficient charge is accumulated in the channel region after which current starts flowing in the channel region between drain to source electrodes. Positive or negative value of threshold voltage for a n type thin film transistor determines whether the transistor is working in enhancement mode or depletion mode. Generally enhancement type is preferred over depletion type as no turn off gate voltage is required to switch off the transistor current. Therefore reduces the power consumption and complexity of the design circuit. There is lots of ambiguity in determining the value of threshold voltage one method is linear extrapolation of drain current versus gate voltage plot for low value of drain voltage or square root of drain current and gate voltage for high value of drain voltage. Hence Von is largely used parameter it can be obtained from the log of drain current versus gate voltage graph. It is the voltage which is fully required to switch off the transistor [20].

***Mobility* (μ)**: It indicates the efficiency of transport of charge carriers in the material. It has a direct impact on frequency of operation and maximum value of drain current. There are various scattering mechanism like grain boundaries, ionized impurities and lattice vibrations which affects the value of mobility. There are various other sources of scattering as scattering due to surface roughness, interface state and dielectric charges results in columbic scattering. These other effects come into picture due to the proximity of channel region near to dielectric interface. Gate voltage has large influence on the value of mobility so affect of these scattering mechanisms becomes less relevant. There are various methods to calculate mobility. According to Schroder's nomenclature following are the different motilities:

Effective mobility (μeff): Obtained by the conductance (g_d) with low V_D:

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L}(V_G - V_T)} \qquad eq.2.5$$

Field-effect mobility (μ_{FE}): Obtained by the transconductance (g_m) with low V_D:

$$\mu_{EF} = \frac{g_m}{C_i \frac{W}{L} V_D} \qquad eq.2.6$$

Saturation mobility (μsat): Obtained by the transconductance with high V_D:

$$\mu_{sat} = \frac{(\frac{d\sqrt{I_D}}{dV_G})^2}{\frac{1}{2}\frac{W}{L}C_i} \qquad eq.2.7$$

All these methods for calculating motilities have there on advantages and disadvantages [20,26]. For example μ_{eff} takes into consideration the important factor of gate voltage but it also requires threshold voltage which heavily depends upon on the contact resistance. Therefore μ_{FE} is a widely used parameter as it is independent of threshold voltage and used in this work to calculate mobility of charge carriers. Similarly even μ_{SAT} is independent of threshold voltage and there has low sensitivity towards contact resistance but its usage is limited to saturation region only.

Chapter 3

Transistor Topology

There are four possible configurations in thin film transistors depending upon the relative position of its source/drain electrode and gate electrode: staggered with bottom gate, staggered with top gate, coplanar with bottom gate, coplanar with top gate. Staggered devices only have the semiconductor in contact to the gate dielectric where as in coplanar configuration device have the source/drain and semiconductor adjacent to the same side of the gate dielectric. There is another term which is commonly used for bottom gate is inverted hence staggered with bottom gate is also known as staggered –inverted and coplanar with bottom gate configuration is known as coplanar inverted. There is no special terminology for top gate so staggered with top gate is simply staggered and coplanar with top gate configuration is simply coplanar. There different advantage and disadvantage of each configuration based on the application it is used for as different application requires different configuration.

Each of these configurations has different advantage and disadvantages depending upon the material used for fabrication and application of device. For example the staggered inverted configuration is widely used for the fabrication of a-Si:H TFTs, due to easier processing and improved electrical properties. As a-Si:H is light sensitive, the usage of this configuration is advantageous for the application of these TFTs in LCDs, since the metal gate electrode shield the semiconductor material from the effect of the backlight present on these displays. Other example is of coplanar top gate structure which is normally preferred for poly-Si TFTs. The reason of using this configuration is the fabrication process, the crystallization process of semiconductor material generally requires high temperatures that can potentially degrade the properties of other materials and their interfaces, which are previously deposited, and this configuration is normally used when semiconductor is a flat and continuous film without layers beneath it.

Also, an insulating film is often deposited on top of the semiconductor layer in staggered bottom-gate structures. This can allow for more accurate etching of the source-drain electrodes, without damaging the semiconductor surface, i.e. act as etch- stopper. This insulating layer can also have interesting effects on semiconductor films that strongly interact with environmental species such as oxygen or moisture, which is reflected in large variations of the electrical properties exhibited by the TFTs [20]. This is particularly relevant for some of the first semiconductors used in TFTs, such as CdSe, and also for oxide semiconductors. Additionally, the insulating layer on top of the TFT structure can work as an effective mechanical and chemical protection of the devices from subsequent processes.

For protection a thin insulating film is always deposited on staggered bottom gate structure

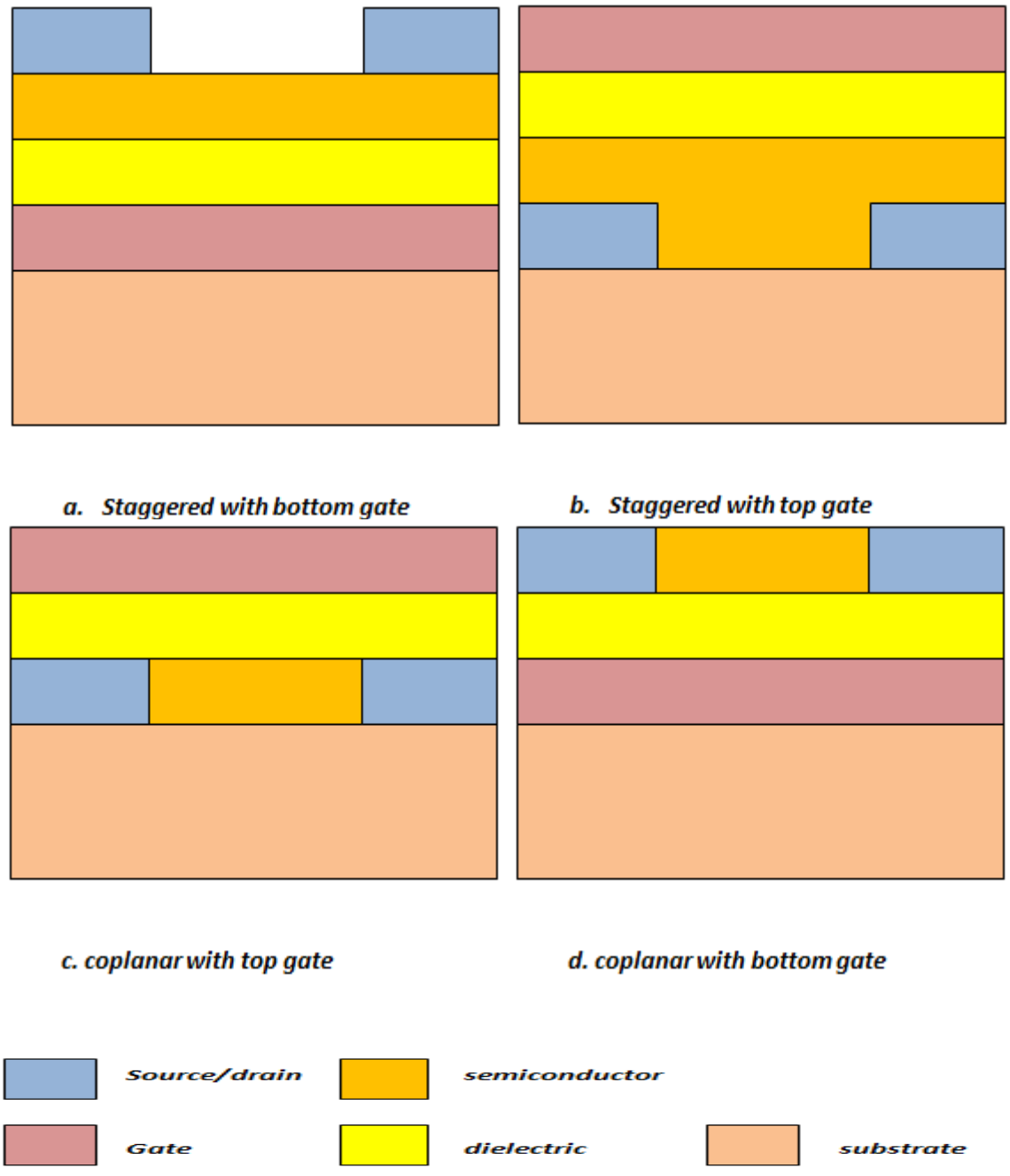

Fig 3.1 all the four topology possible which are commonly used

Chapter 4

Design and simulation

4.1 Basic structure of TFT

In this report the effect of dielectric material and thickness of active layer on the I_D Vs V_D and I_D Vs V_{GS} is observed. Two different dielectric materials are used in this project. One is a polymer based high K dielectric material of relative permittivity Ɛ = 12 and other is an inorganic compound Ta_2O_5 with relative permittivity Ɛ = 27. Thickness of dielectric layer is kept constant in all the devices only the thickness of active semiconducting layer is varied and its effect on mobility and on current of the device is observed.

Four device structures are simulated using silvaco. In First two structures dielectric material is high k resist in the remaining two structures dielectric material is Ta_2O_5.

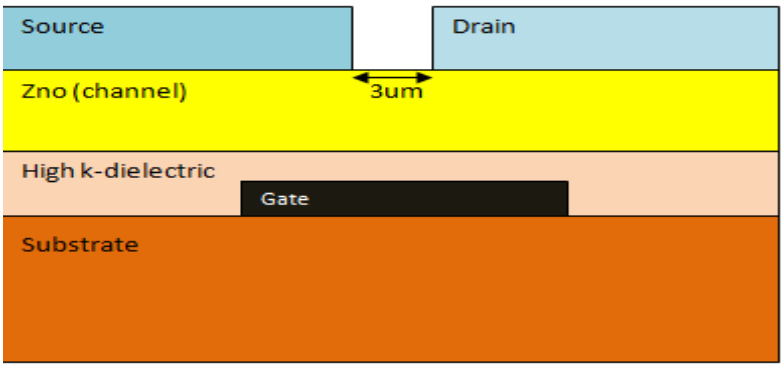

Fig.4.1 Inverted staggered topology used in all four TFTs

Inverted staggered topology is used in all the four TFTs. Source, drain and gate electrodes are made of aluminum, reason of using aluminum is the large difference in work function of aluminum and ZnO second reason is ease of fabrication process. Active layer is of zinc oxide semiconducting material. Substrate is made up of flexible polymer polyethylene terephthalate (PET). As shown in Fig. 4.1

4.2 Device dimension and material used

Table 4.1 Dimensions of device 1

S.NO	STRUCTURE	LENGTH	WIDTH	THICKNESS
1.	GATE	33 um	500 um	50 nm
2.	SOURCE	125 um	500 um	150 nm
3.	DRAIN	125 um	500 um	150 nm
4.	SUBSTRATE	253 um	500 um	300nm
5.	DIELECTRIC	253 um	500 um	160nm
6.	SEMICONDUCTOR	253 um	500 um	300nm

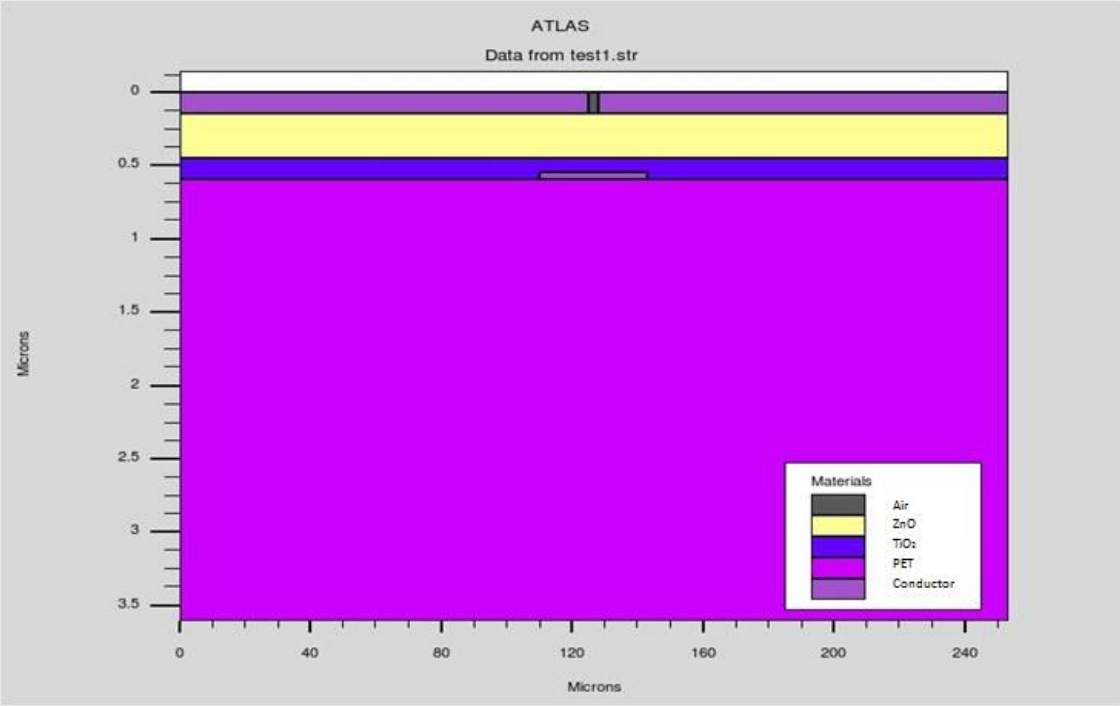

Fig.4.2 device1 2D structure

Table 4.2 Material used in device 1

S.NO	STRUCTURE	MATERIAL
1.	GATE	ALUMINUM
2.	SOURCE	ALUMINUM
3.	DRAIN	ALUMINUM
4.	SUBSTRATE	PET
5.	DIELECTRIC	HIGH K (K =12)
6.	SEMICONDUCTOR	ZNO

Table 4.3 Dimensions of device 2

S.NO	STRUCTURE	LENGTH	WIDTH	THICKNESS
1.	GATE	33 um	500 um	50 nm
2.	SOURCE	125 um	500 um	150 nm
3.	DRAIN	125 um	500 um	150 nm
4.	SUBSTRATE	253 um	500 um	300nm
5.	DIELECTRIC	253 um	500 um	160nm
6.	SEMICONDUCTOR	253 um	500 um	200nm

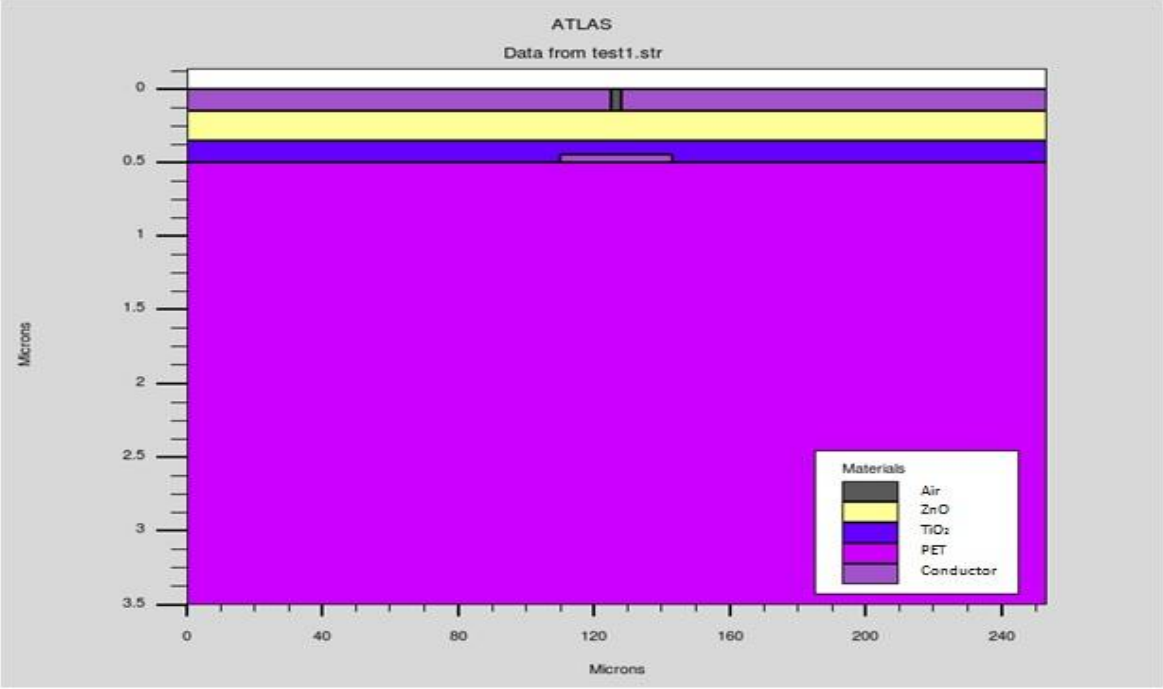

Fig.4.3 device2 2D structure

Table 4.4 Material used in device 2

S.NO	STRUCTURE	MATERIAL
1.	GATE	ALUMINUM
2.	SOURCE	ALUMINUM
3.	DRAIN	ALUMINUM
4.	SUBSTRATE	PET
5.	DIELECTRIC	HIGH K (K =12)
6.	SEMICONDUCTOR	ZNO

Table 4.5 Dimensions of device 3

S.NO	STRUCTURE	LENGTH	WIDTH	THICKNESS
1.	GATE	33 um	500 um	50 nm
2.	SOURCE	125 um	500 um	150 nm
3.	DRAIN	125 um	500 um	150 nm
4.	SUBSTRATE	253 um	500 um	300nm
5.	DIELECTRIC	253 um	500 um	160nm
6.	SEMICONDUCTOR	253 um	500 um	300nm

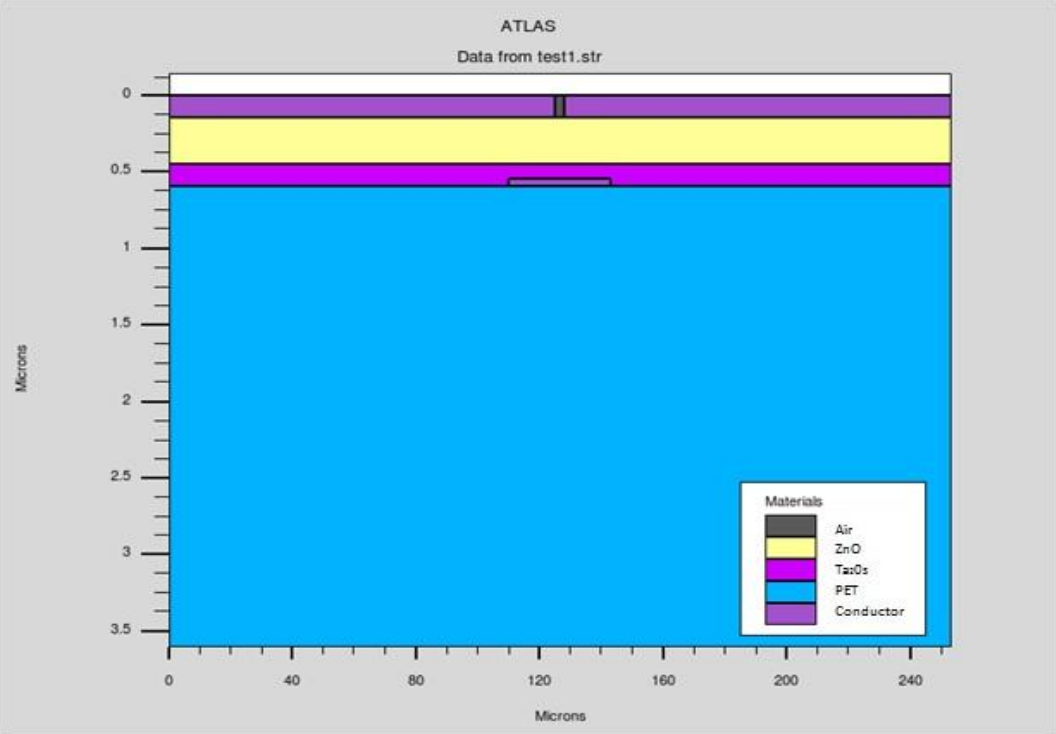

Fig.4.4 device3 2D structure

Table 4.6 Material used in device 3

S.NO	STRUCTURE	MATERIAL
1.	GATE	ALUMINUM
2.	SOURCE	ALUMINUM
3.	DRAIN	ALUMINUM
4.	SUBSTRATE	PET
5.	DIELECTRIC	Ta_2O_5 (k = 27)
6.	SEMICONDUCTOR	ZNO

Table 4.7 Dimensions of device 4

S.NO	STRUCTURE	LENGTH	WIDTH	THICKNESS
1.	GATE	33 um	500 um	50 nm
2.	SOURCE	125 um	500 um	150 nm
3.	DRAIN	125 um	500 um	150 nm
4.	SUBSTRATE	253 um	500 um	300nm
5.	DIELECTRIC	253 um	500 um	160nm
6.	SEMICONDUCTOR	253 um	500 um	200nm

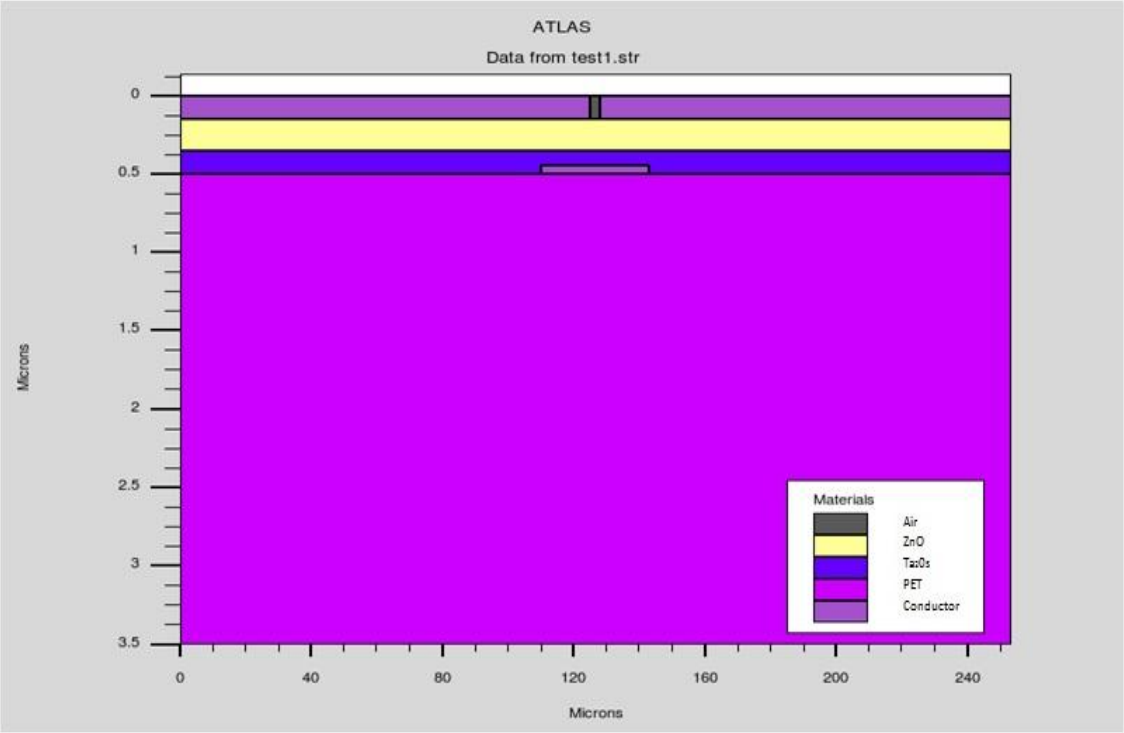

Fig.4.5 device 4 2D structure

Table 4.8 Material used in device 4

S.NO	STRUCTURE	MATERIAL
1.	GATE	ALUMINUM
2.	SOURCE	ALUMINUM
3.	DRAIN	ALUMINUM
4.	SUBSTRATE	PET
5.	DIELECTRIC	Ta_2O_5 (k =27)
6.	SEMICONDUCTOR	ZNO

4.3 RESULTS

Graphs of input output characteristics and transfer characteristics of all four devices produced by simulating the device structures in ALAS silvaco tool. Field effect mobility is calculated by calculating transconductance at lower value of drain voltages by using eq. 2.6 Input/output characteristics are used to determine on to off drain current.

DEVICE 1: dielectric constant 12

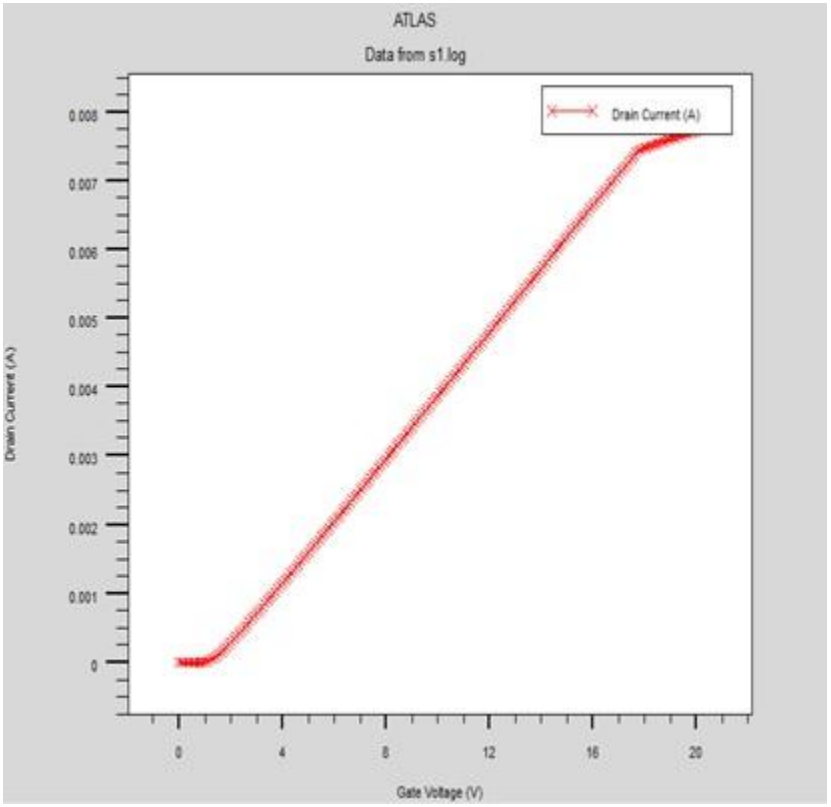

Fig.4.6 I_D/V_{GS} characteristics of device 1for V_{gs} 0-20V and V_{ds} 3V

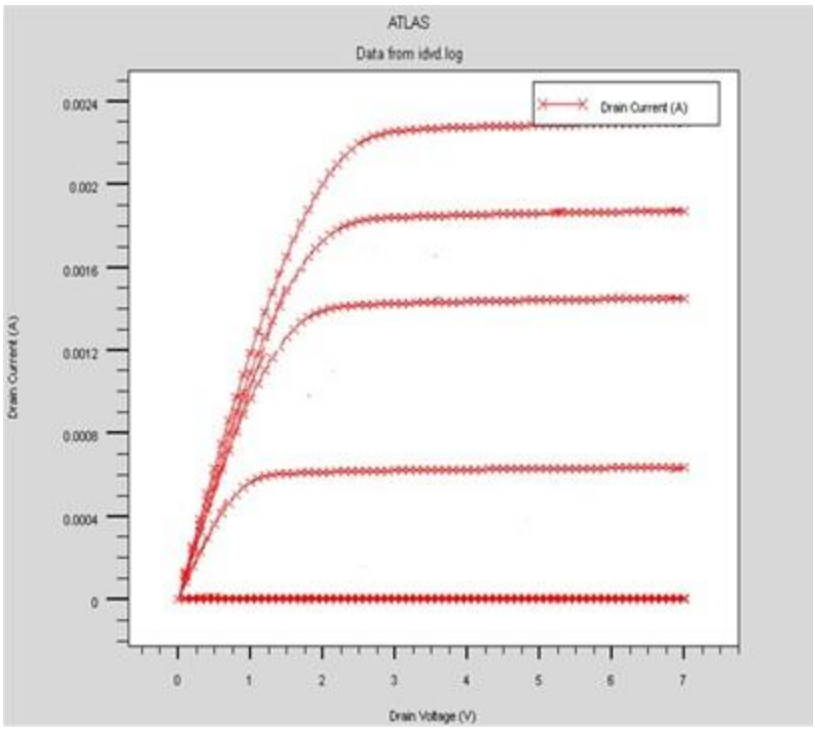

Fig 4.7 I_D/V_{DS} characteristics of device 1 for V_{ds} 0 to 7V and V_{gs} 0 to 5V

DEVICE: 2 dielectric constant 12

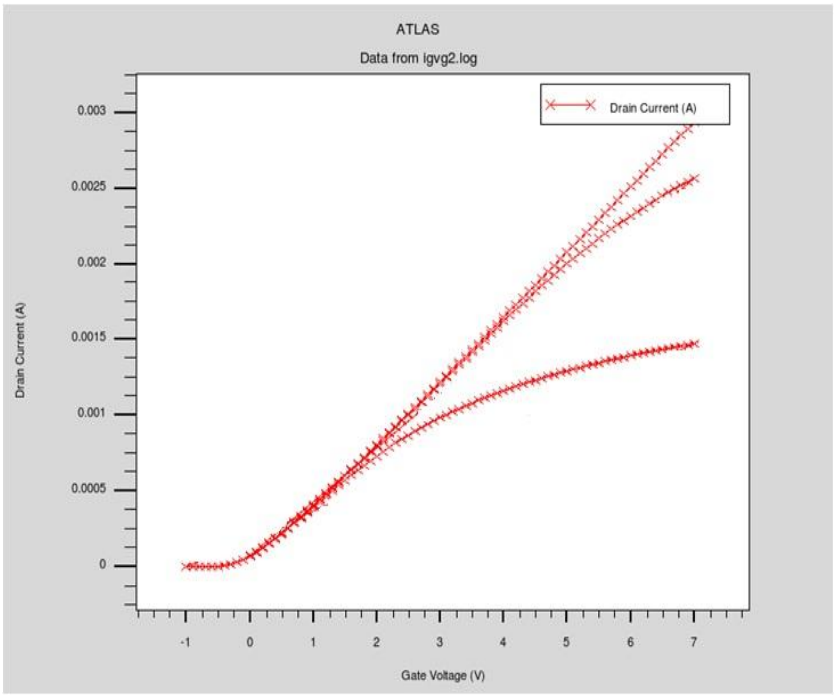

Fig.4.8 I_D/V_{GS} characteristics of device 2 for V_{gs} -1 to 7V and V_{ds} 1to 3V

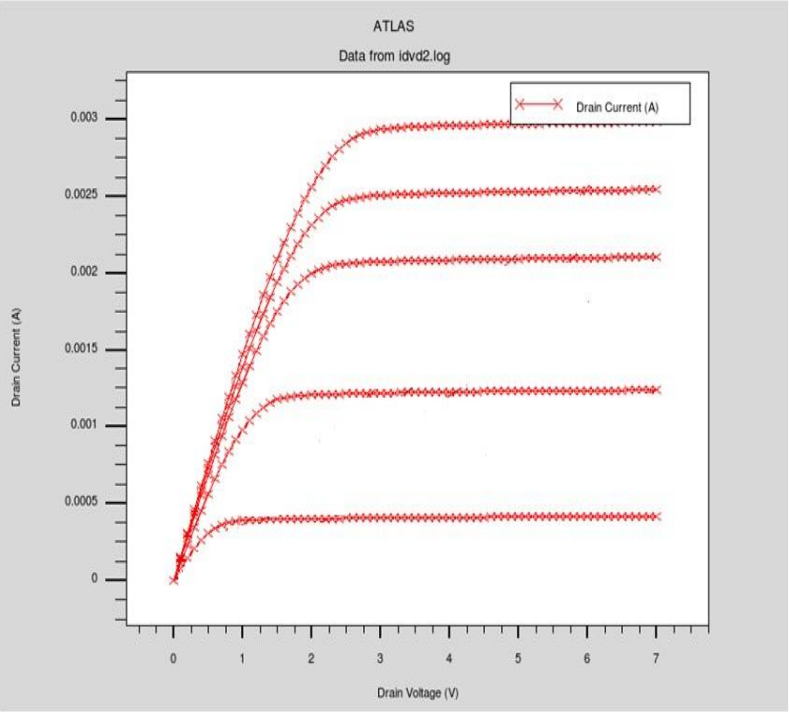

Fig 4.9 I_D/V_{DS} characteristics of device 2 for V_{ds} 0 to 7V and V_{gs} 1 to 5V

DEVICE 3 dielectric constant 27

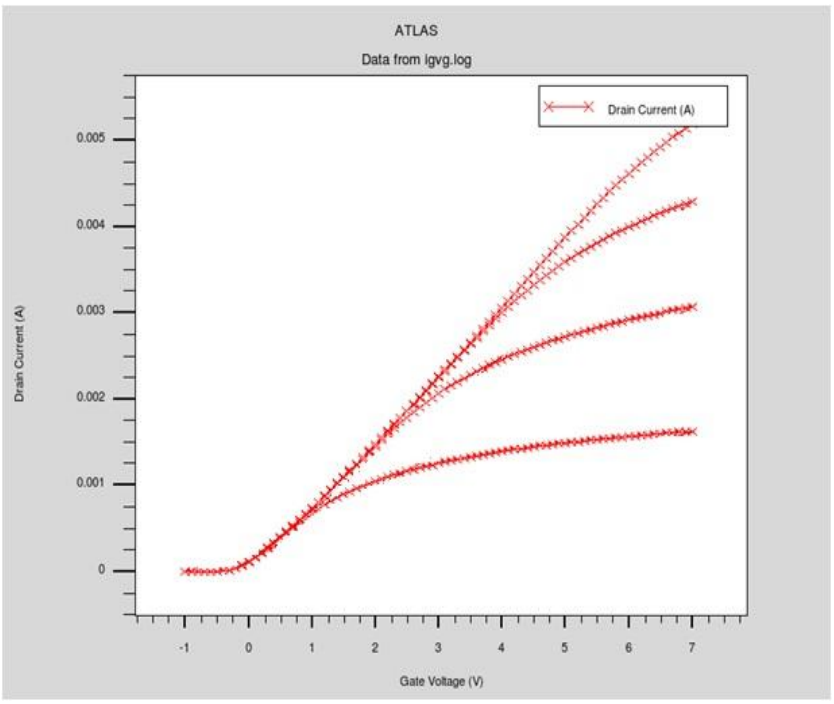

Fig4.10 I_D/V_{GS} characteristics of device 3 for V_{gs} -1 to 7V and V_{ds} 1to 4V

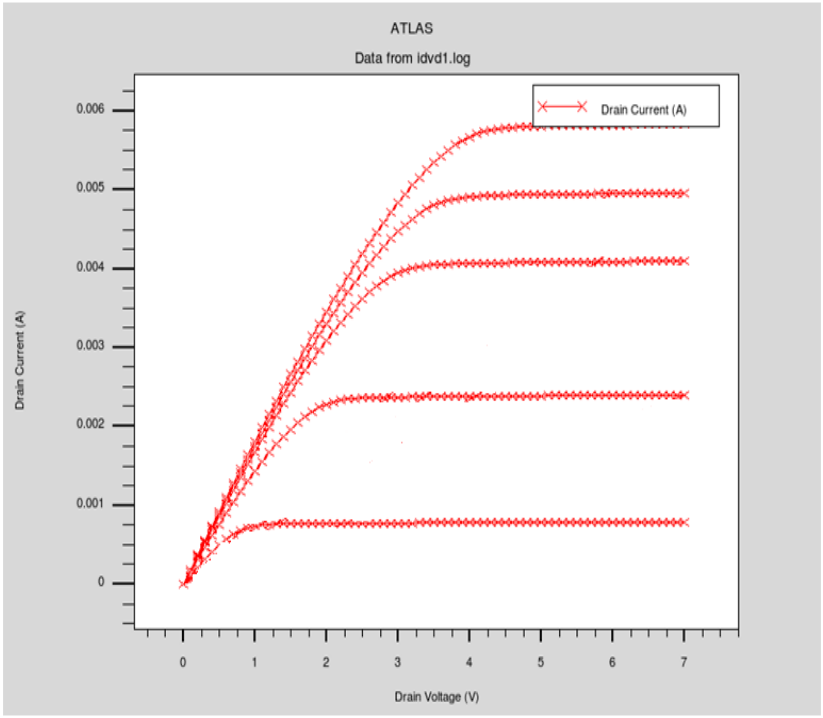

Fig.4.11 I_D/V_{DS} characteristics of device 3 for V_{ds} 0 to 7V and V_{gs} 1 to 5V

DEVICE 4 dielectric constant k = 27

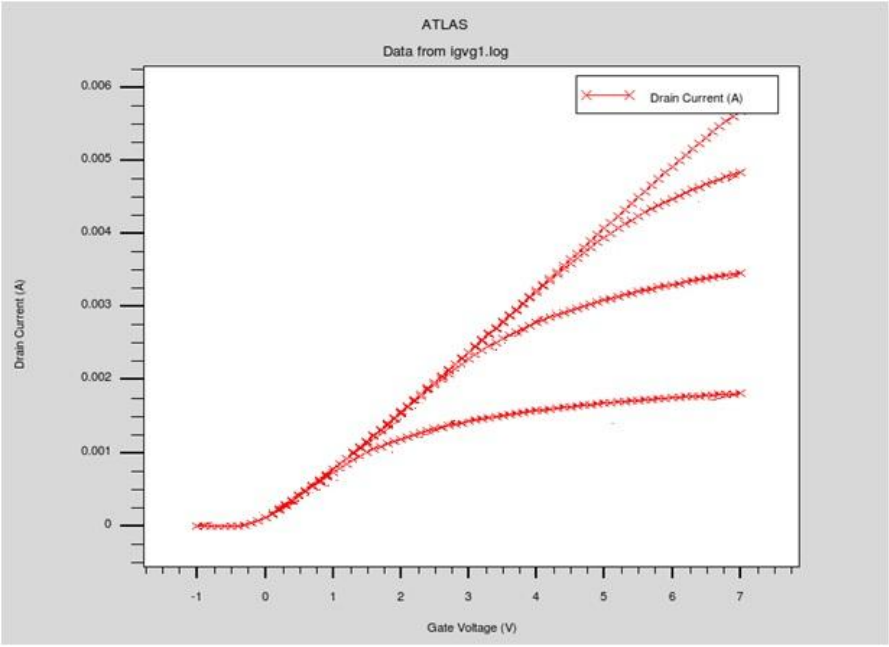

Fig 4.12 I_D/V_{GS} characteristics of device 4 for V_{gs} -1 to 7V and V_{ds} 1to 4V

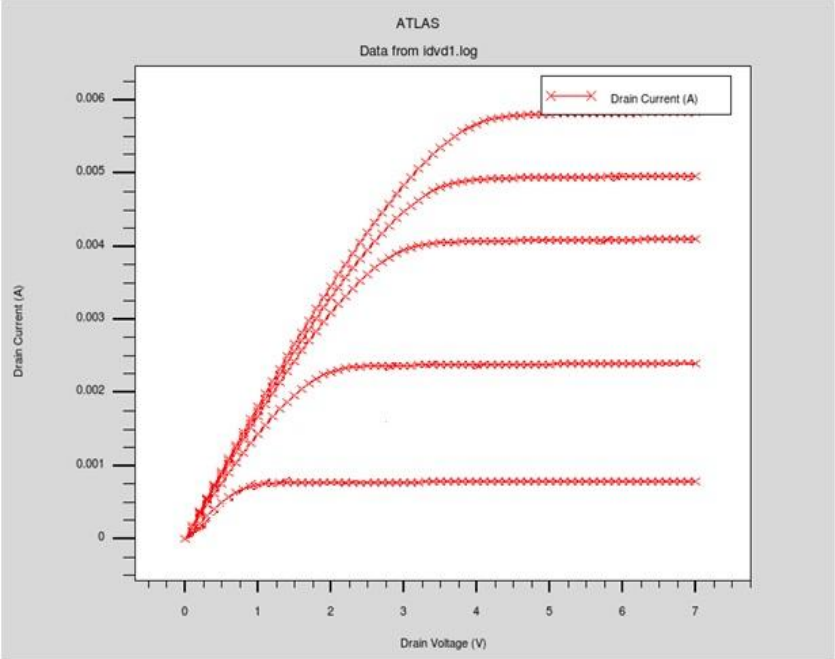

Fig 4.13 I_D/V_{DS} characteristics of device 4 for V_{ds} 0 to 7V and V_{gs} 1 to 5V

Tables below show the parameter extracted from the above input output and transfer characteristics graphs. These parameters are used for comparing the performance of the device.

Table 4.9 parameter calculated for high k dielectric (k =12)

PARAMETERS	DEVICE 1	DEVICE 2
$\mathbf{I_{on/off}}$	10^7	10^9
$\mathbf{\mu_{EF}}$	$19.2cm^2V^{-1}sec^{-1}$	$18.56cm^2V^{-1}sec^{-1}$

Table 4.10 parameter calculated for Ta_2O_5 dielectric

PARAMETERS	DEVICE 3	DEVICE 4
$\mathbf{I_{on/off}}$	10^8	$4.99X10^9$
$\mathbf{\mu_{EF}}$	$29.6cm^2V^{-1}sec^{-1}$	$25.9cm^2V^{-1}sec^{-1}$

Chapter 5

Discussion and Conclusions

5.1 Discussion

Zinc oxide is selected as the material of semiconducting layer because of its suitable properties like insensitivity towards the visible light, high work function and mobility of charge carrier makes it suitable material for semiconducting layer. The two dielectric materials were selected because of large value of dielectric constant which results in large drain to source current as drain current is directly proportional to C_i both in saturation and linear region hence makes device suitable for high performance application. Aluminum is used to decrease the contact resistance. And polymer based substrate is used to provide flexibility to the transistor which further increase the range of application were it can be used therefore a zinc oxide based thin film transistor with high drain to source current ratio, high field effect mobility and low threshold voltage which is suitable for high speed display application is designed.

In this work a thin film transistor with bottom gate staggered architecture is designed on a PET substrate gate is made up of aluminum over gate dielectric layer is deposited. In this work two dielectric material one with dielectric constant value 12 and another with dielectric material value 25 is used it can be seen in the result with increase in value of dielectric constant drain on to off current ratio increased along with the mobility of charge carrier in the channel.

For different thickness of semiconductor layer simulation is performed it can be seen in the results that with decrease in thickness leakage current decreases because with decrease in thickness charge carrier which are stored in the layer also decreased. Reduction of leakage current results in increase of drain on to off current ratio. A high on to off current ratio is suitable for high performance application.

5.2 Conclusion

A thin film transistor with high mobility and high drain current on to off ratio is obtained for a channel length of 3nm. This simulation results shows that with increase in dielectric constant value drain current is increased and a semiconducting layer thickness also has impact on leakage current which also have impact on drain current ratio. Mobility of device is also affected by the dielectric material and thickness of channel layer. Therefore this device is suitable for display application or digital circuit application.

5.3 Future Prospects

The above transistor can be used in various applications of display electronics like switches for each pixel in AMLCD and can also be used in digital application for gate design like NAND, NOR and NOT gate because of the high mobility and large current ration. Performance of this device is further improved by using amorphous Indium Gallium ZnO semiconducting layer.

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PART B: Design and Verification of Bridges Based on AXI, APB, and OCP using System Verilog

Chapter 1

Introduction

1.1 Motivation

In this era of growing chip size and increasing design complexities resulted in very complex ICs. A large number of components are integrated on chip. SoCs are mostly heterogeneous. They include a large number of programmable components for example, digital signal processor cores, application-specific intellectual property cores, on chip memory and I/O devices. SoC is an IC that can perform approximately all the function that are performed by complete electronic system. On chip communication between different IPs is one of the major challenges that are faced by SoC technology due to rapid increase in operation frequencies a fast and reliable bus communication architecture is required. the efficiency of bus architecture has a major influence on the performance of SoC design. IPs used in SoCs is designed with different interfaces based on different communication protocol. Integrating such cores in SoC requires communication between these different protocols , therefore bridges are required to convert different protocols into one standard protocol that can be used by the bus on chip for communicating with all the IPs.

AMBA from ARM is widely used for on chip bus architecture. It is beneficial to convert IPs based on different communication protocols to AXI or APB or other AMBA bus protocol. Open core protocol is one of the most flexible protocols and is most widely used to design IPs because it is easy to convert or make it compatible with other protocol because of the wide range of functionality and flexibility offered by it.

In this report in the first section protocol specification of AXI 4, OCP1.0, OCP2.2 and APB 3 are described. In second section features and micro architecture of the four bridges between OCP2.2 to AXI4, OCP1 to AXI4, OCP1 to OCP2, OCP1 to APB3 are given in detail.

RTL coding is done using system verilog. As system verilog provides various features like interfaces, packages etc. which can be used in the design and saves designer effort of re- writing the redundant information. Using interface provide the benefit of connecting different design unit easily. More over design problems like designing a latch instead of flip flop can be easily avoided using system verilog. It provides compatibility with the verification environment which is mostly in system verilog only.

1.2 Thesis Outline

The thesis is organized as follows:

Chapter2 this chapter is consist of protocol specification of OCP2, OCP1, AXI 4, and APB3. Architecture of the protocols and detail signal description is given in this chapter.

Chapter 3 this chapter is comprised of architecture and features of the designed bridges.

Chapter 4 this chapter includes result and conclusion.

Chapter 2

Protocol specification

2.1 AXI 4

ARM's Advanced Microcontroller Bus Architecture (AMBA) is a worldwide accepted standard for on chip bus interconnect specification. To facilitate management of functional block and connections between them, system bus is required so that all units, controllers, multi- processors and any number of peripherals can communicate with each other on the same chip. Usage of AMBA is not just limited to system on chip, it is commonly used in parts of system on chip like application processor which are the part of television and smart phones, ASIC and microcontroller.

In 1996 ARM introduces Advanced Microcontroller Bus Architecture. In starting it introduced two bus system Advanced Peripheral Bus (APB) and Advanced system Bus (ASB) basically used in low performance application system. High performance AHB bus was introduced in the second version in 1999. To achieve a further higher performance Advanced Xtensible Interface (AXI) was introduced in 2003. Now AXI is used in almost all high performance system. In 2010 AXI 4 was introduces o achieve even higher functionality.

The AMBA AXI4 protocol supports high-performance, high-frequency system designs.

The AXI protocol:
• is suitable for high-bandwidth and low-latency designs
• provides high-frequency operation without using complex bridges
• meets the interface requirements of a wide range of components
• is suitable for memory controllers with high initial access latency
• provides flexibility in the implementation of interconnect architectures
• is backward-compatible with existing AHB and APB interfaces.

The key features of the AXI protocol are:
• separate address/control and data phases
• support for unaligned data transfers, using byte strobes
• uses burst-based transactions with only the start address issued
• separate read and write data channels, that can provide low-cost *Direct Memory Access* (DMA)
• support for issuing multiple outstanding addresses
• support for out-of-order transaction completion
• permits easy addition of register stages to provide timing closure.
The AXI protocol includes the optional extensions that cover signaling for low-power operation.

2.1.1AXI ARCHITECTURE

It has five independent channels. Out of five three channels are for write transactions and two channels are for read transaction. All the channels are independent from each other.

The AXI protocol is burst-based and defines the following independent transaction channels:
• read address
• read data
• write address
• write data
• write response.

An address channel carries control information that describes the nature of the data to be transferred. The data is transferred between master and slave using either:

• A write data channel to transfer data from the master to the slave. In a write transaction, the slave uses the write response channel to signal the completion of the transfer to the master.
• A read data channel to transfer data from the slave to the master.

The AXI protocol:
• permits address information to be issued ahead of the actual data transfer
• supports multiple outstanding transactions
• supports out-of-order completion of transactions.

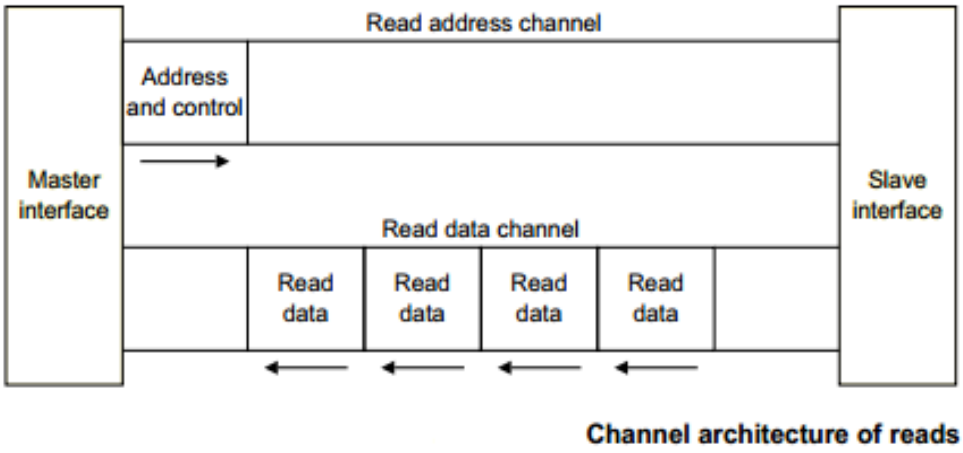

Fig.2.1. read channel architecture

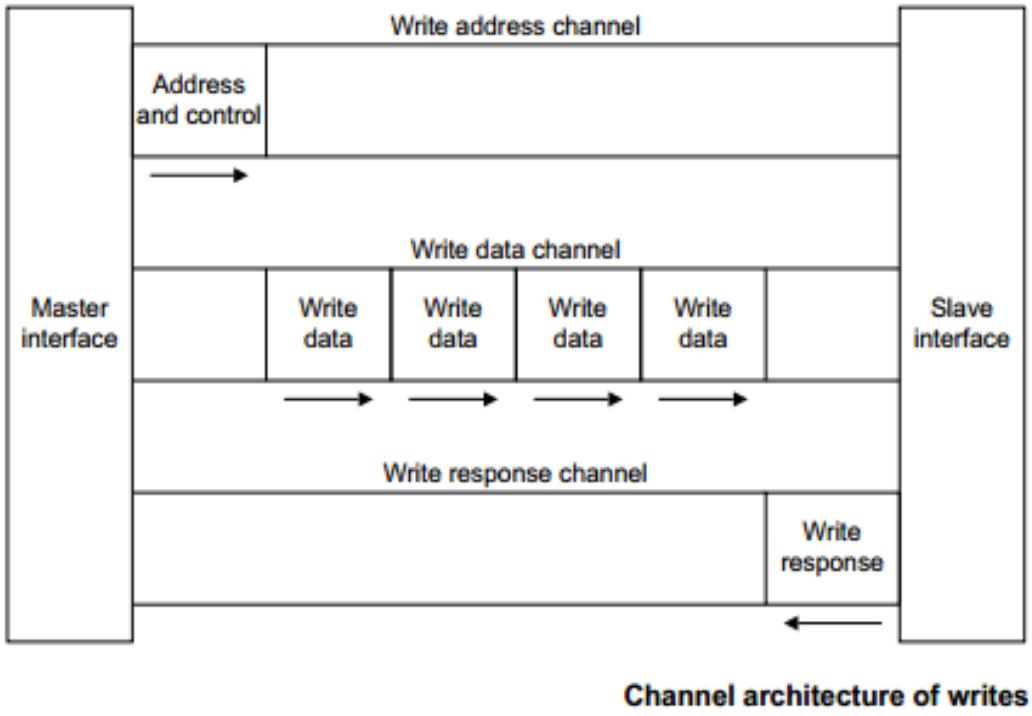

Fig 2.2 writes channel architecture

2.1.2 Channel Description

1. Read address channel: it consist of two handshake signals ARVALID and ARREADY. ARVALID indicates that a valid address and command information is present on the bus, ARREADY indicates that whether the slave is ready to accept the valid information.

2. Read data channel: it consist of two handshake signals RVALID and RREADY. This channel consists of both read data and read response. RVALID indicates the that a valid response and read data is present on the bus , RREADY indicates that whether the master is ready to accept that data from the slave.

3. Write address channel: it consist of two handshake signals AWVALID and AWREADY. AWVALID indicates that a valid address and command information is present on the bus, AWREADY indicates that whether the slave is ready to accept the valid information.

4. Write data channel: it consist of two handshake signals WVALID and WREADY. WVALID indicates presence of valid data on the bus. WREADY indicates that whether the slave is ready to accept the data.

5. Write response channel: it consist of two handshake signals BVALID and BREADY. BVALID indicates that a valid response is present on the bus for the write transaction. BREADY indicates that whether the master is ready to accept the valid response from the slave.

All the channels are independent of one another. Simultaneously we can give read and write command as there are separate and independent channels , similarly read and write data and response can be received and transmitted simultaneously and independently. A response signal for a particular command indicates completion of transfer for that command. AXI supports 8 , 16 ,32,128 512.1024 bit wide data bus.

2.1.3 Register Slices

These are the delay element inserted in different channels. As each channel is independent and transfers information in only one direction. We can use this delay element to resolve any time mismatch issue or to connect and high speed device with a low speed device. It is basically a tradeoff between latency and frequency of operation.

2.1.4 Signal Description

Table 2.1 Signals present in write channel

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	ACLK	1bit	Clock signal. it is global signal
2.	ARESETn	1bit	Reset signal. It is also global signal and it is active low
3.	AWID	configurable	ID for write address channel. It is tag for identification of a command.
4.	AWADDR	32bits	Write address. It gives the initial address of the write transaction.
5.	AWLEN	7bits	Burst length. It gives the exact number of beats in the burst
6.	AWSIZE	3bits	Burst Size. It gives the size of each transfer in the burst.
7.	AWBURST	2bits	Burst type. It gives the information how the next address for each transfer of a particular burst length will be calculated.
8.	AWCACHE	4bits	Memory type. It indicates how transactions are allowed to progress in the system
9.	AWPROT	3bits	Protection type. This signal indicates the privilege and security level of the transaction, and whether the

			transaction is a data access or an instruction access
10.	AWQOS	configurable	Quality of service
11.	AWVALID	1bit	Write address valid. This signal indicates that the channel is signaling valid write address and control information
12.	AWREADY	1bit	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals.

Table 2.2Signals present in Write data channel

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	WID	configurable	Write ID tag. Not supported in AXI4. But was supported in previous versions
2.	WDATA	64/128/256/512bits	Write data corresponding to the valid ID
3.	WSTRB	8/16/32/64bits	This signal indicates which byte lanes hold valid data. There is one write strobe for each 8 bit of the write data bus.
4.	WLAST	1bit	This signal indicates the last transfer in write burst
5.	WVALID	1bit	This signal indicates that write data and strobes are valid.
6.	WREADY	1bit	This signal indicates that slave is ready to accept the data

Table 2.3 Signals present in write response channel

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	BID	Configurable	Slave response tag ID. This signal indicates ID of write response
2.	BRESP	2bits	Write response. This signal indicates the status of the write transaction.
3.	BVALID	1bit	This signal indicates that a valid write response is present on the response channel.
4.	BREADY	1bit	This signal indicates that the master is ready to accept the write response

Table 2.4 Signals present in Read address channel

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	ARID	configurable	This is the ID associated with read transaction in the read address channel
2.	ARADDR	32bits	This is the initial address for read transaction
3.	ARLEN	7bits	Burst length. This signal indicates the exact number of transfers in the burst.
4.	ARSIZE	3bits	This indicates size of each transfer in the burst.
5.	ARBURST	2bits	Indicates the burst type of the transaction eg. INCR, WRAP
6.	ARCACHE	4bits	This signal indicates how transactions are required to progress through the system.
7.	ARPROT	3bits	This signal indicates the privilege and security level of the transaction
8.	ARQOS	configurable	Quality of service. QoS identifier sent for each read transaction
9.	ARVALID	1bit	This signal indicates that channel is signaling valid address and control information
10.	AAREADY	1bit	This signal indicates that slave is ready to accept the command.

Table 2.5 Signals present in read response channel

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	RID	configurable	This signal is ID for read response channel generated by slave same as the read request
2.	RDATA	64/128/256/512bits	Read data. Data transferred by slave corresponding to the request.
3.	RRESP	2bits	Read response. Status of read transfer
4.	RLAST	1bit	Indicates the last response of a transaction
5.	RVALID	1bit	Indicates that the data and response present on the data bus are valid for a read transaction
6.	RREADY	1bit	Indicates that master is ready to accept the response from the slave.

2.2 OCP2.2

In system on chip for establishing communication between different IP cores which are the functional unit the open core protocol interface can be used. The advantage of using open core protocol is that without even sacrificing high performance access to on chip bus interconnect it provides independence from system bus protocol. By using open core protocol to design interface boundary reusable IP cores can be developed without taking into consideration the final target system. As IP core has a wide range of functionality interface requirement and performance. Full spectrum of interface protocol cannot be addressed by fixed definition interface protocol. Complexity of the interface further increase as it has to support test nad verification environment. Open core protocol defines a highly configurable interface to address this range of specification.

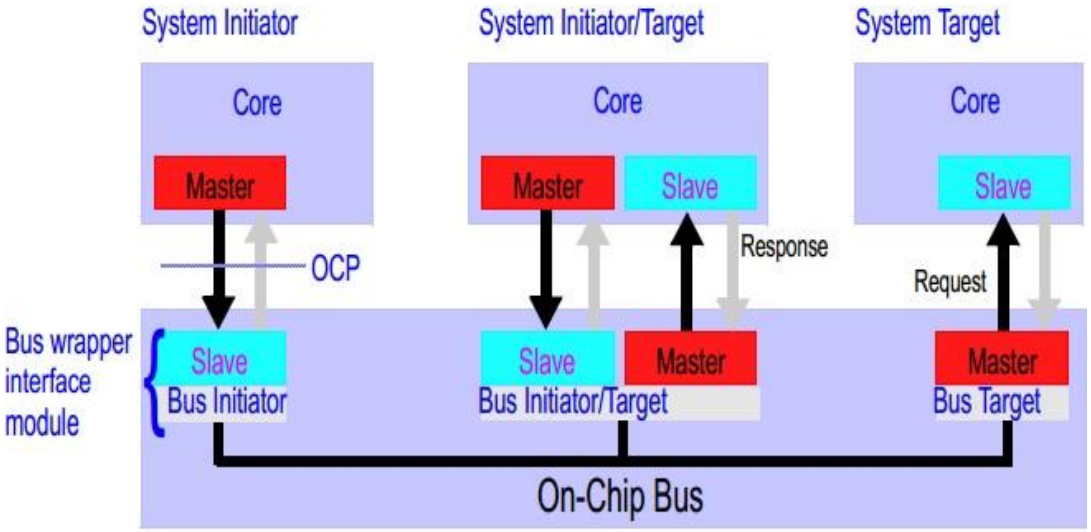

Fig 2.3 shows the connection between bridge with on chip bus initiator system and target system

Point-to-Point Synchronous Interface

In open core protocol to simplify general comprehension, timing analysis and physical design it is made up of only uni directional signals which are sampled and driven with respect to positive edge of the clock. There are no multi cycle timing paths with respect to the OCP clock and OCP is synchronous with OCP clock (except reset signal). Except clock signal all signal are strictly point to point.

Bus Independence

An IP core using open core protocol can be interfaced with any bus. There is one test for all bus independent interfaces are to make a direct connection between a slave and a master without any interleaving on chip bus. This testing method helps to resolves other issues not just drives the specifications towards a fully symmetric interface. One of the best examples is slave selection methods vary greatly among on chip buses. Some generate independent signal for slave selection other use decoder circuits. These complexities should be hidden from core. Open core protocol based slaves receives this device or slave selection information in the basic command field.

Commands

There are two basic commands, Read and Write and five command extensions. The WriteNonPost and Broadcast commands have semantics thatare similar to the Write command. A WriteNonPost explicitly instructs the slave not to post a write. For the Broadcast command, the master indicates that it is attempting to write to several or all remote target devices that are connected on the other side of the slave. As such, Broadcast is typically useful only for slaves that are in turn a master on another communication medium (such as an attached bus).The other command extensions, ReadExclusive, ReadLinked and WriteConditional, are used for synchronization between system initiators. ReadExclusive is paired with Write or WriteNonPost, and has blocking semantics. ReadLinked, used in conjunction with WriteConditional has non-blocking (lazy) semantics. These synchronization primitives correspond to those available natively in the instruction sets of different processors.

Address/Data

For efficient area implementation it is necessary to tune the open core protocol data and address widths as shared on chip address and data buses are of wide widths. Only relevant bits of address which are significant for the core should pass from open core protocol to slave device. Ocp has flat address space and is composed of octets (8 bit bytes). Mostly IP cores have data field width larger than the 8 bit bytes to improve the transfer efficiency. Open core protocol allows multiple bytes to be transferred together hence it supports configurable data width. In OCP data width is referred as the word size.

Pipelining

Pipelining of transfers is allowed in OCP. To provide support to this feature, write data is delayed and the return of read data is also delayed after the acceptance of command.

Response

In OCP request phase are separated from response phase. Slave can accept the request from master on one cycle and can give response in another cycle or same cycle. This division of response from request phase is necessary to support pipelining feature. Write command can be

handled in two ways one is to finish it immediately without any response or to wait for the response.

Burst

Burst transfer is essential for many IP cores to provide high transfer efficiency this version of OCP supports annotation of transfers with burst information. There are two type of burst transfer one is single request multiple data transfer other is multiple request multiple data transfer. In single request is sent to slave carrying the information for entire burst transfer. In MRMD for each data byte command information is transferred.

Tags

tags are necessary to support out of order response. When tag IDs are same responses are returned in order when different master can accept them in any order. Similarly for write channel data can be committed in any order or out of order commit of write data. Similar to response channel if tag IDs are same write are committed in order if different tag iDS then it can be committed in any order.

2.2.1 CHANNEL DESCRIPTION

There are three channels or signal groups which are request groups, response group and data handshake group. These groups are independent of each other but there is ordering restriction on each group. Signals in single group must be valid at the same time.

- Request group signals are not valid when IDLE command is present on the MCmd signal. For all other command this group is valid.
- Whenever response other than NULL is present on the SResp signal response becomes invalid. For any other response it becomes valid.
- Data handshake group becomes valid when MDataValid signal becomes high otherwise data present on MData field is not valid.

The accept signal associated with a signal group is valid only when that group is valid.

- The SCmdAccept signal is taken into consideration only when command signal on MCmd filed is not IDLE. Even the high value of SCmdAccept signal is not considered in that case.
- Similarly for response channel when response is not NULL then only value of MResponseAccept is taken into consideration.
- When MDataValid signal is high then only value of SDataAccept in taken into consideration.

In OCP for each transfer first request phase is activated after that data handshake phase arrives which must be followed by request phase. These are the following constraints that must be followed.

- Request phase starts first after that handshake phase starts, handshake phase can also start in the same clock cycle in which the request phase started.
- Request phase ends first with SCmdAccept signal after that the data phase associated with request can end or it can end with the request phase only but cannot end before request phase.
- Similarly response phase can begin in the same clock cycle in which request phase begin with the request phase but cannot end before the request phase ends.
- Response phase can end in similar clock cycle as request phase but cant end before request phase is completed.
- If there is a datahandshake phase and a response phase, the response phase cannot begin before the associated datahandshake phase (or last datahandshake phase for single request/multiple data bursts) begins, but can begin in the same OCP clock cycle.
- If there is a datahandshake phase and a response phase, the response phase cannot end before the associated datahandshake phase (or last datahandshake phase for single request/multiple data bursts) ends, but can end in the same OCP clock cycle.

Phase Ordering Between Transfers

When tag IDs are not used ordering of different phase of different transfer is determined by the order of their request phases. There are certain rules that shoul be followed.

- for request phase there is one set of signals, so if two transfers has to start together there response phases has to arrive first but there is only one set of wire which is not possible therefore before a the request phase for new transfer arrive previous transfer phase must be completed.

- Similarly for data channel there is only one set of handshake phase signal therefore to new handshake phase to start previous one must gets complete. Therefore after request is accepted then only data handshake phase begins so similar order is followed by datahanshake phase. For SRID instruction there are multiple data handshake phases.

- Same goes with response phase it should also follow the same order followed by the request phase. For SRID type of read command there are multiple response phases for a single command.
- When order established by previous rules is not valid. Then effect of transfers which are specifying same address should remain same irrespective of the order in which they are executed and there should not be any phase overlap between those two transfers.

- These rules are necessary so that hazards which occur by read and write transfer are predictable. Suppose if a read command arrives after the write command is accepted now the handshake phase of write command should be completed first after that its response phase than only response of read can start if this sequence is not followed the master will not be able to read the latest value of data present at that location.

2.2.2 Signal Description

Table 2.6 Basic signals of ocp2

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	Clk	1bit	Input clock signal for the OCP clock. The rising edge of the OCP clock is defined as a rising edge of Clk that samples the asserted EnableClk.
2.	EnableClk	1bit	EnableClk indicates which rising edges of Clk are the rising edges of the OCP clock,
3.	MAddr	configurable	The Transfer address, MAddr specifies the slave-dependent address of the resource targeted by the current transfer.
4.	MCmd	3bits	Transfer command. This signal indicates the type of OCP transfer the master is requesting
5.	MData	Configurable	Write data. This field carries the write data from the master to the slave.
6.	MDataValid	1bit	Write data valid. When set to 1, this bit indicates that the data on the MData field is valid.
7.	MRespAccept	1bit	The master indicates that it accepts the current response from the slave with a value of 1 on the MRespAccept signal.
8.	SCmdAccept	1bit	A value of 1 on the SCmdAccept signal indicates that the slave accepts the master's transfer request.
9.	SData	Configurable	This field carries the requested read data from the slave to the master
10.	SDataAccept	1bit	The slave indicates that it accepts pipelined write data from the master with a value of 1 on SDataAccept.
11.	SResp	2bits	Response field from the slave to a transfer request from the master.

Table 2.7 Basic Signal Extension of ocp2

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	MByteEn	Configurable	Byte enables. This field indicates which bytes within the OCP word are part of the current transfer.
2.	MDataByteEn	Configurable	Write byte enables. This field indicates which bytes within the OCP word are part of the current write transfer.
3.	MBurstLength	Configurable	The number of transfers in a burst. For precise bursts, the value indicates the total number of transfers in the burst, and is constant throughout the burst
4.	MBurstSeq	3bits	This field indicates the sequence of addresses for requests in a burst. To configure this field into the OCP, use the burstseq parameter.
5.	MBurstSingleReq	1bit	The burst has a single request with multiple data transfers. This field indicates whether the burst has a request per data transfer, or a single request for all data transfers.
6.	MDataLast	1bit	Last write data in a burst. This field indicates whether the current write data transfer is the last in a burst
7.	SRespLast	1bit	Last response in a burst. This field indicates whether the current response is the last in this burst

2.3 OCP 1.0

In system on chip for establishing communication between different IP cores which are the functional unit the open core protocol interface can be used. The advantage of using open core protocol is that without even sacrificing high performance access to on chip bus interconnect it provides independence from system bus protocol. By using open core protocol to design interface boundary reusable IP cores can be developed without taking into consideration the final target system. As IP core has a wide range of functionality interface requirement and performance. Full spectrum of interface protocol cannot be addressed by fixed definition interface protocol. Complexity of the interface further increase as it has to support test nad verification environment. Open core protocol defines a highly configurable interface to address this range of specification.

Point-to-Point Synchronous Interface

In open core protocol to simplify general comprehension, timing analysis and physical design it is made up of only uni directional signals which are sampled and driven with respect to positive

edge of the clock. There are no multi cycle timing paths with respect to the OCP clock and OCP is synchronous with OCP clock (except reset signal). Except clock signal all signal are strictly point to point.

Bus Independence

An IP core using open core protocol can be interfaced with any bus. There is one test for all bus independent interfaces are to make a direct connection between a slave and a master without any interleaving on chip bus. This testing method helps to resolves other issues not just drives the specifications towards a fully symmetric interface. One of the best examples is slave selection methods vary greatly among on chip buses. Some generate independent signal for slave selection other use decoder circuits. These complexities should be hidden from core. Open core protocol based slaves receives this device or slave selection information in the basic command field.

Commands

There are two basic commands write and read. There are two more type of write command one is WriteNonPost and broadcast. And there is one more type of read command readExclusive. A simple write command can be without response or with response (nonposted) and there is separate WriteNonPosted in which response is compulsory. In case of broadcast command master indicates that it is writing the same to multiple slaves. As such, Broadcast is typically useful only for slaves that are in turn a master on another communication medium (such as an attached bus). Readexclusive is used for synchronization between system initiators. ReadExclusive is followed by write or writeNonPost command. It has blocking semantics.

Address/Data

For efficient area implementation it is necessary to tune the open core protocol data and address widths as shared on chip address and data buses are of wide widths. Only relevant bits of address which are significant for the core should pass from open core protocol to slave device. Ocp has flat address space and is composed of octets (8 bit bytes). Mostly IP cores have data field width larger than the 8 bit bytes to improve the transfer efficiency. Open core protocol allows multiple bytes to be transferred together hence it supports configurable data width. In OCP data width is referred as the word size. In OCP 1 only 128 bit maximum data bus size is supported.

Pipelining

Pipelining of transfers is allowed in OCP. To provide support to this feature, write data is delayed and the return of read data is also delayed after the acceptance of command.

Response

In OCP request phase are separated from response phase. Slave can accept the request from master on one cycle and can give response in another cycle or same cycle. This division of response from request phase is necessary to support pipelining feature. Write command can be handled in two ways one is to finish it immediately without any response or to wait for the response.

Burst

Burst transfer is essential for many IP cores to provide high transfer efficiency this version of OCP supports annotation of transfers with burst information. There are two type of burst transfer one is single request multiple data transfer other is multiple request multiple data transfer. In single request is sent to slave carrying the information for entire burst transfer. In MRMD for each data byte command information is transferred.

2.3.1 CHANNEL DESCRIPTION

There are three channels or signal groups which are request groups, response group and data handshake group. These groups are independent of each other but there is ordering restriction on each group. Signals in single group must be valid at the same time.

- Request group signals are not valid when IDLE command is present on the MCmd signal. For all other command this group is valid.
- Whenever response other than NULL is present on the SResp signal response becomes invalid. For any other response it becomes valid.
- Data handshake group becomes valid when MDataValid signal becomes high otherwise data present on MData field is not Valid.

The accept signal associated with a signal group is valid only when that group is valid.

- The SCmdAccept signal is taken into consideration only when command signal on MCmd filed is not IDLE. Even the high value of SCmdAccept signal is not considered in that case.
- Similarly for response channel when response is not NULL then only value of MResponseAccept is taken into consideration.
- When MDataValid signal is high then only value of SDataAccept in taken into consideration.

In OCP for each transfer first request phase is activated after that data handshake phase arrives which must be followed by request phase. These are the following constraints that must be followed.

- Request phase starts first after that handshake phase starts, handshake phase can also start in the same clock cycle in which the request phase started.

- Request phase ends first with SCmdAccept signal after that the data phase associated with request can end or it can end with the request phase only but cannot end before request phase.
- Similarly response phase can begin in the same clock cycle in which request phase begin with the request phase but cannot end before the request phase ends.
- Response phase can end in similar clock cycle as request phase but cant end before request phase is completed.
- If there is a datahandshake phase and a response phase, the response phase cannot begin before the associated data handshake phase begins, but can begin in the same OCP clock cycle.
- If there is a datahandshake phase and a response phase, the response phase cannot end before the associated datahandshake phase (but can end in the same OCP clock cycle).

2.3.2 Signals Description

Table 2.8 basic signals ocp1

S.NO	SIGNAL	WIDTH	DESCRIPTION
1.	Clk	1bit	Input clock signal for the OCP clock. The rising edge of the OCP clock is defined as a rising edge of Clk that samples the asserted EnableClk.
2.	EnableClk	1bit	EnableClk indicates which rising edges of Clk are the rising edges of the OCP clock,
3.	MAddr	configurable	The Transfer address, MAddr specifies the slave-dependent address of the resource targeted by the current transfer.
4.	MCmd	3bits	Transfer command. This signal indicates the type of OCP transfer the master is requesting
5.	MData	Configurable	Write data. This field carries the write data from the master to the slave.
6.	MRespAccept	1bit	The master indicates that it accepts the current response from the slave with a value of 1 on the MRespAccept signal.
7.	SCmdAccept	1bit	A value of 1 on the SCmdAccept signal indicates that the slave accepts the master's transfer request.
8.	SData	Configurable	This field carries the requested read data from the slave to the master
9.	SDataAccept	1bit	The slave indicates that it accepts pipelined write data from the master with a value of 1 on SDataAccept.
10.	SResp	2bits	Response field from the slave to a transfer request from the master.
11.	MByteEn	Configurable	Byte enables. This field indicates which bytes within the OCP word are part of the current transfer.

12.	MBurst	3bits	This field indicates the sequence of addresses for requests in a burst. And also the length of burst.

2.4 APB 3

Advanced Microcontroller bus architecture (AMBA) has APB, Advanced peripheral Bus to support slow speed slave devices to reduce power consumption and interface complexity. These slow peripheral devices don't require high efficiency interface they doesn't required features like pipelining.

Operation of APB can be explained by three states, state machine.

1. IDLE
2. SETUP
3. ENABLE

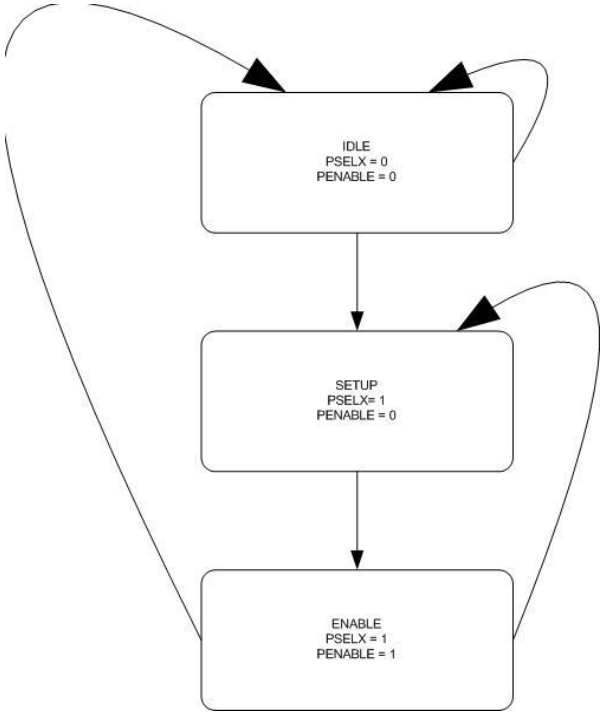

Fig 2.2 state diagram of APB for a transaction

IDLE: This is the default state of the peripheral bus.

SETUP: When a valid command arrives bus moves from IDLE state to SETUP state. In SETUP state a valid PSELx signal is asserted. SETUP state is only once clock cycle long. After SETUP state, state changes to ENABLE state on the next rising edge of clock.

In this state PENABLE is asserted. All the valid signals remain in a stable state during the transition from SETUP to ENABLE state this state also lasts for a signle clock cycle after that bus moves to the SETUP state if there is another valid command is present or it will move to IDLE state when immediate transfer is not required. but if PREADY signal is low ENABLE state is extended to the next cycle only after it becomes high state change will take place.

2.4.1 Signal Description

Table 2.9 signals of abp3

S.NO	SIGNALS	WIDTH	DESCRIPTION
1.	PCLK	1bit	Global signal.
2.	PADDR	32bits	Address given by the master for write or read command.
3.	PWRITE	1 bit	It indicates the type of command. one on this pin indicates write command and a low value indicates read command.
4.	PSEL	1 bit	This signal is generated by bridge by Decoding address for selecting slave.
5.	PENABLE	1 bit	It indicates access phase all control signals remain valid during this phase. Transfer is complete after penable becomes low.
6.	PWDATA	32 bits	Write data.
7.	PRDATA	32 bits	Read data from slave to master.
8.	PREADY	1 bit	Used to extend the access phase. It is driven low by the slave when it is not ready for the transfer.

Chapter 3

Micro architecture of bridges

In this project work 4 bridges are designed based on AMBA AXI and APB protocol and different version of OCP protocol (OCP1 & OCP2.2). System verilog is used for RTL coding.

1. OCP2 TO AXI 4
2. OCP1 TO OCP2
3. OCP1 TO AXI 4
4. OCP1 TO APB 3

3.1OCP2 TO AXI 4 BRIDGE

This bridge coverts the transaction from OCP2 master into AXI 4 transaction for AXI slave. In bridge slave instance of OCP2 is present which accept the command from OCP2 master in OCP protocol format and converts into AXI 4 transaction and on other side master instance of AXI 4 is present in the bridge which sends the transaction to the AXI 4 slave in AXI protocol format.

3.1.1 OCP2 TO AXI 4 BRIDGE BLOCK DIAGRAMS AND MICRO ARCHITECTURE

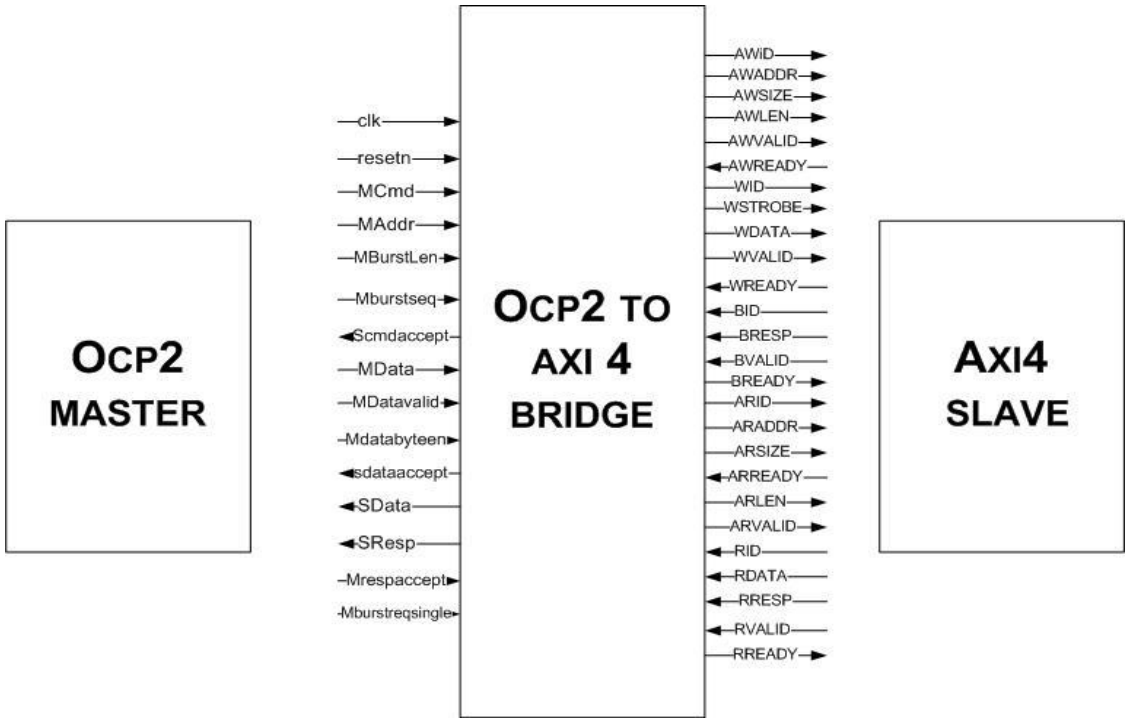

Fig 3.1 architecture of bridge

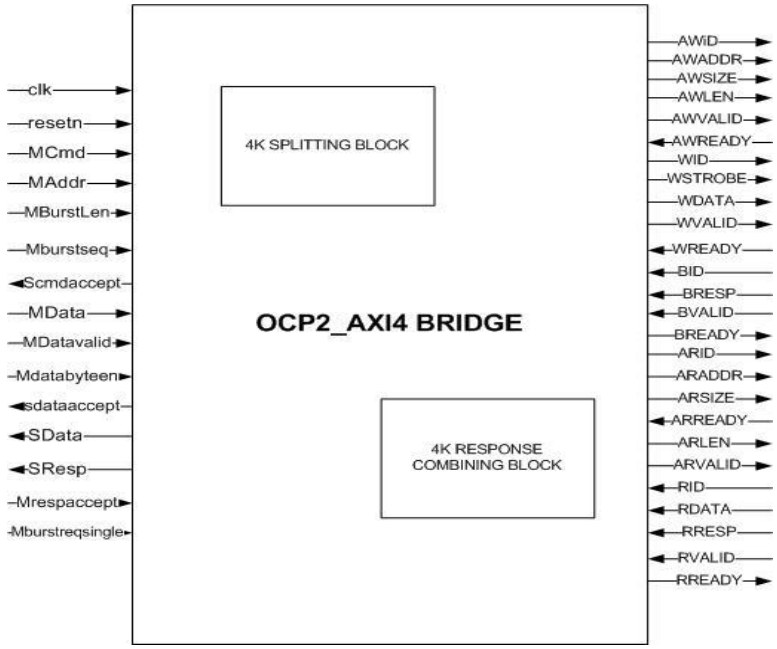

Fig 3.2 micro architecture of bridge

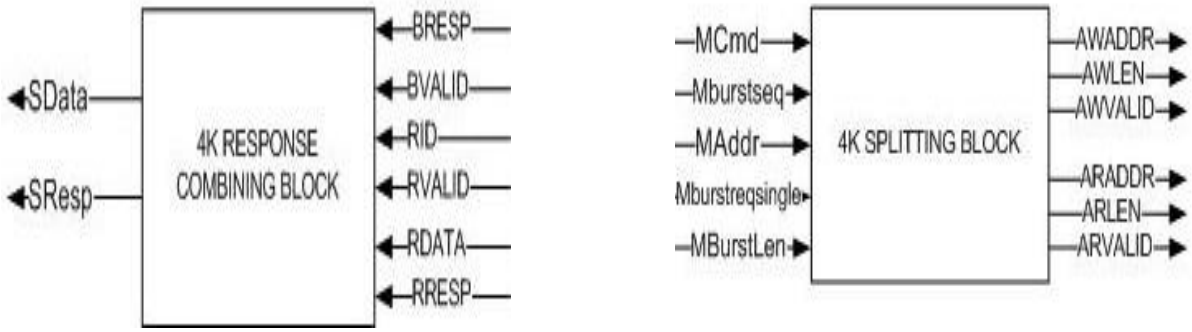

Fig 3.3 block diagram of sub block

3.1.2EXPLANATION OF MICRO ARCHITECTURE

1. There is OCP2 slave instance in the bridge to communicate with OCP2 master and AXI 4 Master instance to communicate with AXI slave.
2. In OCP there is only one channel for command, one for write data and one for response channel.
3. In AXI there are two command channels but there is no signal to indicate write or read type of command. Also there are two response channels.
4. All OCP2 read type commands are given to AXI read channel and OCP2 write commands are given to AXI write channel. Based on the MCmd signal of OCP2.
5. In OCP2 there is no 4KB slave boundary address limitation where as in AXI there is 4KB slave address boundary limitation.

6. It means that no burst in a single command can cross 4KB boundary address range. Therefore a command with burst length crossing 4KB boundary is split into two separate commands with same tag ids.
7. Similarly there are two response channels in AXI where as one response channel in OCP2. As the two response channels of AXI are independent of each other priority is given to write channel response.
8. Responses of split transactions are combined together and then transferred to the OCP2 master.
9. Only a fixed number of outstanding transactions are supported (parameterized) after that master is back pressured by asserting scmdaccept signal low from the bridge.

3.1.3 FEATURES OF THE BRIDGE

1. Support for fixed number of outstanding transaction.
2. Support for out of order response.
3. Tag ids are supported.
4. Single request and multiple data type of commands are generated by ocp2 master.
5. Increment and wrap type of burst are supported.
6. Read and write type commands with response are supported.
7. Minimum word size of 32 bits maximum word size of 512 bits is supported.

3.1.4 SIGNAL MAPPING

Table 3.1 ocp2 to axi4 address channel signal mapping

OCP2	AXI4
MTagID	AWID/ARID
MAddr	AWADDR/ARADDR
MBurstLength	AWLEN/ARLEN
To be calculated	AWSIZE/ARSIZE
MCmd(calculated)	AWVALID/ARVALID
SCmdAccept	AWREADYARREADY
MBurstSeq	AWBURST/ARBURST

Table 3.2 ocp2 to axi4 data channel signal mapping

OCP2	AXI4
MDataTagID	Doesn't exist
MData	WDATA
MDataByteEn	WSTROBE
MDataValid	WVALID
MDataLast	WLAST
SDataAccept	WREADY

Table 3.3 ocp2 to axi4 write & read channel response mapping

OCP2	AXI4
STagID	BID/RID
SResp	BRESP/RRESP
SData	RDATA
SRespLast	RLAST
Calculated (SResp)	BVALID/RVALID
MRespAccept	BREADY/RREADY

3.2 OCP1 TO OCP2 BRIDGE

This bridge coverts the transaction from OCP1 master into OCP2 transaction for OCP2 slave. In bridge slave instance of OCP1 is present which accept the command from OCP1 master in OCP 1protocol format and converts into OCP2 transaction and on other side master instance of OCP2 is present in the bridge which sends the transaction to the OCP2 slave in OCP2 protocol format.

3.2.1 OCP1.0 TO OCP2.2 BRIDGE BLOCK DIAGRAM AND MICRO ARCHITECTURE

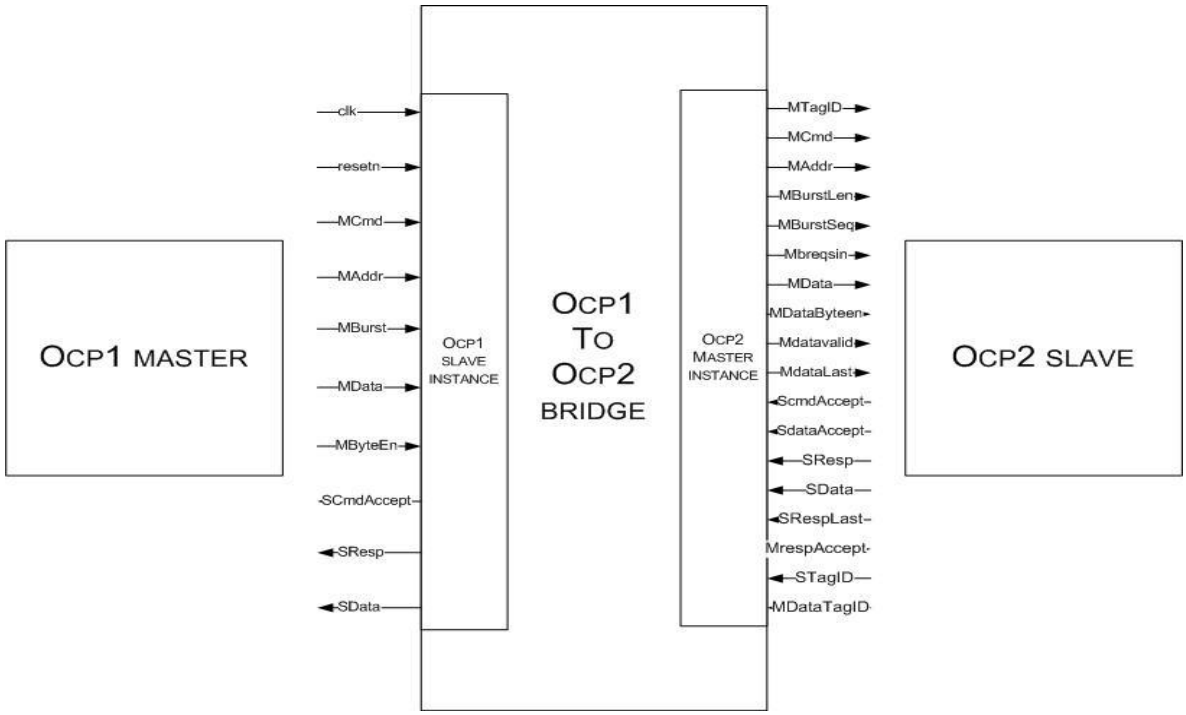

Fig 3.4 architecture of bridge

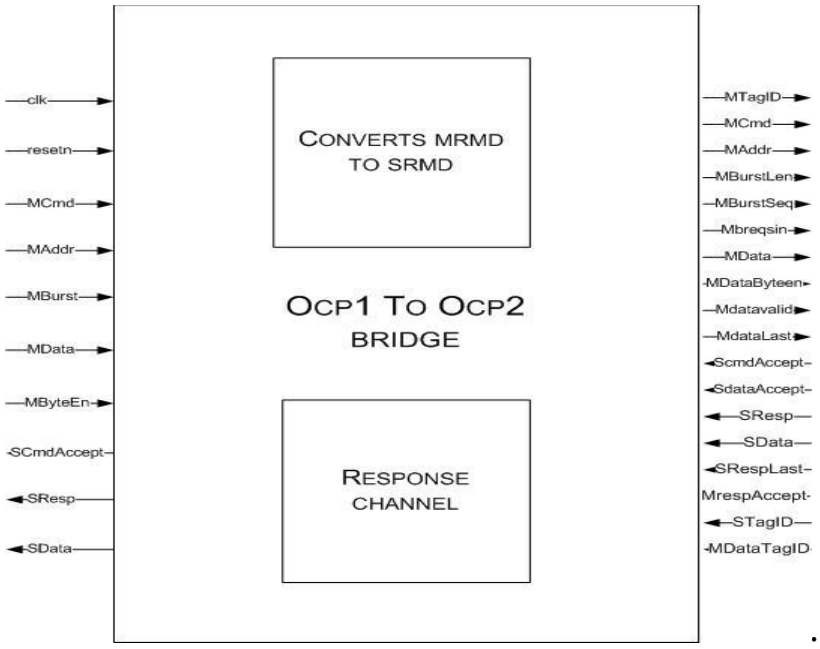

Fig 3.5 micro architecture of bridge

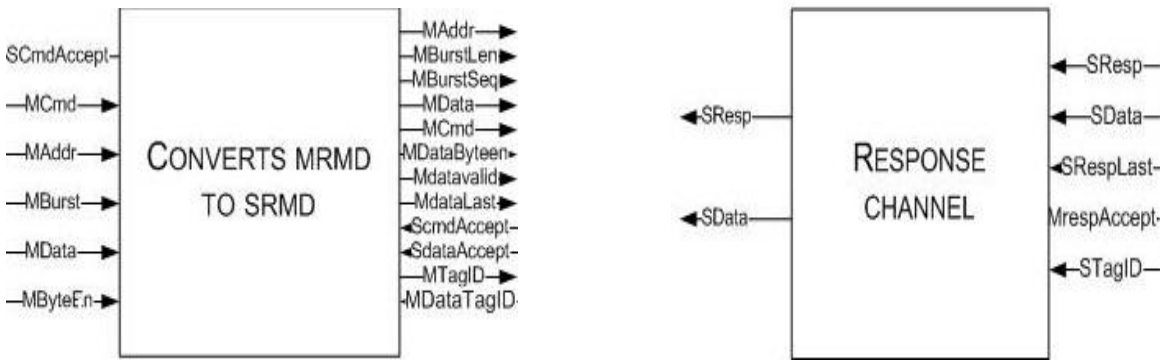

Fig 3.6 block diagram of sub block

3.2.2 EXPLANATION OF MICRO ARCHITECTURE

1. There are two main blocks one for converting multiple request multiple data to single request multiple data.
2. In ocp1 there is only MRMD type of request where as in OCP2 there is SRMD type of request, therefore conversion is required.
3. There is no burst length information in ocp1 mburst signal is used to indicate both length and type of burst therefore length is calculated from mburst signal.
4. Mburstseq is calculated from mburst.
5. In ocp1 there is no Tag Id concept where as in ocp2 tag id is used. In ocp1 response for write channel is not required there needs to discarded
6. To differentiate a read from write response tag IDs are used by bridge.
7. Maintaining order of response and passing only read response. Response channel block is required.

3.2.3 FEATURES OF BRIDGE

1. Outstanding transactions are supported by the bridge
2. Data and command channel of ocp1 are tightly coupled where as on ocp2 side they are independent from each other.
3. Response channel handshake is not used in ocp1 side where as response channel handshake is required on ocp2 side. Bridge takes care of this requirement.
4. Out of order responses are allowed as bridge takes care of maintaining the order and sending only the desired response to the master.
5. Tag ids are generated by the bridge.
6. Only increment type of burst is generated by ocp1.
7. Write without response but read with response is required by the ocp1 master. Where ocp2 side gives response for both read and writes type of transaction.

3.2.4 SIGNAL MAPPING

Table 3.4 basic signal mapping ocp1 to ocp2

OCP1.0	OCP2.2
MCmd	MCmd
MData	MData
MAddr	MAddr
MBurst	MBurstSeq
Calculated	MBurstlength
Generated	MTagID / MDataTagID
Calculated	MdataValid
Calculated	MdataLast
SCmdAccept	SCmdAccept / SDataAccept
SResp	SResp
SData	SData
Generated	MRespAccept
Not required	SRespLast

3.3 OCP1 TO AXI 4 BRIDGE

This bridge coverts the transaction from OCP1 master into AXI 4 transaction for AXI slave. In bridge slave instance of OCP1 is present which accept the command from OCP1 master in OCP 1 protocol format and converts into AXI 4 transaction and on other side master instance of AXI 4 is present in the bridge which sends the transaction to the AXI 4 slave in AXI protocol format.

3.3.1 OCP1 TO AXI 4 BRIDGE BLOCK DIAGRAM AND MICRO ARCHITECTURE

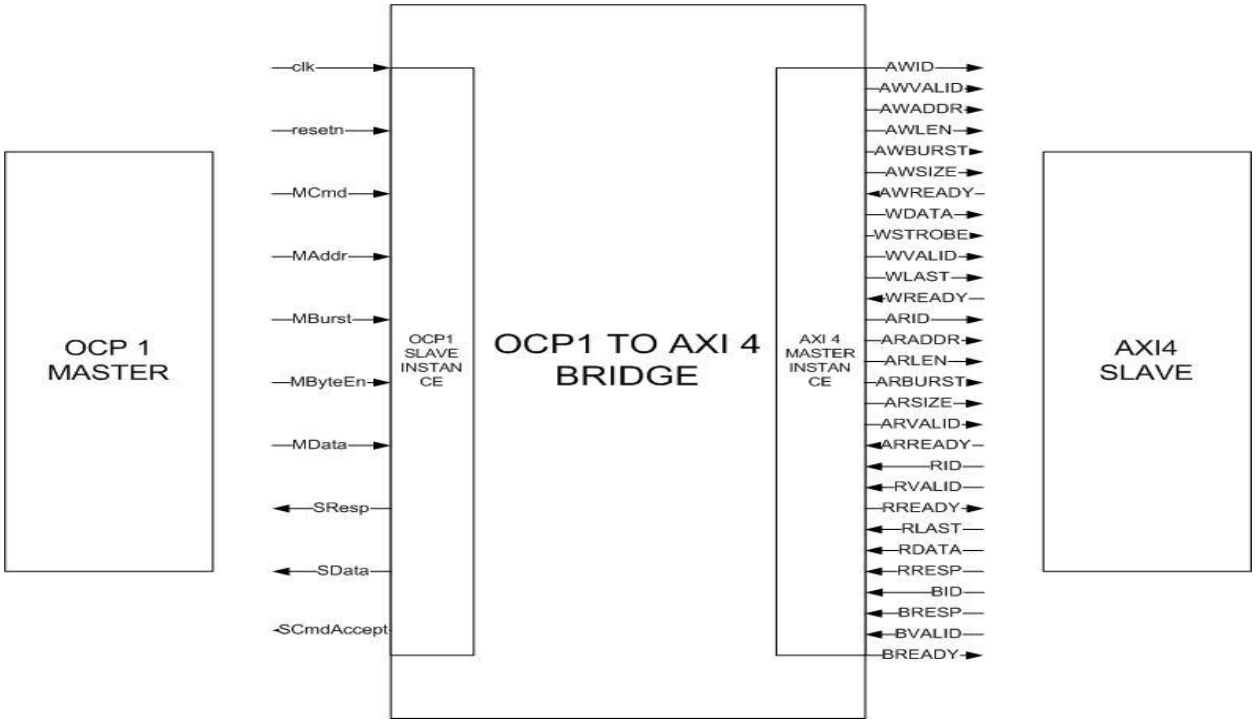

Fig 3.7 architecture of bridge

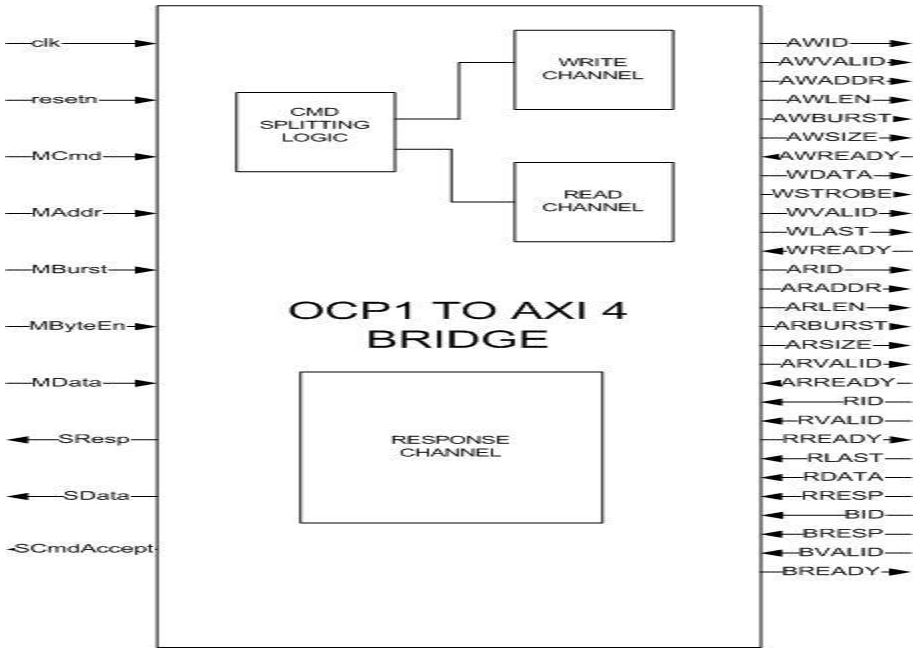

Fig 3.8 micro architecture of bridge

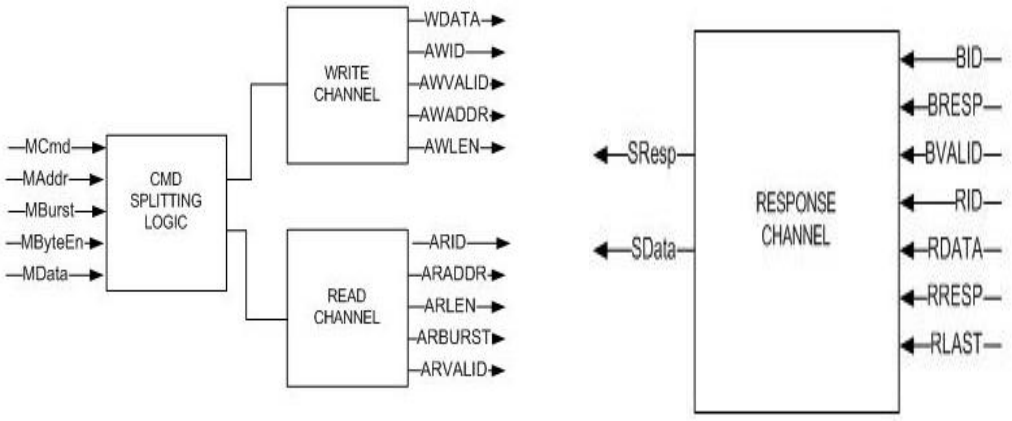

Fig 3.9 block diagram of sub blocks

3.3.2 EXPLANATION OF MICRO ARCHITECTURE

1. Command splitting block activates read or write channel based on the mcmd signal of OCP by making AWVALID or ARVALID high.
2. From mburst signal length and type of transactions is calculated in this cmd splitting block
3. AWID or ARID signal is generated by the bridge.
4. 4k boundary condition is also checked and maintained by the same block.
5. Response channel block maintain the order of responses.
6. In AXI there are two response channels one for read and one for write response.
7. Response for only one channel is accepted at a time. Priority is mostly given to the write channel response.
8. Only a fixed number of outstanding transactions are supported.
9. Response for write channel is not supported and hence selectively discarded by the bridge.
10. Bridge maintains the order of response between write – write transaction and read – read transactions.

3.3.3 FEATURES OF THE BRIDGE

1. Both read and write transactions are supported. Read with response and write transaction without response are supported.
2. Increment type of burst is supported by the bridge.
3. Tag IDs are generated by the bridge.
4. Ordering between responses is maintained by the bridge.
5. Takes care of 4k boundary condition.
6. Data width of 32 bit is only supported.
7. Upsizer can be used after the bridge to increase the data width.

8. 32 bit address range is only supported.

3.3.4SIGNAL MAPPING

Table 3.5 ocp1 and axi4 address channel signal mapping

OCP1	AXI4
Genrated	AWID/ARID
MAddr	AWADDR/ARADDR
To be calculated	AWLEN/ARLEN
To be calculated	AWSIZE/ARSIZE
MCmd(calculated)	AWVALID/ARVALID
SCmdAccept	AWREADYARREADY
MBurstSeq	AWBURST/ARBURST

Table 3.6 ocp1 and axi4 data channel signal mapping

OCP1	AXI4
Doesn't exist	Doesn't exist
MData	WDATA
MByteEn	WSTROBE
Generated	WVALID
Generated	WLAST
SCmdAccept	WREADY

Table 3.7 ocp2 to axi4 write & read channel response mapping

OCP1	AXI4
Not required	BID/RID
SResp	BRESP/RRESP
SData	RDATA
Not required	RLAST
Calculated (SResp)	BVALID/RVALID
Generated	BREADY/RREADY

3.4 OCP1 TO APB3 BRIDGE

This bridge coverts the transaction from OCP1 master into APB3 transaction for APB3 slave. In bridge slave instance of OCP1 is present which accept the command from OCP1 master in OCP1 protocol format and converts into APB3 transaction and on other side master instance of APB3 is present in the bridge which sends the transaction to the APB3 slave in APB protocol format.

3.4.1OCP1 TO APB3 BRIDGE BLOCK DIAGRAM AND MICRO ARCHITECTURE

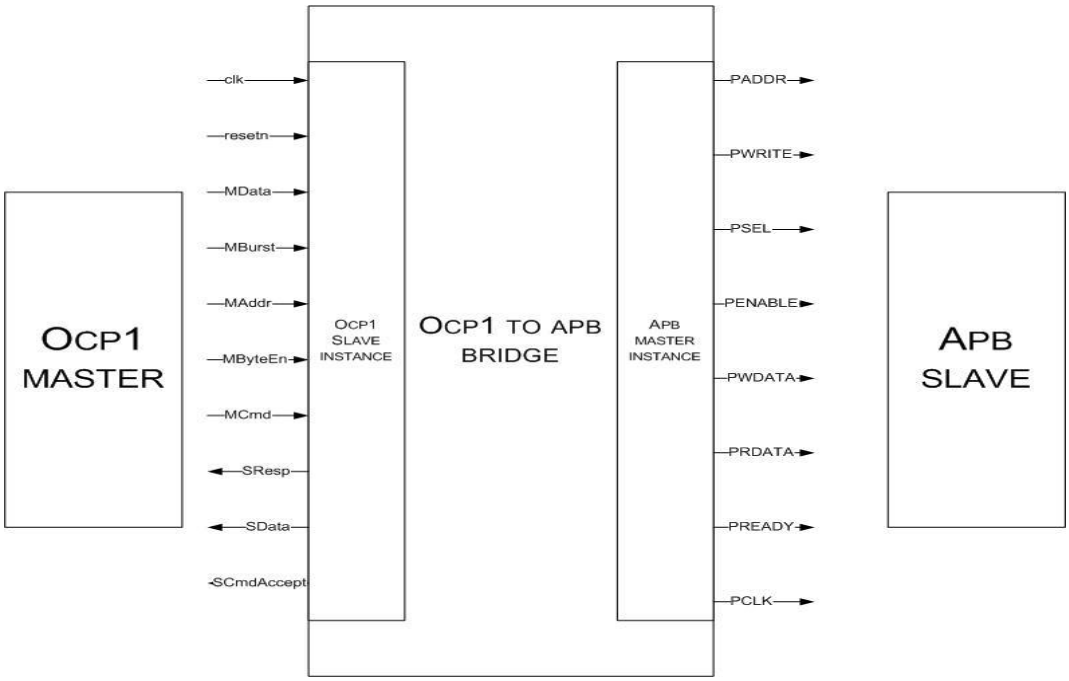

Fig 3.10 architecture of bridge

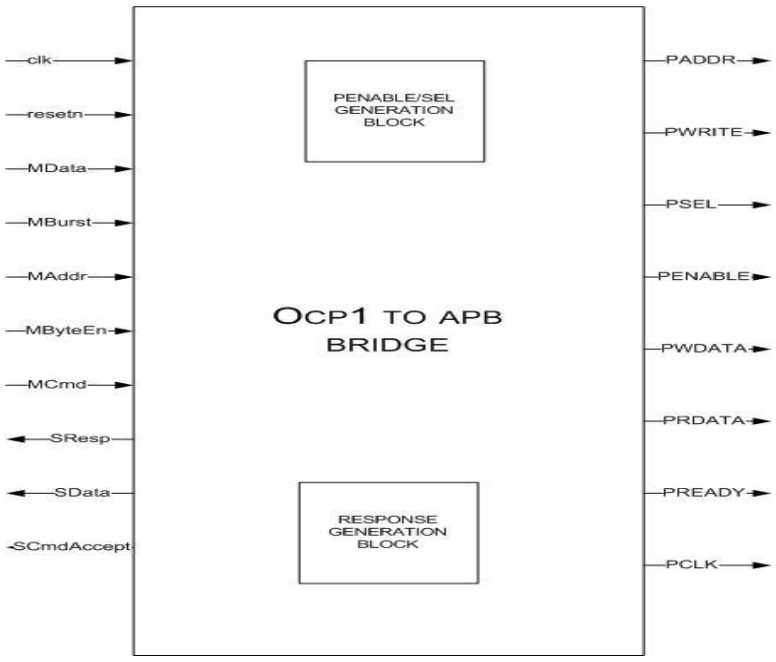

Fig 3.11 micro architecture of bridge

3.4.2 EXPLANATION OF MICRO ARCHITECTURE

1. This burst transfer is not possible single data is transferred at a time.
2. Penable and psel are generated by the block.
3. Psel is uses address decoding circuitry.
4. Response block generate the response as no response is provided by the APB slave.

3.4.3 FEATURE OF THE BRIDGE

1. Response is generated immediately hence there is no concept of outstanding transactions.
2. No out of order response concept.
3. Burst of any length is converted into single burst.
4. 32 bit data width.
5. 32 bit address width

3.4.4 SIGNAL MAPPING

Table 3.8 ocp1 to apb3 signal mapping

OCP1	APB
MADDR	PADDR
MCMD	PWRITE
MDATA	WDATA
SDATA	RDATA
SCMDACCEPT	PENABLE
CALCULATED	PSEL
SCMDACCEPT	PREADY

Chapter 4

Discussion and Conclusions

4.1Discussion

These bridges are designed after studying the specification of each protocol in detail. These are designed for application specific purpose according to the requirement of different master and slave traffic generated by all the IPs has to pass the system bus therefore it is necessary to convert all the traffic into the format which is supported by the system bus. As it is not possible redesign communication interface off each IP such bridges are required. These bridges are capable of handling all the transactions of OCP, AXI, and APB protocol. There are many other module which are the pasrt of system like upsizers, downsizers, routers, adapters, mergers, timers etc which makes the communication possible along with these bridges. As system bus is the main backbone for communication SoC incorrect functionality of these bridges can result in failure of whole chip. Therefore these are highly essential part of bus system and because these bridges reusability of different IPs are possible

4.2 Conclusion

All these bridges are designed and verified by using AXI, OCP and APB master and slaves VIPs. These are fully functional and working correctly as per the requirement and meeting all the constraints of gate count, timing constraints and there are no latches in design. These are bridges are capable of handling all the AXI, OCP and APB based transactions.

References

1. OCP-IP, “Open Core Protocol Specification”, Available at http://www.ocpip.org/.
2. ARM, “AMBA Specification”, http://www.arm.com/.