Design of a large vertical displacement Electrothermal Bimorph Actuator

and

Clock controller Automation, CDC, PLDRC and DFT

by

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2015PEV5047

under the supervision of

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Department of Electronics and Communication Engineering

Malaviya National Institute of Technology, Jaipur

Certificate

This is to certify that this dissertation report entitled "***Design of a large vertical displacement Electrothermal Bimorph Actuator and Clock Controller Automation, CDC, PLDRC and DFT***" by Shilpa Thakral, has been completed under my supervision and guidance, hence approved for submission in partial fulfillment for the award of degree of Master of Technology in VLSI Design to the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur during the academic session 2015-2017.

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We wish her all the best for her future endeavours.

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4. Where it has quoted from the works of other, the sources is always given. With the exception of such quotations, this report is entirely my own work.

5. It has acknowledged all the main sources of help.

Shilpa Thakral
(2015PEV5047)

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Abstract

The thesis work is divided into two parts. In Part A a large displacement out-of-plane MEMS structures have been studied and implemented. Looking at previously fabricated out-of-plane motions structures one would realize that the application of such structures are primarily made in creating tunable filters, ,endoscopy in medical, electronic safety switch, micromirrors , Fourier transform spectroscopy, Bio-AFM, thermostat, scanning probe microscopy ,micro ciliary motion system, zooming lens in mobiles and camcorders, and many more.

In this work, it has been targeted to obtain out-of-plane motion of a plate with a less elaborate and compact mechanism. Bimorphs have been used for the purpose of actuation of the structures while flexible springs have been efficiently put to use to eliminate the need for hinges at the joints.

The basic conceptualization of the electrothermal actuator is based on a folded dual-S-shaped-bimorph (FDSB) actuator design to achieve large displacement at low input voltages. The design is a symmetric design that balances the mirror plate and provide pure vertical displacements with negligible tilt, lateral shift and with low distortion of plate. Gold and Slicon dioxide have been used as the materials for bimorphs. Analysis are done to calculate the maximum rise in temperature, convection loss, initial displacement, stress generated and thrust effect on the structure. The design has been simulated on Coventorware 2012.

In Part B of the thesis the work done in Qualcomm is explained. During my six months of internship I have worked on two different projects in Corporate R&D department, BDC, Qualcomm. I have used several tools and languages for completing the assigned tasks. I have worked on Mentor 0in CDC tool, Spyglass PLDRC tool, ModelSim simulator, Mentor Tessent DFT tool and DC compiler for generating netlist.

In the first project I have worked on automating the clock controller block using Qualcomm developed automation tool. The tool can generate RTL code for the block using an input excel spreadsheet which has all the specifications related to the design. After generating the RTL, I have done CDC and PLDCRC check on the design to verify the synchronization of clocks, synthesizability, reset synchronization, structurability, at speed clock test, etc.

In the second project I have done DFT (Design for test) for an ongoing project in Corporate R&D. For that I have used Mentor Tessent tool that generate ATPG test patterns for the input design. All the scripting is done in Perl and Tcl.

PART A: Bimorph Actuator

Chapter 1

Introduction

1.1 Motivation

For the last few decades, MEMS (Micro-Electro-Mechanical Systems) technology has been used in many application areas such as optics, communications, sensors, fluids and biology. Electrothermal bimorph MEMS actuators with large deflection form an important part of a variety of devices and systems where precise in-plane or out-of-the plane motion is required for obtaining the desired function [1],[2]. Looking at previously fabricated out-of-plane motions structures one would realize that the application of such structures are primarily made in creating tunable filters[3],[4], ,endoscopy in medical, electronic safety switch, micromirrors [5],[7] , Fourier transform spectroscopy[8],[9], Bio-AFM, thermostat, scanning probe microscopy ,micro ciliary motion system, zooming lens in mobiles and camcorders[6], and many more.

In this thesis the focus is on designing a MEMS based Electrothermal large vertical displacement Bimorph actuator which can provide large out of plane displacement using minimum voltage. A novel bimorph actuator design has been proposed to solve the drawbacks with existing micromirror designs. A plate of 1mm x 1mm is lifted using this design. Various structures have been designed to achieve this objective.

1.2Literature Review

A survey of existing publications relevant to the design problem under consideration have been examined before setting out to propose any enhanced design idea.

Si-Hyung Lim et al. has proposed and fabricated a novel flip over beam(FOB) bimorph actuator to increase the deflection and sensitivity of the actuator on temperature rise [10]. The FOB beam is made up of three sections of SiN/Au, SiN/Au/SiN and Au/SiN respectively. The sections are developed in such a way that SiN covers gold for half of its length at its bottom surface and alternate half on top surface. By depositing silicon nitride in this way and then combining multiple these FOB beams together, the deflection of the structure can be approximated as the combined sum of each FOB beam deflection. They find out that 53% higher mechanical sensitivity can be obtained using this FOB beam as compared to conventional bimorph beam design. They have designed a micro-opto-mechanical sensor having a symmetric structure with a sensor area of 100 um x 100 um, and obtained a thermo-mechanical sensitivity S_T = 180 nm/K.

In the literature presented by Sean R. Samuelson et al. [8], a unique ladder actuator that can provide ultralow tilt with large piston motion has been designed, fabricated, and tested with device features tuned to applications requiring ultralow tilt. The device also allows precise positional control of the mirror plate on the submicron scale. This allows the device to function under quasi-static actuation and effectively generate signal in an FTS system that is not subsumed by noise. The design of the micromirror also provides a strong basis for expansion of mirror aperture and increases in displacement. A micromirror based on such ladder actuators shows 0.25° tilt at 90 μm piston displacement. The fabricated MEMS mirror is based on electro thermal actuation and has a footprint of 1.9mm × 1.9mm with a mirror

aperture of 1 mm which is capable of achieving 145μm vertical displacement and a fill factor of up to 55.98%.

The actuator is made of units of inverted series connected or S-shaped bimorph, which has three sections L1, L2 and L3 which contain the following thin film layers of Al/SiO_2, SiO_2/Al/ SiO_2 and SiO_2/Al respectively.

Dong Yan et al.[3] had proposed a unique approach to design tunable dielectric resonator filters with high quality factor. The filter had embedded MEMS tuning elements. The large vertical deflection electrothermal bimorph actuators were used to achieve high tunability by moving the mirror plates or tuning disks to disrupt the electromagnetic field of the dielectric resonators. A center frequency of 15.6 GHz with a relative bandwidth of 1% was experimentally calculated.
A hair pin kind of zigzag structure of bimorph made of gold and polysilicon and a center tuning metal plate of 2mm diameter , made of 3.5-μm polysilicon and 2-μm gold ,were the core of the actuator. An out-of-plane rotation of a 400 μm x 2500 μm x 2 μm plate, produced by MEMS thermal actuators, was successfully demonstrated. The actuation voltage is less than 10 V and a 90-degree rotation is achieved within 1 millisecond.

In the literature presented by Wu, Xie,[7] on the study of bimorph structures, minimization in lateral shift along with large vertical displacement has been reported. The design employs a lateral shift free piston motion in vertical direction. A vertical displacement of 0.646mm, at 5.3V(184mW) has been attained. The resonant frequency of the bimorph structure is 453Hz, with its thermal response time being 25ms.

The lateral shift free structure is concentrically meandered, with each level of bimorph structure being the support frame for the bimorphs extending to the remaining levels in the vertical direction. The device footprint is 2.5mm with bimorphs elements of lengths 150um, 300um and 150um respectively for a three level bimorph and frame structure. The support frame length is 500um. The successive lengths of the bimorph elements are such that the lengths of 1st and 3rd bimorph element equals the length of the 2nd bimorph element. This ensures that the bending arc angles of the bimorph elements also follow the same relation, in effect balance the clockwise and the anti-clockwise moments. Four such bimorph structures are attached to the four sides of a central 800um^2 platform.

The bimorph structure has been composed of a bottom Silicon dioxide [SiO2] layer and a top Aluminum (Al) layer with a layer of Platinum (Pt) heater sandwiched between these two layers. The SiO_2 and Al layers are of 1um thickness while the Pt heater layer in between is of 0.2um thickness. A passivation/isolation layer of SiO_2 of thickness 0.1um has been placed between the Pt and Al layers.

Pal,Xie [11] have explored bimorphs using W(tungsten) as heater as well as active bimorph layer. High decomposition temperature Polyimide (PI 2574) has been used for thermal isolation of substrate & Al mirror plate in place of SiO_2 for more robust structure and thin SiO_2 layer for electrical isolation between Al & W bimorph layers. Series combinations of four parallel bimorph beams connected together as a unit, forming a long array of bimorphs have been employed to ensure fail-safe device working even if any of the currents pathways of W heats gets damaged.

Temperature insensitive multi-morph segments of Al-W-Al have been placed at both ends of bimorphs (where the four parallel bimorph beams meet to form one of the larger series units).

PI layers joins these multi-morphs to the substrate on one side and the mirror on the other end.

In their work, Jain,Xie [6] have reported a 0.5mm displacement (presumed downward) at 15V and a 30 deg. tilt at 12V. There is an initial curl up of 1.24mm after release due to residual stress. The polysilicon heater layer has length 200um and width 7um. The mirror plate is $0.5mm^2$.

Kemiao Jia et al. [12] designed a 1D micromirror in their thesis work. The device has a footprint of 1.9mm x 2.4mm and is capable of achieving 30º of 1-D optical deflection. They have proposed a novel approach of FDS electro-thermal bimorph actuator that solves the initial tilting and lateral shifting problem that occur in previous electro-thermal actuators.
The devices can achieve a piston stroke of up to 480μm with near-zero lateral shifting and ±30º dual axis rotation scanning with fixed rotation axes at small driving voltage of less than 8V. The device shows 10ms response time and a 3dB cut-off frequency of up to 200Hz.

1.3 Approach

The work carried out in this thesis intends to demonstrate the electro-thermal actuators which can show large range of vertical displacements on application of different voltages ranging from 50 mV to 150 mV. A novel approach of folded S-shaped beam electro-thermal bimorph actuator that solves the initial tilting and lateral shifting problem that occur in previous electro-thermal actuators has been used in this design. A bimorph is a stack of two different materials having large difference in their thermal expansion coefficient (TEC), which are joined along their horizontal axis. A variety of structures has been designed to optimize the performance of the actuator. A Flip over beam (FOB) type bimorph structure is configured such that a material layer (silicon dioxide) coats half of the top surface of the beam (gold) at one section and half of the bottom surface at the opposite section. The total deflection of multiply connected FOB beam structures can be approximated as the addition of each FOB beam deflection. Various measures have been taken to reduce the warpage of plate. Different plate geometries and compositions have been designed to obtain the desired results. Convection loss, launch thrust effect, total power consumption, initial displacement of plate due to stress and relation between temperature rise, displacement and potential applied have been calculated.

1.4 Thesis Outline

The thesis is organized as follows:

Chapter 2 discusses the theory behind MEMS about the various processes and techniques used. These discussions provide a fundamental foundation to develop the methodology used in the thesis work. Various MEMS actuation principles are also discussed in this chapter.

Chapter 3 presents a detailed description of the research design. It incorporates the basic principle behind electrothermal actuators and bimorph cantilevers. It also includes the study of stresses in the bimorph material layers and the materials that are commonly used in making bimorphs.

Chapter 4 is dedicated to understanding the basic electrothermal physics and the structure. The detailed study of various heating mechanisms has been done in this chapter. The heat loss due to convection is considered in deep detail. The working mechanism of these structures is also studied briefly to give us a good know how about finalizing the actuating structure.

Chapter 5 is dedicated entirely to presenting the design and simulations of the structures carried out on FEA based software- Coventorware 2012. Simulations are carried out for different structures which are then optimized for displacement by varying the dimensions, geometry and other features of the structures.

In Chapter 6, the conclusions of the study are presented along with the discussions about the findings. Finally the implications of this thesis are derived and future research directions are presented.

Chapter 2

Introduction to MEMS

2.1 MEMS

Microelectromechanical system(MEMS) is a process technology which can be utilized to develop integrated devices and systems that incorporates mechanical as well as electrical components. Fabrication of MEMS systems are done by sophisticated processing and manipulations of silicon, germanium and other substrates using micromachining processes. These devices generally range in size from a few microns to millimetres and are capable of sensing, controlling and actuating on the micro scale [13].

While the IC technology is used to fabricate the device electronics, the micromechanical components are fabricated by utilizing subtle manipulation of silicon or other substrates using micromachining processes. It uses processes like bulk micromachining, surface micromachining and high-aspect-ratio micromachining (HARM) which add structural layers or selectively remove parts of the silicon to create the mechanical and electromechanical devices.While integrated circuits are designed to exploit the electrical properties of silicon, MEMS takes advantage of silicon's mechanical properties and also its electrical properties[1].

The popularity of MEMS devices increase in mid-1990's and the MEMS products began appearing at various commercial places, with a wide range of their applications like accelerometers to control airbag deployment in vehicular security systems, inkjet printer heads, and pressure sensors for biomedical applications. Later other products were also developed like oscillators, displays, FBAR and microphones. Later it got enhanced to diverge into specific domains such as MOEMS and BioMEMS[2].

MEMS products can be classified into four groups, which ultimately lead to four intertwined fields i.e. microstructures, microsensors, microactuators, microelectronics [13]. The micro-sensors detect changes in the environment of operation and measure various information or phenomena viz. mechanical forces and displacements, thermal variations, magnetic fields, chemical compositions and electromagnetic fields. The microelectronic components process this information and cause the microactuators to react and create some form of changes to the environment.

MEMS provide multiple advantages and some unique solutions. Their low cost, miniature size, mechanical durability, high accuracy, low power consumption, immense switching density along with the low-cost batch processing of MEMS-fabricated devices bring out a innovative solution to various problems[11].The most noticeable benefit of MEMS devices compared to their classical macroscopic counterparts is the size reduction: many rigid materials become flexible in micro dimensions. And with the use of single-crystal material, fatigue phenomenon is less of a problem due to the absence of grain boundaries. Other advantages include increased speed, lower power consumption, increased reliability, better performance, lower cost, etc. This is a rich field of research and development in which some applications have already reached the commercial level and other show a promising future.

Figure 2.1 depicts the general forms of MEMS devices.

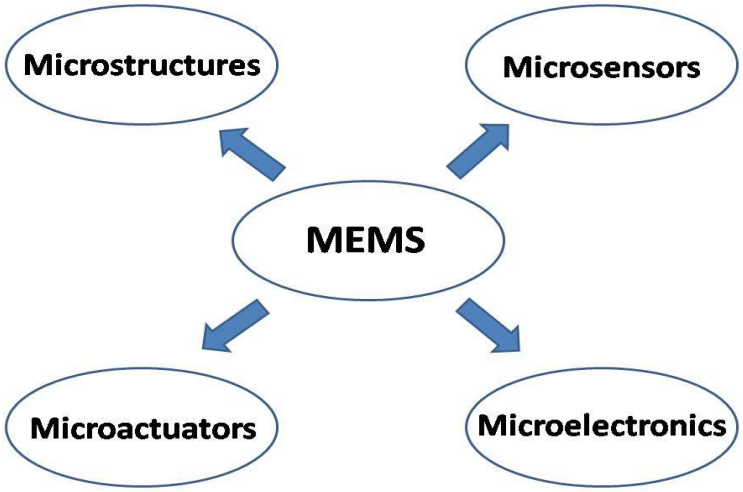


Figure 2.1: General Form of a MEMS system [2]

2.2 Microfabrication Techniques

The foundation of MEMS fabrication lies in the integrated circuit (IC) industry. Most of the processes which are used to produce ICs can be used to develop MEMS devices. Some recent devices require certain specific processes or a combination of them for their development. A variety of materials can be used in MEMS fabrication. Silicon is by far the most common. Single crystal silicon acts as an outstanding electronic material and mechanical material [14]. One of the most important aspects for mechanical applications in sensing is mechanical stability. In large temperature range, the mechanical properties of silicon (bulk) is determined by the theory of elasticity otherwise it is assumed to be practically constant. Also the miniaturization of the size of the structures does not alter its properties. In micrometer scale the mechanical properties for silicon mechanical structures are almost the same as compared to bulk material and it is safe to assume that mechanical properties of a silicon micro structure are ideally elastic, the Young's modulus of silicon being 160GPa. This assumption implies that, if the deformation produced by external forces does not exceed a certain limit, it disappears once the forces are removed [15]. However the performance of mechanical sensors is more significantly affected by the variations of geometric parameters determined by process.

MEMS devices can be distinguished into three fabrication classes: bulk micromachining, surface micromachining and high-aspect-ratio micromachining (HARM).

2.2.1 Bulk Micromachining

Bulk micromachining is the oldest of the micromachining techniques. In this micromachining technique channels, cavities, holes, or any other shape, is created by removing parts of the bulk substrate. It is a reductive process. In order to create these shapes, it uses wet etching (isotropic or anisotropic) techniques or a dry etching techniques (Reactive Ion Etching (RIE) and its variants).

Wet Etching: In wet etching part of the material (generally a silicon wafer) is removed by immersing the material in a chemical etchant (liquid) and can be used for cleaning, removing damages to the surface of the substrate and creating sensing structures. There are two types of etchants : anisotropic and isotropic. Isotropic etchants removes the material at a uniform rate

in all the directions, and as a result removes material below the etching masks at the same rate as they etch through the material. Hence masking to achieve precise geometries is difficult and so is controlling the vertical geometry [16].

Anisotropic etchants etch more rapidly in a favoured direction. KOH (Potassium hydroxide) and T-MAH (Tetramethyl ammonium hydroxide) are the most commonly used anisotropic etchants. The structures are made in the substrate depending on the orientation of crystal of the wafers or substrates. The rate of etching is high in the direction perpendicular to the plane (110) and is low in the direction perpendicular to the plane (100). The perpendicular direction to the plane (111) etches at a slower rate [15].

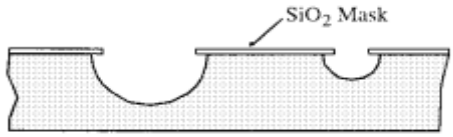


Figure 2.2: Isotropic Wet Etching

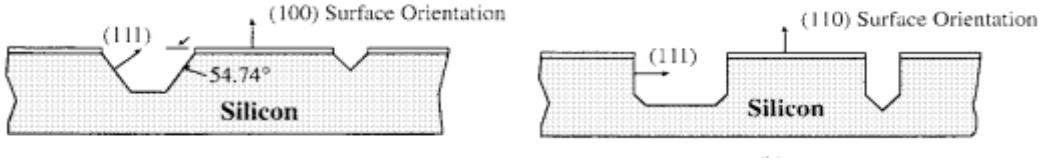


Figure 2.3: Anisotropic Wet Etching

Dry Etching: It consists of techniques by which a substrate is etched either by ion bombardment or by using chemical reactions by introducing reactive species at the surface of the substrate or by combining the two mechanisms [17]. Reactive ion etching (RIE) is the most commonly used dry etchingtechnique for MEMS. It requires additional RF power to speed up the chemical reaction. The etchant is changed into plasma phase on exposure to this energy and generates energetic electrons, photons, ions and highly reactive radicals which are accelerated towards the material to be etched and supplies the additional energy needed for the reaction; as a result the etching can occur at much lower temperatures (typically 150º - 250ºC, sometimes room temperature). Unlike Anisotropic etching, RIE is not restricted by the silicon's crystal planes, and hence deep channels and pits, or vertical walls can be etched.

2.2.2 Surface Micromachining

Surface micromachining involves processing above the substrate by addition of a material over the substrate while using it as a foundation layer to build the desired structure which is in contrast to the Bulk micromachining in which features are etched into the substrate material. The thin films of materials are deposited on the surface of the substrate, which is mostly a wafer of silicon. The layers can either be structural layers or can act as spacer layers which can be later removed in which case they are to be addressed as sacrificial layers. The structural layer is used to make free standing structures and sacrificial layer is deposited where an open area under the free standing structure is required [17].

These layers are deposited and subsequently patterned and to free the final structure, the sacrificial layer is finally etched. The level of complexity keeps on increasing with addition of layers and makes the fabrication process more difficult. A typical surface micromachined cantilever beam is shown in Figure 2.3. Here, a sacrificial layer of oxide is deposited on the

silicon substrate surface and patterned using photolithography. A polysilicon layer is then deposited and patterned using RIE processes to form a cantilever beam with an anchor pad. The wafer is then wet etched to remove the oxide (sacrificial) layer releasing and leaving the beam on the substrate.

2.2.3 HARM (High aspect ratio Micromachining)

High aspect ratio micromachining in short HARM, is a micromachining tooling process. It consists of methods like injection, moulding, embossing or even electroforming to reproduce microstructures on substrate from the moulded parts. Till today, it is one of the proven and most efficient technology to duplicate microstructures at a high performance-to-cost ratio. It also includes a highly efficient technique known as LIGA. Products micro-machined using this technique include modernized high aspect ratio fluidic structures for example moulded nozzle plates for ink jet printers and micro-channel plates for disposable microtitre plates for diagnostic applications in medical science. The materials used are electro-formable plastics and metals, including polycarbonate, acrylate, styrene and polyimide.

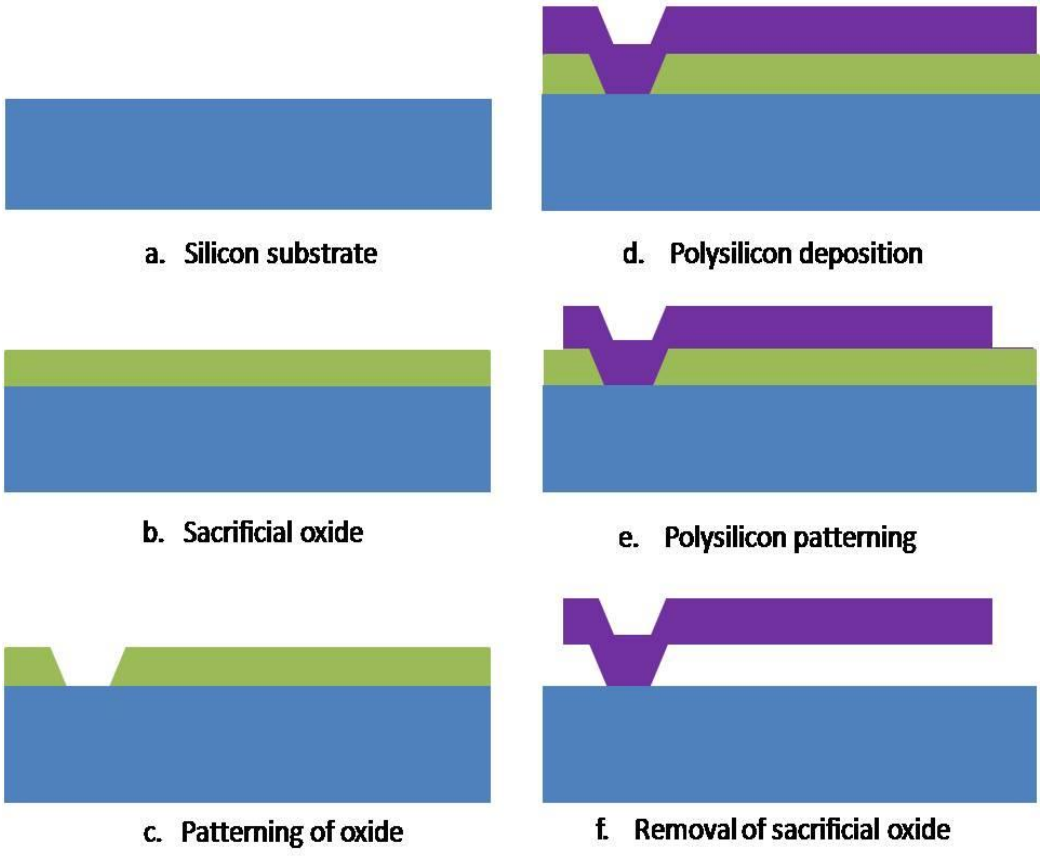


Figure 2.3: A Surface micromachined Cantilever [17]

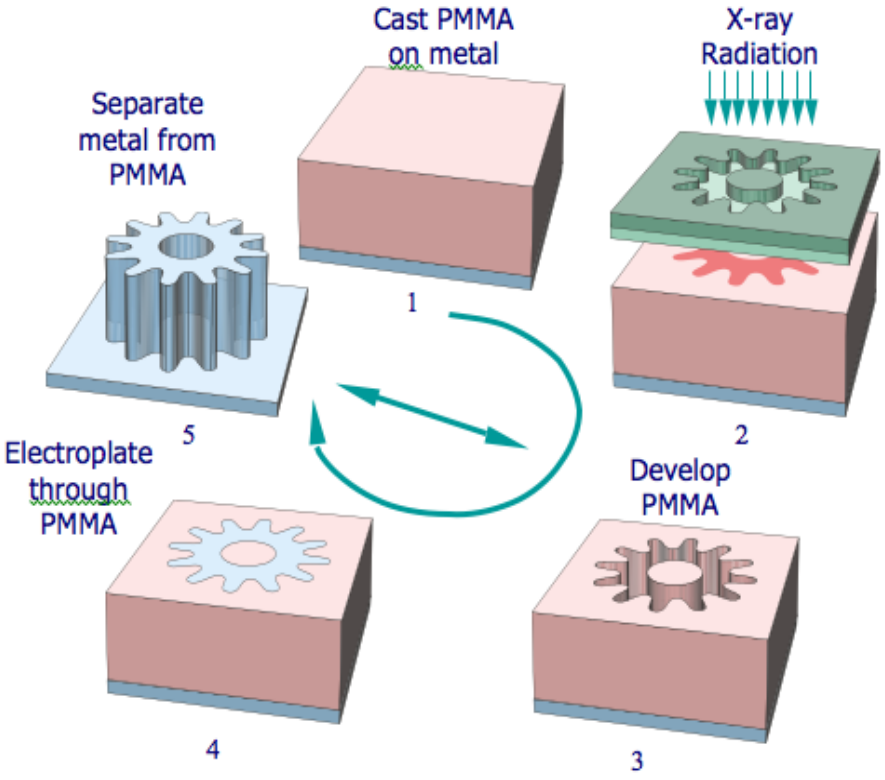


Figure 2.4: LIGA Process [16]

LIGA: It is an important tooling and replication method to create microstructures of very high-aspect-ratio. This advanced technique involves X-ray synchrotron radiation to expose thick PMMA acrylic resist under a lithographic mask. The exposed areas on the substrate are dissolved chemically. Further metal is electroformed in regions from where the resist is removed, thereby realizing the final product or the tool insert for the succeeding moulding step. LIGA has the capabilities of creating very minutely defined microstructures, which can go up to thousand micrometers high[16]. LIGA provides a radically new way to produce small, precise micro-machined parts at relatively low cost.

2.3 Materials for MEMS

Silicon is an ideal substrate material for MEMS. It is low in cost and is already being used in the form of wafer for IC fabrications. Silicon (Si) is a material, which is found in ample amount on earth. It mostly exists in the compound formed with other elements such as silicon compounds (SiO_2 , SiC, polysilicon, etc.), metals (aluminium, gold, etc.), PZT, polymers [2].

The popularity of silicon for MEMS application is evident due to following properties. It has high mechanical stability and can integrate with electronic circuits. It can provide different transduction and control by simple doping of p-type or n-type. It's Young modulus is almost as of steel (~ $2x10^5$ MPa). At the same time, it is as light as aluminium. As It has a density of about 2.30 g/cm^3. Its melting point is 1400^oC, which is almost two times higher as compared to aluminium, which makes it suitable to operate in extreme conditions of temperature and pressure. Along with this, it has around eight times smaller thermal expansion coefficient as compared to thermal expansion coefficient of steel and, simultaneously ten times smaller than that of aluminium [15].

2.4 MEMS actuation principles

The actuating mechanisms that are most commonly used in MEMS devices are: piezoelectric, magnetic, electrostatic, and thermal actuation [1], [2]. The most common actuation mechanism in MEMS is electrostatic because of its straightforward principle, compatibility with CMOS processes and materials, and relatively low consumption of power. Disadvantages include potentially high driving voltage and non-linear voltage response.

The electrically induced strain is approximately proportional to the applied electric field in piezoelectric actuation. Its advantages include large force, fast response time, and potentially low operating voltage. Disadvantages include small dimensional variations and a need for a sophisticated fabrication process.

There are many advantages of using magnetic actuation (electromagnetic or magnetostrictive). For example, magnetic forces can be both attractive and repulsive. They are large in magnitude and effective over a long range. The major disadvantage of magnetic actuation is the lack of mature fabrication technology. This is mainly because it requires more complicated components, such as coils and magnetic materials.

Thermal actuation provides large force and deflection. It has the advantages of low driving voltage and a nearly linear deflection versus-power relationship. Thermally actuated device processes are often based on fairly straightforward fabrication steps and can be easily integrated with circuitry using, for example, a standard CMOS process. The main disadvantages are relatively long response time and large power consumption. Other actuation mechanisms include Shape Memory Alloy (SMA) actuation, chemical reaction actuation, or a combination of two or more of any of the previously discussed mechanisms. Each may have a particular specialized application area.

In summary, there are many actuation mechanisms to choose from that can be used in MEMS. None has dominance over the others: some are better in certain areas, some are mature and some promise potential benefits. The choice is a balance between many factors, such as design specifications, application constraints, process compatibility and cost. Table 1.1 is a brief comparison of the different actuation mechanisms.

Electro-thermal bimorph actuators are popular in MEMS devices. The most important applications of these actuators are in field of micromirrors , fourier transform spectroscopy, RF switches, Infrared detectors , nanoprobes and read–write cantilevers for storing data [3], [5]. Electrothermal bimorphs can attain large mechanical deflections by using materials with different thermal expansion coefficients (TECs) which in turn can create large strain differences as compared with other types of actuators such as electrostatic actuators. Bimorph structures have long been studied and used for sensors and actuators because of their sensitivity, fast response time and ease of integration with semiconductor technology [1].

In this thesis electrothermal actuation principle has been used to design a large out of plane vertical displacement actuator which can provide large range of displacements using minimum voltage.

Table 2.1 A brief comparison of the different actuation mechanisms used in MEMS [2].

Actuation Mechanisms	**Advantages**	**Disadvantages**
Electrostatic	Straightforward principle CMOS compatible Less power	High driving voltage Non linear response
Piezoelectric	Large force Short response time Low driving voltage	Sophisticated fabrications steps
Magnetic	Large force Effective over a long range Can be attractive or repulsive	Complicated components Need magnetic materials No mature fabrication technology
Thermal	Large force and deflection Low driving voltage Linear deflection response with power Simple fabrication and IC compatible	High power consumption Long response time

Chapter 3

Principle of Electrothermal Bimorph Actuation

3.1 What is a Bimorph?

A bimorph cantilever is a stack of two layers of two different materials with different physical, thermal and electrical properties with one end of the cantilever is free to move and the other end is fixed. For a cantilever to act as a thermal bimorph the thermal expansion coefficient (TEC) of the two layers should be different, more the difference, larger is the deflection on heating the bimorph [16]. Generally, a material which has high TEC such as metals, gold, aluminum , etc. is combined with a material that have low TEC such as a dielectric, SiO_2, polysilicon, etc. The cantilever bimorph beams can be wisely joined together to form more complex bimorph actuators. In order for understanding the basic principle of electrothermal actuation a two layer bimorph is explained here [5]. A typical thermal bimorph and its dimensions are shown in Figure 3.1, where L is the length of the beam, t_1 , t_2 are the thickness and w_1, w_2 are the width of top and bottom layer, respectively. 1 is used as subscript for top layer and 2 is used for bottom layer. α_1 and α_2 are the TEC and E_1 and E_2 are the Young's modulus of each layer with $\alpha_1 < \alpha_2$.

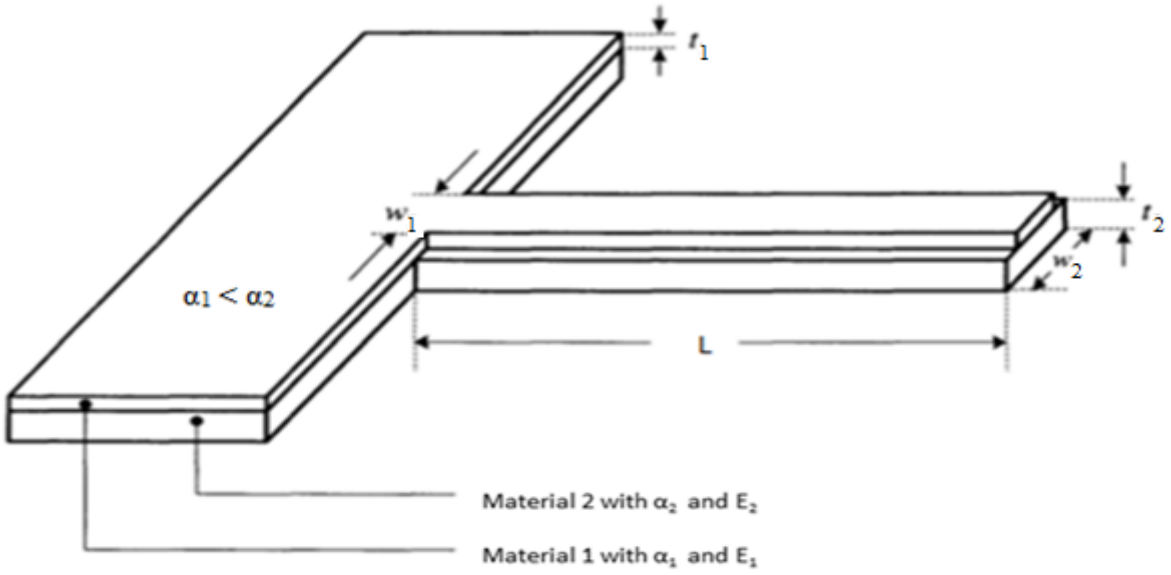


Figure 3.1 A typical thermal bimorph Cantilever [15]

Assuming there is no residual stress in the layers at room temperature (T_o), the bimorph is in a relaxed state i.e., there is no stress in the beam and it is not deflected in any direction. When the cantilever bimorph is heated by any means i.e., by Joule heating or a heater embedded in the bimorph, based on thermal expansion principle the interatomic spaces in material starts increasing. As the two materials have different TECs (Thermal expansion Coefficients), each layer will change its dimensions differently. Each material expands according to $_1 = \alpha_1(T - T_0)$, $\Delta L_2 = \alpha_2 L(T - T_0)$, where (T- T_0) is the change in temperature. Assuming the length L and change in temperature to be same for two layers, due to different TECs, the layers will expand at different rates. This small disparity in expansion leads to a large stress on the

junction of two layers and forces the cantilever to bend in the direction of lower TEC material. The stress is tensile in one layer and compressive in the other layer. The layer which has compressive stress tries to expand along its width while the layer with tensile stress tends to contract parallel to the substrate. The bimorph will try to bend out of plane in order to release this induced stress and this stress will keep on decreasing with the deflection of beam. The beam will generate a counter force to oppose this bending which increases with the increase in deflection. The cantilever will regain its equilibrium position when these two forces, induced and counter force, will balance each other. The stress and the force that is generated by this thermal expansion are large, whereas the strain is lesser (small) [18]. Bimorph cantilever beams can generate large out-of-plane displacement from this small, as shown in Figure 3.2. The linear stress distribution is along the thickness of the bimorph cantilever assuming that the end of cantilever is plane prior and after the deflection and the resultant deflection is within the elastic limits for the materials.

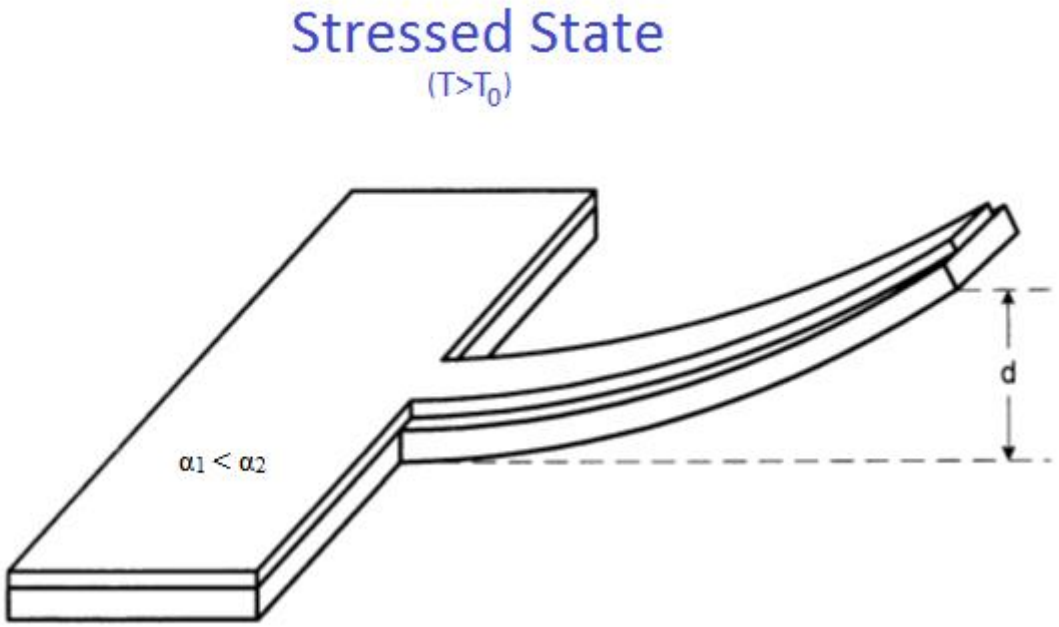


Figure 3.2 Deflection of the bimorph due to increase in temperature

3.2 Stress Analysis

3.2.1 Thermal Stress

The strain created in a free material layer due to thermal expansion is given by:

$$\varepsilon = \alpha.\Delta T \tag{3.1}$$

where, ε is the strain generated in the material, α is the thermal expansion coefficient, and ΔT is the change in temperature[15].

$$\sigma = E.\varepsilon \tag{3.2}$$

Using 3.1,

$$\sigma = E.\alpha.\Delta T \tag{3.3}$$

where, E is the Young's modulus and σ is the stress developed in the material. This equation does not depend on dimensions of the design which implies that the stress generated in the device due to thermal expansion is independent of dimensions of the design. Therefore, as long as material can tolerate the thermal stress, the analogous force scales with the area.

Figure 3.3 represents the direction of bending of cantilever when temperature increases and decreases. The cantilever will move in the direction of lower TEC material when temperature increases and it will move in the direction of high TEC material when temperature decreases[19].

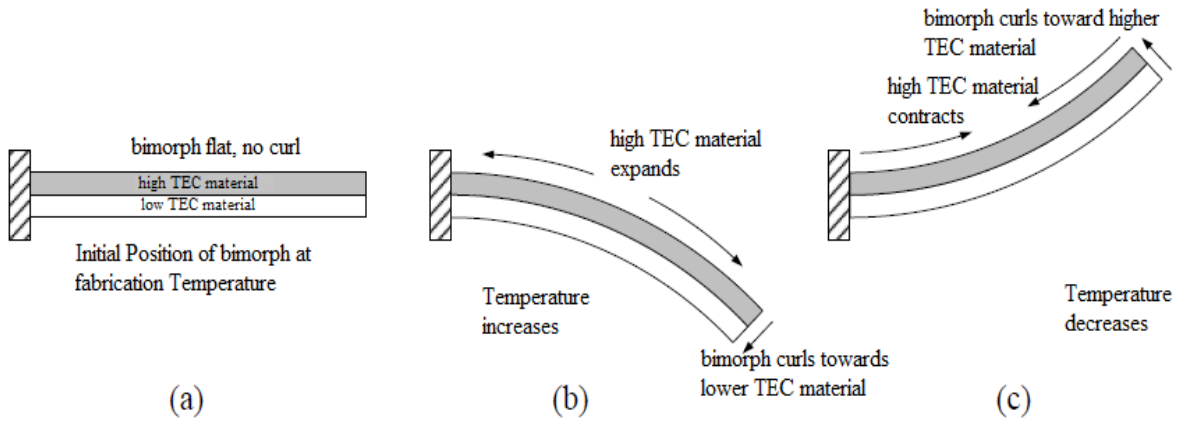


Figure 3.3 a) at room temperature cantilever , b) temperature increases and c) temperature decreases.

At initial state indicated by T_o , the strain distribution in the bimorph cantilever before and after increasing the temperature is represented in Fig 3.4. Both the layers will try to elongate on increasing the temperature[18]. Consider layer 2 has a more thermal expansion coefficient than layer 1 so, it will try to expand more. Therefore, layer 1 is in compressive stress and layer 2 is in tensile stress. An equilibrium position can be found by balancing these two forces:

$$\sum F = \int_{A1} \sigma_1 \, dA + \int_{A2} \sigma_2 \, dA = 0 \qquad (3.4)$$

Where, σ_1 and σ_2 are the stress in each layer, A_1 and A_2 are the cross section area of layer.

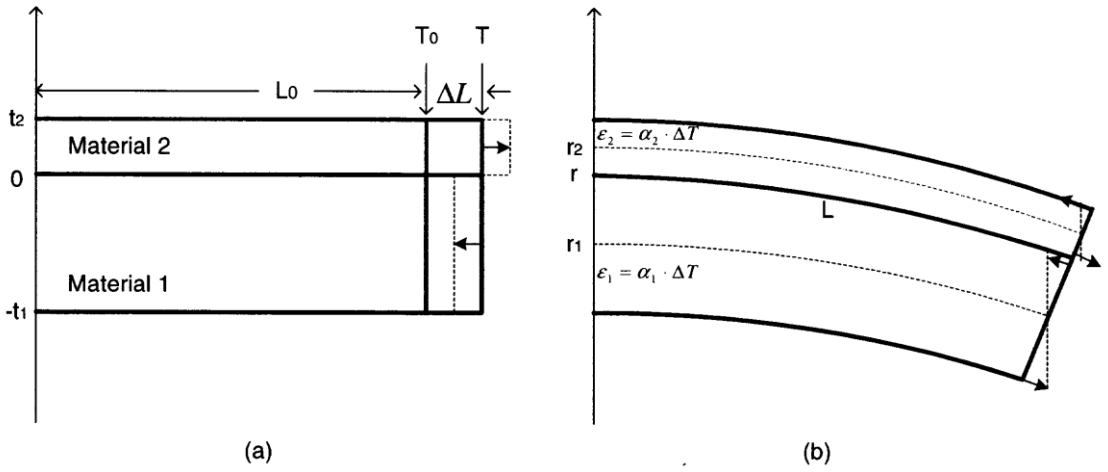


Figure 3.4 Strain distributions within a thermal bimorph cantilever before (a) and after (b) release. Note the existence of neutral planes after release.

Once the beam is released, the cantilever will bend down due to the fact that layer 1 is in compressive stress and tries to contract while layer 2 is in tensile stress and tries to expand. Layer 2 will be tensed and compressed to some extent; the stress within it will change gradually from tensile to compressive. Hence, there exists a neutral plane where there is no stress. Similarly, the stress distribution in layer 1 changes from compressive to tensile, and there exists another neutral plane. The equilibrium state of the released cantilever is reached when the total bending moments and the total force are equal to zero:

From equation 3.4, $$\sum F = \int_{A1} (\sigma_1 .dA) + \int_{A2} (\sigma_2 .dA) = 0$$

$$\boxed{\sum M = \int_{A1} (\sigma_1 .t.dA) + \int_{A2} (\sigma_2 .t.dA) = 0} \quad (3.5)$$

Assume linear strain distribution is alongside the thickness of the bimorph cantilever:

$$\boxed{\varepsilon = \Delta\varepsilon - \frac{t}{r}} \quad (3.6)$$

where, $\Delta\varepsilon$ is the strain at the interface of bimorph , and r is the radius of curvature of cantilever.

The curvature of the beam can be calculated after solving equation 3.4 to 3.6. Using these equations the stress distribution within each layer and position of both neutral planes can also be calculated. It is not necessary for neutral plane to exist within the layers. For example, if layer 1 is very thick and hard compared to layer 2, then post release it may still be compressed. In this case, the neutral plane moves out of the layer.

$$\boxed{r = \frac{(w_1 E_1 t_1^2)^2 + (w_2 E_2 t_2^2)^2 + 2w_1w_2E_1E_2t_1t_2 (2 t_1^2 + 3 t_1t_2 + 2 t_2^2)}{6 w_1w_2E_1E_2t_1t_2 (t_1 + t_2) (\alpha_1 - \alpha_2)(T - T_0)}} \quad (3.7)$$

where w_1, w_2, t_1, t_2, E_1 and E_2 are width, thickness and Young's modulus of top and bottom material, respectively, $\alpha_1 - \alpha_2$ is the difference between thermal expansion coefficient of these two materials, and $\Delta T = T - T_0$ is the temperature change between the initial and increased temperature [2]. Following assumptions are made to derive this model :

- The distortion is within the elastic region of the materials,
- There is a linear strain distribution through the thickness of the cantilever,
- Materials are considered to be isotropic and uniform,
- There is no stress along the thickness direction,
- The temperature distribution is uniform over the whole beam, and
- Material properties remain constant.

3.2.2 Residual Stress

Generally, at room temperature all the fabricated bimorph cantilevers have a common situation of non-zero tip deflection due to residual stress in the layers. Nearly all films , irrespective of the method by which they are deposited, are found to have non-zero residual internal stress in them. The stress can either be tensile or compressive. Residual stresses developed in the material are composed of intrinsic stress and thermal stress. Intrinsic stress is developed during the nucleation of film and thermal stress is developed due to deposition thermal conditions. Intrinsic stresses are not yet completely comprehended. Several stress-causing mechanisms have been proposed. Some of them are: rapid film growth, lattice mismatches between the film and substrate, recrystallization processes, inclusion of impurities into the film and transformations of phases [15],[16],[17]. The stress value defined in the various literatures should be taken as a reference not as precise values. Even though the film is developed in the same conditions as published data, still the results can be inconsistent. Over-all in a film the intrinsic stress depends on rate of deposition, thickness, ambient pressure, deposition temperature, method of film preparation, type of substrate and machine used for development (fabrication) , and several other factors.

G. Lammel et al. stated [20] that the initial curvature and thermally induced curvature are additive by analyzing the internal stresses. Thus, for example, a zero deflection state can be attained by changing the temperature.

3.3 Stress Correction

Stress in thin films can be avoided in certain ways [21]. Some of those have been mentioned below:

1. use of material with zero or minimal internal stress
    - Single crystal bulk silicon (SCS) has zero stress as it is a homogeneous material with perfect lattice structure.
    - Parylene, a polymer, which can be deposited by CVD at room temperature, has negligible stress.
2. optimizing fabrication process parameters in order to control stress that are generated during deposition of materials
    - Process induced stress in polysilicon and silicon nitride can be reduced by tuning gas mixture, growth rate and pressure.
3. sandwiching of a tensile layer between two compressive stress layers or vice versa to nullify the effective stress gradient between the top and bottom surfaces as shown in Fig. 3.5.
4. Tensile-Compressive-Tensile sandwiched (composite) layers; SiN - SiO2 –SiN

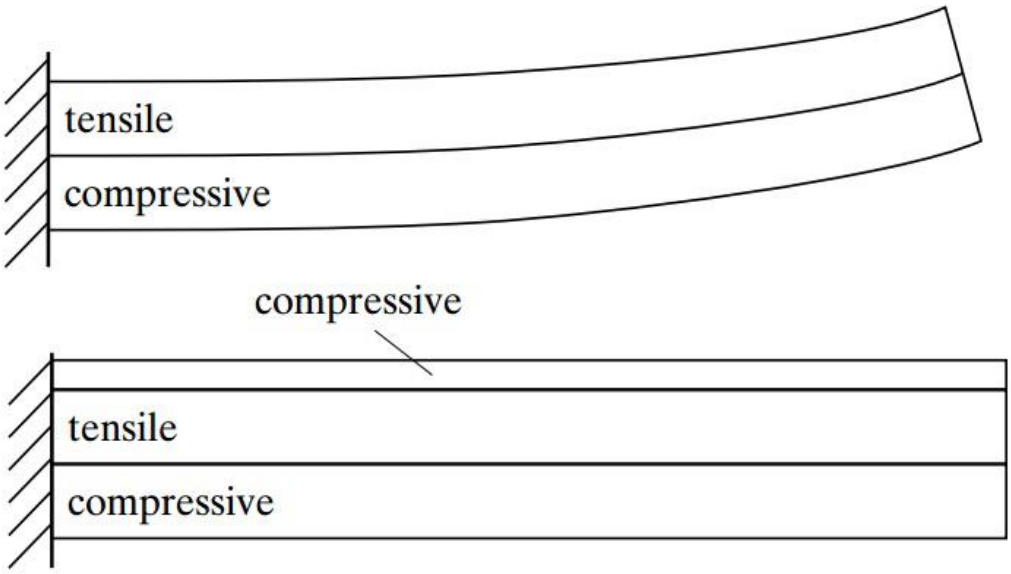


Figure 3.5: Counter balancing the bending moment between the two layers by depositing a third layer on top which produces an opposite (downward) bending moment to get an unbent beam.

3.4 Deflection

The deflection of the tip of a thermal bimorph cantilever can be derived from Fig. 3.6 :

$$d = r - r\cos\theta = 2r\sin^2\left(\frac{\theta}{2}\right) = 2r\sin^2\left(\frac{L}{2r}\right) \quad (3.8)$$

where, θ/2 is defined as the angle of deflection, r is the radius of curvature and L is the length of the cantilever [1]. For simplification, neglecting the small change in length due to expansion, $L \cong L_0$.

For small angles, $\sin(\theta/2) \cong \theta/2 = \frac{L}{2r}$, thus equations 3. and 3.10 combine to give:

$$d = 0.5r\theta^2 = L^2/2r \quad (3.9)$$

Therefore, the tip displacement is linearly proportional to the difference of the TECs of the two materials and the temperature change, inversely proportional to thickness and quadratically proportional to the length of the bimorph. The force due to thermal stress generated by the bimorph is given by applying Hook's Law: $F = kd$, with k the stiffness coefficient of bimorph which depends on the Young modulus of materials and the bimorph area moment of inertia. When used as an actuator, a thermal bimorph cantilever needs to generate a large tip deflection for a given change in temperature. The thin and long beams with large TEC difference will have large deflection according to equation 3.7.

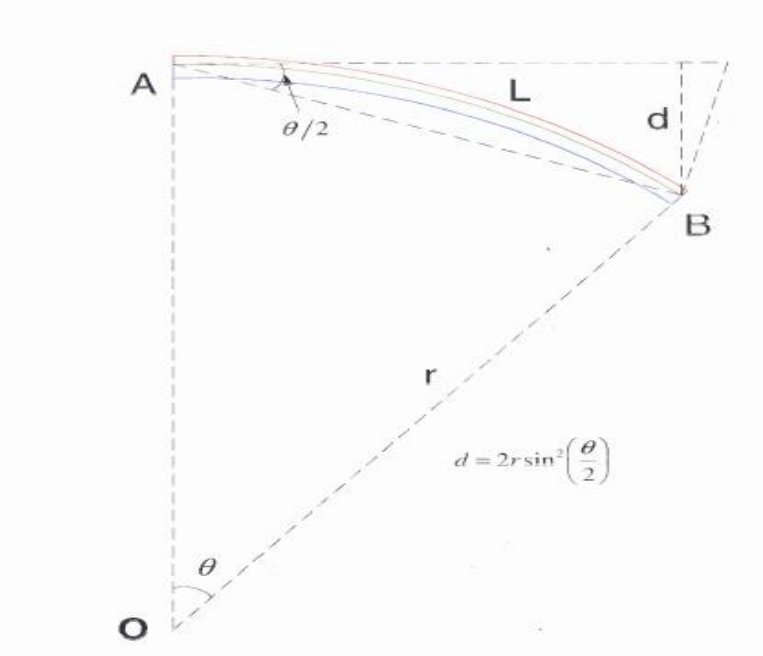


Figure 3.6 Schematic of bent bimorph cantilever

3.5 Materials used in Bimorph

The selection of materials to be used to form a bimorph plays an important role in achieving the desired performance in a design. To ensure high displacement and fast response, several parameters must be prudently balanced. The Young's modulus of elasticity, E , defines the force required to elastically compress or expand the material. Thus it plays a crucial role in the displacement and output force in a bimorph [6]. The thermal expansion coefficient (TEC) is an important property to be considered as the difference between the TEC of two materials straightforwardly indicates the maximum displacement, more the difference more is the displacement that can be achieved in the bimorph. The specific heat and thermal conductivity of the material determine the thermal frequency response of the bimorph whereas the maximum achievable temperature is determined by its electrical conductivity. The melting point of the material indicates the temperature range in which the material can operate safely. Lastly, for reliability , the ability of the materials to retain their strength at high temperatures and after many heating/cooling cycles is also crucial. In that regard, refractory materials are preferred.

The Al/SiO_2 combination is mostly used in bimorph [8]. The difference between the TEC is very high as compared to any other combination. The surface machining process for these is two is widely developed and moreover aluminum is cheaper than other metals.

The properties of materials that are commonly used in bimorphs is given in Table 3.1.

Table 3.1 Material properties at room temperature [16]

	Density (kg/m^3)	Young's Modulus (GPa)	Poisson's Ratio	TEC ($10^{-6}/K$)	Thermal Conductivity (W/m·K)	Heat Capacity (J/kg·K)	Electrical Resistivity (Ω·m)
Si	2330	169	0.3	2.6	148	705	2300
P-Si	2230	165	0.23	2.8	148	705	2300
SiO_2	2200	75	0.17	0.5	1.4	835	∞
Si_3N_4	3100	380	0.27	1.6	30.1	710	∞
Al	2700	70	0.35	23.1	237	898	2.655e-8
Au	19300	78	0.35	14.1	315	128	2.35e-8
Cr	7150	248	0.3	4.9	93.7	447	1.29e-7
Cu	8960	128	0.36	16.8	398	384	1.673e-8
Ni	8900	206	0.3	12.7	90.7	443	6.84e-8
Ti	4510	116	0.32	8.6	21.9	522	4.2e-7

3.6 Thermal expansion coefficient

Coefficient of linear thermal expansion

The linear thermal expansion coefficient of a material indicates the rate of change in length of the cantilever on changing the temperature. The values of coefficient of linear thermal expansion, α varies from 10^{-6} to 10^{-7} per degree kelvin [2].
It is expressed in units of simply K^{-1} or µstrain/K (1 µstrain/K = 10^{-6} K^{-1}).
It may also change with temperature when thermal expansion through a wide range of temperature is considered.
The change in length with temperature can be given by:

$$\Delta L = L\,(\alpha\,\Delta T) \tag{3.10}$$

where, L is the length of the cantilever, ΔT is the difference between the applied temperature (T) and room temperature (T_0).

$$\Delta T = T - T_0$$

Volumetric thermal expansion coefficient

The volumetric thermal expansion coefficient (β) indicated the change in dimensions along all the three axis due to change in temperature.
For a differential element of original volume, V:

$$\text{Volumetic strain} = \frac{\Delta V}{V} = (1+\varepsilon_x)(1+\varepsilon_y)(1+\varepsilon_z) - 1 = \beta\,\Delta T = 3\alpha\,\Delta T \tag{3.11}$$

where, ε_x , ε_y and ε_z are the strain in x, y and z direction respectively.
The volumetric change with temperature is given by:

$$\Delta V = V\,(\beta\,\Delta T) \tag{3.12}$$

Chapter 4

Understanding Electrothermal Physics and Structure

The principle of operation of electro-thermal actuator is non-uniform Joule heating which leads to differential thermal expansion and hence results in the distortion of the structure. In order to understand the actuation behavior of an electrothermal bimorph actuator, it is very important to understand the electro-thermal response of the actuator to an applied electrical input and thermo-mechanical response to a change in temperature [3]. Thermomechanical models of bimorph actuators are well established, and they have been used for MEMS bimorph actuators. Meanwhile, electrothermal models have been developed for several MEMS bimorph actuators. All these models have been developed considering uniform temperature distribution along the surface. But generally most actuators exhibit a non-uniform temperature distribution and a non-zero thermal coefficient of electrical resistivity (TCR), which results in a complex relationship between the electrical inputs and the thermal outputs of a device.

4.1 Thermal Physics

Thermal Physics is based on heat transfer which is the exchange of heat energy between systems.

Heat transfer is the flow of energy in terms of heat. The direction of heat transfer is from a region of high temperature to another region of lower temperature [22].

Heat transfer occurs until thermal equilibrium is achieved, at this point all involved system and the surroundings reach the same temperature. Thermal expansion is the ability of material to change its dimensions in response to a change in temperature. Heat can be transferred in three different modes: conduction, convection, and radiation.

4.1.1 Fourier's Law of Heat Conduction

Heat conduction is the transfer of internal energy of a physical body from the hot part to the cold part of the body. Heat is transferred at microscopic scale by vibration of atoms or when energetic electrons move from one atom to another. Conduction is the major mode of heat transfer within a solid object and in between solid objects which are in thermal contact. Solids such as metals are good conductor of heat while liquids and gases are less conductive. In short, conduction is the transfer of heat energy from the more energetic particles of an object to the adjacent less energetic particles resulting from interactions between the particles, and is expressed by Fourier's law of heat conduction as [22]:

$$Q_{cond} = kA\frac{dT}{dx} \tag{4.1}$$

where, k is the thermal conductivity of the material in W/m.K
A is the area normal to the direction of heat transfer
dT/dx is the temperature gradient.

The thermal conductivity is defined as the rate of heat transfer through a unit thickness of the material per unit area per unit temperature difference. It is the property of material to conduct heat through it. More the thermal conductivity faster is the heat transfer in the body.

4.1.2 Convection: Newton's law of cooling

Convection is the mode of heat transfer between a solid surface and an adjacent liquid or gas that is in motion, and involves the combined effects of conduction and fluid motion [23].
The rate of convection heat transfer is expressed by Newton's law of cooling as:

$$Q_{conv} = h(T_s - T_\infty)A \quad (4.2)$$

where, h is the convection coefficient in W/m^2K , A is the surface area through which convection heat transfer take place, T_S is the absolute temperature of fluid (in Kelvin) and T_∞ is the temperature of the fluid sufficiently far from the surface (in Kelvin).

Table 4.1 Typical values of convection heat transfer coefficient.

S. No.	Type of convection	Convection Coefficient (w/m^2K)
1.	Free convection of gases	2-25
2.	Free convection of liquids	10-1000
3.	Forced convection of gases	25-250
4.	Forced convection of liquids	50-20,000
5.	Boiling and condensation	2500-100,000

Convection is mainly of two types: natural convection and forced convection. In natural convection the flow of heat within fluid occurs naturally without application of any external force, this occurs when the fluid is expanded by thermal expansion and hence simulates its own transfer. In forced convection the flow is forced in the fluid by some external force such a pump, fan or any other mechanical means.

4.1.3 Radiation: Stefan Boltzmann Law

Radiation is the energy emitted by matter in the form of electromagnetic waves (or photons) as a result of the changes in the electronic configurations of the atoms or molecules [22]. The maximum rate of radiation that can be emitted from a surface having area A, at a thermodynamic temperature T_R is given by the Stefan Boltzmann law as:

$$E = \varepsilon \sigma T_R^4 \quad (3.3)$$

where, ε is the emissivity of material , σ is the Stefan-Boltzmann constant, and T_R is the absolute temperature (in Kelvin).
Thermal radiation occurs through a vacuum or any transparent medium (solid or fluid). It is the energy emitted by a matter as electromagnetic waves, due to the pool of thermal energy in all matter with a temperature above absolute zero. Thermal radiation is a direct result of the random movements of atoms and molecules in matter. Since these atoms and molecules are composed of charged particles (protons and electrons), their movement results in the emission of electromagnetic radiation, which carries energy away from the surface.

4.2 Joule heating

Joule heating which is also known as resistive heating or ohmic heating, is the process by which the flow of an electric current through a conductor produces heating effect. Joule heating is the most widely used phenomena in the world. When a potential is applied across a conductor, an electric current flows through it. This flow of current generates heat in the conductor due the internal resistance offered by the conductor to the current flow. In order to overcome this resistance work is done and is generated in terms of heat [13].

The joule heating effect is governed by Joule's first law, also known as the Joule–Lenz law, which states that the power of heating generated by an electrical conductor is proportional to the product of its resistance and the square of the current. The heat generated in a conductor is:

$$P=i^2R \tag{4.4}$$

where, i is the current flowing in the conductor
R is the resistance offered by the conductor.

4.2.1 Lumped element modeling

A simple modeling of the bimorph actuator is through the lumped element approach. This method, although not as accurate as a full finite element numerical model, allows us to quickly isolate the important parameters and interdependencies. We apply this method to the thermal and subsequently the mechanical domains of the system. This process is described below [24].

Joule heating is usually the preferred mechanism used to heat the bimorph, either through an external heater element or through the bimorph layer itself. The thermal resistance increases as we move further away from the heat sinking anchor, along the length of the bimorph beam. Furthermore, as electrical resistance is a function of temperature, heat generation is also non-uniform along the bimorph. As a result, the bimorph exhibits non uniform temperature distribution along its length and should ideally be modeled as a distributed thermal RC line, charged by distributed joule heat sources. However, for the sake of simplicity, the system thermal time constant can be roughly approximated by a single heat capacitance $C_{th,b}$ charged through a heat resistance $R_{th,b}$. A more elaborate thermal model including thermal conduction, convection, an actuator load and thermal isolations can be seen in Figure 4.1. Explanations of the parameters are found in Table 2. In general, thermal resistances depend on the cross-sectional area and material thermal conductivity and thermal capacitances are a function of mass and material specific heat. Convection depends on the surface area and the coefficient of convection h, which includes information on the medium (air) and the type of convection (forced or natural).

Thermal isolations decouple the thermal response between the different parts [26]. Given sufficient isolation, a fast response can still be achieved even with a big thermal capacitance attached as an actuator load. Also, from the schematic in Figure 4.1 we can infer that heating up and cooling down times can be minimized by removing the thermal isolation to the anchor to allow for unobtrusive thermal conduction. In this case and for large $R_{th,isol.load}$, the bimorph thermal time constant is approximately

$$\tau_{th} = R_{th,h,b} \sim l^2 \rho C/k \tag{4.5}$$

where k and C are the material thermal conductivity and capacitance respectively , l is the actuator size and ρ is the material density . The thermal cutoff frequency of the system is thus given by:

$$f_{T,h} = 1/2\pi\tau_{th} \quad (4.6)$$

From these equations it is obvious that fast response is achieved with an overall small actuator size and materials of high thermal conductivity and small specific heat [25]. In Table 3 we summarize the parameters of the thermal model and their physical correspondence.

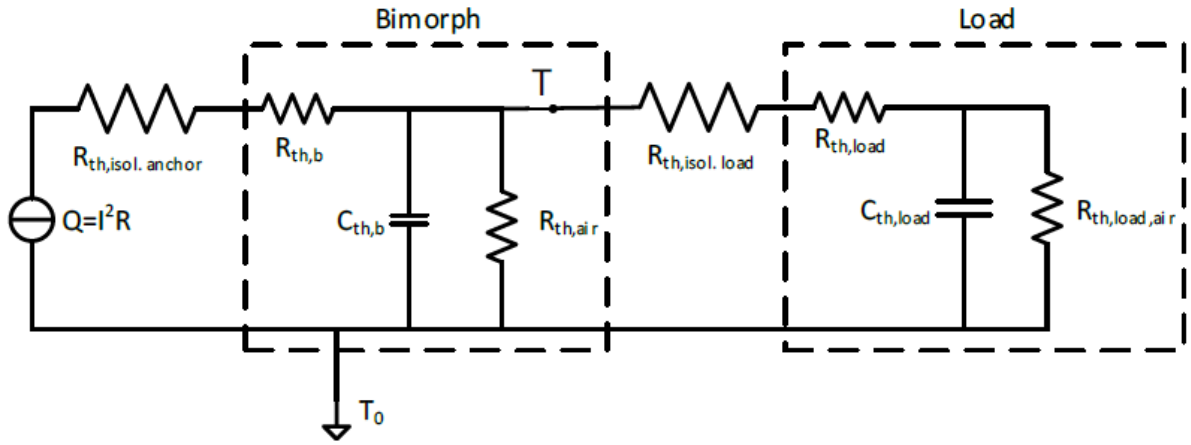


Figure 4.1 Thermal model

Table 4.2 Explanation of symbols: k – thermal conductivity, Cp – specific heat, hair – convection coefficient, m – mass.

Parameter	Description	Physical Dependency
$R_{th,b}$	Bimorph thermal conduction resistance	k_1, k_2, cross-section (t_1, t_2, w_1, w_2)
$C_{th.b}$	Bimorph thermal capacitance	$Cp_{,1}$, $Cp_{,2}$, m_b
$R_{th,air}$	Bimorph thermal convection resistance	hair, total bimorph surface area
$R_{th,load}$	Load thermal conduction resistance	k_{load}, cross-section
$C_{th.load}$	Load thermal capacitance	$Cp_{,load}$, m_l
$R_{th,load,air}$	Load thermal convection resistance	h_{air}, total load surface area
$R_{th,isol.\ anchor}$	Anchor-bimorph junction thermal resistance	$k_{isol..anchor}$, cross-section
$R_{th,isol.\ load}$	Load-bimorph junction thermal resistance	$k_{isol.\ load}$, cross-section
T_0	Ambient temperature	

The mechanical model of the system takes as input the temperature of the bimorph, translates it to thermal force and applies this force to a second order under-damped spring mass system to produce displacement. The schematic can be seen in Figure 4.2. The thermal model output *T* is considered through the variable ΔT, which is defined as $\Delta T = T - T0$. F_{TH} is the thermal bending momentum, given by $F = kd$ for a simple mass spring system, and is related to ΔT

through the equations mentioned above [26]. *k* is the actuator stiffness and it is related to the effective Young modulus of all the layers. *m* refers to the actuator mass and *b* is a parameter related to the amount of mechanical damping in the system. Frequency-wise, this model only predicts the bimorph resonance at its lowest, natural frequency and not any higher frequency modes. This is sufficient for our purposes, as actuation in higher frequencies is usually not achievable. Finally, in Table 4.3 there is an overview of the mechanical model parameters and their physical interpretation.

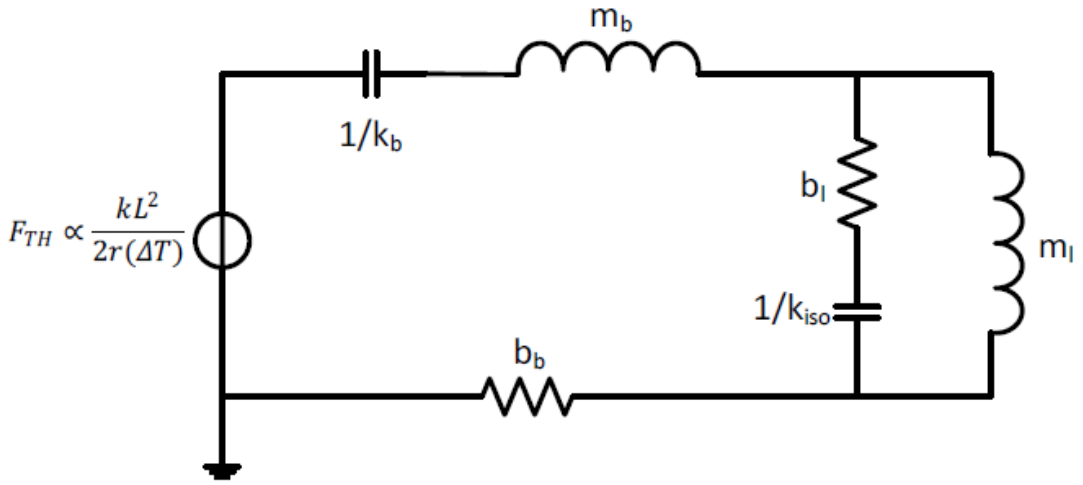


Figure 4.2 Mechanical model. Subscripts b and l stand for bimorph and load respectively, while iso is for isolation.

Table 4.3 Explanation of symbols: E – Young modulus, Δα – difference in thermal coefficient of expansion between the two materials.

Parameter	Description	Physical dependency
K	Effective stiffness	E_1, E_2, t_1, t_2
R	Radius of curvature	E_1, E_2, t_1, t_2,w_1, w_2, Δα, ΔT
M	Mass	
B	Total damping through air, mechanical clamping points, thermoelastic losses,etc.	

In order for the lumped element model to give any meaningful predictions, we need to extract several material and geometry dependent parameters with sufficient accuracy. This however is difficult for certain parameters, such as total damping *b*, as there are no analytic expressions or even generally agreed upon models that we can immediately apply. As a result, the lumped element approach can be used only to get a qualitative estimation of which parameters are going to play a major role.

An insight gained from the lumped element model is the decoupling of the thermal cutoff frequency and the mechanical resonance frequency. In order to maximize the oscillations amplitude, it would be advantageous to have the mechanical resonance frequency of the system below or close the thermal cutoff frequency. At first glance this may seem not

possible because the mechanical resonance and thermal cutoff frequencies are initially widely apart and are both largely influenced in the same way by the system mass. However, we can de-couple the two by attaching a thermally insulated mass to the actuator, such as a movable platform. In this way, we can shift mechanical resonance to a lower frequency without affecting much the thermal cutoff frequency, effectively bringing the two closer together.

4.3 Flip over beam structure

In this design novel FOB structure has been used. Flip over beam (FOB) is also known as inverted series connected (ISC). In this structure two beams of inverted composition are connected to each other. It consists of three sections: L_1 L_2 and L_3. L_1 is made of thin layers of SiO_2/Au (non-inverted bimorph) , L_2 is made of thin layer of SiO_2/Au/SiO_2 (overlap) and L_3 is made of thin layers of Au/SiO_2 (inverted bimorph). It is called flip over beam because the layer composition of L_1 is just inverted version of L_3. Two such FOB structures are connected with a hinge or joint to form one folded dual S-shaped bimorph (FDSB) actuator structure. The main advantage of using folded dual S-shaped bimorph structure is that the tip bending of bimorph is nullified. When the voltage is applied across the structure the current flowing through it will increase the temperature of structure due to Joule heating. Due to this increase in temperature both gold and SiO_2 will try to expand and since they have different TEC, their expansion will lead to vertical deflection of the beam with some tilt angle. The inverted and non-inverted bimorph combination of FOB structure will cancel this tilt angle and lateral shift. Hence, pure vertical displacement is achieved using flip over beam structure. A simple FOB structure is shown in Figure 4.3.

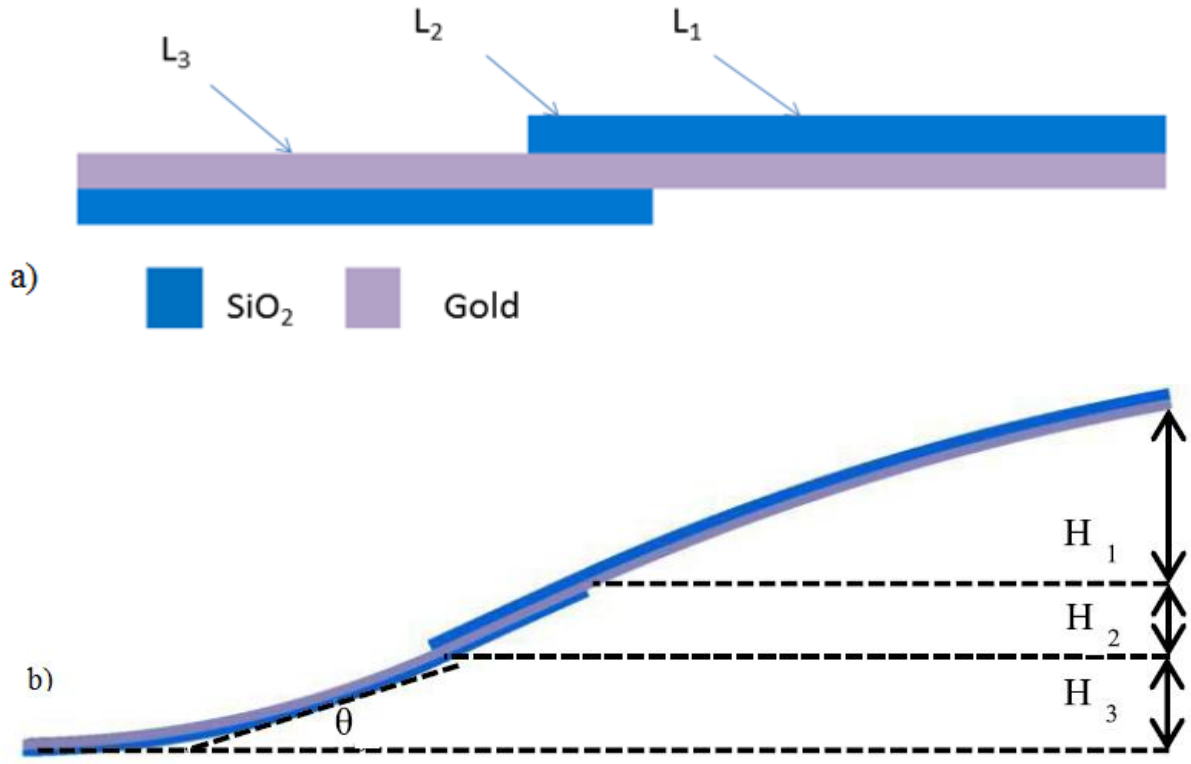


Figure 4.3 a) Cross sectional view of FOB b) vertical displacement on increasing the temperature.

In order to further increase the vertical displacement, three folded dual S-shaped beam actuators are connected with each other using a hinge made of gold. The vertical displacement of FSDB on increasing the temperature can be expressed as:

$$H = 4\,(H_1 + H_2 + H_3) \tag{4.7}$$

where, $H_1 = R_1\,(1 - \cos L_1/R_1)$, $H_2 = L_2 \sin\theta$, and $H_3 = R_3\,(1 - \cos L_3/R_3)$, and R_1 , R_3 are the radius of curvature of section L_1 and L_3 respectively. θ is the tip angle of inverted bimorph section where $\theta = L_3/R_3$. In order to calculate H_1 and H_3 it has been assumed that section 1 and section 3 have a uniform radius of curvature. The equation for H_2 is derived on the section by forming an approximately straight strain-compensated section.
In the design eight such FSDB structures with two on each side of mirror plate has been used as shown in figure 4.4. Using symmetric FSDB structures on all sides of mirror plate balances the plate, out of plane torque and provide pure vertical displacement of the plate on applying the voltage.

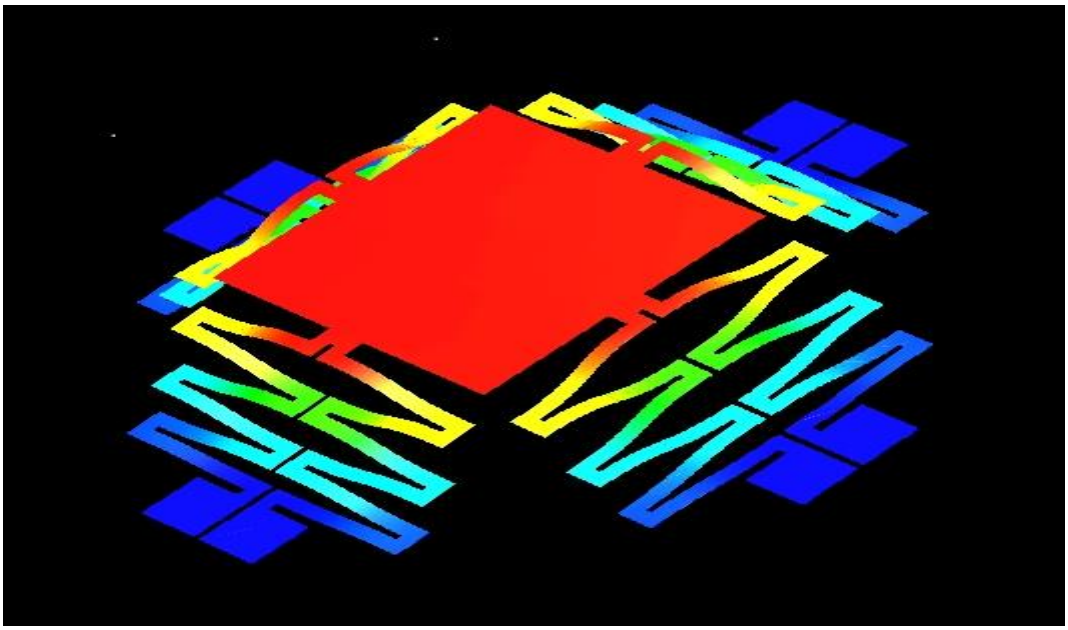


Figure 4.4 FOB based actuator design

4.4 Materials used

In this design, gold and SiO_2 have been used as the materials for bimorph. The main advantage of using this combination is that gold has very high melting point as compared to aluminum, so it can be used at high temperatures(more than 400K) while aluminum will start softening at this temperature. SiO_2 has been used instead of polysilicon because it is feasible to deposit silicon dioxide at low temperatures. Polysilicon can be deposited at temperatures greater than 800K. Deposition at this temperature can lead softening of pre-deposited gold layer. The TEC difference in gold and SiO_2 is sufficiently high and hence high displacement can be achieved using this combination. The properties of materials used in the design is included in table 4.4.

Table 4.4 Properties of materials used in the design

S.No.	Property	Gold	Polysilicon	SiO_2	Silicon
1.	Melting Point(in ºC)	1060	1000-1400	1728	1414
2.	Thermal Expansion Coefficient(in 1/K e-6)	14.1	2.9	0.5	2.33
3.	Thermal Conductivity(in W/m.K)	315	148	1.422	157
4.	Electrical Conductivity(in 1/Ω.m)	4.4e7	3.65e-4	7e-10	2e4
5.	Specific Heat(in J/Kg.K)	128.74	100	1000	712
6.	Tensile strength(in MPa)	127	800-2840	9520	6000
7.	Young's Modulus(in GPa)	78	165	66	169
8.	Density(Kg/m^3)	19280	2230	2200	2300
9.	Poisson's ratio	0.35	0.23	0.17	0.3
10.	Heat Capacity(J/Kg.K)	128	678	835	705
11.	Residual Stress(inMPa)	67-74(t)	-20MPa	-	-

Chapter 5

Design and Simulation

A large vertical displacement electrothermal bimorph actuator based on folded dual S-shaped structure has been designed. The actuator designed can be used for a variety of applications such as tunable filters, cavity resonators, DMDs, fourier transform spectroscopy, etc. In this structure bimorph has been used as a fundamental cell and it is based on the principle of electrothermal actuation. The central plate is suspended between the bimorph structures. As the bimorphs heat up and bend upwards, the central plate also go up with them. Depending on the voltage applied the central plate gets elevated to different levels above the surface of the wafer. An up and down motion of the central plate can thus be performed with the proper actuation sequence. The electro-thermo-mechanical simulation and study of the electrical, thermal and most importantly the mechanical behavior of the design is done using Coventorware.

5.1 FOB based design

The design is based on electrothermal actuation and uses flip over beam (FOB) series connected ladder type structure to lift the central mirror plate. The design provides large vertical movement of plate with ultra-low horizontal motion i.e. minor tilting. Gold and Silicon dioxide have been used as the materials for bimorph. Different modifications were made to the structures and finally an optimized structure has been designed.

a) Gold Plate

The first iteration of this design used gold plate as a mirror, shown in figure 5.1. Flip over beam bimorphs are used to lift the plate. The substrate is of silicon and bimorph is made of gold and SiO_2. The design is simulated for three different thicknesses i.e. 2 ,2.5 ,3 um of gold plate. The main limitation of this design is that the current is not restricted to the bimorphs.

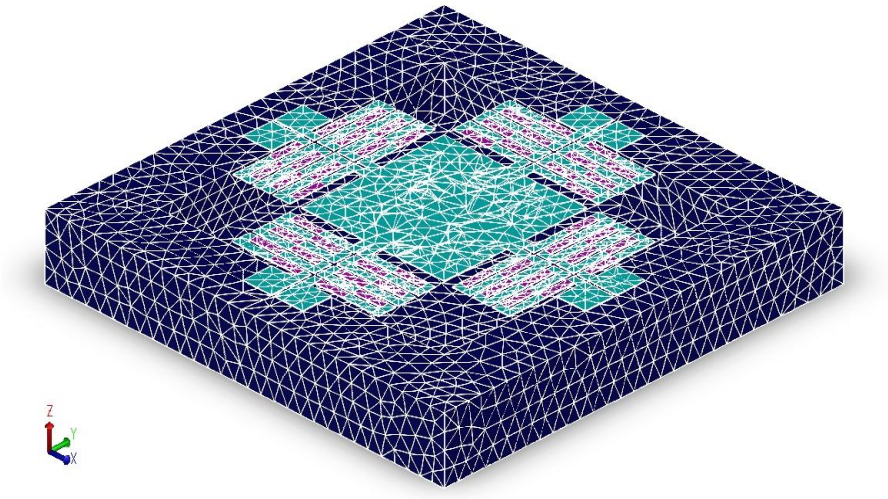


Figure 5.1 Gold plate actuator

Since plate is of gold and is in direct contact with meanders of bimorphs, current was flowing through the plate and due to this power is getting wasted in the plate and it itself bends due to thermal heating. With this design a displacement of 262um at 150mV voltage is observed in simulations.

b) SiO_2 Plate:

In an attempt to overcome the limitations of previous design, this structure was designed. In this particular design the central plate is made up of SiO_2 only which is in direct electrical contact with the meanders, shown in figure 5.2. Each pair of FOB is connected to the mirror plate with a pure joint of SiO_2. The advantage of this modification is that the current won't flow in the plate since SiO_2 is a dielectric. The current will be restricted to bimorphs and hence no heat loss through the plate will take place and the central plate will be thermally and electrically isolated from the lifting structure and won't deform. But this design has its own limitations. SiO_2 has very high internal stress in it because of which the plate is curled and moreover the use of dielectric as a plate make this design unusable for tunable filter applications. For the plate to act as a mirror plate it should be able to perturb the electric field in the cavity it is placed, so this design was rejected keeping tunable filter application in mind. A maximum displacement of 302 um is observed in simulations at 150mv voltage.

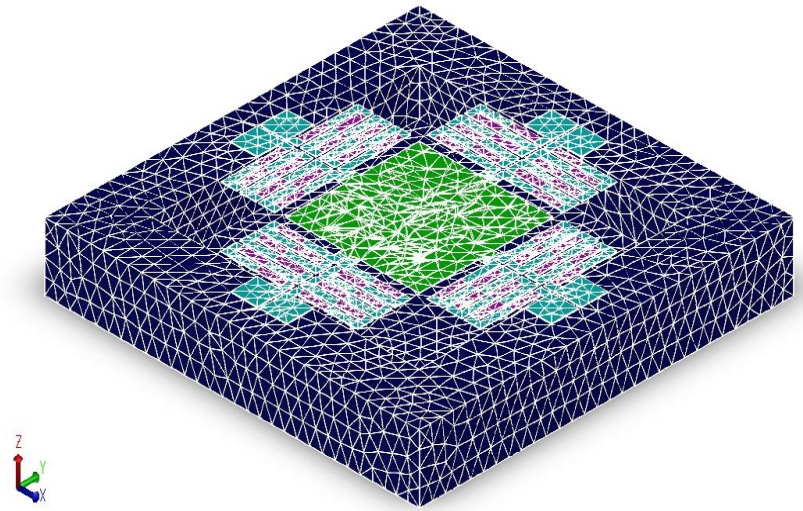


Figure 5.2 SiO_2 plate actuator

c) Gold and SiO_2 plate:

The third iteration of this structure is gold and SiO_2 plate which combines the advantages of both the design and gives no current through plate and applicable for tunable filter applications. The plate is made of SiO_2 and gold with SiO_2 under gold, figure 5.3. The SiO_2 plate is in direct contact with the FOB structures and ensures that the plate won't heat up and deform and then pass the motion to gold top plate which is in direct exposure to electric field. The structure is simulated for electrothermal actuation, conduction and convection losses. However, on application of voltage to the structure, the plate shows warpage issue. The plate is of SiO_2 and gold which itself form a bimorph, so on heating the plate will bend downwards or warped due to the bimorph effect. This warpage decreases the effective vertical displacement of the plate. The maximum displacement of this structure is 364 um at 150mV voltage.

Figure 5.3 Gold and SiO_2 plate actuator

d) Gold and SiO_2 Perforated plate:

In this design, the mirror plate is perforated and is made of gold and SiO_2. By perforating the plate, the problem of warpage reduces, figure 5.4. Current is limited to bimorphs as SiO_2 is a dielectric, it provides isolation to the mirror plate. Top plate is of gold which is a very good conductor, it easily perturbs the electric field. The design is simulated for electrothermal actuation, conduction – convection losses and initial stress bending. Tetrahedral meshing has been used. Stress in the structure is increased. With this structure a maximum displacement of 395 is observed in simulations when 150 mV potential is applied.

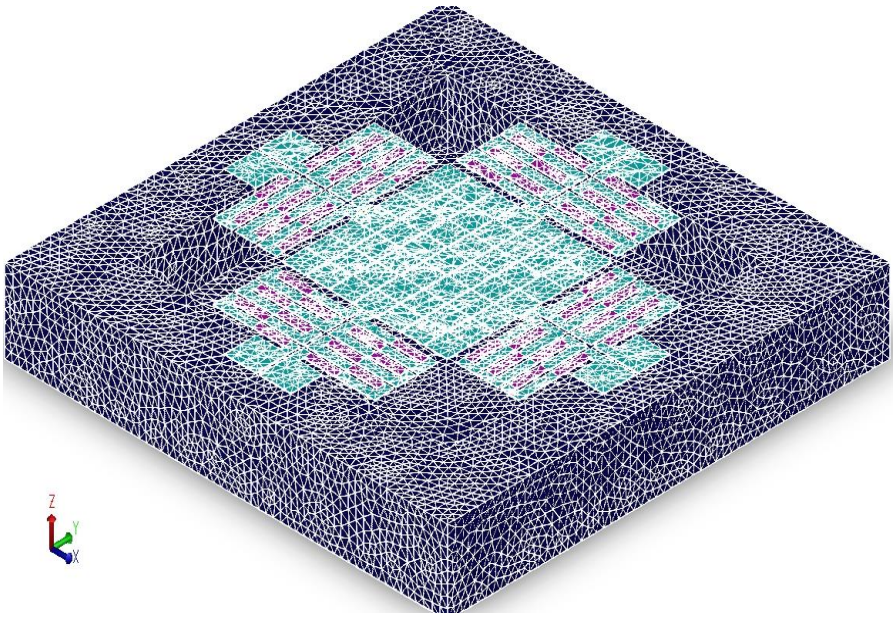


Figure 5.4 Gold and SiO_2 perforated plate actuator

e) Octagonal Plate:

In this design the gold and SiO_2 octagonal perforated plate is used as a mirror plate(Figure 5.5). The octagonal geometry of plate reduces warpage and rest of the advantages of previous

structure is also there. The design is simulated for electrothermal actuation, conduction – convection losses and initial stress bending. Tetrahedral meshing has been used. Stress in the structure is increased. A maximum displacement of 407um is obtained on simulations for 150mV applied potential.

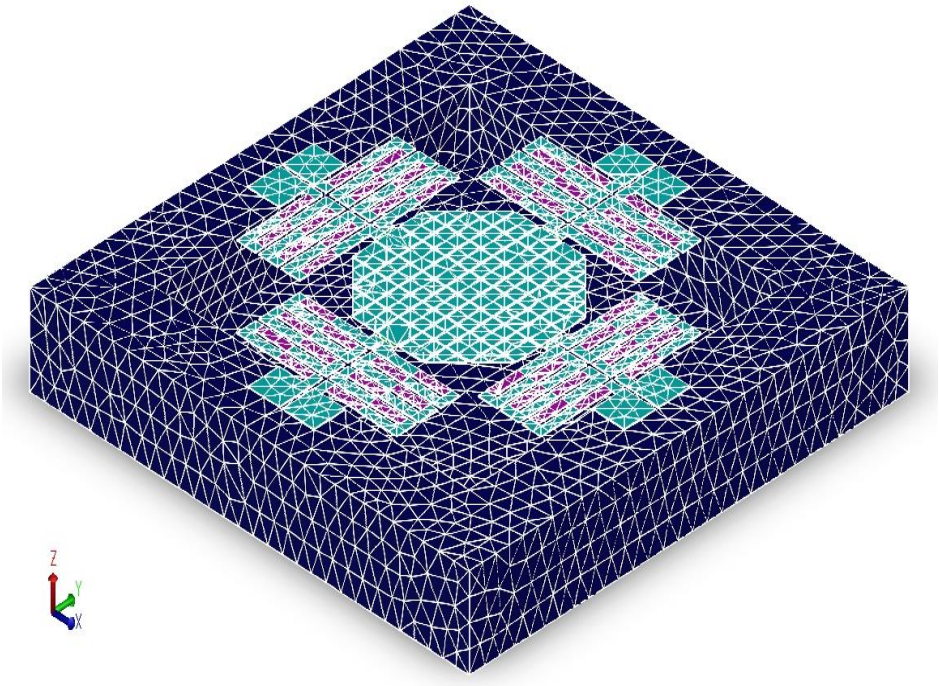


Figure 5.5 Gold and SiO_2 octagonal perforated plate actuator

Final Design: Gold plate on SiO_2 frame:

After all these iterations, a final structure is designed. In this design a perforated gold plate is used as a mirror plate and the plate is resting on a SiO_2 frame. SiO_2 frame provides electrical isolation to the plate from the FOB actuator structure and save electrical and thermal power by isolating the mirror plate from electric current and save plate from getting deformed. The frame of SiO_2 reduces the warpage as bimorph of gold and SiO_2 is present only on the frame area not the whole plate. All the advantages of above designs are combined to form one optimized structure that gives high vertical displacement with minimum warpage.

5.1.1 Design Features

1. Vertical movement of the central plate without and horizontal shift due to symmetrical positioning of the bimorph structures.
2. The gold-silicon dioxide bimorph has been split into flip over beam structures made in the bimorph region so as to increase the bending and vertical lift of the central plate.
3. Hinges have been avoided and instead flexible meander springs have been used to allow the bimorphs to move without causing the central plate to deform under stress.
4. Silicon dioxide used between the mirror and the bimorph structures to electrically and thermally isolate the mirror.
5. The mirror plate has been designed with three different thicknesses of gold layer to ensure its flatness.
6. Gold has been used as bimorph material as a contrast to aluminum which has been used in quite a lot of previous works.
7. The Gold plate is supported by a frame of Silicon dioxide.

5.1.2 Simulation Parameters

- Electrothermo-mechanical analysis, Thermo-mechanical analysis, Nonlinear, Steady state analysis.
- Convection-Radiation Heat Transfer
- Convection Coeffcient: 2W/m^{2}K (free convection of air)
- Emissivity: 0.03 (Polished Gold surface) Emissivity: 0.5 (PolySi & SiO_2)
- Ambient Temperature: 300K
- Potential: 0V to 0.15V with steps of 0.01V
- Tetrahedral meshing: 100
- Potential at contact pads of gold
- Fixed Temperature Surface BC 300 K at the bottom of Silicon Substrate
- Input heat energy provided by application of voltage results in joule heating.

5.1.3 Layout

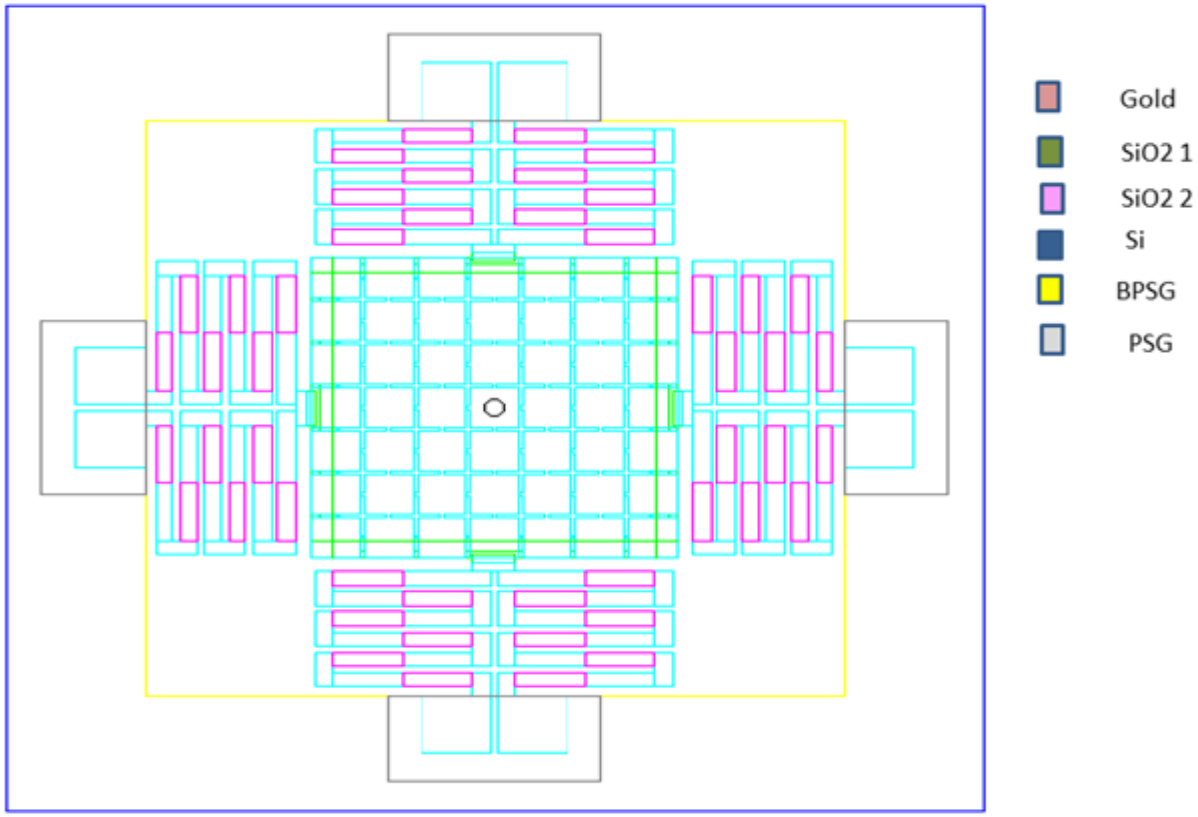


Figure 5.6 Design mask layout

The layout of the device presents the different masks stacked on top of each other as shown in Figure 5.6. The flip over beam geometry in the bimorph regions is visible in the layout.

The large yellow box is the sacrificial layer deposited in order to fabricate the cavity. The cyan mask represents the gold layer patterning. The green and magenta colour represents the silicon dioxide fins deposited above and below gold layer. The blue mask represents the substrate.

5.1.4 Material and 3D meshed model

Gold: anchor pads, bimorph frames, joint between the mirror and the bimorph, thick mirror plate.

Silicon dioxide: the second bimorph layer on top and below the gold layer, frame to support gold mirror plate.

Silicon: substrate to support the structure.

BPSG: sacrificial layer

The 3D meshed model is shown in figure 5.7.

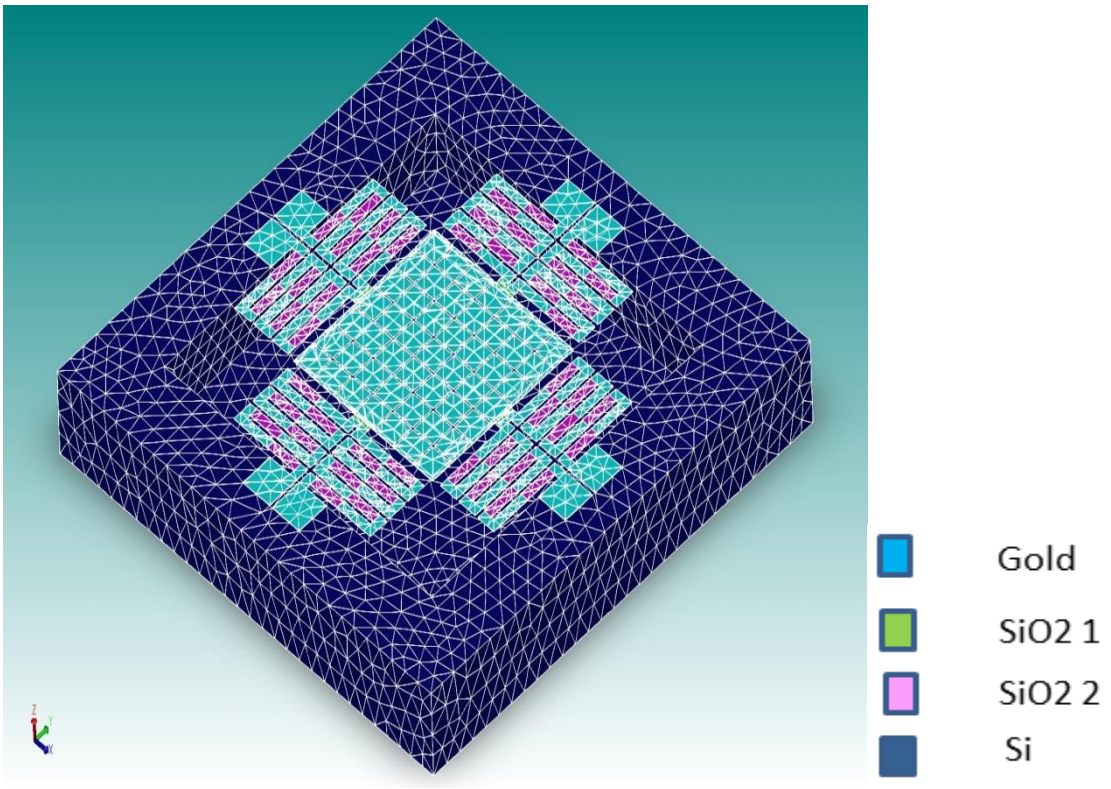


Figure. 5.7 Material & 3D meshed model

5.1.5 Device dimensions

The thicknesses of the different layers are as follows:

Gold: a) bimorph : 2um
b) anchor :3um
c) mirror plate: 2um

Silicon dioxide: a) bimorph : 1um
b) frame: 1um

Silicon: substrate 365um , Cavity: 300um.

The planar dimensions of the design are as follows:

The central mirror plate is of 1000um x 1000um.

The bimorph gold beam is of total length 400um and the silicon dioxide is of 200um with widths of 50um

The slits in the meanders are of length 500um and width of 20um.

The silicon substrate is of 2800um x 2800um.

The cavity is of 2000um x 2000um.
The frame is of 1000 x 900 um.

The dimensions of the design is presented in tabular form in table 5.1.

Table 5.1: Dimensions of the design

Structure	**Length(in µm)**	**Width (in µm)**	**Thickness (in µm)**
Gold beam	400	50	2,2.5,3
SiO2 beam (top)	200	50	1
SiO2 beam (bottom)	200	50	1
Plate(gold)	1000	1000	2,2.5,3
Frame(SiO2)	1000,900	900,1000	1
Silicon substrate	2800	2800	365
Cavity	2000	2000	300
Contact pad	200	200	3,3.5,4

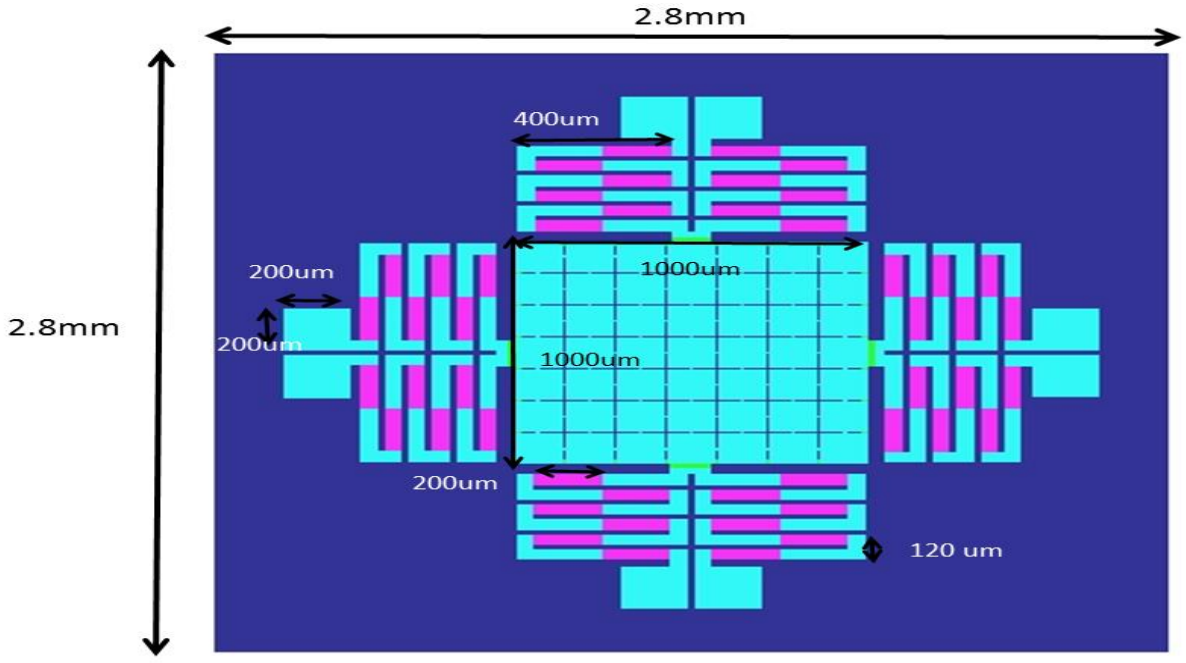


Figure 5.7 Design dimensions

5.1.6 Results

a) Deflection v/s applied voltage:

The maximum movement of the plate for 100mV voltage is observed to be 165.87um.

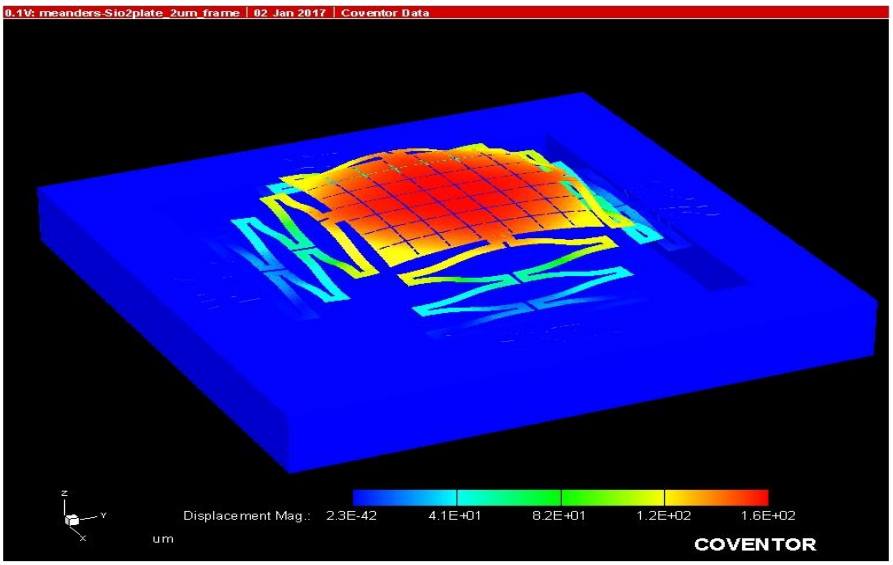


Figure 5.8 Deflection of the plate at 100mV voltage

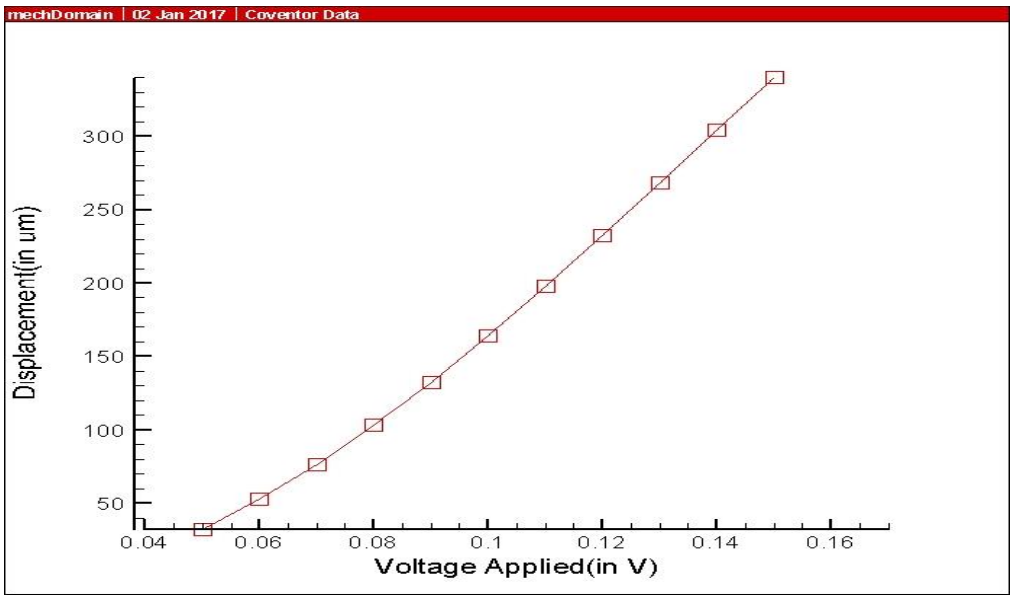


Figure 5.9: Deflection vs voltage graph

b) Temperature v/s applied voltage:

The temperature of the plate for 100mV voltage is observed to be 477 K .

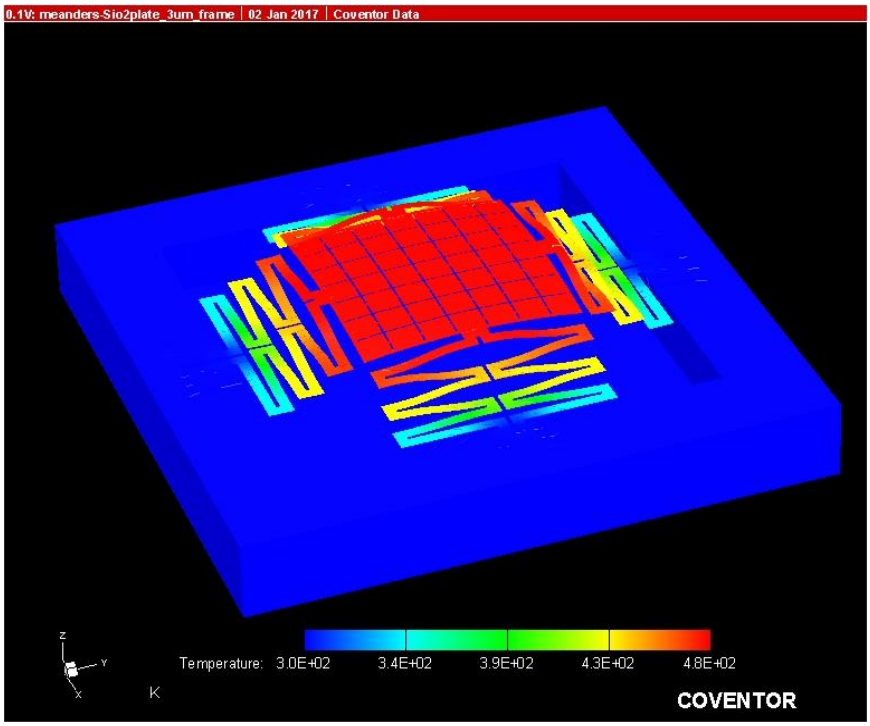


Figure 5.10 Temperature of the plate at 100mV

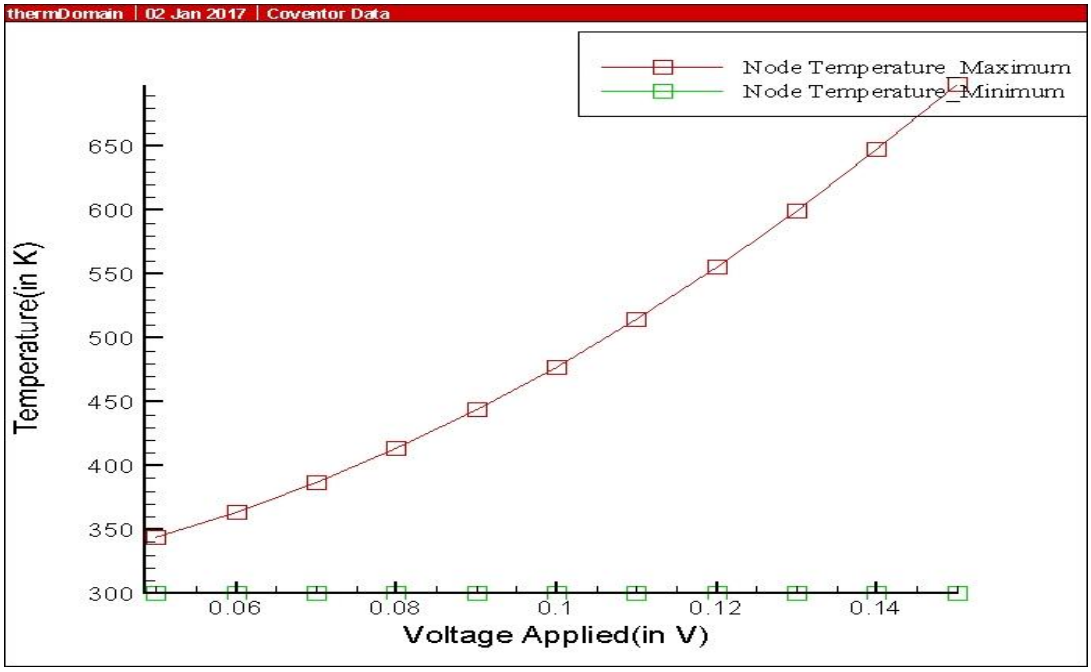


Figure 5.11: Temperature v/s Applied voltage

c) Pressure on structure at launch event:

Mass calculated using inertial mass analysis in Coventorware and is found to be 1.0e-7 Kg. During the launch event of a satellite a total thrust of 1000*g*m(approx.) is exerted on the device placed inside the satellite.

Using this approximation, this pressure has been calculated.

Pressure= (1000*9.8*1.0*10e-7)/(1000*1000*10e-12) = 1100 Pa

The maximum displacement at the above calculated pressure is 160 µm.

This structure can endure this initial displacement at the launch event without getting permanent damaged.

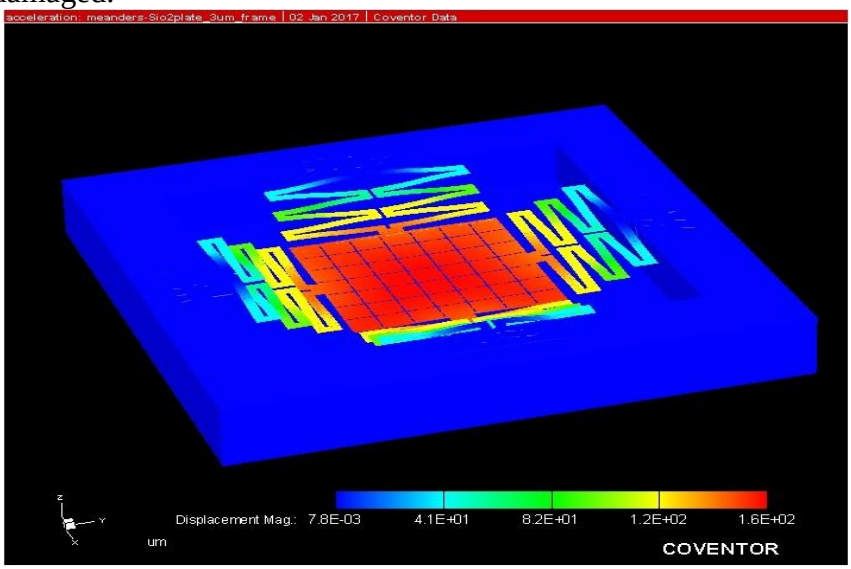


Figure 5.12 Displacement at initial launch event.

d) Initial displacement of structure:

The initial displacement of the released device resulting from intrinsic stress generated during fabrication at 300 K is found to be 62um (in –Z direction) and is shown below in the fig below. The internal stress of gold is considered to be 50MPa (tensile) and that of SiO2 is -50MPa(Compressive).

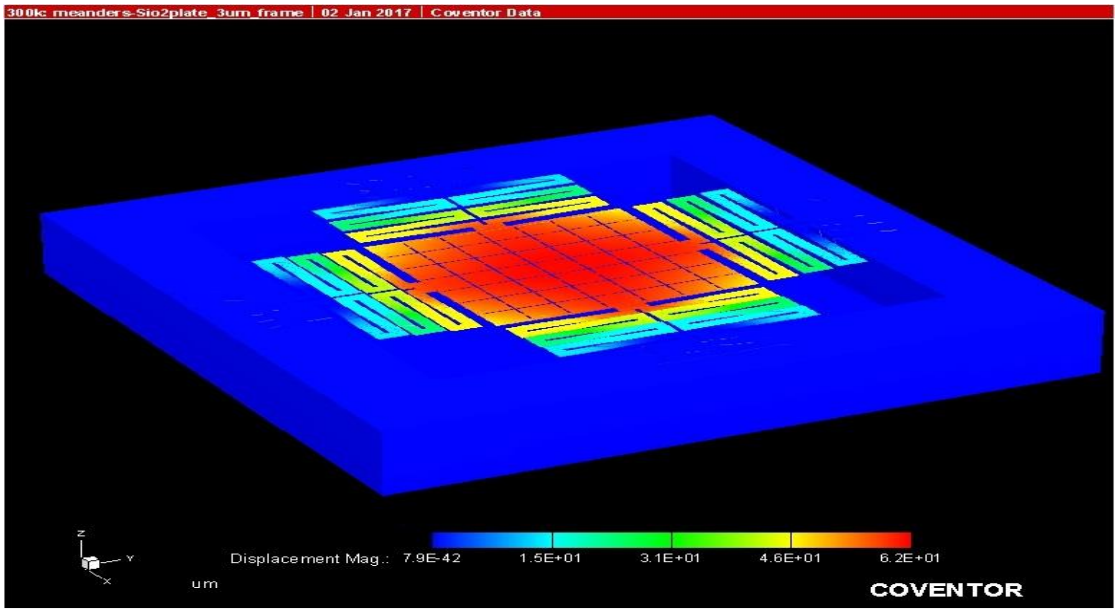
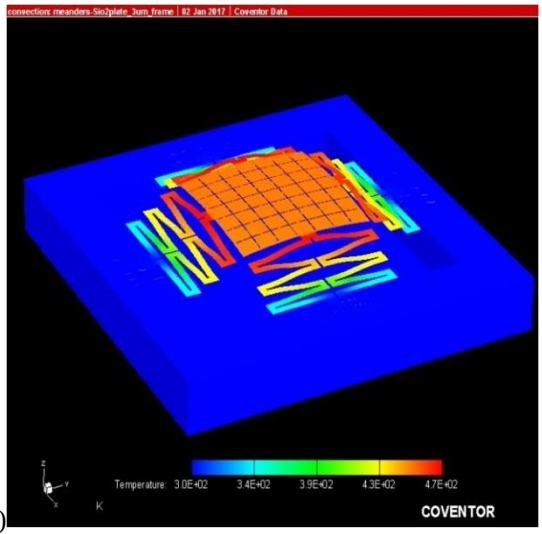


Figure 5.13 Displacement at 300K temperature.

e) Convection heat loss

The heat is lost from the structure due to air enclosed in the cavity. This convection loss can be calculated using Convection radiation boundary condition in MEMMech electrothermo-mechanical analysis. Convection coefficient of air is $2W/m^2$ K and emissivity for gold and SiO2 is 0.03 and 0.5 respectively.

a) 

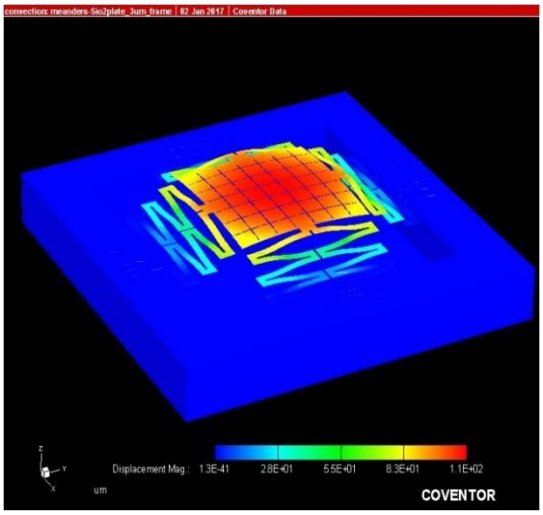
b) 

Figure 5.14 Convection loss a) displacement b) temperature

The maximum temperature of structure reduces from 478 K to 470 K and maximum displacement reduces from 115 to 110um for 100mV voltage applied at the terminals.

f) Potential

The potential is applied at the contact pads made of gold. A 100mV potential is applied for the simulation and then it is varied from 0 to 150 mV in the steps of 10mV.

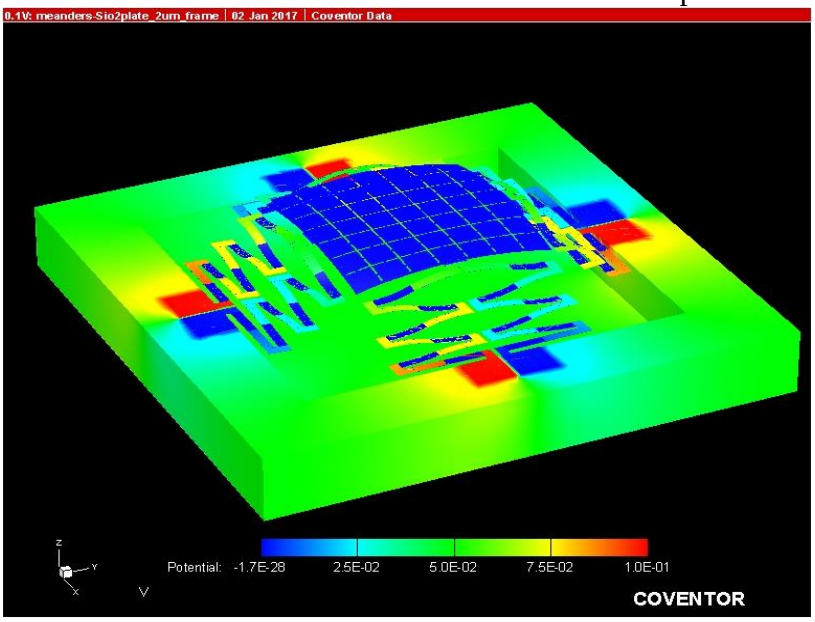


Figure 5.15 Potential applied at contact pads of device

g) Current Density

The current density in the structure for 100mV potential is 1.9e09 A/m^2. The current is limited to meanders and no current flows through the plate.

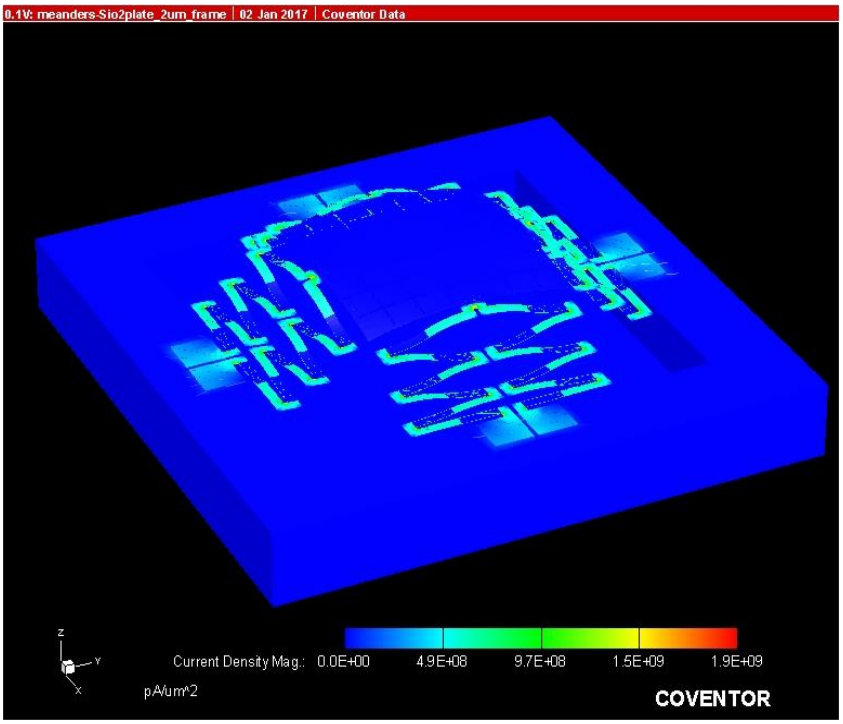


Figure 5.16 Current density in the structure

h) Stress

The stress in the structure at 100mV potential is 250 MPa which is less than the yield strength of the structure. So structure won't break.

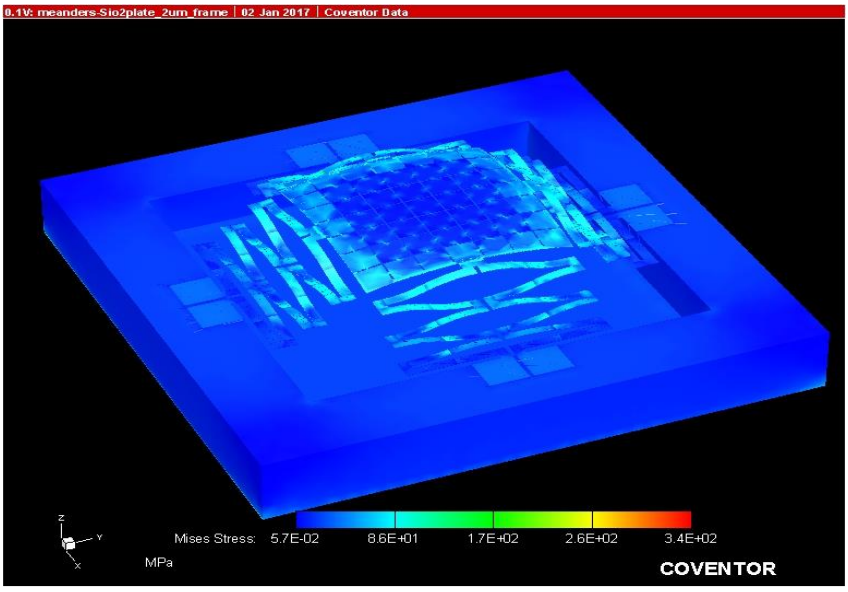


Figure 5.17 Stress generated in the structure

i) Heat Flux

The heat flux in the structure is 6.6e07 W/m^2. The heat is restricted to meanders of bimorph and does not flow into the plate.

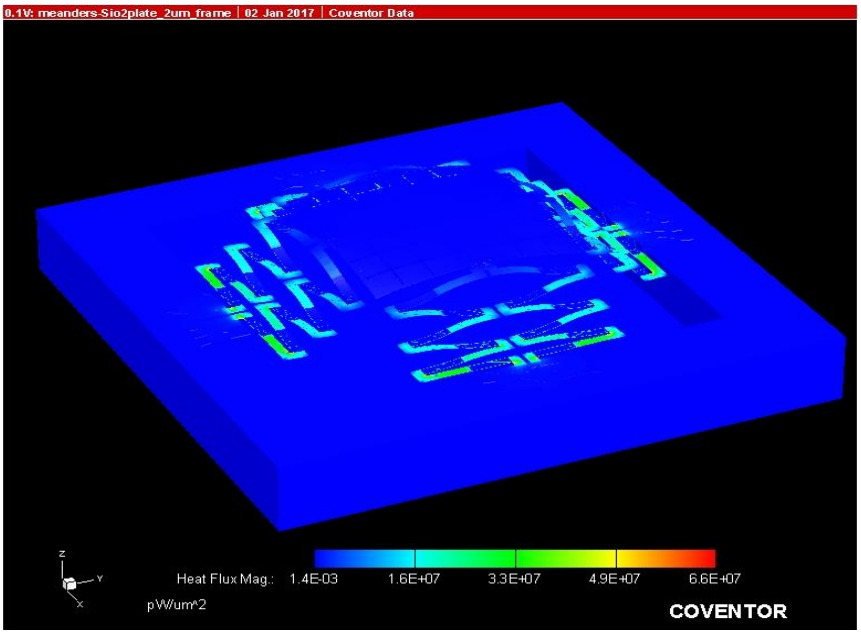


Figure 5.18 Heat flux in the design

5.1.7 Comparison of deflection for various thicknesses of gold plate

The design has been simulated for various thicknesses of gold plate i.e., 2um, 2.5um and 3um. With the decrease in thickness deflection increases but the stress in the structure also increases. The warpage in the plate decreases on increasing the thickness. At low voltages the deflection in the structure is almost same but as we keep on increasing the thickness the weight of the plate increases and because of this the vertical displacement of the plate decreases.

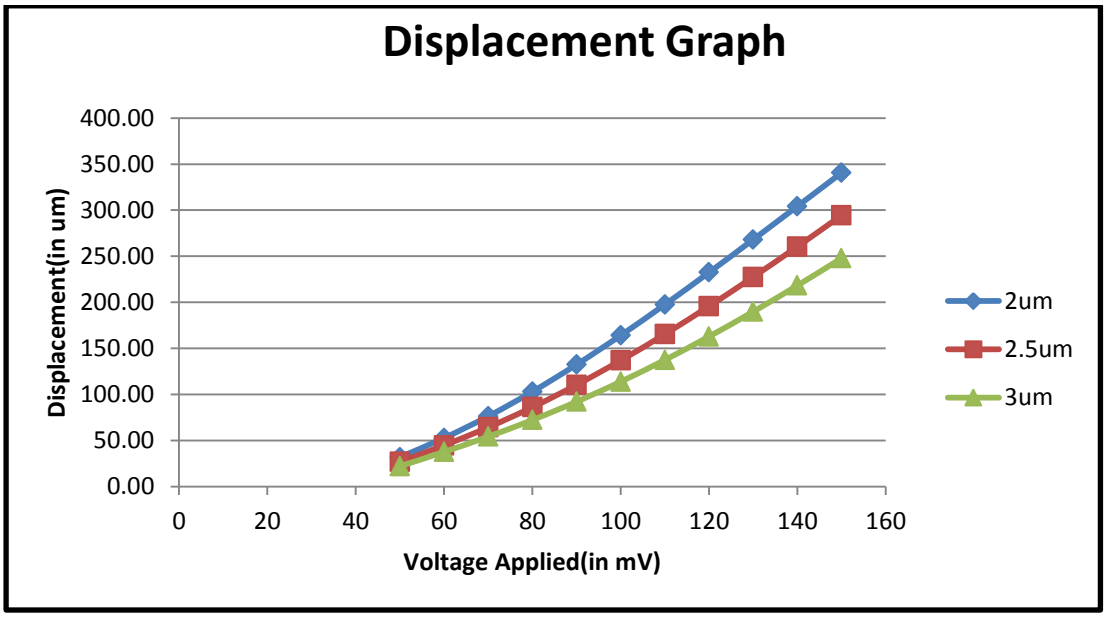


Figure 5.19 Displacement vs voltage applied for 2, 2.5, 3um thicknesses of gold

Table 5.2 Displacement vs voltage applied for 2, 2.5, 3um thicknesses of gold

S. no.	Voltage (in mV)	2.0µm		2.5µm		3.0µm	
		Temperature (in K)	Displacement (in µm)	Temperature (in K)	Displacement (in µm)	Temperature (in K)	Displacement (in µm)
1.	50	344	31.95	344	27.03	344	22.14
2.	60	363	52.76	363	44.81	363	37.69
3.	70	386	76.37	386	64.35	386	54.30
4.	80	413	103.03	413	86.18	413	72.33
5.	90	443	132.44	443	110.42	443	92.14
6.	100	477	164.14	477	136.92	477	113.89
7.	110	514	197.63	514	165.47	514	137.51
8.	120	555	232.43	555	195.77	555	162.89
9.	130	600	268.09	600	227.54	600	189.88
10.	140	647	304.25	647	260.49	647	218.23
11.	150	700	340.55	700	294.33	700	247.83

5.1.8 Comparison of displacement in different structures for 2um thickness

The different structures are compared in terms of the displacement of central plate at 100mV applied voltage. As it can be seen from the graph the octagonal perforated plate, square perforated structure shows more displacement of plate than frame design but there is high warpage of plate in these structures. The frame based design although doesn't shows maximum displacement among other structures but it ensures that the plate has minimum warpage and it remains almost flat on deflection and is the most optimized, reliable and accurate design.

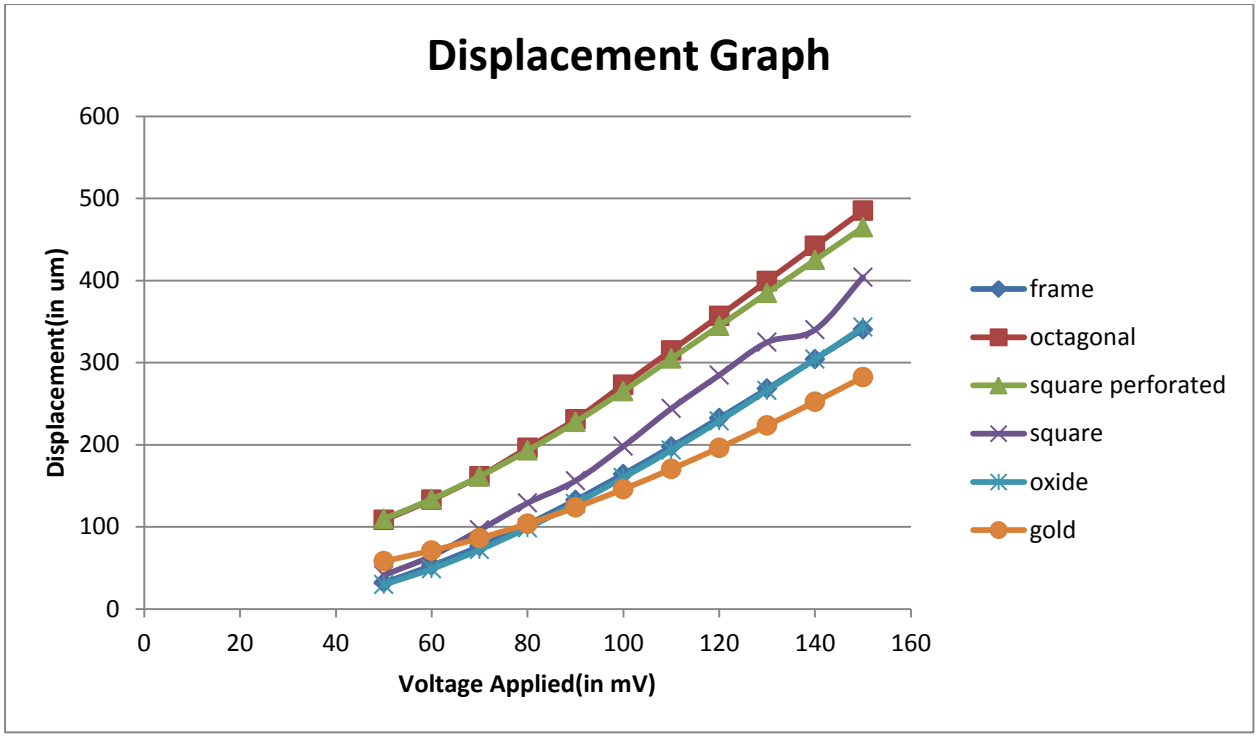
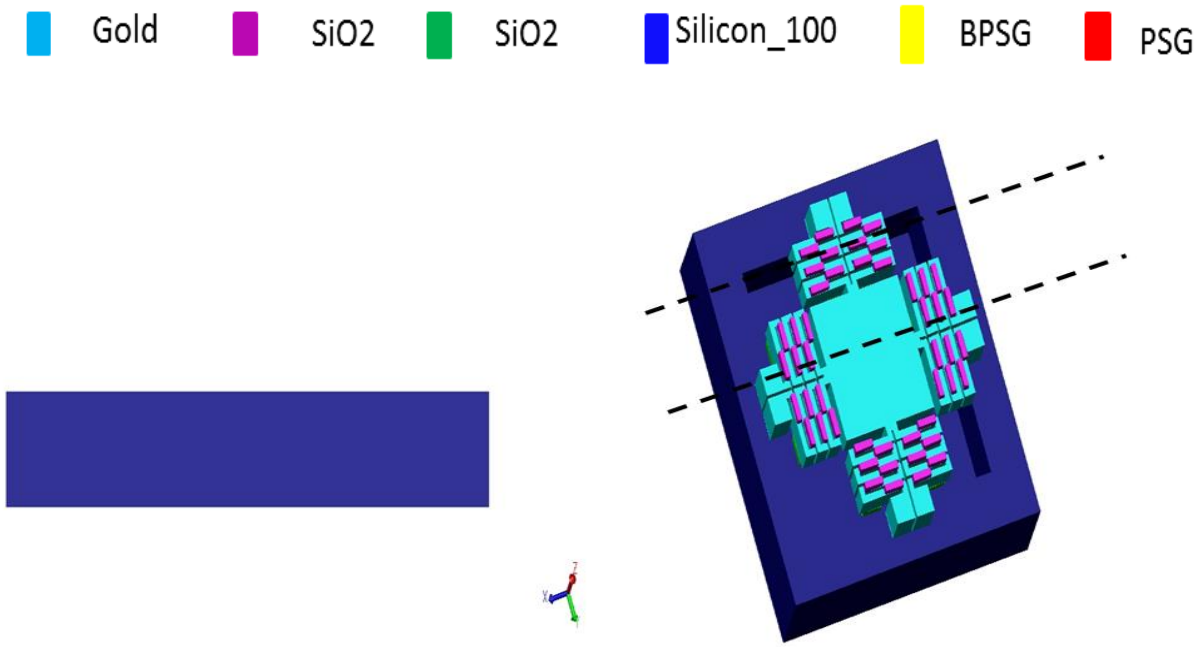


Figure 5.20 Comparisons of displacement of different structures

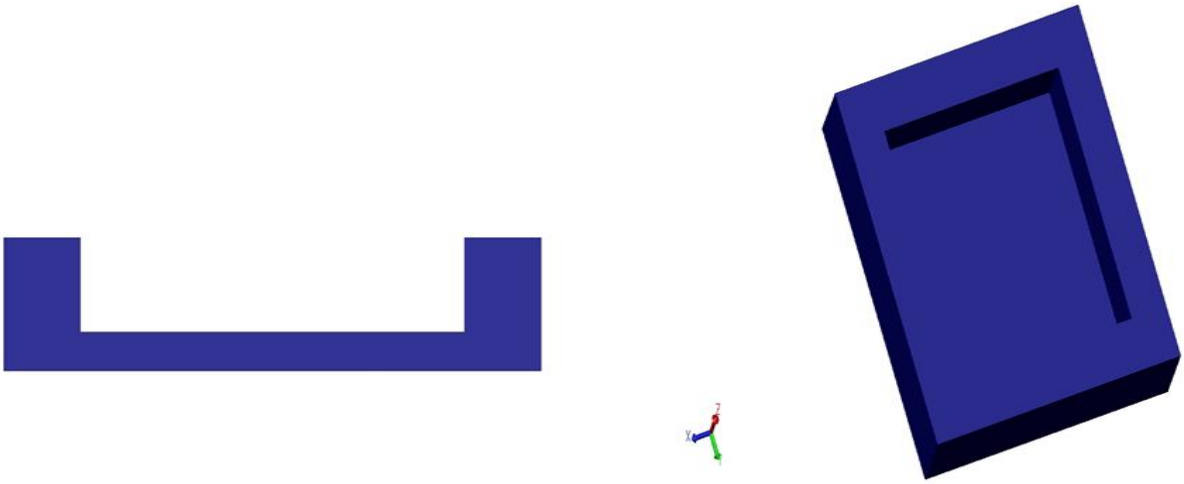
5.1.9 Process flow

The process flow of the design is shown below in figure 5.21. Blue colour is for substrate, red BPSG, green sio2, cyan gold, magenta sio2 and yellow is PSG.

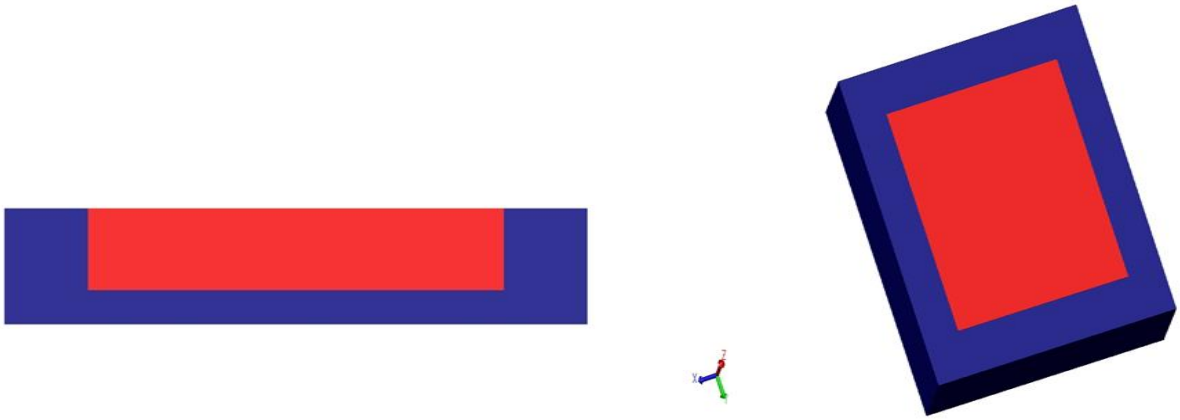
a) Silicon Substrate: A substrate of Si<100> is used.



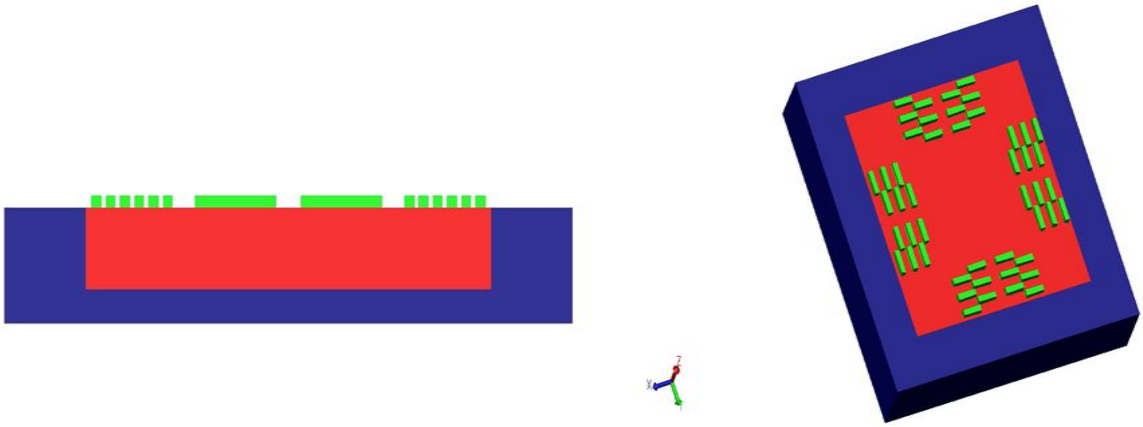
b) Etch a cavity in the substrate : Create a 300um deep cavity in the substrate using etching.



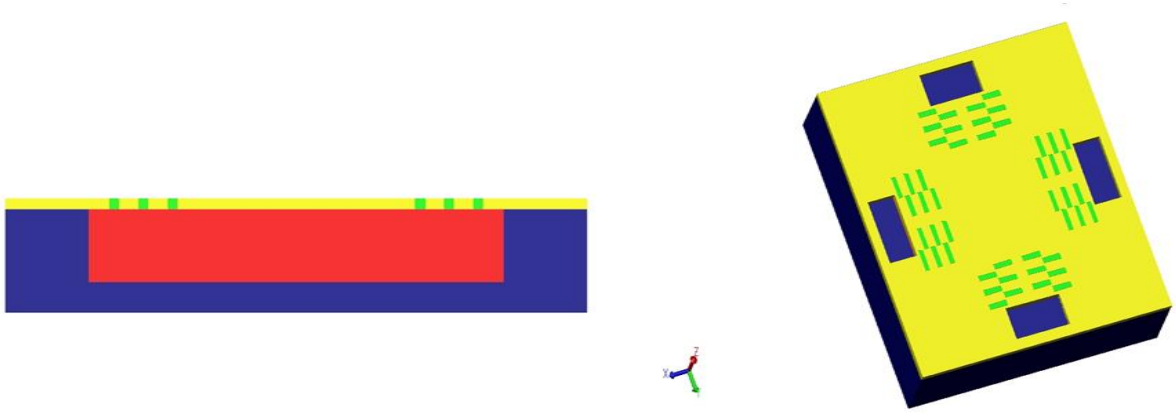
c) Deposit a sacrificial layer: deposit PSG in the cavity to work as sacrificial layer.



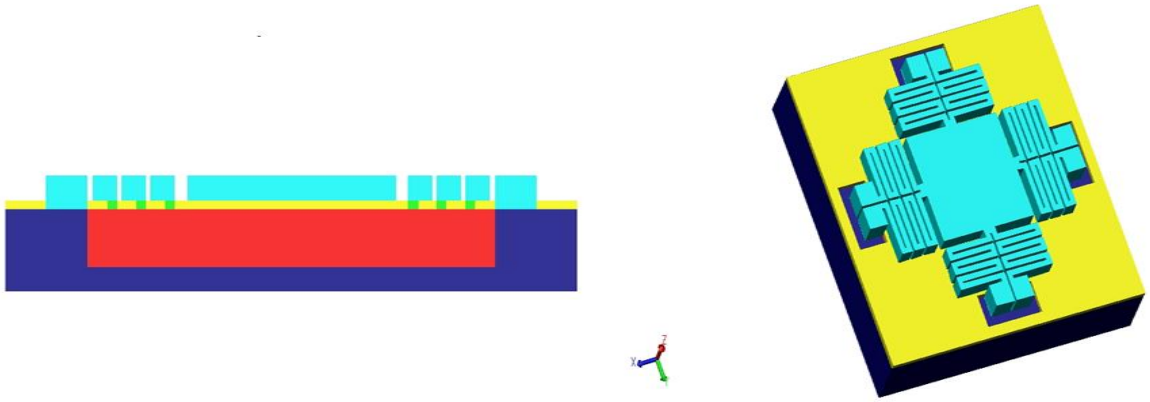
d) Deposit first layer of SiO2: above PSG layer pattern and deposit SiO2 layer which will become the part of FOB structure and frame.



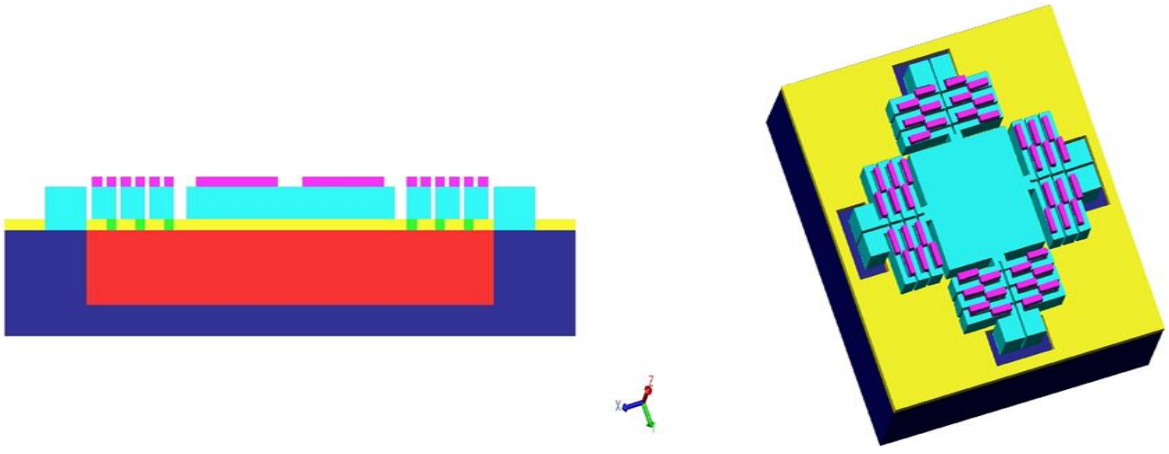
e) Deposit second sacrificial layer: pattern and deposit BPSG sacrificial layer over sio2 layer.



f) Deposit gold : pattern and deposit gold layer over the BPSG layer which will form a part of mirror plate and bimorph.



g) Deposit second layer of SiO2: after this pattern and deposit the second layer of sio2 on gold layer which will complete the fob structure.



h) Release sacrificial layer: Finally remove both the sacrificial layers.

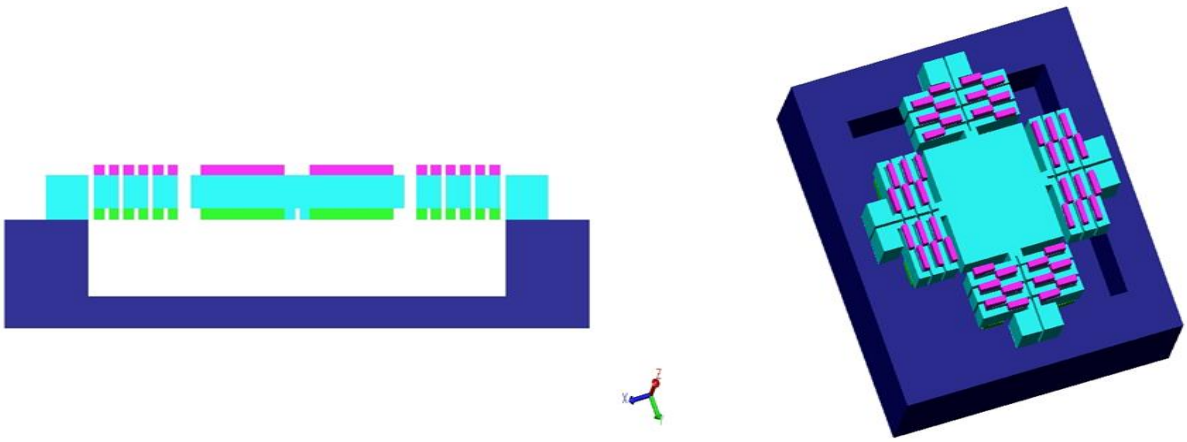


Figure 5.21 Process Flow

Chapter 6

Discussion and Conclusions

6.1 Discussion

The thesis work consists of designing of an electrothermal bimorph actuator which can provide large range of vertical movements. A series of designs have been simulated to obtain a structure which would provide optimum performance over the entire range of operation.

A flip over beam based actuator has been designed which provides pure vertical deflection without any tilting motion. After designing this basic structure an actuator which can lift a 1mm x 1mm plate is designed. Gold and SiO_2 (Silicon dioxide) are used as the materials for making bimorphs. Folded dual S-shaped actuator structures are combined to give large vertical displacement. The voltage is applied at the contact pad connected to the FSDB structures. The substrate of silicon<100> is used for the simulations.

Various iterations are done to reach the final design. In the first iteration a mirror plate made of gold is used and the maximum deflection of 263um is observed on applying 150mV voltage and corresponding temperature rise is 700 K. The main problem with this design is that the current is not limited to the FSDB structures, it flows through plate also. As a result heat and power loss occurs in the mirror plate. In order to remove this problem in the second iteration the plate made up of silicon dioxide only is used. It gives a maximum displacement of 302um with 700K temperature rise on applying 150mV voltage. The main problem with this design is that plate is of dielectric material so it could not be used for tuning filter applications.

In the third iteration a plate made of gold and silicon dioxide is used with the contact between FSDB and plate made of SiO_2 only. The design shows a displacement of 364 um at the same voltage. However, this design shows a lot of curling down of plate and measures were taken to control this warpage. In the final design, the plate of gold resting on a silicon dioxide frame is used. The plate is perorated to further reduce the warpage. The frame of SiO_2 is in direct contact with FSDB structure and ensures that no current flows through the plate and maximum displacement is achieved. A maximum displacement of 340 um is possible at 150mV with this design.

For every design initial displacement due to internal stresses of gold and silicon dioxide is measured and displacement at initial thrust is calculated. Heat loss in the structure due to convection loss is also calculated for each structure.

Thus, with the designs presented in the thesis robustness, low actuation voltage and power efficient, compactness, friction free motion and conduciveness to fabrication have been achieved using an uncomplicated bimorph actuation mechanism to obtain vertical out-of-plane motions at micro scale.

6.2 Conclusion

An electrothermal bimorph actuator based on Joule heating that gives large pure vertical displacements has been designed. A structure based on FOB structure has been designed and simulated. The structure is made of gold, silicon dioxide and silicon substrate with gold and SiO_2 forming the bimorph. The use of silicon dioxide layer to isolate the central plate from the actuation mechanism has been found to have considerable effect on the power efficiency of the devices designed. The designs have been simulated for various plate compositions, shape and geometry. Each design has been simulated for three different thicknesses of gold keeping SiO_2 thickness constant. Each design has been simulated for a voltage range of 0-

150mV. The final design shows a maximum displacement of 340um at 150mV with temperature of structure at 700K. Convection heat loss and residual stress analysis has been done for each structure. Since the structures use only three materials and are planar in nature without any complicated structure such as hinges the fabrication of these designs is relatively a lot convenient and require much less number of process steps. Thus, with the designs presented in the thesis: robustness, low actuation voltage and power efficiency , compactness, friction free motion and conduciveness to fabrication have been achieved using an uncomplicated bimorph actuation mechanism to obtain large out-of-plane motions at micro scale.

6.3 Future Prospects

The above designed actuator can be combined with other structures to act as tunable filters, cavity resonators, dielectric resonators, digital mirror displays, fourier transform spectroscopy etc. A variety of materials can be studied to replace gold and silicon dioxide that can show better displacement results at lower voltages. A process flow has to be developed to fabricate this design so that the test structures can be fabricated.

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PART B: Internship at Qualcomm

Chapter 1

Introduction

1.1 Motivation and Approach

I have worked on two projects during my internship at Qualcomm. The first project was related to generating a RTL code for clock controller block. In a commercial chip hundreds of clocks are required. These clocks are fed to different parts of the chip and have different frequencies , and all are not used at the same time. It is very hectic to write a RTL code manually for the clock controller block. In order to ease this, a tool has been developed by Qualcomm to automate the RTL code generation for different clock controller blocks. The input to the tool is an excel spreadsheet , which includes all the information related to the clocks such as their operating frequency, their master and slave clock, generator, registers, dividers, clock block controller(CBC), test clocks, resets, enables and disables, etc. The other inputs to the tool are mapper file, override file and other setup files. The tool generates the RTL corresponding to the input excel spreadsheet. After this RTL is generated , several tests are performed on the design to check its synthesizability, connectivity, structural, synchronization, UAR compliance, etc. Clock domain crossing (CDC) and Progressive Lint Design Rule Check (PLDRC) has been performed to check the above mentioned objectives. In order to perform CDC check, I have used Mentor 0in tool version 15.6 and for PLDRC Spyglass tool have been used.

In the second project I have done DFT (Design for Test) for an ongoing project in R&D, Qualcomm. DFT is done to check the bug in design and process defects post silicon. ATPG (Automatic Test pattern generation) generates test patterns for the design and after the fabrication of chip, these test patterns are passed through the chip to verify whether the chip is defect-free or not. For doing this Mentor Tessent tool has been used. This tool generates the chain test and serial scan test patterns for the design. Simulations are run on the design using these patterns as an input to verify whether the design is passing these patterns or not. Extra functionality is added in the design to make it testable. This functionality is used only during DFT and it is redundant during normal operation of chip [1].

1.2 Thesis Outline

The part B of thesis is organized as follows:

Chapter 2 discusses the Clock domain crossing tool. The need of the tool and its flow is discussed in detail in this chapter.

Chapter 3 discusses the PLDRC tool. The applications of the software, the tool flow and its scope is discussed in detail in this chapter.

Chapter 4 is dedicated to understanding the DFT tool and its need. The tool flow and its applications is discussed in detail in this chapter

.

Chapter 2

Clock Domain Crossing

2.1 Introduction

Clock domain crossing (CDC) check enables designers to detect design issues during RTL development. It mainly deals with structural CDC analysis and targets synthesizable RTL with multiple asynchronous clocks. Whenever changes are made to the designs, designers need to re-run CDC [2].

2.2 Why CDC?

As modern System-on-Chip (SoC) designs continue to face increasing size and complexity challenges, multiple asynchronous clock domains have been employed for different I/O interfaces. A CDC-based (Clock Domain Crossing) design is a design that has one clock asynchronous to, or has a variable phase relation with, another clock. A CDC signal is a signal latched by a flip-flop (FF) in one clock domain and sampled in another asynchronous clock domain. Transferring signals between asynchronous clock domains may lead to setup or hold timing violations of flip-flops. These violations may cause signals to be meta-stable. Even if synchronizers could eliminate the meta-stability, incorrect use, such as convergence of synchronized signals or improper synchronization protocols, may also result in functional CDC errors. Functional validation of such SoC designs is one of the most complex and expensive tasks. Simulation on register transfer level (RTL) is still the most widely used method. However, standard RTL simulation cannot model the effect of meta-stability. Important design considerations require that multi-clock designs be carefully constructed at Clock Domain Crossing (CDC) boundaries.

Within one clock domain, proper static timing analysis (STA) can guarantee that data does not change within clock setup and hold times. When signals pass from one clock domain to another asynchronous domain, there is no way to avoid meta-stability since data can change at any time.

To address clock domain problems due to meta-stability and data sampling issues, designers typically employ several types of synchronizers. The most commonly used synchronizer is based on the well-known two-flip-flop circuit. Other types of synchronizers are based on handshaking protocols or FIFOs.

To accurately verify clock domain crossings, both structural and functional CDC analysis should be carried out. Structural clock domain analysis looks for issues like insufficient synchronization, or combinational logic driving flip-flop based synchronizers. Functional clock domain analysis uses assertion-based verification to check the correct usage of synchronizers.

2.2.1 Metastability

Metastbility refers to signals that do not assume stable 0 or 1 state for some duration of time at some point during normal operation of a design. In a multi-clock design, metastability cannot be avoided but the detrimental effects of metastability can be neutralized.

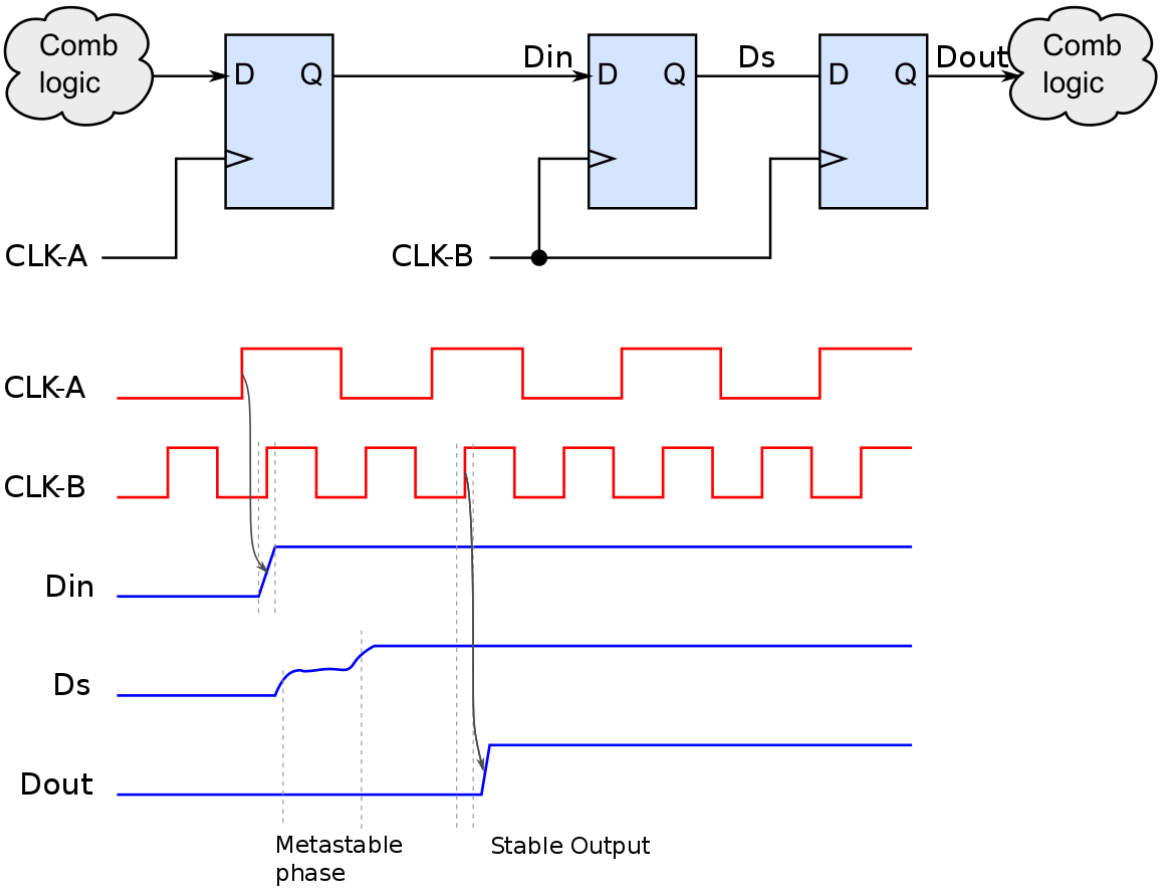

Fig. 2.1 Metastability due to synchronization failure

Figure 2.1 shows the metastability condition that occurs when two asynchronous clocks cross clock boundaries and leads to synchronization failures. Consider the 1-bit CDC signal D, which is sampled by register 1. Since Din comes from a different clock domain (CLK A), its value can change at any time with respect to Ds clock (CLK B). If the value of Din changes during Ds's setup and hold time, the register 3 might/might not assume a state between 0 and 1. In this state, the register is said to be meta-stable. A meta-stable register may/may not (unpredictably) settle to either 0 or 1, causing illegal signal values to be propagated throughout the rest of the design. In a multi-clock design, meta-stability is inevitable, but there are certain design techniques that help to avoid the chance of getting meta-stable such as two flip flop synchronizers, mux synchronizers, handshake protocols, etc.

2.3 Mentor 0in tool for CDC

CDC Mentor 0in tool has been used to perform this check. CDC reference flow has the following main features:

- Apply at any design level, including chip, core or block level.
- Generate design file list automatically or used one directly provided by the user.
- Supports structural CDC analysis to analyze clock domain crossings in the design.
- Supports CDC hierarchical analysis, generally run at sub-system or chip level.
- Supports CDC model analysis for different functional asynchronous modes in the design.

- Supports CDC protocols assertion analysis to perform assertion based CDC verification during simulation.
- Supports CDC formal analysis to prove formal verification of promoted checkers.
- Supports user customization.

2.4 Flow Architecture

CDC reference flow is a make- based flow and all the flow steps are managed using single set of variables. The flow step uses a Makefile template and config template that the users can customized. The Makefile is the fi.rst level user customizable Makefile that contains pointers to the flow locations and user config to be used.

CDC reference flow runs the Makefile targets that will create flow directories, analyze/compile the design and associated libraries, run CDC, and view CDC results.

The CDC flow architecture is depicted in figure 2.2

3.4.1 Flow Inputs

Following are the inputs to the CDC flow:

1. Design filelist
   This refers to the RTL filelist. The filelist can be generated automatically using the FE gen flow provided by the users. FE gen flow runs fe_filelist script to generate a filelist from either makefile or compile.xml.

2. Library filelist
   Users need to create and provide library filelist. A common synthesis based library list can be provided and flow will only process the libraries needed for CDC. This typically has standard cell libraries, designware components, custom memory, etc.

3. Design constraint files
   This refers to block-level constraint files for running CDC analysis. These control files are optional and the flow picks up based on the naming convention.

4. Global constraint files
   These refer to constraint files that can be applied globally to any design. The flow picks up all Verilog files in this directory including the flow generated global settings constraint file. The flow reads the block level constraint files under the directory specified by directory variable.

5. Configuration files
   The flow provides makefile and config template to specify the flow inputs and parameters. Users should modify them based on their needs. The flow provides the users the flexibility to customize the templates during different steps of the flow.

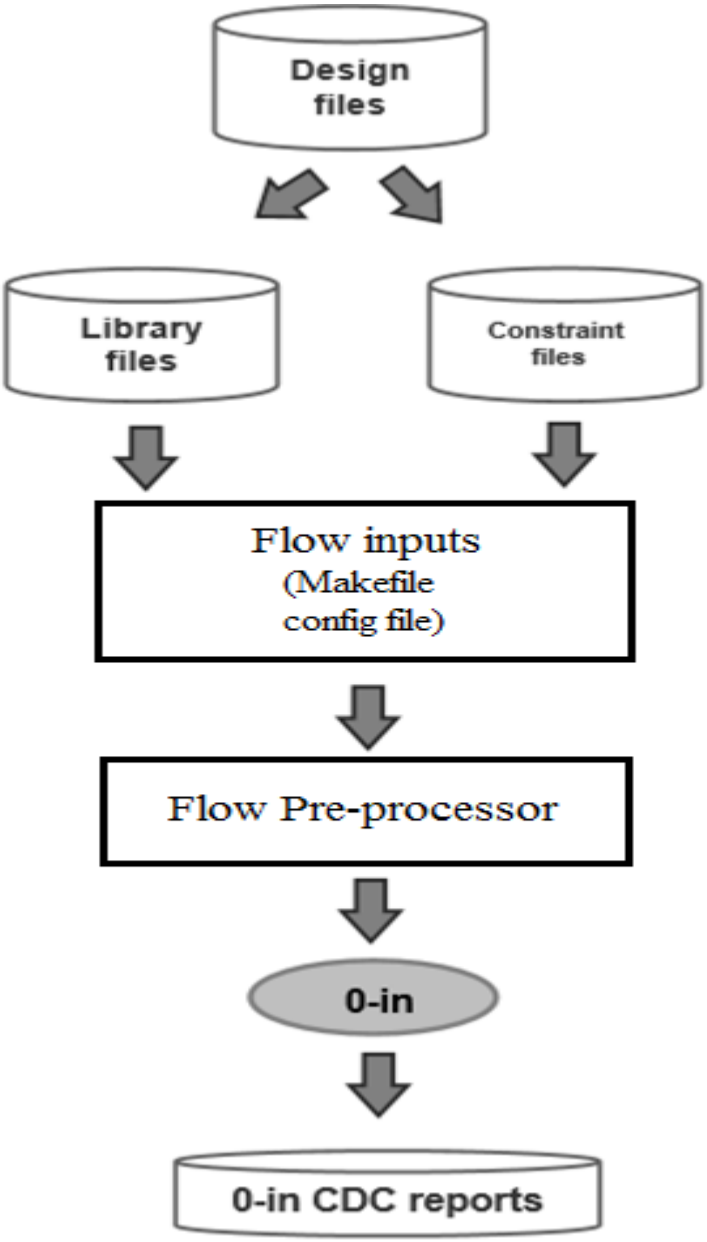

Figure 2.2 CDC Flow Architecture

6. Configuration files
   The flow provides makefile and config template to specify the flow inputs and parameters. Users should modify them based on their needs. The flow provides the users the flexibility to customize the templates during different steps of the flow.

3.4.2 Execution Steps

1. gnumake filelist:
   This step is run to generate cdc filelist in analyze directory. This fileslist has all the information related to the input files, constraint files, library, etc.

2. gnumake analyze
   This step is run to analyze the design and the associated libraries.

3. gnumake cdc
   This command run cdc analysis on the design and reports clock domain crossings. All the reported violations are removed after reviewing.

4. gnumake debug
   This command is run to bring up 0-in GUI by running in interactive mode. Reviewing the violations become very easy in GUI mode.

5. gnumake all
   This command executes the entire cdc flow upto cdc step.

3.4.3 Flow Outputs

The flow generates run scripts, log files, analyze report, cdc crossing reports and HTML metrics. It is required to review the log and report files to ensure that the run is successful.

Chapter 3

PLDRC

3.1 Introduction

Progressive Logic Design Rule Checking (PLDRC) enables designers to detect design issues during RTL development. Progressive, as in PLDRC, denotes a standard methodology for combining all checks into a single common flow using pre-defined goals. Lint checks are done to remove the inefficiencies during RTL design which can come out as serious design issues during the later stages of design implementation. These issues lead to several iterations on detection and can lead to chip rejection (after fabrication) if these are not detected. This is done to make sure that the design functionality is not altered during the optimization stage. Whenever changes are made to the RTL, the libraries, or the input constraints, PLDRC should be run again.

PLDRC tool by Spyglass from Atrenta has been used to run PLDRC check on the RTL generated by clock generation tool. SpyGlass provides an integrated solution for analysis, debug and fixing with a comprehensive set of capabilities for structural and electrical issues all tied to the RTL description of design [3].

3.2 Methodologies

There are several classes of checks that are a part of the PLDRC rule set. These methodologies contain various rule sets that check for specific types of problems. These rule sets ,or goals(as often referred to), are groups of rules that are run as a part of the overall design life cycle.

The goals which are required to run are:

1. Lint-Mustfix, Lint-Must and Lint-Review:
   Lint checks are basically RTL syntax checks. These three checks are done for verifying the structural, connectivity, simulation, synthesizability of the design.

2. Lint-Reset :
   Lint-Reset checks for asynchronous resets for UAR compliance.

3. DFT-Analysis :
   DFT- Analysis checks for scan/testability issues.

4. DFTDSM-Analysis :
   DFTDSM performs at-speed checks for test clock and frequency connectivity.

5. LP-Analysis :
   Low power (LP) Analysis checks for clock gating coverage, connectivity of clock gating signals.

3.3 Spyglass PLDRC tool

Spyglass tool has been used to perform lint checking or PLDRC check on the design. The main features and benefits of this tool are:

- Sophisticated static and dynamic analysis identifies critical design issues at RTL
- A comprehensive set of electrical rules check to ensure netlist integrity
- Includes design reuse compliance checks, such as STARC and OpenMORE to enforce a consistent style throughout the design
- Customizable framework to capture and automate company expertise
- Integrated debug environment enables easy cross-probing among violation reports, schematic and RTL source
- The most comprehensive knowledge base of design expertise and industry best practices
- Supports Verilog, VHDL, V2K, SystemVerilog and mixed-language designs
- Tcl shell for efficient rule execution and design query
- SoC abstraction flow for faster performance and low noise

3.4 Flow architecture

PLDRC reference flow is a make- based flow and all the flow steps are managed using single set of variables. The flow step uses a Makefile template and config template that the users can customized. The Makefile is the fi.rst level user customizable Makefile that contains pointers to the flow locations and user config to be used.

PLDRC reference flow runs the Makefile targets that will create flow directories, analyze/compile the design and associated libraries, run PLDRC goals, and view PLDRC results for each goal.

The PLDRC flow architecture is depicted in figure 3.1

3.4.1 Flow Inputs

Following are the inputs to the PLDRC flow:

1. Design filelist
   This refers to the RTL filelist. The filelist can be generated automatically using the FE gen flow provided by the users. FE gen flow runs fe_filelist script to generate a filelist from either makefile or compile.xml.

2. Library filelist
   Users need to create and provide library filelist. A common synthesis based library list can be provided and flow will only process the libraries needed for PLDRC. This typically has standard cell libraries, designware components, custom memory, etc.

3. Design constraint files
   This refers to block-level constraint files for running CDC analysis. These control files are optional and the flow picks up based on the naming convention.

4. Global constraint files
   These refer to constraint files that can be applied globally to any design. The flow picks up all Verilog files in this directory including the flow generated global settings constraint file. The flow reads the block level constraint files under the directory specified by directory variable.

5. Configuration files
   The flow provides makefile and config template to specify the flow inputs and parameters. Users should modify them based on their needs. The flow provides the users the flexibility to customize the templates during different steps of the flow.

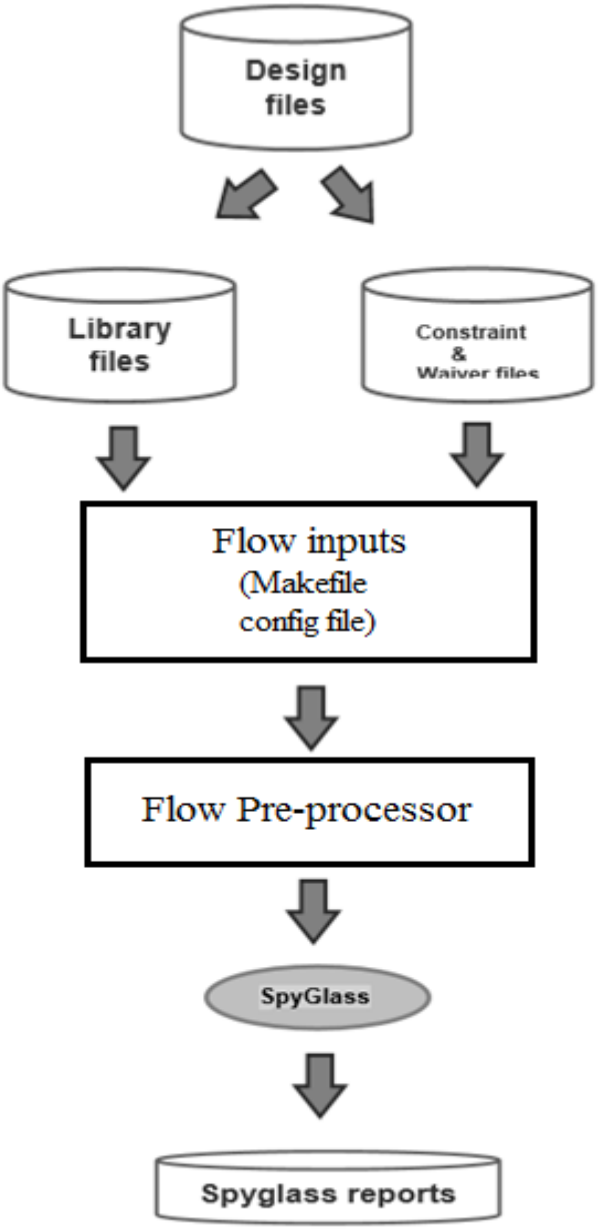

Figure 3.1 PLDRC Flow Architecture

6. Configuration files
   The flow provides makefile and config template to specify the flow inputs and parameters. Users should modify them based on their needs. The flow provides the users the flexibility to customize the templates during different steps of the flow.

3.4.2 Execution Steps

1. gnumake filelist:
   This step is run to generate pldrc filelist in analyze directory. This fileslist has all the information related to the input files, constraint files, library, etc.

2. gnumake analyze
   This step is run to analyze the design and the associated libraries.

3. gnumake sg_run
   This command sets up block-levrl and globalconstraint/waiver directory and run pldrc analysis on the design and reports violations. All the reported violations are removed after reviewing. Only those goals that are defined in config files are run.

4. gnumake sg_view
   This command is run to bring up Spyglass GUI by running in interactive mode. Reviewing the violations become very easy in GUI mode.

5. gnumake gen_metrics
   This command generates html metrics reports based on pldrc results in <PASS>

6. gnumake all
   This command executes the entire pldrc flow upto gen_metrics step.

3.4.3 Flow Outputs

The flow generates run scripts, log files, analyze report, pldrc crossing reports and HTML metrics. It is required to review the log and report files to ensure that the run is successful.

Chapter 4

Design for Test

4.1 Introduction

Design for test (DFT) is done on the design to verify the design functionality after the fabrication of chip. It determines whether the manufactured chip is good or not. It facilitates the design to become testable after production. It is the extra logic which we put in the normal design, during the design process, which helps its post-production testing. Post-production testing is necessary because, the process of manufacturing is not 100% error free. There are defects in silicon which contribute towards the errors introduced in the physical device. Of course a chip will not work as per the specifications if there are any errors introduced in the production process. But the question is how to detect that. Since, to run all the functional tests on each of say a million physical devices produced or manufactured, is very time consuming, there was a need to device some method, which can make us believe without running full exhaustive tests on the physical device, that the device has been manufactured correctly. DFT is the answer for that. It is a technique which only detects that a physical is faulty or is not faulty. After the post-production test is done on a device, if it is found faulty, trash it, don't ship to customers, if it is found to be good, ship it to customers. Since it is a production fault, there is assumed to be no cure. So it is just a detection, not even a localization of the fault. That is our intended purpose of DFT. For the end customer, the DFT logic present on the device is a redundant logic [4].

To further justify the need of DFT logic, consider an example where a company needs to provide 1 Million chips to its customer. If there isn't any DFT logic in the chip, and it takes for example, 10 seconds (Its very kind and liberal to take 10 seconds as an example, in fact it can be much larger than that) to test a physical device, then it will take approximately three and a half months just to test the devices before shipping. So the DFT is all about reducing three and a half months to may be three and a half days. Of course practically many testers will be employed to test the chips in parallel to help reduce the test time.

There are many reasons due to which a manufactured chip can fail. It can be due to the incorrect logic design or physical design or both. The logic design verification is not done properly. It might be possible that sufficient test cases were not run during the design verification. The defect can be due to incorrect physical design also. This includes manufacturing defects, wear-out defects and performance, power, temperature specification violations. The defect can occur during manufacturing because of immaturity of fabrication process. This can be detected by including more fault models. Wear out defects can be detected by stress tests. The performance, power, temperature specification violations can be detected by at speed tests, leakage tests, etc.

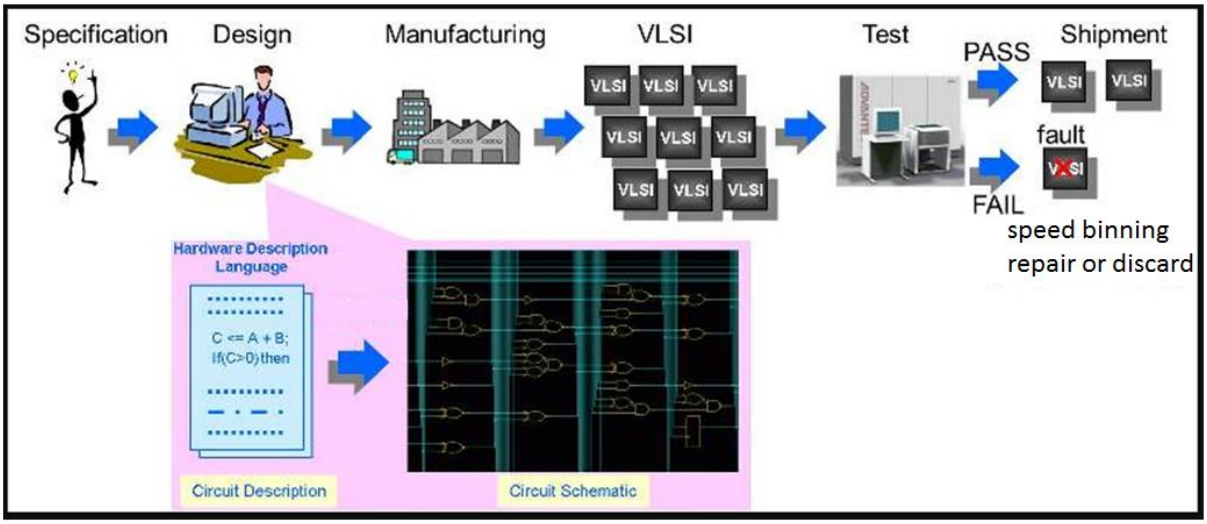

Figure 4.1 Design for test

4.2Design for test

The main objective for doing design for test is to make the design testable with maximum coverage and minimum test time. The DFT flow is shown in figure 4.2

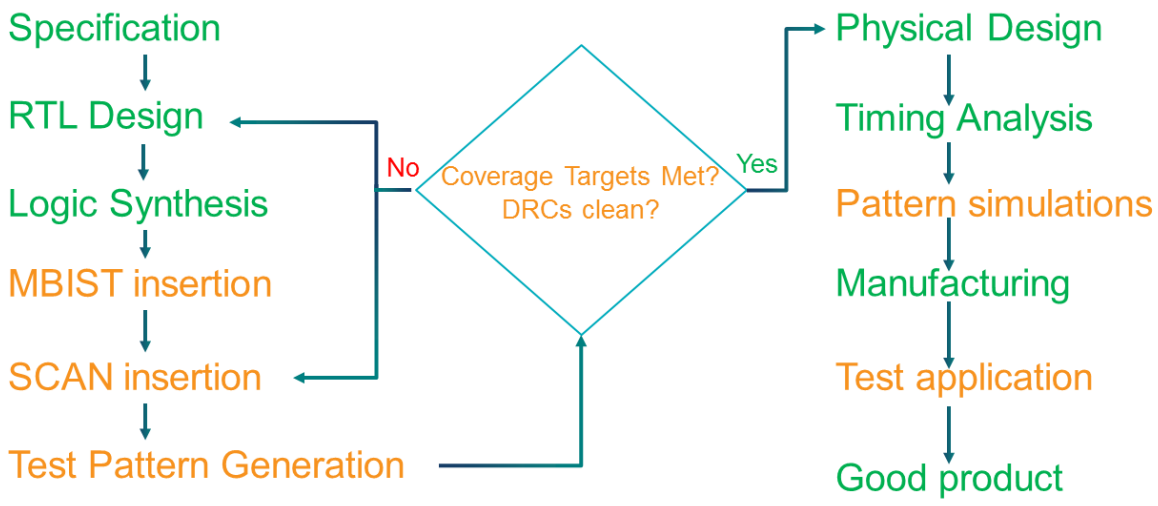

Figure 4.2: DFT flow

Additional logic is added to the design for making the design testable. All the registers in the design are stitched together to form the chain of registers. ATPG patterns are generated that are given as scan in patterns to the scan chains. The coverage of scan chain patterns are calculated and ideally it should be more than 99.5%. The design is simulated by passing these test patterns as an input to the design. The design rule checking is done at last to verify that all the design rules are met after DFT.

4.2.1 Automatic test pattern generation (ATPG)

ATPG procedure involves generating a set of input vectors that can detect all modeled faults and ascertain presence or absence of fault(s) at some location(s) in a circuit. For detecting the faults fault simulation is done which determines which faults the pattern detect. The goal of

ATPG is to create a set of patterns that achieves a given test coverage. The test coverage is the total percentage of detectable faults the pattern set actually detects.

$$Coverage = \frac{faults\ actually\ detected\ by\ patterns}{total\ testable\ faults.} \quad (4.1)$$

The input to the generator is a circuit (usually at gate level) and a fault model (usually stuck at type). The performance metrics of ATPG is determined by the:

a) Number of patterns generated for detecting the faults
b) Number of fault models detected.
c) Time required to run the test, more the number of patterns more is the time required to run the test.

These metrics indicates the test quality and test applications. ATPG is much easier if appropriate DFT rules and suggestions have been implemented. ATPG is a search problem which search the input vector space for a test. It initialize all signals to unknown (X) state so that complete vector space becomes the playing field. It activates the given fault and sensitizes a path to a PO which narrow down to one or more tests. There are many ways to generate the patterns: Random, exhaustive and deterministic pattern generation. In random pattern generation, the patterns are generated randomly, determines how many faults are detected by the random patterns and then re-run the test until no new faults are detected by the random patterns. In exhaustive pattern generation all the input combinations are applied and the functional correctness is checked. For an n input circuit 2^n input combinations are required. In deterministic pattern generation certain patterns are generated manually to find some particular faults. Generally random and deterministic patterns are combined to find the fault models.

4.2.2 Scan test

The method for delivering the test pattern from chip inputs to internal circuits under test and observing their outputs is known as scan design. The main objective is to make all the flip-flops or registers present inside the circuit as internal control and observation points. All flip-flops are stitched into scan chains and then are controlled and observed through chip ports. For checking the defects in flip-flops, chain test is run. A definite pattern of 00110011… is given as an input to the scan chains. In order to check the combination logic around the flip flop, sequential scan test is run and then those patterns are given as scanin input to the scan chain during shift signal and then these patterns are captured for one or more clock and then again scanout from the chains as an output for observation. A complex circuit may need a large number of scan chains and can have large pattern set. Each scan chain requires one input and output port. Since the number of pins are limited in a chip, compression techniques are applied on the patterns which saves run time the number of pins required for DFT. There are three main scan types: MUX D f/f, clocked scan and LSSD. In mux D f/f, a mux is combined with a flip-flop which selects between the functional input and scanin input based on shift signal, one more output pin is connected to the flip flop for scanout signal. During the normal operation of the circuit, these pins will be redundant and only during DFT the select signal ‘shift’ goes high and scanin input is given to the flop and output is taken from

scanout pin. The mux d f/f scan is shown in figure 4.3. LSSD stands for Level sensitive scan design. This is generally used for latch-based design. In this an extra slave latch is added with each latch and during scan only this slave latch is used.

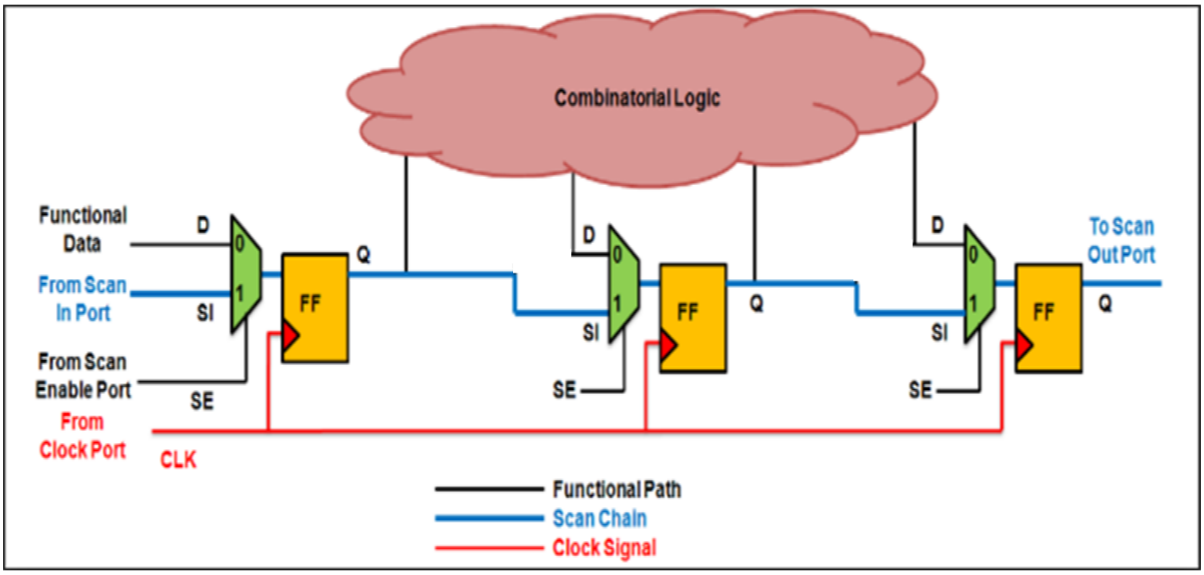

Figure 4.3: Mux D f/f scan

4.2.3 Test types

There are three main test types that are used in DFT: functional test, IDDQ test and At-speed test. Functional test is basically used to detect stuck at 0 or 1 fault models and toggle fault models. Stuck at fault occurs when the output or input pin of a logic design is tied to 0 or 1 during fabrication. In order to detect this fault all the input pins are drive to 0 and 1 and then the output is observed to verify the functionality. For this all the nodes/nets of the design should be controllable and observable using the chip I/O pins. IDDQ test is used to find pseudo stuck at, transistor leakage, transistor stuck at, general node shorts and node toggle fault models. This is done passing the current through the IC and then observing the output current. ATPG tool supports pseudo stuck at transistor based fault models. At speed test is run to find the time taken by the logic circuit to change the state. It supports detection of transition fault models and path delay models. To detect transition fault models, two test vectors are required: initialization vector and test propagation vector. After detecting all the faults, fault manipulation is done. Fault manipulation involves manipulation of detected faults by grouping faults of different regions into different classes and then removing the same faults detected by different patterns from the list or avoiding them during ATPG.

4.3 Structural and functional testing

Structural testing is done to find defects that are generated in the chip during fabrication. The main features of structural defects are:

1. Chip is in test mode
2. Low test time and cost
3. Diagnosis is easier.
4. More generic as no detailed functional information is required.

5. Scalable
6. Coverage quantification

In order to do structural testing extra logic is included in the circuit which is used only during testing and is redundant during normal functioning of the chip.

Functional testing is done to check the functionality of chip. The main features of functional testing are:

1. Chip is operated in functional mode.
2. High test time and cost
3. Diagnosis is difficult.
4. Varied expertise of people for debugging.
5. Not scalable
6. No coverage quantification

4.4 Implementation of DFT in the project

Mentor Tessent tool has been used to generate the test patterns and to find the fault coverage for an ongoing project in Qualcomm. A perl script and DC compiler based Tcl script was written to make the design compatible for the tool. The patterns were generated and then the design was simulated using ModelSim tool. The details of the project can't be revealed because of Qualcomm copyright policies.

Conclusion

All the assigned tasks are successfully completed. The RTL code for clock controller block was generated using clock generation tool. After generating the RTL code, the design was validated by simulations on Modelsim. In order to check the clock domain crossing violations, CDC check was run. All the reported violations were reviewed and then waived. Mentor 0in tool was used for running CDC check. The constraint files and waiver files for the design were written in Tcl and then were given to the tool. In order to check the RTL syntax check, Lint checks were performed. At speed clock testing, DFT analysis, asynchronous rest compliance with UAR and low power linting were done to ensure that the design is bug free. The constraint files and waiver files for all goals were written in Tcl and then were given to the tool.

In the second project DFT (Design for testability) was done for an ongoing project in Qualcomm. ATPG patterns were generated and then were passed through the design for validation. Mentor Tessent tool was used for generating the patterns and for calculating the test coverage, and the simulations were done on Modelsim tool for validating the design. Perl and Dc compiler scripts were written to make the design compatible for the Tessent tool.

The details of the project done can't be disclosed because of Qualcomm CCI.

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