INVESTIGATION ON CASCADED H-BRIDGE FIVE-LEVEL INVERTER-BASED ACTIVE POWER FILTER

Ph.D. Thesis

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by

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DECLARATION

I, **Soumyadeep Ray**, declare that this thesis titled, **"Investigation on Cascaded H-Bridge Five-Level Inverter-Based Active Power Filter"** and the work presented in it, are my own. I confirm that:

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This is to certify that the thesis entitled **"Investigation on Cascaded H-Bridge Five-Level Inverter-Based Active Power Filter"** being submitted by **Soumyadeep Ray (ID No. 2015REE9034)** is a bonafide research work carried out under our supervision and guidance in fulfillment of the requirement for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Malaviya National Institute of Technology, Jaipur, India. The matter embodied in this thesis is original and has not been submitted to any other University or Institute for the award of any other degree.

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(SOUMYADEEP RAY)

ABSTRACT

Recently, power quality (PQ) is becoming an important aspect for engineers and researchers as large amount of grid integration takes place in distribution network. Medium-voltage and high-power distribution system caught every one's attention as large-scale conventional as well as renewable energy integration is taking place in current distribution system. Most of the high-power and medium-voltage equipments used by distribution sector comprises of adjustable electric drive which produces non-linearity into the existing system due to switching action of converter switches. Current harmonics generated by non-linear loads create major problem in distribution system. Current harmonics also produce voltage harmonics in combination with line impedance which propagates to distribution side consumers through point of common coupling. Many national and international regulatory standards are defined like IEEE-519-1992, IEC 61000 etc. in order to describe PQ limits.

Active power filter (APF) is a mature technology till date to counter several major PQ concerns. APF can be used for mitigating current harmonics; reactive power nullification, load current balancing with its effectiveness to solve neutral current issue. Two-level inverters are normally used as a main component of APF in low-voltage and low-power distribution system but for medium-voltage and high-power applications, multilevel inverters (MLIs) have become more attractive solution for their distinct advantages over the two-level inverters. Topology wise three fundamental types of MLIs are projected in literature namely, diode-clamped multilevel inverter, flying capacitor MLI and cascaded H-bridge MLIs (CHB-MLIs). Among these topologies, CHB-MLIs reach to higher voltage and power level due to its modular structure. In view of above theory, a through literature survey on topological aspect and various control techniques of MLI based APF has been done and a comprehensive review is presented. Among all these relevant application, CHB-MLI based SAPF is widely demonstrated in literature due to least number of device counts among all other MLIs and modularity. This topology is one of the most suitable technologies available in present medium-voltage distribution sector for reducing PQ problems. Therefore, this thesis deals with design and

development of CHB-MLI based SAPF for PQ improvement in case of medium-voltage distribution sector.

One significant aspect of harmonic current compensation and reference current generation of SAPF unit is the design of the overall control system. The main concern while designing control algorithm is simplicity, robustness and accuracy. At the same point, its effectiveness should be tested under normal supply as well as under distorted source voltage condition.

In view of above, the efforts have been made to analyze, design and develop appropriate control algorithm for CHB-MLI based SAPF. Current control plays a significant role for defining current shape and magnitude in case of shunt type active filtering applications. PI compensators are replaced by proportional-resonant (PR) compensator in order to acquire better steady-state performance in AC controllability. Stability of the proposed control theory is checked and analyzed with the help of root-locus analysis. PR compensator based advanced current controller is used in current control loop to introduce infinite gain at selected frequency. This controller facilitates the system operation with superior performance over conventional controller in terms of sinusoidal reference signal tracking capacity and disturbance rejection capability. Detailed simulations are carried out in MATLAB™/ Simulink® and verified experimentally using dSPACE 1104 real-time controller.

However, use of PR compensator in current control loop causes reduction in stability margin of the closed-loop SAPF system and it is also responsible to create undesired peaks during real-time applications. Therefore, PI-vector-proportional-integral (VPI) compensator based current controller is designed in order to maintain superior SAPF performance during its operation. This compensator is able to mitigate high-frequency components from current control loop and therefore, source current of sinusoidal wave-shape is obtained in case of MLI based SAPF operations. A systematic methodology is presented for tuning PI-VPI compensator parameters using particle swarm optimization (PSO) technique by minimizing source current steady-state error and source current total harmonic distortion. Effectiveness of proposed control has been also thoroughly tested with rigorous simulation and hardware results.

Advanced PLL based control algorithm is used for CHB-MLI based active filtering application which can work under ideal as well as distorted supply voltage conditions. Advanced PLL is capable of exact measurement of phase angle, fundamental component extraction from polluted signal and DC component removal. Eigen value analysis is used as an effective tool to design of constant parameters for this PLL. Detailed simulation and real-time performance analysis of CHB-MLI based SAPF with proposed PLL based control algorithm is tested in different non-linear loading conditions which confirm the effectiveness of the projected control.

CHB-MLI based filtering approach can provide transformer-less interconnection of converters, gives cost-worthy solution and provides better power quality. Therefore, single-phase CHB-MLI based transformer-less grid-tied PV system is proposed so that system can supply active as well as reactive power in day time and can act as SAPF during night time. The proposed grid-tied PV system is rigorously tested with different irradiations in MATLAB™/Simulink® platform. Transient and steady-state behavior of the proposed system decides effectiveness of the proposed scheme during night-time and in different weather conditions.

To summarize, five-level CHB-MLI based SAPF is designed using MATLAB™/Simulink® and simpower system toolbox. Advanced current controller composed of PR compensator is designed in order to get zero steady-state error in source current. However, use of PR compensator in current control loop is having limitations during real-time applications. Therefore, PI-VPI compensator based current controller is designed in order to maintain zero steady-state error during SAPF performance. An advanced PLL is also designed for CHB-MLI based active filtering application which is able to perform its proper operation in case of normal and distorted source voltage condition. A small-scale prototype of five-level CHB-MLI has been developed in the laboratory, where dSPACE 1104 is used for implementing control algorithms. Finally, use of CHB-MLI based SAPF is extended for grid-tied PV applications for active power injection as well as reactive power minimization. Detailed steady-state and transient performance analysis through simulative and experimental study prove that source current becomes sinusoidal and this is maintained according to IEEE-519 standard under different non-linear loading conditions.

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LIST OF SYMBOLS

I_{SC}	Maximum short-circuit current at point of common coupling
I_{Ld}	Maximum demand load current at point of common coupling
$H_{dc\text{-}PI}(s)$	Transfer function of PI compensator
$H_{PR\text{-}I}(s)$	Transfer function of ideal PR compensator
$H_{PR\text{-}NI}(s)$	Transfer function of practical PR compensator
$e(t)$	error signal fed to PR compensator in time domain
ω	Nominal frequency
ω_C	Cut-off frequency
k_p	Proportional constant of PI compensator
k_i	Integral constant of PI compensator
i_{La}, i_{Lb}, i_{Lc}	Load current of phase ‘A’, phase ‘B’, phase ‘C’
$i_{L\alpha}$, $i_{L\beta}$, i_{Lo}	alpha, beta and zero sequence current in alpha-beta reference frame
i_{Ld} , i_{Lq} , i_{Lo}	d, q and zero sequence current in ‘d-q-0’ reference frame
R_{Lf}	Equivalent interfacing resistor
L_{Lf}	Equivalent interfacing inductor
R_L	Equivalent linear loads present in distribution sector
R_S	Source resistance
L_S	Source inductance
T_i	Integration time
$G_1(s)$	Transfer function of current control loop
V_{Sa}, V_{Sb}, V_{Sc}	Source voltage of phase ‘A’, phase ‘B’, and phase ‘C’

I_{Sa}, I_{Sb}, I_{Sc}	Source current of phase ‘A’, phase ‘B’, and phase ‘C’
V_d	DC-link voltage of CHB-MLI based SAPF
V_{Ca}, V_{Cb}, V_{Cc}	Inverter voltage output of phase ‘A’, phase ‘B’, and phase ‘C’
I_{Ca}, I_{Cb}, I_{Cc}	Compensating current of phase ‘A’, phase ‘B’, and phase ‘C’
V_S	Source voltage in single-phase condition
I_S	Source current in single-phase condition
I_C	Compensating current in single-phase condition
I_L	Load current in single-phase condition
V_C	Inverter output voltage in single-phase condition
$G_{M\text{-}PR}$	Transfer function of multiple PR compensator
$G_{PI\text{-}MR}$	Transfer function of PI-multiple resonant compensator
G_{VPI}	Transfer function of vector proportional integral controller
K_{rh}	Resonant gain parameter
K_{ph}	Proportional gain parameter
R_f	Equivalent circuit resistance
L_f	Equivalent circuit inductance
h_n	'n' th order harmonic content
v_d, v_q	Source voltage quantities in 'd-q' frame
x_k, x_{k+1}	Particle position for k^{th} and $(k+1)^{th}$ instant
v_k, v_{k+1}	Velocity of particle for k^{th} and $(k+1)^{th}$ instant
Θ_0	Estimated phase angle
Θ_A	Phase angle of input voltage
e	error signal

dc_{in}	DC voltage input to the PLL
K_0, K_1, K_2, K_3	Constant parameters of advanced PLL
P_1	Forward path gain
L_1, L_2, L_3	Non-touching forward loops
X_1	Filtered component of polluted signal
X_2	orthogonal component of filtered version
X_0	Low-pass component of polluted signal
i_1	Inductor current of boost converter
$P_{max,m}$	Maximum power at particular instant
$V_{mpp,m}$	Maximum voltage at MPP in a particular instant
$I_{mpp,m}$	Maximum current at MPP in a particular instant
C_{dc1},C_{dc2}	DC-link capacitor for PV fed single-phase CHB-MLI based SAPF
D_1, D_2	Duty ratio of boost converters
h	Overloading factor
ΔD	Variation in duty ratio
ΔE	Amount of energy stored in the capacitor

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
ASD	Adjustable Speed Drive
APF	Active Power Filter
ANN	Artificial Neural Network
CHB-MLI	Cascaded H-Bridge Multilevel Inverter
CSI	Current Source Inverter
DAC	Digital to Analog Converter
DC	Direct Current
DC-MLI	Diode-Clamped Multilevel Inverter
DFT	Discrete Fourier Transform
DFRM	Double Frequency Ripple Minimization
DSP	Digital Signal Processing
DVR	Dynamic Voltage Restorer
EMI	Electro Magnetic Interference
FC-MLI	Flying Capacitor Multilevel Inverter
FFT	Fast Fourier Transform
GTO	Gate Turn-off Thyristor
HF	Harmonic Distortion Factor
HV	High Voltage
HVDC	High Voltage Direct Current

IEC	International Electro-technical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
kV	Kilo Volt
kVA	Kilo Volt Ampere
kVAR	Kilo Volt Ampere Reactive
KVL	Kirchoff's Voltage Law
kW	Kilo Watt
LPF	Low Pass Filter
LV	Low Voltage
MLI	Multilevel Inverter
MV	Medium Voltage
MVA	Mega Volt Ampere
MW	Mega Watt
PCC	Point of Common Coupling
PI	Proportional Integral
PI-VPI	Proportional Integral- Proportional Vector Integral
PR	Proportional Resonant
PLL	Phase Lock Loop
PQ	Power Quality
PWM	Pulse Width Modulation
PS-PWM	Phase-Shifted Pulse Width Modulation
RMS	Root Mean Square

RTW	Real-time Workshop
SAPF	Shunt Active Power Filter
SRF	Synchronous Reference Frame
SMPS	Switch Mode Power Supply
SCC	Short Circuit Current
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioner
UPS	Uninterruptible Power Supply
VAR	Volt-Ampere Reactive
VSI	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

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INTRODUCTION

[This chapter presents an overview and issues related to power quality. Different sources of harmonics and their effects are summarized briefly. Mostly recommended international standards of power quality have been also emphasized. Possible solutions of power quality problems like passive and active filtering approach have been also mentioned. Limitations of the active power filters in medium voltage and high power distribution system and suitability of cascaded H-bridge multilevel inverter based shunt active power filter in medium-voltage and high-power distribution system is also presented. The brief organization of the thesis is given at the end of this chapter.]

1.1 OVERVIEW

Recently, power quality (PQ) is becoming a significant element for power engineers and researchers as large number of energy integration are taking place in existing low- to medium-voltage (MV) distribution grid network. Grid-tied and standalone energy is gaining its importance in MV and high-power distribution sector as number of electrical equipments found their application in industries [1-3]. Linear loads present in distribution sector draw current of sinusoidal shape when source voltage applied to the load is sinusoidal in nature. Source voltage and source current waveforms are shown in Figure 1.1 for linear loads. But, in modern day scenario, maximum numbers of electrical equipments like adjustable electrical drives system, traction drives, arc furnaces etc. are driven by power electronics converter in low- to medium-voltage distribution sector. Non-linear characteristics of the power electronics switches used in the converters are responsible for non-linearity in the existing system. Source current becomes non-sinusoidal even though source voltage is sinusoidal in nature. The nature of non-linear source current is shown in Figure 1.2 which is drawn by non-linear loads in distribution system with sinusoidal source voltage [4, 5].

As non-linear currents are propagated through line, harmonic contents are introduced in distribution sector due to non-linear behavior of such converter fed loads. Current harmonics, generated by these non-linear loads present in distribution system, propagated to the source side through point of common coupling (PCC) and pollute the

supply current. These current harmonics, in combination with source impedance, generates voltage harmonics, which further affects utility by producing voltage distortion and notches. This voltage and current harmonics create serious problems in distribution side consumers as it results overheating of cables, motors, transformers and mal-operation of various safety devices [4-6]. Such power quality problem results more amount of losses in distribution and transmission sector. High frequency component in the voltage and current waveforms may also cause electromagnetic interference (EMI) in the line. Many national and international regulatory standards are defined like IEEE-519-1992, IEC 61000 etc. in order to describe PQ limits.

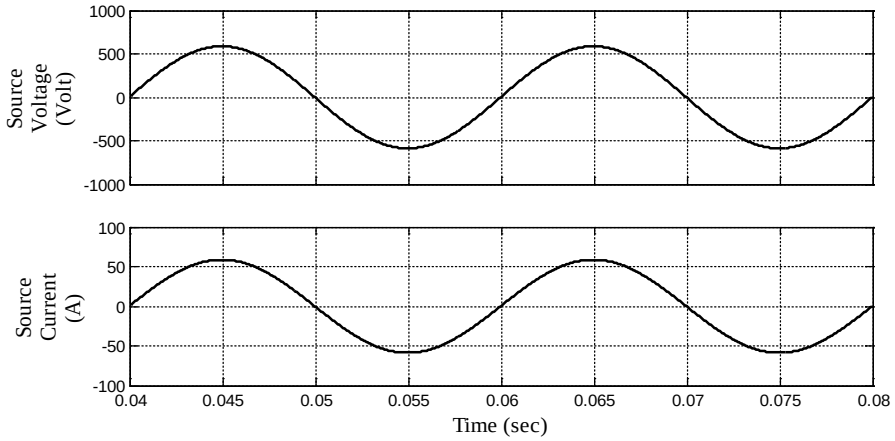


Figure 1.1 Source voltage and source current waveforms due to linear loads

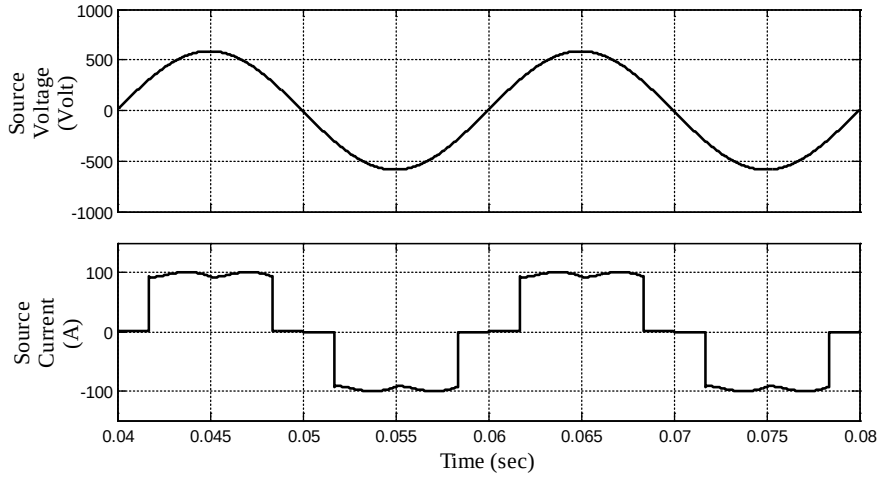


Figure 1.2 Source voltage and source current waveforms due to non-linear loads

Conventionally, passive filters composed of inductor and capacitors are used in passive filtering applications which are simple approach for mitigating PQ problems.

However, size, weight, tuning for particular frequency elimination, resonance are major concerns while installing these setups. Also, the conventional methods of power factor correction and passive filters are not able to respond in dynamic loading conditions. Dynamics of the power system and the random behavior of current harmonic components have motivated researcher community to explore alternate solutions in order to solve these current related PQ problems [7]. Various custom power devices such as distribution static compensator (DSTATCOM), series-, shunt-, and hybrid- APF, unified power quality conditioner (UPQC) etc. are used in order to suppress the drawbacks of conventional passive filters. Shunt APF (SAPF) is a mature technology till date to oppose numerous major PQ concerns like mitigation of current harmonics, reactive power etc. SAPF may also be capable of balancing of load current with its usefulness to solve neutral current in case of three-phase, four-wire system [8-12].

Two-level inverters are conventionally used as a main module of SAPF in low-voltage distribution sector. Two-level voltage source inverters (VSIs) in MV applications face problems related to higher voltage, current and power rating, higher dv/dt and di/dt ratings of switching devices, EMI etc. The use of line-frequency transformer is also becoming cost and space constraint while connecting to the grid. MLIs are evolving as major breakthrough in MV systems for their distinctive advantages over conventional inverters like less power and current stress on switches, smaller filter size, better voltage output with lower harmonic distortion, less EMI etc [13-20].

Three fundamental types of MLIs are projected in literature such as diode-clamped multilevel inverters (DC-MLI), flying capacitor multilevel inverters (FC-MLI) and cascaded H-bridge multilevel inverters (CHB-MLIs). Among these topologies, CHB-MLIs reach to higher voltage and power level due to its modular structure [13, 15]. These MLIs accumulate the attention of the researcher community as it found appropriate relevance in high-power & MV industrial drives, STATCOMs, DSTATCOMs, traction drives, large-scale non-conventional energy incorporation etc. Among all these relevant application, CHB-MLI based SAPF is widely demonstrated in literature and one of the most suitable technologies in present MV distribution sector for reducing PQ problems. Researchers are exploring new/ modified control techniques of CHB-MLI based SAPF for both single- and three-phase applications. The performance of five-level CHB-MLI

based SAPF is investigated with voltage and current-type of non-linear loading under normal/ distorted supply voltage in this thesis.

1.2 POWER QUALITY ISSUES

The term power quality has been used to illustrate the variation of the voltages, current and frequency in the electrical power system. It includes all the possible situations in which the waveform of the supply voltage or supply current waveform deviates from the sinusoidal shape at rated frequency. Due to the presence of power electronics converters and circuits, the shape of source voltage and source current get deviated from sinusoidal shape and this leads to poor quality power. Electrical equipments have their limit to tolerate the poor power quality. Continuous presence of poor quality power in the system can damage the electrical equipment. Hence visualization of quality of power and its improvement is necessary for making the system more efficient. A good quality of power means the ability of power system to provide sinusoidal current, voltage with rated frequency. Some terms are defined to measure the quality of power, like harmonics, total harmonic distortion, distortion factor, displacement factor etc. Among these, harmonics are causing the major trouble in electrical networks [6, 9].

Harmonics are periodic current and voltages which have frequency as integral multiple of supply frequency or fundamental frequency. Many electrical equipment and apparatus (specially consisting of power electronics switch based converters) having non-linear characteristic is the main source of harmonic injection in the electrical power system. They cause problems such as malfunctioning of electrical devices, error in power measurement, overheating, false tripping of devices, excessive neutral current, conductor overheating etc. Other adverse effects of harmonics in electrical power system are introduction of EMI and increased heating loss. Poor power factor leads to more reactive power demand. Generally, 50 Hz or 60 Hz are considered as fundamental frequency. The dominating harmonics, which affect the system more adversely are lower order harmonics i.e. integral lower order multiple of fundamental frequency. Third, fifth and seventh harmonic components are most dominating harmonic orders. There are some significant terms which are defined in the standard to study, understand and classify the concept of harmonics which can help in research of their mitigation. Even-, odd-, triplen-

harmonics are the general terms used in the study of harmonics. Some other important terminologies like inter-harmonics, intra-harmonics, sub harmonics are used to classify the harmonic orders present in the system. It is necessary to find the mitigation technique for current and voltage harmonics.

1.2.1 Causes of Harmonics

Harmonics are caused by loads in which the current waveform does not conform the fundamental waveform of the supply voltage. Developments in digital electronics and power semiconductor devices have led to a rapid increase in the use of nonlinear devices. The requirement of controlled power through power electronic converter for automation processes in industries is the main source of current harmonics [4-8]. The source of harmonics in power system can be classified as shown in Figure 1.3.

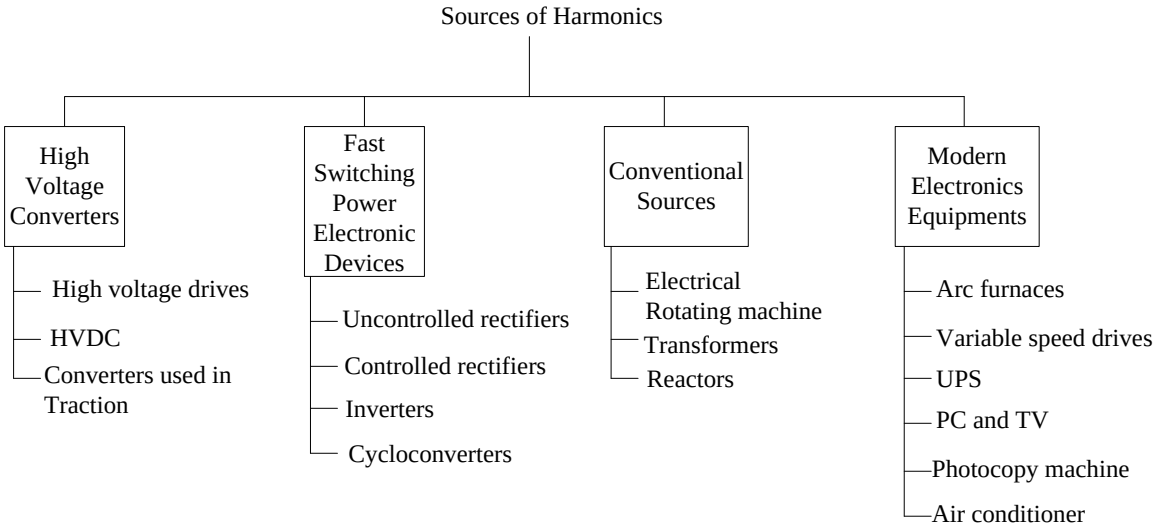


Figure 1.3 Sources of harmonics in power system

High voltage converters are used in medium-voltage to high-voltage electric drives, electric traction and high-voltage DC transmission (HVDC) systems. The applications of advanced technologies in industrial sectors include semiconductor systems which are designed using fast switching semiconductor devices such as phase controlled rectifiers, uncontrolled rectifiers, inverters, AC voltage controllers and cycloconverters. Commercial facilities such as office complex, department stores, hospitals, internet data centers and others are dominated with energy efficient fluorescent lighting with electric ballasts; which employs switch mode power supply, uninterruptable power supply, personal computers, printers etc. The conventional sources are electrical

rotating machines, transformers and reactors. Harmonics are generated due to non-linear magnetizing characteristics of the steel used in the magnetic core. The transformer exciting current is also rich in harmonics even at normal operating conditions [21-28].

1.2.2 Effects of Harmonics

Current harmonics generated by the non-linear loads propagate throughout the power network. Harmonic current passing through the system impedance causes a voltage drop for each harmonic and result in voltage harmonics appearing in the system bus and this leads to power quality problems [25, 26].

These currents interact adversely with a wide range of power system equipment, most notably capacitors, transformers and motors causing additional losses and consequently overheating happens. Shunt capacitors which are used for power factor correction causes resonance [26].

Harmonic currents may result in the transformer RMS current being higher than its capacity. The increased total RMS current results in increased conductor losses and heating. Harmonic current component in transformer also increases eddy current losses and core losses [27].

The performance of motors is deteriorated by voltage harmonics. This distortion in motor terminals is translated into harmonic fluxes within the motor causing high frequency current in the rotor and resulting in additional losses, decreased efficiency, vibration and high pitch noises [28].

Higher order harmonics cause problems of electromagnetic interference (EMI), especially with sensitive electronics equipments (e.g. navigation, communication control and automation).

Harmonic currents from non-linear loads also affect the accuracy of watt-hour and demand meters. Conventional magnetic disks watt-hour meter tend to have negative values at harmonic frequencies. This error increases with increasing frequency.

The digital relays and their control algorithms depend on the sampling data and zero crossing, which may be adversely affected in presence of harmonics in both voltage and current. Current harmonic distortion can also have an effect on the interruption capability of circuit breakers and fuses.

1.3 POWER QUALITY STANDARDS AND INDICES

Several indices have been defined to indicate the level of harmonics in the voltage and current waveforms. The most important index is the Total Harmonic Distortion. It is defined as the ratio of the RMS value of the total harmonic currents to the RMS value of the fundamental current and usually expressed as a percentage of the fundamental current. The THD of the current is given as

$$\mathrm{THD} = \left(\sqrt{\sum_{h=2}^{\infty} {I_h}^2} \right) \Big/ I_1 \tag{1.1}$$

The other useful term is the Total Demand Distortion (TDD). It is defined as the ratio of RMS value of total harmonic currents to the RMS value of maximum demand of current. There are various organizations viz. users, equipment manufacturers and research institutes working together to come up with standards, recommended practices and harmonic limits. IEEE-519 standard was first issued in 1991[13]. It gave preliminary guidelines and revised in 1992. IEEE 519-1992 recommended practices and requirements in harmonic control in electrical power systems provide guidelines to determine acceptable limits. The IEC-61000 series is an internationally accepted set of standards. The IEC 61000 and IEEE 519-1992 describes the harmonic standards. Some commonly used power quality standards are given in Table 1.1 [29-33].

Table 1.1 Current distortion limits for general distribution systems (120 V to 69 kV) (IEEE 519-1992)

I_{sc} / I_L	**Harmonic order (odd harmonics)**					
	h < 11	**11 ≤ h < 17**	**17 ≤ h < 23**	**23 ≤ h < 35**	**h ≥ 35**	**TDD**
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonics limits above						
I_{sc} = maximum short-circuit current at point of common coupling I_L = maximum demand load current at point of common coupling						

1.4 CURRENT HARMONIC COMPENSATION TECHNIQUES

Current harmonic component compensation is need to be done near load terminal in distribution sector so that the harmonic current do not flow into the existing system. This current harmonic compensation phenomenon greatly reduces the distortion level in the voltage profile at point of common coupling (PCC). The imposition of many national and international power quality standards force consumers to maintain the amount of harmonic content which is injected by non-linear loads into the existing power system. Various methods are already proposed in literature in order to counter current harmonic content in distribution sector. Among all these methods, passive and active filters are viable solutions used and adopted by industry personnel [34-36].

1.4.1 Passive Filters

Passive filters are composed of inductance, capacitance and resistive elements. Different combinations of these elements are properly tuned in order to mitigate current/voltage harmonic components. Passive filters are commonly used by industries till date. These filters are relatively less expensive as compared to other techniques which are available in literature for harmonic component elimination. These filters either connected in series with line in order to block current harmonic components or in shunt manner, in order to filter current harmonics from line. Shunt type of passive filters are also capable for power factor correction with above mentioned features [36].

Single-tuned ‘notch filter’ is the most commonly used passive filter. This type of filter is the most economical one and this is sufficient for common type of loads. This is connected with line in shunt manner which develops a low impedance path to a particular harmonic component. The double-tuned filter performs the same operation which is composed of two numbers of single-tuned filters. Double-tuned filters have advantages like, lower power losses, and lower impedance at the frequency of parallel resonance over single-tuned filter. The high-pass filters are another type of single-tuned type filter where resistive and inductive elements are connected in parallel manner instead of series. This connection results in a wide-band filter having impedance at high frequencies limited by resistance. The three types of passive filters are shown in Figure 1.4. One of the main conditions of implementing passive filters in existing line is it should be placed

on a bus where the short circuit reactance can be expected to remain constant. Efficacy of parallel resonance is greatly affected by the changes in system impedance, as the notch frequency remains fixed [35, 36].

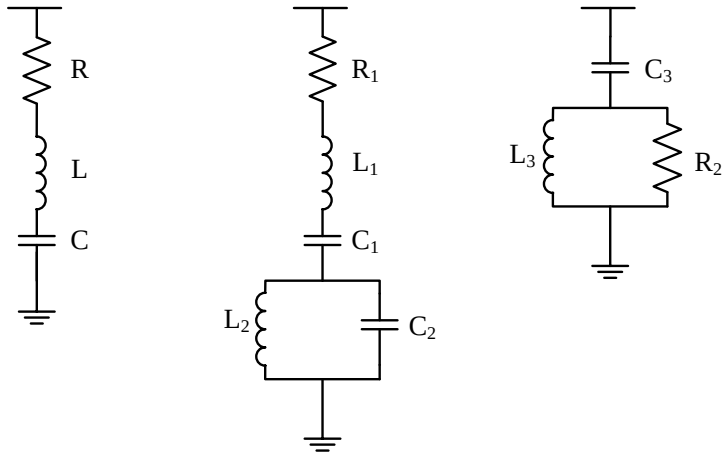


Figure 1.4 (a) Single-tuned filter, (b) double-tuned filter, and (c) second-order high pass filter

Another type of passive filter is series passive filter, which is connected in series with the load. Series filter, parallel combination of inductance and capacitance, are tuned in such way that they can provide high impedance at selected frequency. The flow of harmonic component in load current is blocked the high impedance created at selected harmonic frequency. At fundamental frequency, filter would be designed to yield low impedance, thereby allowing the fundamental current to flow with only minor addition to the source impedance and losses.

Multiple harmonic components in load current are blocked by series filters. Each filter need to be tuned for each harmonic current component. Series filters need to be designed in such a way that it can carry full load current. These filters must also have an over current protection in addition.

Despite simplicity and lower cost of passive filters, their use is limited and reasons are summarized as follows [36]

- Passive filters are not suitable for use in distribution sector if system conditions are changing in nature. Once installed, passive filters are rigidly in place. These passive filters are tuned for a particular frequency. Therefore, if any other

frequency components need to be removed from the system, it will be very difficult to change the size and installation of another set of passive components.

- A filter need to be designed in such a way that it can adjust with system parameter variation including load changing conditions. Filter need to be re-tuned with change in system parameter in case of passive filters.
- The system impedance is one of the main considerations while designing passive filters. The passive filter impedance must be less than the system impedance in order to design system properly.
- Special protective and monitoring devices are required.

1.4.2 Active Filtering Approach

Active power filter (APF) is a mature technology till date to oppose numerous major power quality concerns like mitigation of current harmonics, reactive power, regulation of the terminal voltage, suppression of voltage flicker etc in presence of non-linear loads [37]. APF may also be capable of balancing of load current with its usefulness to solve neutral current in case of three-phase, four-wire system. Figure 1.5 shows the basic compensation principle of the shunt APF. Two-level pulse width modulated (PWM) inverters with capacitors as energy source are conventionally used as a main module of APF. The PWM inverter switches are switched in such a way that inverter can generate compensating current of equal and opposite magnitude of harmonic component generated by load current. This phenomenon helps to make sinusoidal source current even in presence of non-linear load current with almost unity power factor.

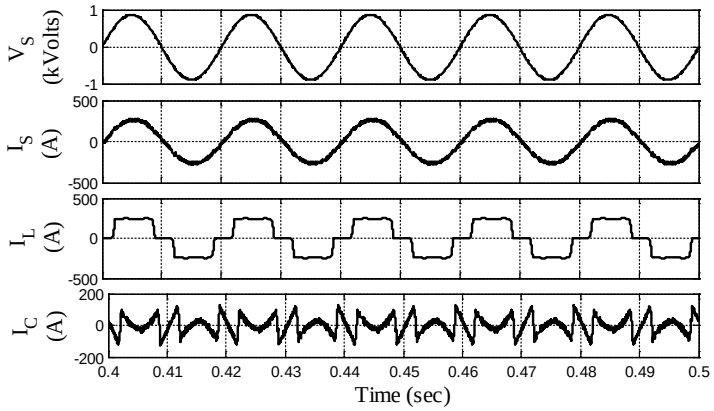


Figure 1.5 Basic compensation principle of shunt APF

The wide ranges of objectives are achieved either individually or in combination depending upon the requirement of control strategy and configuration. The APFs can be broadly classified as the shunt APF, series APF, and hybrid APF.

Significant advancement in the switching speed of solid state devices, self commutating power semiconductor devices namely MOSFET, IGBT, IGCT along with progress in high-speed processors such as DSP, FPGA has made APFs more efficient and effective to mitigate current harmonics which are generated by non-linear loads in low to medium voltage system. Many research articles related to SAPF technology have been presented during last two decades. Most of the research articles dealt with principle of operations, design and development of different control algorithms including several reference current generation techniques and different pulse width modulation techniques. Still, maximum research articles do not address its limitations in medium-voltage and high-power distribution sector.

1.5 LIMITATIONS OF CONVENTIONAL APF IN MEDIUM TO HIGH VOLTAGE SYSTEMS

In present scenario, industrial sector uses many controlled process applications which are being carried out at medium-to-high voltage and high-power levels. The specifications of electric drives used in industries have reached up to 20 MW with supply voltage range from 3.3 kV to 13.8 kV at rated 50/ 60 Hz frequency. The large size passive filters for different harmonic components are used in high voltage DC (HVDC) systems which result in high space requirement and high cost. Alternatively, application of APFs in high voltage is gaining importance and interest of researchers.

Two-level VSIs in medium-to-high voltage applications face problems related to higher voltage, current and power rating, higher dv/dt and di/dt ratings of switching devices, EMI etc. The use of line-frequency transformer is also becoming cost and space constraint while connecting to the grid. MLIs are evolving as major breakthrough in medium-voltage and high-power systems for their distinctive advantages over conventional two-level inverters like less power and current stress on switches, smaller filter size, better voltage output with lower harmonic distortion, less EMI, lesser voltage and current rating of power electronic devices etc [13, 15, 16, 19, 20].

SAPFs can be installed in high voltage system in two methods. In the first method, semiconductor devices can be used in series manner in order to share voltage ratings among switching devices. But, this idea faces challenge of unbalanced static and dynamic voltage sharing due to deviations of device characteristics. Furthermore, this configuration requires large number of snubber circuits associated with switching devices. This phenomenon causes additional losses and thus affects SAPF system efficiency adversely. The second method is to connect SAPF unit to the grid at PCC through step-up transformer. In this method, problem with transformer lies with size, VA rating of the system because harmonic current will flow through transformer. Even the transformer core may saturate in transient condition due to DC magnetizing and overvoltage problems due to the presence of high frequency components. This arrangement makes the overall system costly and bulky in size.

1.6 MLI BASED SAPF FOR HIGH VOLTAGE SYSTEM

Development of high voltage inverter based on MLIs has attracted the attention of power electronics community. MLIs consist of an array of power semiconductor switches and capacitors as passive elements. The switch timing of power electronic switches is such that it allows the summation of capacitor voltages. With the help of proper switching phenomenon, high voltage output may be obtained, while power electronic switches are subjected to lesser amount of switching stress. Staircase output voltage is obtained in case of MLI. However, voltage may become sinusoidal if number of levels is high enough. Therefore, it may be well possible that harmonic distortion of output voltage is quite low [13].

A MLI basically produces a staircase type waveform with proper switching pattern of several lower rating dc sources. As the number of levels in the output voltage increase, the staircase type output voltage becomes more like a sinusoidal one with minimum possible harmonic distortion. However, in real-time scenario, number of voltage levels is limited by voltage unbalancing issue among switches, clamping requirement as per application etc. Batteries and capacitors, renewable energy source such as solar, fuel cell etc. are used as dc voltage source in MLIs.

Basically, MLI topologies are broadly classified into three major categories and these are DC-MLI, FC-MLI and CHB-MLI. Cascaded MLIs are increasingly being adopted in high power applications due to its modular structure which makes this easy to design, assemble and control with respect to other types of MLIs [13, 20].

In operation of MLI based SAPF, the harmonic component of load current is derived through harmonic detection circuit and used it with opposite polarity as the reference compensating current. Switching signals of MLI are generated in such a manner that AC side output current of SAPF follows the reference current nearly free from harmonics. The application does not require active power output from inverter; therefore separate source for each converter bridge is not required. The SAPF also draws small power from source to compensate the switching and capacitor losses in the SAPF. DC voltage of each converter should be balanced for proper compensation. The capacitor voltages are sensed and compared with the reference voltage. The error is processed in a controller to generate loss component of SAPF which is used to generate the reference signals of SAPF. In a five-level CHB-MLI, voltage across each capacitor is nearly half of the supply line voltage. This reduces the rating of switching devices which is an important advantage to support the use of MLI based SAPF in high voltage system. Further, the voltage waveform in the AC side of MLI is of reduced THD as compared to two-level inverter.

1.7 ORGANIZAION OF THESIS

The thesis is organized in eight chapters and the work included in each chapter is briefly outlined as follows:

Chapter 1 presents an overview of different power quality problems especially due to harmonics, their effects on different power system equipments. Mostly recommended international standards of power quality have been also emphasized. Possible solutions of power quality problems like passive and active filtering approach have been also mentioned. Limitations of the two-level inverter based active power filters in medium-voltage and high-power distribution system and suitability of cascaded H-bridge multilevel inverter based shunt active power filter in medium-voltage and high-power

distribution system is also presented. The organization of the thesis is also presented in this chapter.

Chapter 2 presents a widespread review on multilevel inverter based active power filter by assessing its potential to replace two-level inverter based APF in medium-voltage distribution sector. Different possible configurations, control techniques, selection of power semiconductor switches and their different applications are reviewed comprehensively. The scope of the proposed research work and author's contributions are also presented in this chapter.

Chapter 3 deals with the system hardware development for a laboratory prototype model of CHB-MLI based SAPF for the experimental verification. A prototype model of five-level CHB-MLI has been built in the laboratory. H-bridges are designed with IGBT STGW30NC120HD. A driver circuit is composed of TLP 250 opto-coupler and delay circuit. The dSPACE 1104 is used for real-time generation of CHB-MLI gate pulses for all power electronic switches. The system hardware is composed of H-bridge inverter circuits, driver circuits for IGBTs, voltage and current sensors, signal conditioning circuit, inductors, diode-bridge rectifier based non-linear loading and dSPACE 1104 real-time controller. The complete procedure for building this set-up is described in detail.

Chapter 4 presents an advanced current control loop which consists of a new breed of compensator called proportional-resonant compensator for cascaded H-bridge multilevel inverter based shunt active power filter in order to maintain zero steady-state current error. Stability of proposed current control loop and closed-loop control mechanism is extensively checked and analyzed using transfer function approach and root-locus criteria. A complete mathematical analysis of the proposed control system has been presented and parameters of proportional-resonant regulator are finely tuned using bode-plot technique. The performance of proposed control mechanism is tested using MATLAB/Simulink. A detailed experimental analysis of single-phase five-level CHB-MLI has been carried out to verify effectiveness of the proposed controller over conventional one. Source current waveform becomes sinusoidal and harmonic limits are in compliance with IEEE-519 standard after successful operation of filtering unit.

Chapter 5 presents PI-vector-proportional-integral (VPI) compensator based current control strategy for CHB-MLI based SAPF in order to nullify steady-state source current

error. This controller shows excellent selective harmonic elimination capability thereby steady-state current error is nullified. Mostly, frequency selection based methods are used for selecting compensator gain parameters. But, this technique leads to deficits in accuracy. Therefore, particle-swarm optimization (PSO) technique is used for tuning the PI-VPI compensator gain parameters in order to fill the gap for proper tuning methodology of compensator gains. PSO approach operates with a cost function by minimizing source current total harmonic distortion and steady-state error of current control loop. Detailed simulated and experimental analysis of proposed system shows effectiveness of proposed controller over conventional current controller.

Chapter 6 presents an improved synchronous reference frame theory based control algorithm for solving current related power quality problems. This proposed control is a complete solution in case of balanced and/or unbalanced loading condition in existing distribution system. This control algorithm is equally effective in case of distorted and/or unbalanced supply voltage condition due to the use of advanced PLL. An advanced PLL having dc and harmonic rejection capability is presented in this chapter. The advanced PLL can track frequency and phase angle accurately even though source voltage is polluted. A detailed mathematical modeling and stability analysis of this PLL is presented using Routh-Hurwitz criteria. A systematic design procedure using Eigen value analysis is proposed for calculating PLL parameters. Closed-loop SAPF control stability is tested using root-locus analysis. An extensive simulation and experimental study of advanced PLL and CHB-MLI based SAPF has been performed under highly distorted source voltage and different non-linear loading conditions to show the effectiveness of the proposed control.

Chapter 7 presents modeling of two-stage CHB-MLI based SAPF for active and reactive power management in grid-tied PV application. A boost converter is used in between PV and CHB-MLI for scaling up voltage level. Control algorithm of this two-stage conversion system is composed of boost converter control and CHB-MLI control. Perturb and Observe (P and O) MPPT is used for ensuring maximum power point tracking during variable irradiance. Self-charging algorithm is used for balancing dc-link voltages of five-level CHB-MLI. PS-PWM technique is used for generating MLI gate pulses. Advanced

PLL is used in control algorithm in order to ensure its operation under non-ideal source voltage conditions.

Chapter 8 summarizes the main conclusion and significant contribution of the thesis and states the scope for further research in this area. List of important references is given in the end.

CHAPTER 2

LITERATURE REVIEW ON MULTILEVEL INVERTER BASED ACTIVE POWER FILTER

List of Published Papers

1. **S. Ray**, N. Gupta, R. A. Gupta, "A Comprehensive Review on Cascaded H-bridge Inverter-Based Large-Scale Grid-Connected Photovoltaic," *IETE Technical Review*, Taylor and Francis, vol. 34, no. 5, pp. 463-477, Sep. 2017.
   DOI: https://doi.org/10.1080/02564602.2016.1202792
2. **S. Ray**, N. Gupta, R. A. Gupta, "Power Quality Improvement using Multilevel Inverter Based Active Filter for Medium-Voltage High-Power Distribution System: A Comprehensive Review," *International Journal of Power Electronics*, Inderscience. **(In Press)**

CHAPTER 2

LITERATURE REVIEW ON MULTILEVEL INVERTER BASED ACTIVE POWER FILTER

[Medium-voltage distribution system faces great challenges as number of medium-voltage; high-power loads such as electric drives etc. are increasing which inject non-linearity into the grid. On the other side, sinusoidal and uninterrupted voltage and current waveform at rated frequency is highly desirable at low to high power consumer end. Voltage/ current harmonic content, poor power factor, reactive power burden, poor voltage regulation and excessive neutral current create major problem in balanced/unbalanced loading condition. In such cases, active power filters provide a viable solution to overcome the aforesaid power quality problems. Conventional two-level inverter based active power filter is becoming popular and cost effective solution due to its simple structure and easier control. However, this configuration is facing great challenges in medium-voltage distribution network due to use of high rating switching devices and use of line-frequency transformer. Multilevel inverter (MLI) posses a great solution in such scenario as it generates higher voltage output with lower rating switching devices. As a result, voltage and current of improved quality can be maintained using MLI which is based on lower rating semiconductor devices. MLI based filters are successfully used in medium-voltage distribution sector and a lot of research around the globe are already carried out in this area. However, capacitor voltage balancing is a major research domain in MLI based filters. Despite of this, MLI technology is widely accepted in medium- to high-voltage industrial applications. Therefore, this chapter presents a widespread review on MLI based active power filter (APF) by assessing its potential to replace two-level inverter based APF in medium-voltage distribution sector. Different possible configurations, control techniques, selection of power semiconductor switches and their different applications are reviewed comprehensively.]

2.1 INTRODUCTION

Recently, power quality (PQ) is becoming an important aspect for engineers and researchers as large amount of grid integration takes place in distribution network. Moreover, use of large numbers of non-linear loads is becoming a major concern to consumers and utilities [7-9]. Excessive neutral current, power factor degradation, voltage regulation, voltage sag, swell, voltage flicker, burden of current harmonics and balancing issue contrive in distribution system itself [10-14]. Among these problems, current harmonics generated by non-linear loads create major problem in distribution system. Current harmonics also produce voltage harmonics which propagates to

distribution side consumers through point of common coupling (PCC). PQ problems can create serious issues like overheating of cable, transformer, motor and other electrical and electronics devices and malfunction of various protection equipments [6, 7, 11]. Several power electronics converter based topologies such as active power filter (APF), distribution static compensator (DSTATCOM), unified power quality conditioner (UPQC) and dynamic voltage restorer (DVR) can mitigate these kinds of problems in distribution system [6,7]. APF is a mature technology till date to counter several major PQ concerns. APF can be used for mitigating current harmonics; reactive power nullification, load current balancing with its effectiveness to solve neutral current issue [11]. Medium- voltage distribution system plays an important role in present scenario as number of high power medium voltage drive usage increases in industries. Two-level inverters are normally used as a main component of APF in low-voltage distribution system but for medium-voltage, multilevel inverters (MLIs) have become more attractive solution for their distinct advantages over the two-level inverters, such as lesser voltage and current stress on switching devices, small filter size, better output waveform with low total harmonic distortion, less electromagnetic interference and acoustic noise [13].

This chapter aims at addressing a widespread investigation on MLI based APF which helps to find out possible research gaps. Research papers of MLI based APFs for reactive power compensation and power quality improvement are critically reviewed and classified into three major categories. The first category [39-61] is on the development and survey related to MLI based APF, while the second and third categories are based on single-phase [62-85], and three-phase connection [86-158] of MLI based filtering applications, respectively.

2.2 LITERATURE REVIEW

This segment portrays the shortcomings of conventional filters and also highlighted the advancement related to MLIs and current status of MLI based APFs. Traditionally, passive filters (PF), which are developed in early stage, are one of the best solutions available in industry with its simplest and rugged structure. However PF suffers with problems like resonance, size, fixed compensation etc. [16, 17]. The performance of passive filter is also affected by source impedance. APF is another matured filtering solution for mitigating power quality problems and to overcome the drawbacks of PF.

Conventional two-level APF technology is a proven solution for mitigating current-based PQ problems which is created by non-linear loads in distribution network. APF is basically a combination of voltage/ current source converters and passive elements which can store energy (capacitor/ inductor) [18, 19]. APF can be primarily of two types i.e. series APF and shunt APF [77, 80], as shown in Figure 2.1 (a) and 2.1 (b), respectively. Rigorous research leads to another cost-effective solution by the development of hybrid filters [85], as shown in Figure 2.1 (c). In hybrid filters, lower order harmonics are compensated by passive filters whereas higher order harmonics are compensated by APF which gives cost-effective solution. Another topology of APFs is unified power quality conditioner (UPQC), as shown in Figure 2.1 (d). It serves the same purpose with additional features of series compensation [61]. UPQC comprises of shunt and series active filter having dc-bus in common. Moreover, two-level active filtering is the most suitable and widely used technology among all these kind.

Recently, Industrial high-power, medium-voltage drives and large-scale grid-connected photovoltaic and wind energy system leads to expansion of medium-voltage distribution system. Though, two-level inverter based APF is a cost-effective solution for low-voltage distribution system but in medium-voltage distribution sector, MLI based APF is having advantages over two-level inverter as enumerated in [13]. This leads to research for MLI- based APF. Three basic types of MLIs are proposed in literature such as diode-clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI) and cascaded H-bridge MLIs (CHB-MLI) [19]. Among these three types of topologies, CHB-MLIs reach to higher voltage and power level due to its modular structure [14, 15]. MLIs are now a mature technology which is already been researched for 25-30 years. DC-MLI is found in literature in 1980s [62, 63]. CHB-MLIs found their suitable application in mid 90s [64]. CHB-MLI is primarily used for electrical drives system and utility application, which can be found from literatures [67]. Major literatures are found on the basis of regenerative application of CHB-MLI based electrical drive system. Capacitor-clamped MLI came into picture in 1990s [68]. These MLIs found their suitable application in high-power & medium-voltage industrial drives [69], STATCOMs [70], DSTATCOMs [71-73], traction drives [36], large-scale renewable energy integration [15, 37] etc. In recent times, modular multilevel inverters (MMIs) are found suitable in HVDC applications [20].

Recently, research is also going on in the direction of reduction of power electronics components used in the topology for reduction of complexity in the driver as well as power circuit [40].

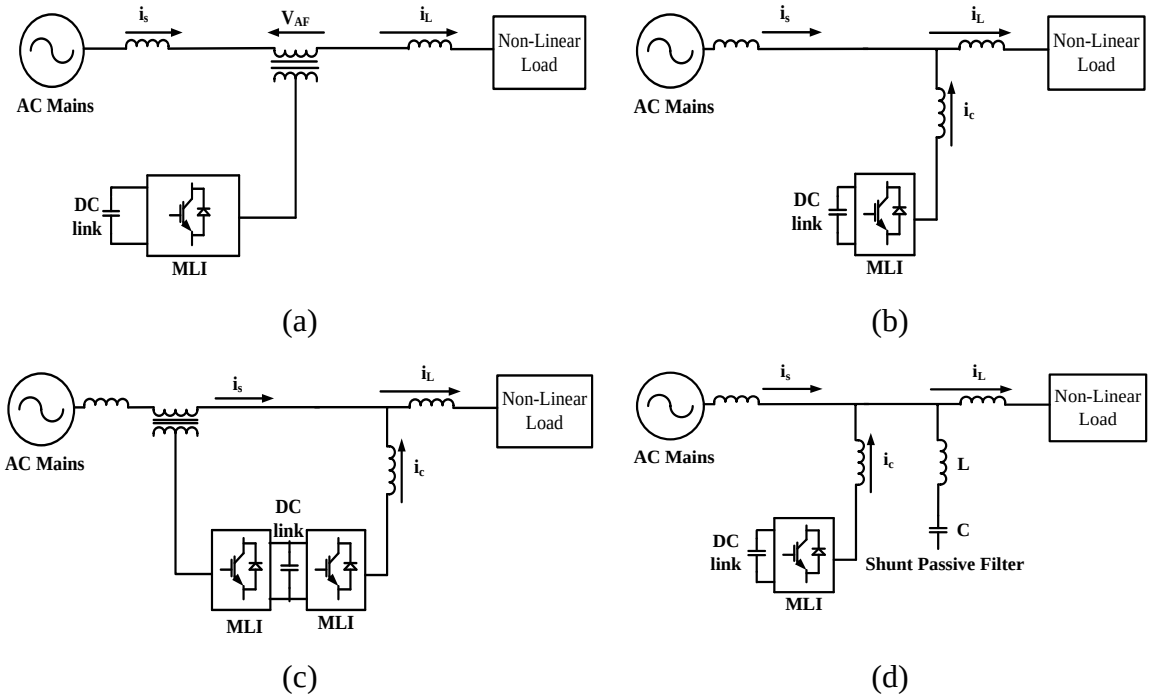


Figure 2.1 (a) Block diagram representation of MLI based series APF, (b) MLI based shunt APF, (c) MLI based UPQC, and (d) MLI based hybrid APF

Among all these applications, multilevel inverter based active filtering is widely demonstrated in literature and one of the most suitable technologies in present distribution scenario to mitigate power quality problems. A significant amount of publications are reported on single-phase [62-73], [75-84] MLI based shunt APF. Three-phase, three-wire (3P3W) and three-phase, four-wire (3P4W) MLI based shunt active compensation have been reported in [85-103, 105-112, 114-118, 121, 122, 125-129, 131] and [84, 104, 113, 119-120, 123-124, 130], respectively. MLI based series type APF [120, 139, 145], combination of series and shunt [96, 143], as well as passive filters connected with shunt APF [85, 138] are also reported in literature but in low volume due to cost and complexity constraints. Self-commutating power electronics devices, hall-effect sensors, amplification and isolation circuits are major components in MLI based APF technology. A lot of research is also focused in the area of control technique related

to MLI based SAPF. Research in the direction of control theories and topologies is also helpful for boosting the performance of active filtering.

2.2.1 Multilevel Inverters (MLI)

Multilevel inverters consist of an array of power semiconductor switches and capacitors as passive elements. The switch timing of power electronic switches is such that it allows the summation of capacitor voltages. With the help of proper switching phenomenon, high voltage output may be obtained, while power electronic switches are subjected to lesser amount of switching stress. A MLI basically produces a staircase type waveform with proper switching pattern of several lower rating dc sources. As the number of levels increase, the staircase type output voltage becomes more like a sinusoidal one. Therefore, it may be well possible that harmonic distortion of output voltage is quite low.

However, in real-time scenario, number of voltage levels is limited by voltage unbalancing issue among switches, clamping requirement as per application etc. Batteries and capacitors, renewable energy source such as solar, fuel cell, etc are used as dc voltage source in MLIs.

Many topologies of MLI have been presented by researchers in last two decades. The MLI is first proposed by Akagi et al. in the year of 1981 [103]. An early traceable patent is published in 1975, in which CHB-MLI was first mentioned which connects separate dc voltage sources to form a stair case type ac output voltage. However, its use in industrial applications starts in the mid 1990s. After 1990, different high-power MLI topologies have been presented in literature for different industrial applications [52]. Patents were filed in order to show the superior performance of CHB-MLI for industrial motor drive over conventional inverters [93]. Great demand of medium-voltage and high-power inverters in power industry have drawn remarkable attention in the CHB-MLIs. MLIs are comprehensively used in traction drives, different heavy electric drive systems, conveyer belts, pumps, fans, blowers, mills, compressors etc. A MLI is superior in terms of performance than two-level inverter such as lesser switching stress, lesser dv/dt, di/dt, less voltage and power handling capacity of switching devices, less THD at output voltage, lower distortion and less EMI etc.

2.2.1.1 *Conventional MLI topologies*

Basically, MLI topologies are broadly classified into three major categories and these are diode-clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI) and CHB-MLI. Brief descriptions of these MLIs are presented in later section.

Diode-Clamped Multilevel Inverter (DC-MLI)

An ‘m’ level DC-MLI produces ‘m’ levels of phase voltage and ‘(2m-1)’ levels of line voltage as shown in Figure 2.2 [62]. This ‘m’ level DC-MLI consists of (m-1) capacitors. The three-phases of MLI share a common DC link. This has been divided equally into four capacitors (V_{dc}). Voltage across each capacitor is equal. These voltages are summed up to form output voltage ($4V_{dc}$). However, clamping diodes limit voltage stress across each device.

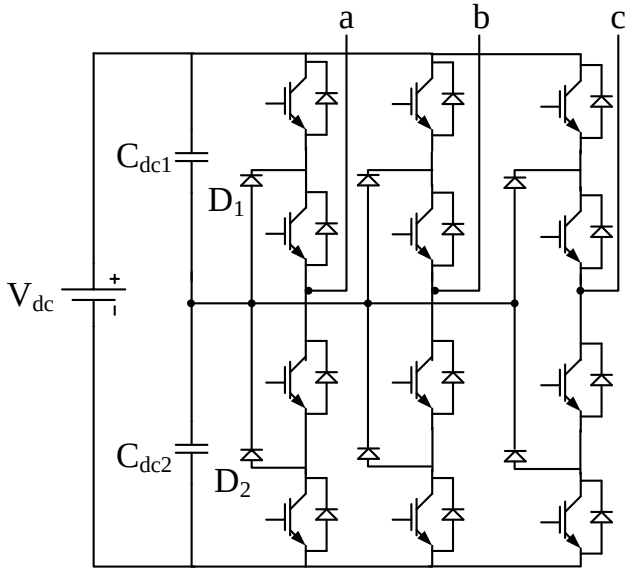


Figure 2.2 Diode-clamped multilevel inverter

Proper switching combination decides different levels associated with inverter output voltage. Although, each power electronic switch needs to block minimum and same voltage level, the clamping diodes need to handle different voltage ratings based on the switching pattern. The number of diodes required for each phase of output voltage is (m-1) x (m-2). DC-MLIs are used in medium-voltage and high-power drives, static VAR compensator, interface between high voltage DC and AC line. The main advantages and disadvantages are enlisted as follows:

Advantages

1. As all the three phases share common dc-link, this phenomenon reduces the requirement of capacitors in inverter unit. This makes DC-MLI suitable for medium-voltage to high-voltage applications such as adjustable speed drives.
2. This maintains high efficiency for fundamental switching.

Disadvantages

1. Requirement of clamping diodes increases excessively as the number of inverter levels increases.
2. This inverter is not modular in structure. Therefore, if any fault happens, inverter malfunction happens.

Flying Capacitor MLI (FC-MLI)

The structure of FC-MLI is similar to DC-MLI except the use of clamping diodes as shown in Figure 2.3. FC-MLI uses capacitors for generating stair case output voltages

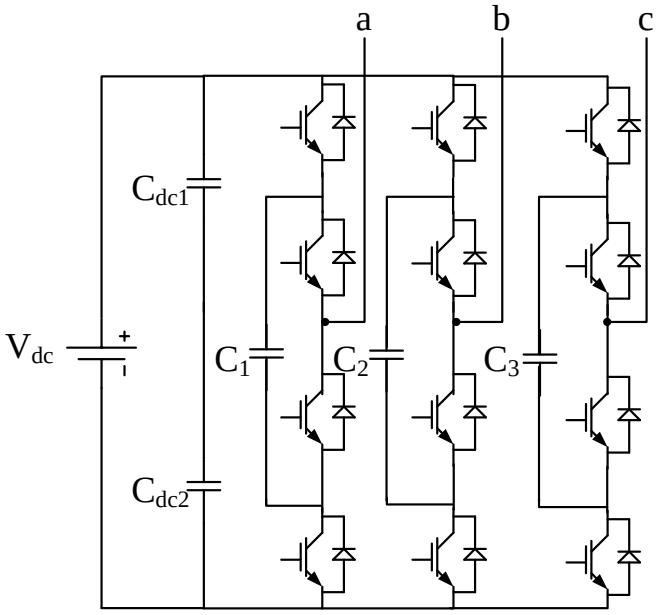


Figure 2.3 Flying-capacitor multilevel inverter

instead of diodes in DC-MLI. This particular topology has a ladder structure of dc-link capacitors, in which voltage of each capacitor differs from the next capacitor. Flexibility wise, FC-MLI [62] is more suitable than DC-MLI. Various switching combinations can be used for generation of stair case type of voltage waveform for each phase. FC-MLI

does not require all the switches conducting in series as well as FC-MLI is having phase redundancies. This phenomenon allows charging and discharging of capacitors and as a result, output voltage can be balanced in various levels. An ‘m’ level FC-MLI which produces ‘m’ level of output voltage, require (m-1) dc-link capacitors. This inverter additionally requires (m-1) x (m-2)/2 auxiliary capacitors per phase. The main advantages and disadvantages associated with this topology are enlisted below:

Advantages

1. Phase redundancies are available for balancing capacitor voltage levels,
2. Real as well as reactive power can be controlled through this inverter.

Disadvantages

1. Use of lot of capacitors makes voltage balancing very difficult. Therefore, control system associated with this becomes very complex as the number of levels increase. Also, pre-charging of different capacitors to the same voltage level are complex.
2. Use of large number of balancing capacitors make the system bulky in nature as well as it becomes costly,
3. Switching utilization efficiency is quite low for real power transmission.

Cascaded H-Bridge MLI (CHB-MLI)

Cascaded H-Bridge multilevel inverter (CHB-MLI) [63] topology is symmetrical in structure with the use of separate dc-link voltage as shown in Figure 2.4. This MLI is relatively newer among the other two types of MLIs. This structure is modular in nature. This inverter unit needs least number of components among all three types of MLIs in order to generate same voltage level. This CHB-MLI is basically a series connection of single-phase H-bridge inverter units. Two H-bridge per phase needs to be connected per phase in order to get five-level of output voltage. However, different H-bridges require separate dc-link voltages. As these H-bridges are cascaded in manner, staircase output may be generated with the help of proper switching technique. Symmetric dc-link voltage is used for each H-bridge cell. If the levels are higher enough, switching can be done in fundamental frequency. Harmonics can be controlled by adjusting conducting angles of different switches at different output voltage levels. Three-phase CHB-MLI can be used

in industries with star type or delta type of loads. Now a day, CHB-MLI is used for high-power medium voltage drive system, renewable energy integration, static VAR compensator, active power filter etc. The main advantages and disadvantages related to this structure are as follows:

Advantages

1. Least number of components is required in CHB-MLI among all other MLI topologies for generating same number of voltage levels.
2. As 'H-bridge' inverters are used in a cascaded manner, this structure is modular in nature. This makes packaging and manufacturing cost less with less time consuming.
3. Replacement of H-bridge modules can be done easily with other modules if one module gets damaged. Even operation of inverter module is still possible with bypassing the faulty module with the help of proper control algorithm.

Disadvantage

1. This structure needs separate dc-link supplies for power conversions, thus the applications are limited to renewable energy integration, shunt active power filter etc.

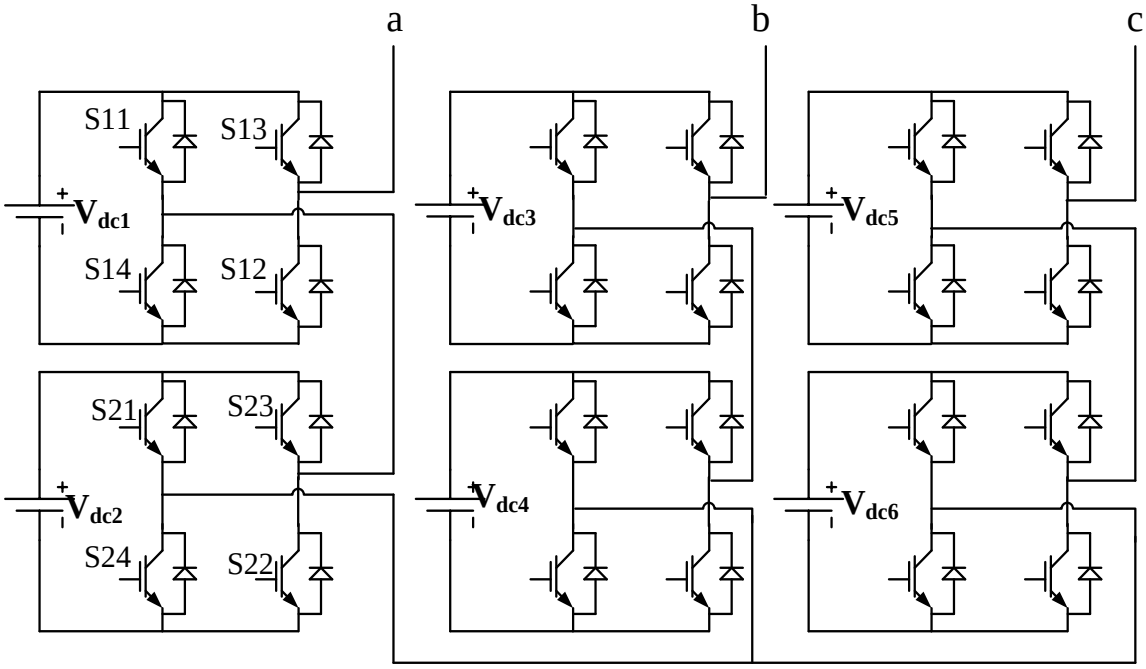


Figure 2.4 Cascaded H-bridge multilevel inverter

2.2.1.2 *Hybrid MLI Topologies*

Not only conventional topologies, different hybrid topologies are also proposed in the literature by researchers [62, 92]. In the hybrid topology, each dc-link may drive the system into a separate voltage level. Due to this characteristic, these inverters are called asymmetric. The hybrid concept is related to the power electronic switches which are used in inverter circuitry [73, 92].

This topology can be used with symmetric and asymmetric [62] dc sources. Symmetric CHB-MLI is having DC voltage of same magnitude whereas asymmetric CHB-MLI is having DC voltages of different magnitudes. 2:1 DC voltage source with 2 H-Bridge modules is capable of generating seven levels at output voltage with highest magnitude of $3V_{dc}$. 3:1 DC voltage source with 2 H-bridge module is capable of generating nine levels at output voltage with highest magnitude of $4V_{dc}$ [62]. In both the cases harmonic profile is improved in the output voltage waveform with same connection and same number of power electronics switches as used for five-level symmetric CHB-MLI. At the same point of time, voltage distribution among switches are different, therefore rating of switching devices is major concern along with balancing of different voltages across capacitors [92].

2.2.2 Review Based on Topologies of MLI based APF

MLI based APFs can be firstly classified as per different topologies/ circuit structures used by the researchers. Figure 2.5 represents different classifications of MLI based filtering. Available topologies are used for compensation of different power quality issues in distribution system. These topologies are suitable for single-phase two-wire (1P2W), 3P3W, 3P4W based configurations in medium-voltage and high-power distribution system. Mainly, six types of topologies are used in literature. It can be classified as per its use in single-phase two-wire, three-phase three-wire and three-phase four-wire system which depends on its application to distribution sector. Requirement of different compensating variables in distribution scenario leads to develop different combinations of active filter topologies. The main criteria of this classification are (a) topology, (b) compensating variables and (c) different connections. Special

configurations such as soft-switching based converters and other topologies are also discussed for the sake of this review.

Classification based on topologies:

APFs can be used in medium-voltage, high-power distribution system by connecting semiconductor switches in series manner or by using a two-winding transformer before connecting APF into the system. Series connection of semiconductor devices faces challenges in design of circuitry and its optimum use due to unequal distribution of voltages among power electronic switches while in blocking condition. Requirement of snubber circuitry also affects its reliability and system efficiency as it increases losses. Set-up with line-frequency transformer faces great challenges as sizing of total set-up increases and cost also in higher side with large foot-print area. Keeping these issues in mind, multilevel inverter provides best solution in recent distribution scenario, as number high power non-linear loads increases in industries.

Multilevel inverters are combination of power electronics switches and energy storing devices i.e. inductor and capacitor. The switching pattern of switches creates higher voltage level at output terminal with lower voltage withstand capacity of switching devices [15, 61].

In case of medium-voltage, high-power APF application, six foremost categories have been classified as per different circuit topology as presented in Figure 2.5 and discussed in this chapter i.e. DC-MLI, FC-MLI, CHB-MLI, Modular Multilevel Inverter (MMI), Three H-Bridge topology (THB) and Soft switching based Multilevel Inverter (SS-MLI). The DC-MLI based Shunt active filtering topology is mentioned with and without transformer in literature. The 3P3W transformer-less DC-MLI, FC-MLI, CHB-MLI and MMI are shown in Figure 2.6 (a), 2.6 (b), 2.6 (c) and 2.6 (d), respectively. DC-MLI is widely accepted by electrical drives industry as rating of drive system increases day by day [24]. More number of levels present in output voltage creates less harmonic content and results better power quality. But DC-MLI does not have modular structure [15]. It is the main reason that three to seven level inverters are mainly used and accepted by industries and researchers because of complex control system and complex driver circuit requirements. It requires one active DC source which further creates its different voltage levels by splitting voltage with the help of capacitors. An m-level DC-MLI

consists of (m-1) dc-bus capacitors. These (m-1) dc-bus capacitors create m-level output voltage between line and neutral terminal [62]. Typically three-phase and three-level DC-MLI based shunt APF is shown in Figure 2.6 (a), where N, denotes neutral point. Three-level DC-MLI output voltage is having three levels: 0, $V_{dc}/2$ and $-V_{dc}/2$. In case of APF application, no active source is required. Only (m-1) dc capacitors are present into the structure for supplying energy. Although power electronics switches need to block same amount of voltages but different voltages may appear across clamping diodes in blocking modes. In this topology, (m-1) X (m-2) numbers of blocking diodes are required per-phase. At the same time, conduction time of power electronics switches during on-time is also different which may cause different amount of current to flow through the device. Therefore, this structure becomes impractical if m becomes high enough because of large number of blocking diodes.

Output voltage level of FC-MLI, as shown in Figure 2.6 (c), is analogous to DC-MLI i.e. (m-1) bus-capacitors are required for generating m level phase-voltage where as clamping-capacitors present in the circuit are (m-1) x (m-2)/2 per phase [141], [147]. In this topology, m level output voltage can be generated by selecting possible combinations of power electronic switches. Each phase is having identical structure.

In CHB-MLI topology, each power electronic switch needs to block same amount of voltage but different voltage is being applied across capacitors while in reverse blocking mode. At the same time, CHB-MLI structure requires large number of clamping capacitors [95, 97, 76]. Depending on switching combination, each device needs to be blocked different voltage in different instant of time. Compare to DC-MLI, it requires more capacitors including dc-bus and auxiliary clamping capacitors. Different combination of clamping capacitors can produce same voltage level which gives redundancy in the circuit. As number of level goes high, bulky and costly power capacitors limit the use of it in industrial sector [13], [62].

CHB-MLI based APF, as shown in Figure 2.6 (c), is a combination of single-phase H-Bridge cells, which can be connected in series manner to generate higher level voltage output. It is modular in structure as compared to DC-MLI and CHB-MLI [15]. Industry is using this topology in different applications like renewable energy integration to medium-voltage and high-power induction motor drives [13, 62, 19]. This topology

leads least count of devices among DC-MLI, FC-MLI and CHB-MLI. In case of filtering applications, no active power source is required. Separate capacitors need to be used with each H-bridge. This modular structure offers transformer-less and cost-worthy solution to industry in case of high-power and medium- to high-voltage applications [13, 92]. This topology can be easily used for higher voltage levels because of its modular structure. If number of levels are high enough, inverter can be switched even in fundamental frequency also, which leads to less switching loss [113, 140]. Efficiency will be in higher side which attracts researchers in recent scenario. Large number of researches is going on in the area of selective harmonic elimination technique.

This topology can be used with symmetric and asymmetric [62, 92] dc sources. Symmetric CHB-MLI is having DC voltage of same magnitude whereas asymmetric CHB-MLI is having DC voltages of different magnitudes. 2:1 DC voltage source with 2 H-Bridge modules is capable of generating seven levels at output voltage with highest magnitude of $3V_{dc}$ as shown in Figure 2.7 (a). 3:1 DC voltage source with 2 H-Bridge module is capable of generating nine levels at output voltage with highest magnitude of $4V_{dc}$ as shown in Figure 2.7 (b) [73, 92]. In both the cases harmonic profile is improved in the output voltage waveform with same connection and same number of power electronics switches as used for five-level symmetric CHB-MLI. At the same point of time, voltage distribution among switches are different, therefore rating of switching devices is major concern along with balancing of different voltages across capacitors [92]. CHB-MLI can be further classified based on its DC-bus configuration [73, 148, 155] and its connection i.e. star-connected CHB-MLI, as shown in Figure 2.7 (c) and delta-connected CHB-MLI [152], as shown in Figure 2.7 (d). Each H-bridge is powered by separate DC source.

New breed of technology introduced in MLI topology is MMI. This topology consists of simplest half-bridge structure which is termed as sub-module. Each sub-module consists of half-bridge and one voltage-balancing capacitor. Combination of these modules generates higher voltage level. This structure needs two extra inductors [137, 143, 150]. Main advantage of this MMI based filtering topology is that, only one dc-bus is required with modular structure with least number of components, as shown in Figure 2.6 (d).

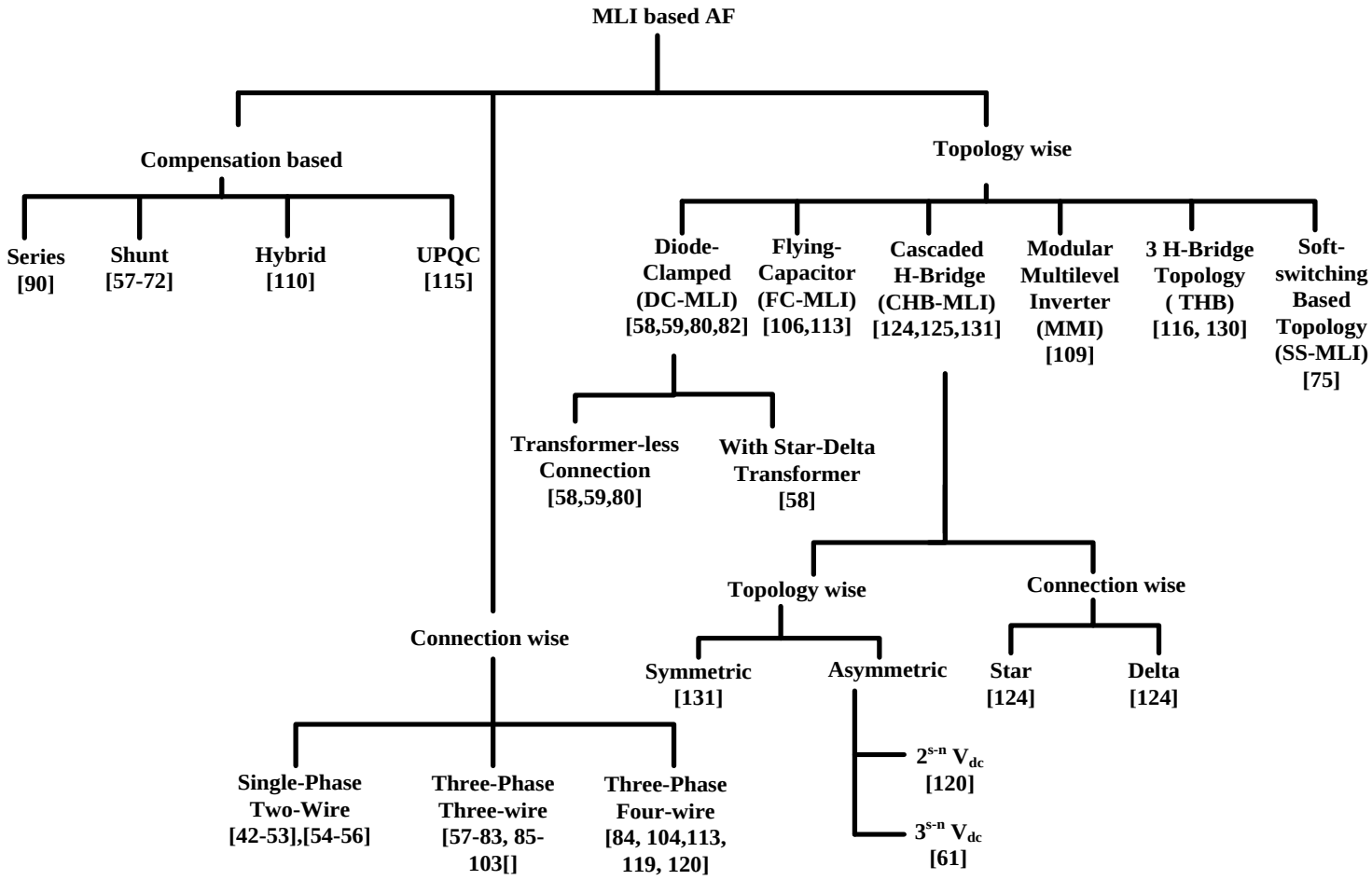


Figure 2.5 Topological classification of MLI based SAPF

Minimized losses with fast, reliable and direct control also attract researchers. But, circulating current issue due to inductors present before output terminal and larger size of capacitors are major concerns. Hence, research is focused on these above mentioned areas [20]. Three H-Bridge topology is widely used in shunt type filtering applications, in 3P3W and 3P4W system, as shown in Figure 2.8 (a) and 2.8 (b), respectively. This structure is having three numbers of H-Bridges which are connected in three phases and only one capacitor is connected with it [114, 158]. This structure essentially provides isolation between distribution line and shunt APF unit, which can inject current in medium-voltage, high-power grid with isolation. Though this arrangement does not have multilevel structure, this topology found suitable for medium-voltage and high-power applications. This arrangement is having disadvantages like harmonic content in output voltage and use of bulky line-frequency transformer with respect to other multilevel topologies. Further research in MLI based filtering is focused on reduction of switching loss, improvement of inverter efficiency, better utilization of components and available structure.

Keeping these issues in mind, DC-MLI with line-frequency transformer is used in [89], as shown in Figure 2.9 (a). DC-MLI and two-level inverter based novel topology is demonstrated in literature [101], as shown in Figure 2.9 (b). New/ modified topologies have been developed with extra inductors to assure zero-voltage switching while turning on/ off power electronics switches [61, 97], as shown in Figure 2.9 (c). System efficiency is improved with this topology but meticulous research needs to be done with different set of conditions to prove its efficacy. Further research in case of multilevel inverter is going on for improving its efficiency by reducing circuit complexity. This can be possible with less number of power electronic switches which can generate same number of levels in the output voltage with conventional MLI topologies [71, 74], as shown in Figure 2.9 (d).

A detailed comparative analysis of MLI based APFs is presented in Table 2.1 which is based on cost, complexity of the circuitry, feasibility, number of active switches and passive devices and fault tolerance capability. It can be depicted from Table 2.1 that, all mentioned topologies are having their distinct advantages based on their applications and uses. However, CHB-MLI and MMI based topologies are widely used due to more

modular and easily replaceable structure, better fault tolerance capacity and lower cost [13, 137, 143].

Classification based on compensating variables:

Different power quality issues related to voltage and current are voltage sag, swell, voltage harmonics, negative sequence voltage burden, current harmonics, reactive power, poor power factor, and unbalanced current profile etc. [73-158].

These issues are mainly created by distribution sector loads such as computers, industrial drive system which produces non-linearity into the system. A large number of electrical drive systems are used in industry and large rating electric drives are increasing with time [92].

To counter these problems, researchers found various solutions based on power electronics devices. These devices are mainly placed on distribution side so that these issues can be resolved and grid voltage and current can maintain its defined shape.

Mainly four categories of MLI based custom power devices are found in literature i.e. MLI based series APF [120, 139], shunt APF [73-84, 86-119, 121-137, 140-142, 144-158], hybrid APF [85, 138] and UPQC [143]. Among these MLI based filtering configurations, shunt APF is most vastly used by industries and researchers because of its potential to minimize reactive power, current harmonics compensation, power factor improvement and balancing of unbalanced component of current. MLI based shunt filtering topology consists of one converter with interfacing inductor which supplies harmonic current, with phase-opposition of line-current for cancelling current harmonics, minimizing reactive power which results improvement of power-factor [51]. DC-bus capacitor supplies energy during transient condition. MLI based shunt APF is one of the cost-worthy solution available for extenuating important power quality problems [92] in medium-voltage distribution sector. Another research is going in the direction of MLI based series compensation which is a challenging task in high-power, medium-voltage distribution network because of high voltage and current requirement of devices. At the same time, non-linear loads in distribution network are producing current harmonics which is a severe issue where as voltage related power quality problems are solved by series APF [120].

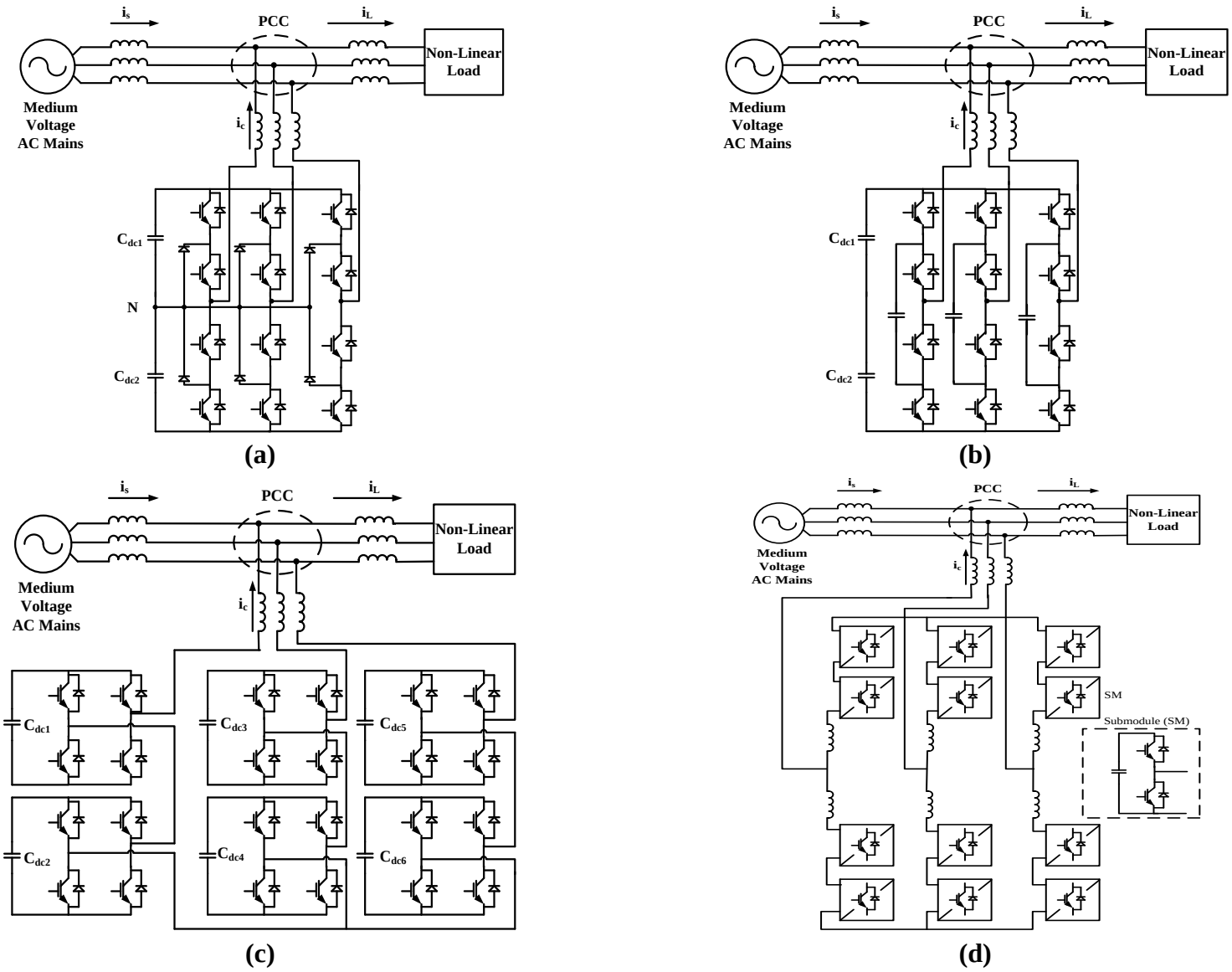


Figure 2.6 Different three-phase, three-wire topologies used as MLI based SAPF, (a) DC-MLI based SAPF, (b) FC-MLI based SAPF, (c) symmetrical star-connected CHB-MLI based SAPF, and (d) MMI based SAPF

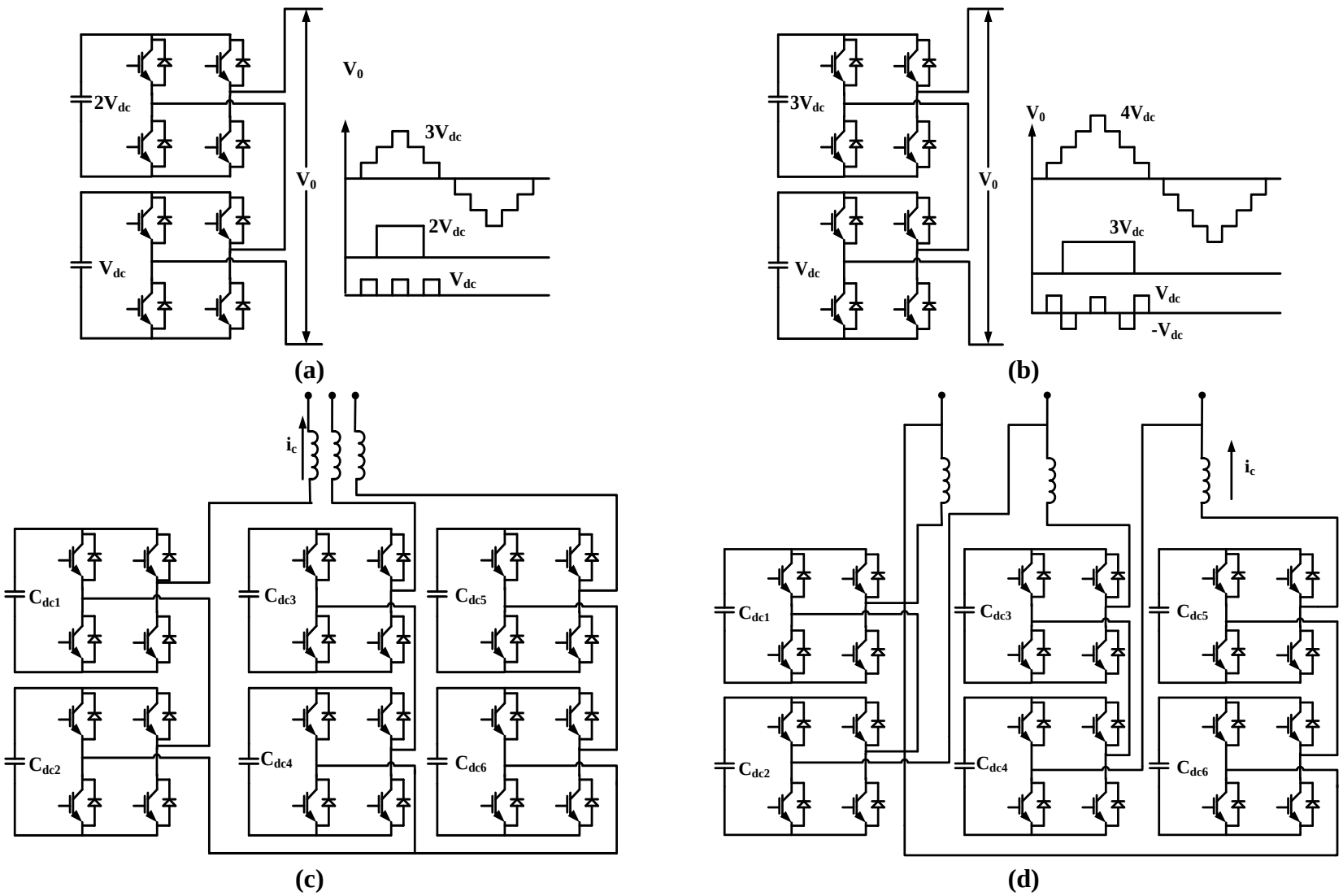


Figure 2.7 (a) Asymmetric CHB-MLI (2^{s-n}), (b) asymmetric CHB-MLI (3^{s-n}), (c) star connection of CHB-MLI, and (d) delta-connection of CHB-MLI

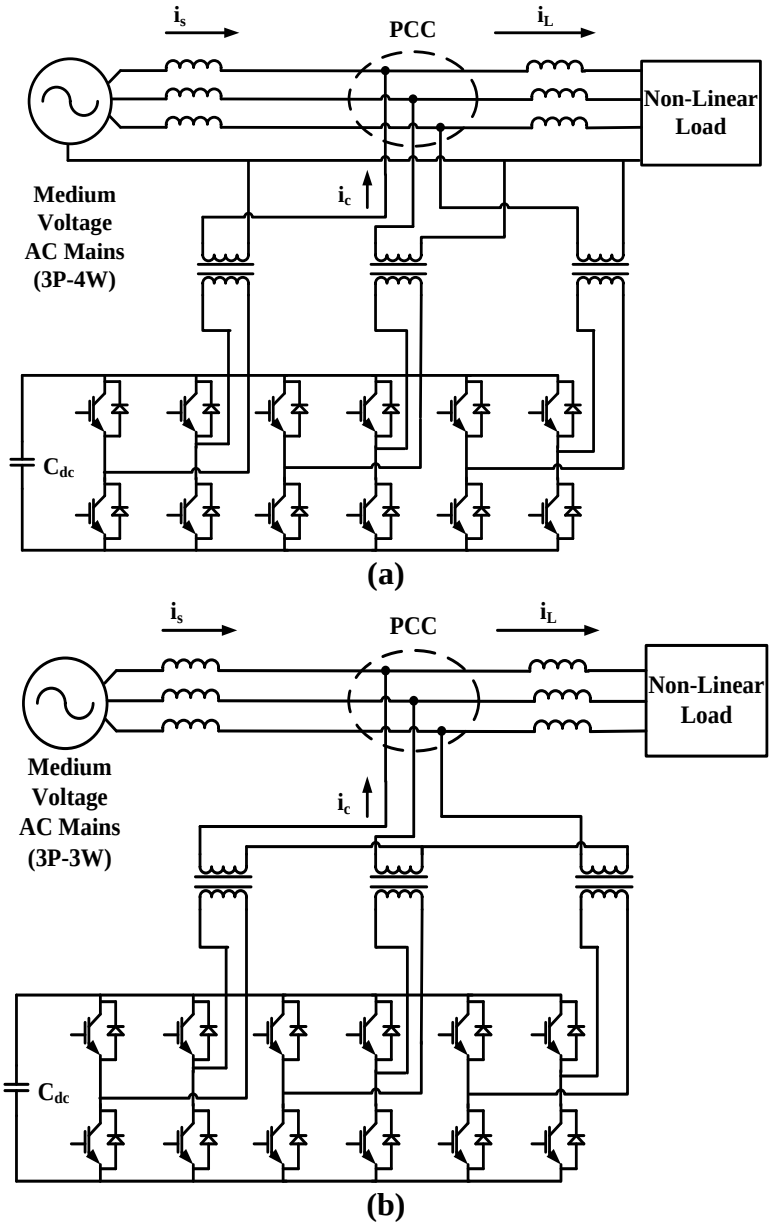


Figure 2.8 Three H-bridge topology for (a) three-phase, three-wire system , and (b) three-phase, four-wire system

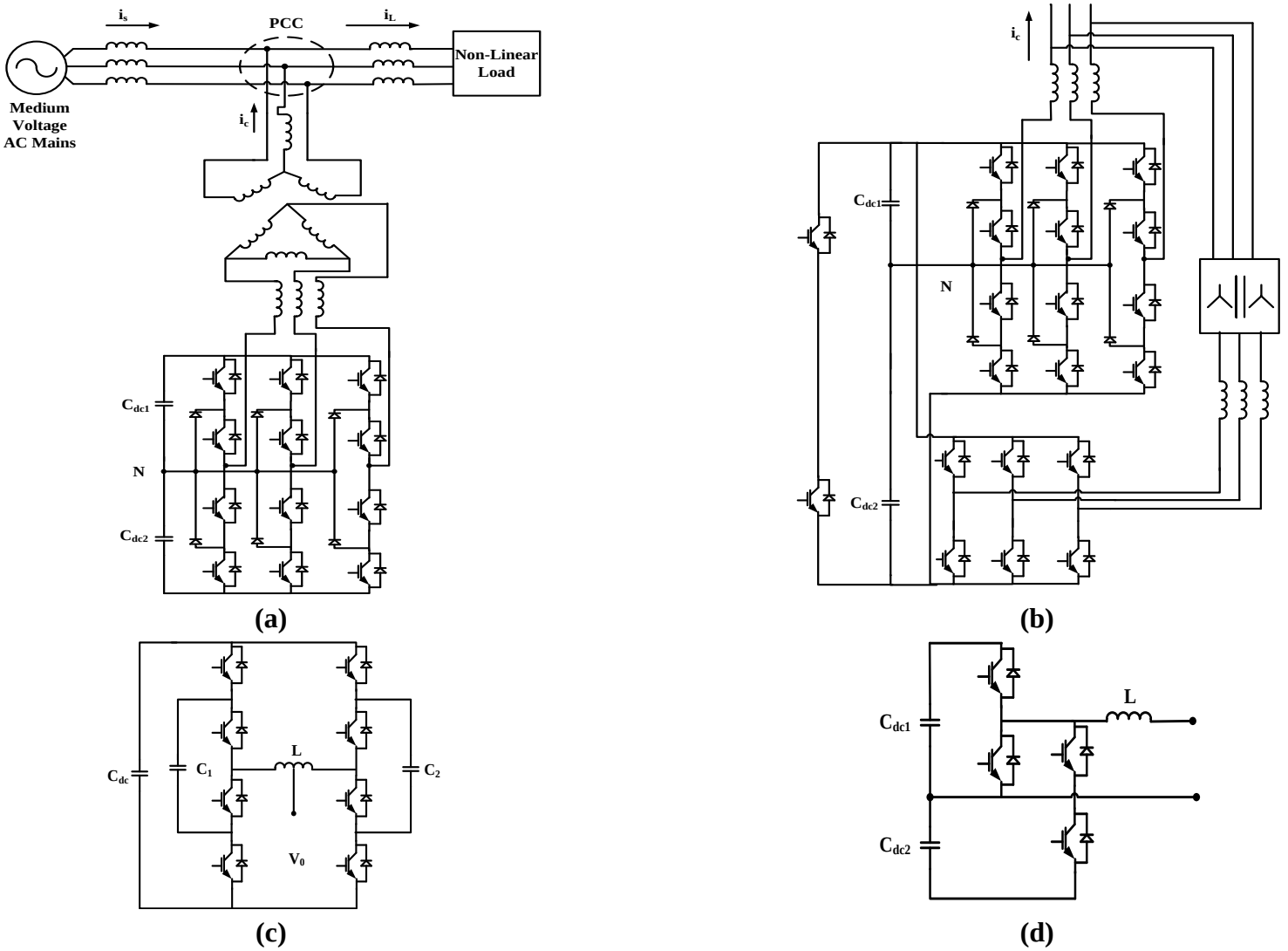


Figure 2.9 (a) Diode-clamped inverter with line-frequency transformer, (b) parallel connection of DC-MLI with two-level Inverter, (c) reduced switch topology MLI for shunt APF application, and (d) zero-voltage transition MLI

Table 2.1 Comparative analysis of different MLIs for APF application

Factors Considered for MLI based SAPF (considered for 3 Ph-3W)	DC-MLI	FC-MLI	CHB-MLI	MMI	THB
Number of DC bus capacitors	3x(m-1)	3x(m-1)	(3m-1)/2	2	1
Power electronic switches	6x(m-1)	6x(m-1)	6x(m-1)	12x(m-1)	6
Diodes	6x(m-1)	6x(m-1)	6x(m-1)	12x(m-1)	6
Clamping diodes	3x(m-1)x(m-2)	0	0	0	0
Clamping capacitors	0	3x(m-1)x(m-2)/2	0	0	0
Inductor used	0	0	0	2	0
Transformers used	0	0	0	0	3
Modularity	**	***	*****	*****	****
Design complexity	*****	****	***	**	**
Control schemes	LSPWM, SVM. PSPWM	LSPWM, SVM. PSPWM	SVM, PSPWM	PODPWM	PWM, SVM
Fault tolerance	***	***	*****	*****	****
Cost	*****	****	***	**	***
Reference	[58],[59],[126]	[64],[101],[102]	[60],[62],[72],[73]	[109],[115],[122]	[84], [116]

[LSPWM: Level shifted Pulse Width Modulation, SVM: Space Vector Modulation, PSPWM: Phase Shifted Pulse Width Modulation, APODPWM: Phase Opposition Displacement Pulse Width Modulation],
[More * means more modular structure, complex design, better fault tolerance capacity and of higher cost]

Moreover a line-frequency transformer is also needed to inject the voltage into the grid. Therefore, MLI based series APF is not a cost-effective solution in most of the applications. By judging its potential, less number of research papers are reported in the area of MLI based series compensation till date. However, it can be useful for voltage harmonic mitigation, proper regulation of line and terminal voltages and also for damping out harmonic proliferation caused by resonance between passive components and line parameters [120, 139].

Series and shunt combination of MLI based filters with one common DC-link is called UPQC which can mitigate voltage harmonics, sag, and swell as well as current harmonics and other load current related problems [143]. In high-power, medium-voltage distribution line, use of MLI for UPQC are not cost-effective solution as number of power electronics switches are high with complicated control scheme.

Combination of MLI based shunt APF and shunt passive filter may be called as hybrid APF. The advantage of this kind of topology is that, it is having potential to mitigate current harmonics at minimum cost [85, 138].

Classification based on distribution system connection:

Another classification of MLI based custom power devices can be done on the basis of its use in medium-voltage distribution system and/or the loads connected with it. Traction drives are fed from 1P2W systems whereas large rating industrial drives are fed from 3P3W system. Household loads computer loads are some of the primary loads fed from 3P4W distribution system. Therefore, MLI based custom power devices can be broadly classified into three categories such as 1P2W [73-87], 3P3W [88-113, 115-131, 133-140, 142-146, 149, 150, 153-1158] and 3P4W [114, 132, 141, 147, 148, 151, 152, 158] based on connection.

Advanced configurations are also studied in literature. Zero-voltage transition MLI [105] is proposed for minimizing switching losses of the converter. MLIs with reduced switch topology based shunt APF is also described in [75] where as some special types of MLI based APF and their parallel combination is also proposed in [108].

Therefore, it can be concluded that, though conventional MLIs are used in medium-voltage SAPF applications, research need to done in the area of reduced switch topology in order to reduce complexity of the power circuit and driver circuit.

2.2.3 Control Strategies of MLI based APF

Control approach is the heart of MLI based APF system. Accurate compensation can only be done with the help of proper control theory. As a result, a lot of research is focused in the area of control theories for better performance of MLI based APFs in steady-state as well as transient condition. Closed-loop control system can be realized in three stages. Necessary voltage and current signals are sensed as a feedback in the first stage. These signals need to be conditioned before going through next stage. Required current or voltage signals are generated as per compensating variables in second stage. Gate pulses for power electronic switches are produced in the final stage. Control system of MLI based shunt APF is represented in Figure 2.10 with its basic blocks. Different techniques used by the researchers are also mentioned in each control block.

Advancement and commercial availability of accurate voltage and current sensors offered great ease of sensing voltage/ current signals. Necessary source/ load/ filter voltage signals can be sensed with the help of hall-effect sensors, PTs and/ or amplifiers, whereas necessary source/load/filter current signals can be sensed with the help of current sensors, CTs and/or amplifiers in first stage. The proper gain factors should be calculated before applying these signals into real-time controller. Signal conditioning is important to make sensed signal readable by the real-time controller platform on which control scheme is implemented. In literatures, DSP, FPGA, dSPACE etc. are used as a real-time processor. Sensed bipolar voltage and current signals need to be converted into unipolar signals in case of DSP processors like TMS320F2812, TMS320F28335. However, in case of dSPACE controller; bipolar signals can be directly processed by the processor. The analog or digital filters with loss-pass, high-pass, or band-pass characteristics are used for signal conditioning [53].

Estimation of Reference Signal

The most significant section of the compensation process is the design and development of control algorithm for active filtering purpose in order to generate required compensating signals. The overall control algorithm should be simpler in structure, robust, and accurate. The effectiveness of the control algorithm not only tested with ideal voltage condition, it should be also tested with distorted supply voltage and

unbalanced loading conditions. Proper estimation of compensating signals for achieving compensation objectives also affects system steady-state and transient performance. A compensation algorithm would not work well if compensation signals are erroneously identified. For this reason, many methods have been already developed by researchers and still modifications are taking place in order to make appropriate use of these techniques. Broadly, reference extraction technique can be realized with frequency based method and time domain method [85, 140].

Operation and execution speed of control theory in real life processor are main concerns for researchers. Frequency based methods are dependent on Fast-Fourier transformation (FFT) which is quite accurate in nature but it requires much more computational time. FFT based techniques are well capable to perform in single-phase as well as in three-phase systems. With the wide use of the DSPs and speed microcontrollers, digital algorithms such as Discrete Fourier Transform (DFT) have been paid a much attention. Harmonic or frequency contents of a discrete signal can be found by using DFT. Discrete signal sequence is obtained by periodic sampling of a continuous signal in time domain using DFT. This reduces the amount of time for calculation by using the number of sampled points N, which has a power of two. But at the same time, this phenomenon introduces delay into the system [85, 140]. Harmonic components are extracted from polluted signal and this information is used to generate reference signal by using Fourier transformation. Inverse Fourier transform is used to estimate the compensation reference signal in time domain. However, the major drawback of this technique is the requirement of a window function to analyze the frequency spectrum of the signal. This method suffers from large memory requirement and large computational power for processor used. Whereas, Kalman filter based approach is more suitable for real time implementation which is based on mathematical modeling for estimation of states [84].

Compensation in time-domain is one of the well established techniques for the extraction of compensating signals. Time domain approach is based on instantaneous estimation of reference signal in the form of either voltage or current signal from ideal/ distorted voltage and current signals. Time-domain methods are simpler to implement and are having less computational burden in comparison to frequency domain based

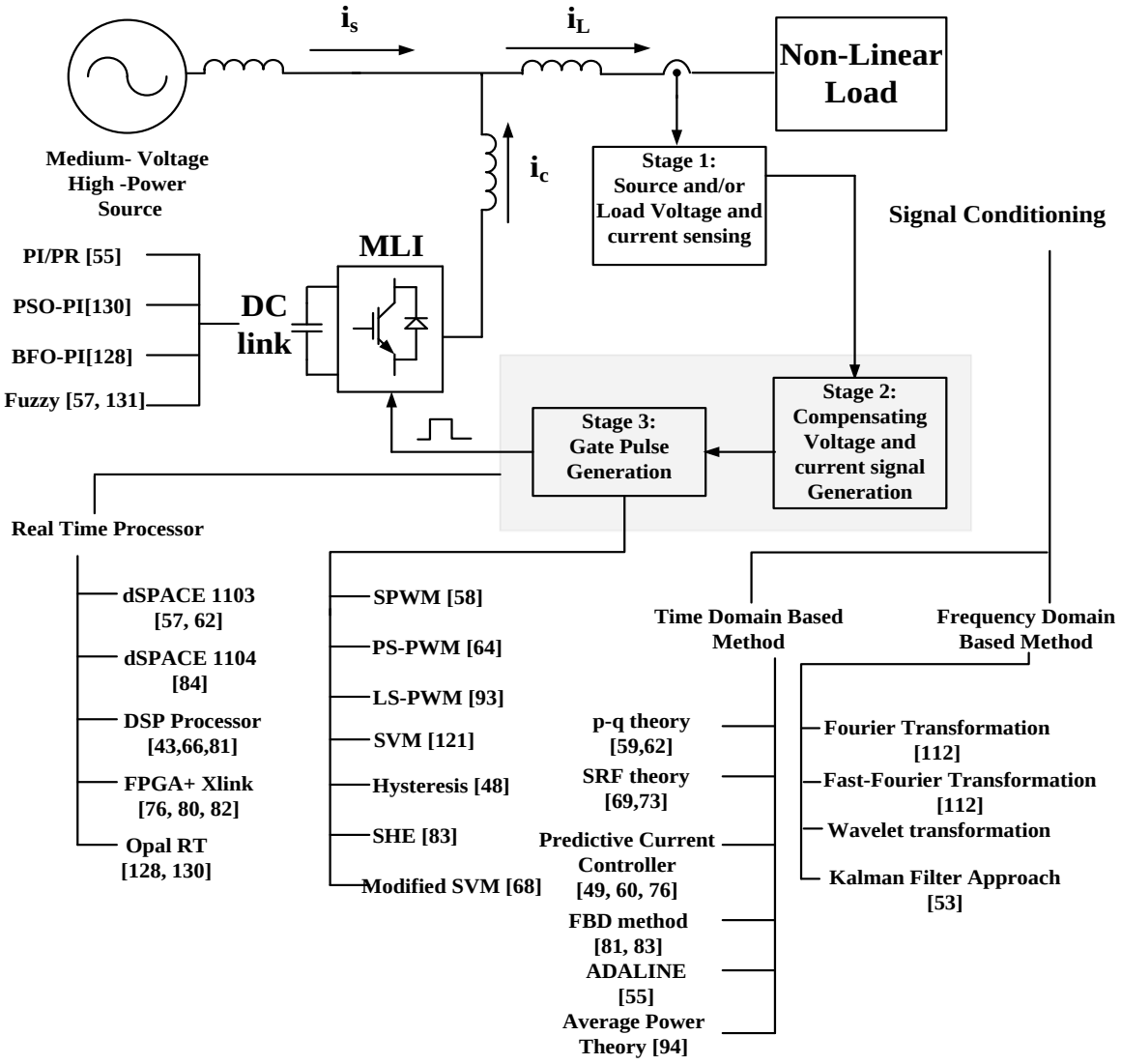


Figure 2.10 Block diagram of detailed control system of MLI based shunt APF with different techniques in literature

technique.

A volume of research papers are reported based on p-q theory [90, 97, 104, 118, 128, 131, 133, 137, 147], SRF theory [100, 105, 110, 112, 125, 138, 153, 154]. Among these, p-q theory can be applied to 3P3W, 1P2W system. Three-phase sensed voltage and current components are converted to α-β coordinates. Instantaneous power (both active as well as reactive) is calculated and required compensating signals are generated with minimum calculation-time. Both power components have average (DC) and oscillating (AC) component. The separation of average and oscillating component is carried out using low-pass or high-pass filter and then compensating current / voltage signal can be derived by taking inverse Clark's transformation. The generation of the reference current signal is based on the calculation of accurate power signals. However, in three-phase-four-wire system zero-sequence power cannot be evaluated with p-q theory [156, 158]. This control algorithm is also not suitable for distorted and unbalanced supply voltage conditions. Distortions in voltage affect the calculation accuracy of the compensation current. This degrades the performance of the control algorithm [127]. This control theory can be extended for the use of MLI based SAPF applications in order to generate proper reference signals. Several DC-link voltage controllers are used by researchers in order to make DC-link voltage stabilized during the steady-state and transient operation for MLI applications. However, use of more than one PI compensators in DC-link voltage control loop makes system more complex one. Tuning of large number of compensator constants are also becoming an issue while using PI compensators in DC-link voltage controller [124]. Waware et al. [136] have used PQ theory for generating reference signal in case of five-level CHB-MLI based SAPF.

Another popularly used theory is SRF theory which depends on conversion of three-phase system parameters into d-q coordinates (synchronously rotating frame) parameters. This system has good stability because it deals with dc quantities only. Load current components are sensed through current sensors and transformed to synchronous reference frame in case of SRF theory which is based on park's transformation. Phase locked loop (PLL) performs matching of frequency with existing grid and it supplies phase information which is required for park's and inverse park's transformation. Loss component is contributed by DC-link voltage regulation which is done by PI controller.

However, some amount of delay is present in the circuit which is caused by filtering of dc quantities at the same time. This method is suitable under balanced and unbalanced distorted source and load conditions. However, the method needs more number of transformations and thus adds to complexities. This SRF method is used for five-level CHB-MLI based SAPF by Mahajan et al. [88] with six numbers of PI compensators in DC-link voltages.

Khomfoi et al. [69] have proposed the p-q-r theory for reference current estimation maintains the compensated input supply currents balanced and sinusoidal, even when supply voltages are distorted and/ or unbalanced. This theory is developed by taking into consideration the advantage of p-q theory and cross vector theory [178]. As per theory, the supply voltage and the load currents are transformed to α-β-0 frame, and then to p-q-r co-ordinates (as v_{sp}, v_{sq}, v_{sr} and i_{Lp}, i_{Lq}, i_{Lr}) using the corresponding transformations.

Single phase p-q theory is also incorporated for single-phase system [73] whereas single phase p-q theory with resonant controller is proposed in [82] in order to maintain sinusoidal source current shape in steady-state condition.

Singh et al. [60] have proposed a new control technique to mitigate current harmonic components and to compensate the reactive power generated by the nonlinear loads by maintaining real power balance. As per this new control technique, the two components of mains supply current are calculated. The active component of source current is corresponding to load and computed from average load power, over a fraction of cycle. The second component of source current maintains the dc bus average voltage at a constant value. This component supplies the active component needed for countering the switching and capacitor losses in the APF. The two components are added and reference source current have been estimated by multiplying this with unit vector templates.

Mi et al. [119] have presented a modified control technique which deals with instantaneous reactive power. However, this theory fails to calculate active alternating power and zero sequence component of power accurately. Rani [121] have introduced the physical meaning of real and reactive powers. Authors also discussed the concept of symmetrical components in unbalanced power system. Peng et al. [94] have presented a

theory based on instantaneous reactive power and computation is done in a-b-c co-ordinates. The sinusoidal fryze current control strategy has been proposed by Abruto et al. [90] in order to overcome the limitations related to p-q theory. Mohan et al. [122] proposed a modified control algorithm for SAPF related to three-phase and four-wire distribution system. This approach considers zero sequence and harmonic component. The performance of the proposed theory is examined through rigorous simulation results. Peng et al. [94] have presented a generalized instantaneous reactive power theory. This theory is well applicable for balanced/ unbalanced and/or normal/ distorted three-phase supply. Detailed mathematical analysis, simulation and hardware prototype results show the effectiveness of the proposed algorithm. These all theories can be applicable to MLI based SAPF in order to generate reference signals. However, for real-time implementation, computational burden of the control algorithm also plays an important role while developing this control algorithm to real-time controller. As, in case of MLIs, number of switching devices is more than two-level inverters, computational burden increases heavily on the real-time controller.

Vodyakho et al. [112] have presented self-tuning filtering approach for extracting fundamental component from normal/ distorter supply voltage in case of three-phase four-leg five-level DC-MLI. This proposed control technique is a modification on PQ theory where i_α and i_β are processed further through self-tuning filter. Fuzzy logic controllers are used for both as DC-link voltage controller and as current controller. This controller however uses only one DC-link voltage controller in order to reduce computational burden on the real-time processor.

Patnaik et al. [158] have presented i_d-i_q control scheme for generating reference signals in case of CHB-MLI based SAPF. This control scheme is a modified version of SRF control theory. In SRF, PLL plays an important role in case of frequency estimation which is important for grid synchronization. However, PLL performance degrades with distorted supply voltage condition. Therefore, this theory presents PLL less control technique. Rest of the control theory is almost similar to SRF theory. The proposed control theory is validated through simulation and hardware results with OPAL-RT used as real-time processor. Azli et al. [85] have proposed decoupled indirect current control method for three-level CHB-MLI based SAPF. Three DC-link voltage sensors are used

for measuring DC-link voltage voltages. One PI compensator is used for regulating DC-link voltages during steady-state and transient conditions. PLL is used for frequency tracking from source voltage. Calculations have been done in 'd-q' frame. PI compensators are used in current control loop. Finally, modulation index is calculated and according to modulation index, inverter switching operation happens.

Lin et al. [74] have proposed control technique for single-phase DC-MLI where neutral point voltage regulation is maintained with another set of PI compensator whereas Miranda et al. [73] have proposed single-phase 'd-q' theory single-phase hybrid MLI.

Miranda et al. [76] have also proposed a suitable DC-link voltage regulation strategy where regulators are used in order to control active, reactive as well as total power of the module.

Xu et al. [82] have used ADALINE based PLL for measuring phase angle information. Voltage balancing controller and average voltage controllers are used for regulating DC-link voltages. Current controller composed of PR compensator is used in this theory. This overall control theory is applied to single-phase CHB-MLI based SAPF. Experimental results have been validated through DSP processor.

Mossoud et al. [103] has proposed predictive current controller for five-level CHB-MLI based SAPF. This control technique also uses three numbers of PI compensators in case of DC-link voltage regulation for three different phases. However, use of more than one PI compensators creates issues with tuning of PI constant parameters.

Apart from these popular control techniques, other techniques are also used for different MLI based active filtering applications such as average power theory [123] for five-level CHB-MLI based SAPF, lyapunov based control for three-phase DC-MLI based SAPF [89], predictive current controller for three-phase CHB-MLI based SAPF [80, 91], single-phase p-q theory for 1:3 asymmetric single-phase CHB-MLI based SAPF [114], sliding mode control [146], asymmetrical and conservative power theory [84] for single-phase DC-MLI based SAPF, i_d-i_q scheme [156, 160] for five-level, seven-level and nine-level CHB-MLI based SAPF, FBD method [111, 113] and decoupled control [150] etc.

Second stage of control system also consists of DC voltage controller. DC voltage controller plays an important role for estimation of losses of DC voltage. Voltage error

signal is processed through PI controller [73-158]. Generally, p-q theory uses this PI output with addition to real power component.

Phase locked loop (PLL) is also an important component in many control theories like SRF theory. In distorted/ unbalanced mains voltage condition, PLL also injects harmonic component into the system which affects system performance. Modified PLL based system [60] and self tuning filter based system [158] are proposed in literature to get rid of these issues.

Comparative analysis of popular control theories based on complexity for development of algorithms and their application is carried out for quick reference which is available in Table 2.2. This table tries to present idea about choosing various control theories of shunt type filtering applications according to its potential in different loading and source voltage conditions in case of 1P2W, 3P3W and 3P4W distribution system.

Artificial Intelligence Technique Based Control Theories

Various control techniques related to SAPF have been discussed in the previous subsection. These control algorithms are proposed by aiming better source current control at steady-state and transient condition. The precision of these compensation techniques depend on accuracy of reference current in different operating conditions. Artificial intelligence (AI) comes into scenario in order to provide better steady-state and transient response in SAPF applications. The researcher community has given attention to the use of AI techniques in electric power applications and in the area of power quality. A lot of works have been reported in different literatures which are based on these applications. AI is a new age technology in order to extract the correct information from process signal with expert acquaintance. This AI either tries to replace a human being in order to perform the control task or it takes thoughts from any biological systems for solving problem. This information is further applied to control the further process. A proper mathematical model and exact parameter selection are two main criteria while designing a robust control algorithm for any system. The system may be non-linear in nature and it can offer lot of complexity.

Table 2.2 Comparative performance analysis of different control techniques

Control techniques	No. of Phases	Control Complexity	Control Accuracy	Performance of system in different operating conditions				Ref
				Unbalanced Supply	Distorted supply	Change in supply frequency	Unbalanced load	
Instantaneous Reactive Power Theory (p-q theory)	Three Phase	**	****	cannot work	cannot work	*	cannot work	[90],[93], [104],[80]
Synchronous Reference Frame (SRF) Theory	Three-Phase	****	****	can work	can work	***	can work	[100],[110], [112],[125]
Single phase p-q theory	Single/Three Phase	**	***	can work	cannot work	*	can work	[71],[82]
ADALINE method	Single/Three Phase	*****	****	can work	can work	****	can work	[86]
Self-tuning filter based method	Single/Three Phase	***	*****	can work	can work	****	can work	[158]

[More * means more complex control algorithm with better accuracy and can work better with variation of supply frequency]

These systems may be even sensible with slight parameter variations. Therefore, control theories need to be robust in order to handle non-linearity. AI technique is admired due to its ability to handle nonlinearity, and to solve complex problems without having information about mathematical modeling of the system. Different types of AI techniques have been proposed in literature such as fuzzy logic, artificial neural network, generic algorithm, wavelet theory etc. for various usages in the field of power quality [44].

Proper tuning of DC voltage balancing capacitor is major concern among researchers. In case of multilevel inverters, a large number of DC bus capacitors are present with increment of number of levels. Maintenance of DC voltage across different capacitors is challenging task for researchers under different loading conditions. Ziegler-Nichols method can be a good solution for tuning PI controller. However, a number of optimization techniques have been incorporated in literature for appropriate tuning of proportional-integral (PI) controller and to solve these above mentioned issues. PSO-PI controller [158], BFO-PI controller [156], fuzzy controller [88] and modified fuzzy controller [157] are used for exact tuning of PI controller which enhances the performance of control algorithm. ANN based control algorithms are used to take out necessary information after dispensation of signal by rigorous learning and training [55, 57].

Agarwal et al. [88] proposed different PI controllers for tuning of all available dc bus capacitors but this increases system complexity whereas Panda et al. [128, 130] proposed control with single PI controller to reduce system complexity. The d-axis component of current signal is summed with this PI output to generate reference signal [103] while in ADALINE based method, it is summed with source current components [55].

Mahajan et al. [88] has proposed control theory for reference current generation in case of five-level CHB-MLI based SAPF where ANN is used for generating current reference and two numbers of fuzzy logic controllers are used for DC-link voltage regulation.

Rao et al. [87] have proposed adaptive neuro fuzzy interface system for MLI based SAPF in order to generate reference current generation. This closed-loop control system lowers the output voltage harmonic content at MLI output terminals.

Gate Pulse Generation

The switching signals for the power electronic devices of the converter circuit are obtained by comparing the reference compensating current signals with modulating signal in a current controller. There are different pulse width modulation (PWM) techniques such as hysteresis controller, predictive controller, carrier based PWM, space vector modulation (SVM) etc. The performance of an SAPF is affected significantly by the selection of control techniques. Therefore, choice and implementation of the PWM technique is very important in order to achieve satisfactory performance of SAPF. The control techniques are generally categorized into two control techniques, voltage and current PWM, sinusoidal internal model controls are used for obtaining the PWM signals. Nonlinear current control technique includes hysteresis control and SVM.

In the third stage of control system, for generating gate pulses, hysteresis controller is first and foremost solution for two-level inverter and MLI based APF [51]. The hysteresis control is robust, but this technique leads to switching frequency variations over a wide range and it is difficult to design the converter circuit parameters.

In hysteresis current controller, the actual current continuously tracks the command current within the hysteresis band. Preset upper and lower tolerance limits are compared to the extracted error signal. As long as the error is within the tolerance band, no switching action is taken. Switching occurs only when the error exceeds the tolerance band. The hysteresis current control is the fastest method with minimum hardware and software requirement. But, this results in high switching frequency. The hysteresis current control based on the magnitude of the error for an ‘m’ level inverter can be associated with the number of bands around the reference current. The first band consists of a main zone and the load current always has to be inside the main zone to minimize the harmonic distortion. The second set of switching bands has a different zones separated by different bands in order to provide a reliable and robust control for an ‘m’ level inverter. Four numbers of hysteresis regions have been defined for a five-level inverter and current error is forced to remain within these different levels.

The advantages of using hysteresis current controller are its excellent dynamic performance and controllability. The main drawback of hysteresis controller is that it produces uneven switching frequency, which adversely affects the APF efficiency.

For an ‘m’ level inverter, (m-1) numbers of triangular signals are used as carrier wave. For a five-level inverter, four numbers of carrier signals are present, each carrier is phase shifted by 90 degree. If first triangular signal magnitude is lesser than sinusoidal reference signal magnitude, then upper switch of one leg and one H-bridge is on and else it will be on zero/ off condition. The other switch of that particular leg will follow the reverse logic. Similarly, switching of the rest of the three legs will be decided by the same manner in case of CHB-MLIs.

A control strategy based on the dynamic programming control is presented in [77], in which the reference current of the APF for specified future time period is predicted. Massoud et al. [103] have used measured voltage and current signals of PCC to predict the reference output voltage of the inverter, required to make the measured current reach its reference at the next sampling instant. An optimized method of model predictive current control suitable for MLIs is proposed in [107], in order to reduce the amount of calculations needed for selection of optimal voltage vectors.

In case of MLI based APF, carrier based PWMs such as phase-shifted pulse width modulation (PSPWM) [76, 85, 102, 111, 115], phase shifted multicarrier unipolar PWM [46], level-shifted pulse with modulation (LSPWM) [122], phase opposition disposition pulse width modulation (PODPWM) [134], sub-harmonic PWM [135] are preferred. PWM technique is having fixed frequency and if number of levels of multilevel inverter is higher, then switching can be done nearer to fundamental frequency [13, 140]. SVM [110, 112, 149] and modified SVM [99] are also used for better voltage output and inverter performance. Fundamental frequency modulation is also one of best available solutions in case of CHB-MLI. However, it is difficult to switch MLI in fundamental frequency for SAPF applications as harmonic pattern is changing with time and switching pattern is continuously decided according to load behavior.

Gupta et al. [79] have proposed a generalized hysteresis current controller for three-level DC-MLI and CHB-MLI. Findings are well supported by detailed simulation results. R. Lin et al. [74] have used PS-PWM technique for DC-MLI based SAPF whereas Mohan et al. [122] has used LSPWM technique for switching of inverter circuit. Miranda et al. [73] have used space-vector modulation for single-phase system. The vector diagram looks like a square one instead of hexagon for its use in single-phase

system. Abruto et al. [90] have used SVM for three-level DC-MLI. However, calculation complexity increases with higher number of levels in case of SVM. Waware et al. [62] have used CPS-PWM technique for five-level CHB-MLI based SAPF whereas unipolar PWM technique has been adopted by Xu et al. [55].

Odavic et al. [80] have used multi sampled carrier based PWM for MLI operation in case of aero-space applications. Lower switching frequency is one of the main advantages associated with this which also ensure mitigation of lowest order carrier frequency terms. However, this phenomena causes phase delay to reference voltage. Mahajan et al. [88] have used PS-PWM technique for switching of five-level CHB-MLI. DSP dSPACE 1103 is used as real-time controller in order to provide the hardware validations. Massoud et al. [106] have proposed phase-shifted SVM and hybrid SVM for switching of five-level CHB-MLI. It has been demonstrates that, for same switching frequency, phase-shifted SVM is having higher effective switching frequency than hybrid SVM.

Vodyakho [112] has proposed novel direct current-space-vector control scheme for three-phase and five-level DC-MLI. This SVM scheme is implemented in synchronously rotating reference frame. This scheme indirectly reduces the switching loss by minimizing the average switching frequency of the converter. This SVM technique can be also applicable to CHB-MLIs and FC-MLIs.

A rigorous review of APF units based on different MLI topologies has been presented in Table 2.3. Various closed-loop control theories applied to MLI based APF including switching techniques are also prepared, which are based on different compensating variables and this is listed on Table 2.3. Different PWM techniques/ switching techniques used by the researchers have been also highlighted. Effectiveness of the control techniques in distorted voltage conditions are also listed. This table can give researchers a clear idea about the various research areas in recent scenario. From the brief review of control techniques, it is apparent that a lot of work has been carried out in the area of harmonic power flow studies. As regards the design, development, analysis and implementation of MLI based APFs based on above control strategies is concerned, different researchers around the world have contributed massively, and their efforts and work done is summarized in Table 2.3 briefly.

Table 2.3 Comparative analysis based on topology and control system parameters

Power Quality issues compensated/ considered	Voltage/ Loading Conditions	Compe-nsation Method used	Topology used	Network Selected (Single/ Three-Phase)	Control scheme used	Optim-ization used	PWM technique used	Cited by
Harmonic current compensation and Reactive power Elimination	Normal/ distorted/ unbalanced load	ShAPF	5 level CHB-MLI	Three-Phase	IRPT	FLC & ANN	PSPWM	[88]
-do-	Normal	ShAPF	3-level DC-MLI	Three-Phase	Direct Lyapunov based control	-	SPWM	[89]
-do-	Normal	ShAPF	3-level DC-MLI	Three-Phase	IPRT (p-q theory)	-	-	[90]
-do-	Normal	ShAPF	CHB-MLI	Three-Phase	Predictive current controller	-	-	[91]
-do-	Normal	ShAPF	5-level CHB	Three-Phase	IPRT(p-q theory)	-	CPSPWM	[93]
-do-	Normal & unbalance	ShAPF	11-level CHB-MLI	Three-Phase	-	-	-	[94]
-do-	Normal	ShAPF	FC-MLI	Three-Phase	-	-	PSPWM	[95]
-do-	Normal	ShAPF	FC-MLI with soft-switching circuit	Three-Phase	IPRT(p-q theory)	-	-	[97]
-do-	Normal	ShAPF	DC-MLI	Three-Phase	-	-	SPWM	[98]
-do-	Normal	ShAPF	3-level DC-MLI	Three-Phase	-	-	Modified SVPWM	[99]
-do-	Normal	ShAPF	Asymmetrical CHB-MLI	Three-Phase	SRF theory	-	Synchronized carrier PWM	[100]
-do-	Normal	ShAPF	3-level DC-MLI and VSI connected parallel	-	-	-	-	[101]
-do-	Normal	ShAPF	CHB	Three-Phase	-	-	CPSPWM	[102]

-do-	Normal	ShAPF	1:3 Asymmetric CHB-MLI	Single-Phase	Single-Phase PQ theory	-	-	[73]
-do-	Normal	ShAPF	Special type	Single-Phase	-	-	-	[74]
-do-	Normal	ShAPF	7-level CHB-MLI	Three-Phase	-	-	Phase shifted SVM	[103]
-do-	Normal	ShAPF	5-level CHB-MLI	Single-Phase	IRP and SRF Theory	-	-	[104]
-do-	Normal	ShAPF	5-level CHB-MLI	Three-Phase	Predictive Current Control		Hybrid & Phase shifted SVM	[106]
-do-	Normal	ShAPF	CHB-MLI	Single-Phase	Passivity based Controller	-	PSPWM	[76]
-do-	Normal	ShAPF	Parallel Interleaved Inverter	Three-Phase	-	-	-	[108]
-do-	Normal	ShAPF	CHB-MLI	-	-	-	Phase shifted multicarrier Unipolar PWM	[77]
-do-	Normal	ShAPF	Multiple VSI with single capacitor sharing	Three-Phase	-	-		[109]
-do-	Normal	ShAPF	3-level DC-MLI	Three-Phase	SRF theory	-	DCSVC-space vector control	[110], [112]
-do-	Normal	ShAPF	5-Level CHB-MLI	Three-Phase	FBD method with PLL	-	PSPWM	[111]
-do-	Normal	ShAPF	CHB-MLI	Three-Phase	FBD method with PLL	-	Selective Harmonic Elimination	[113]
Neutral current compensation , current unbalance, Harmonic current	Normal	ShAPF	3 H-Bridge topology	Three-Phase Four Wire	Single phase d-q theory	-		[114]

compensation and Reactive power Elimination								
Harmonic current compensation and Reactive power Elimination	Normal	ShAPF	7-level CHB-MLI	Three-Phase	-	-	PSPWM	[115]
-do-	Normal	ShAPF	-	Three Phase	-	-	Hybrid Modulation based on LSPWM and PSPWM	[116]
-do-	Normal	ShAPF	New Seven Level topology	Three-Phase	p-q theory	-	Hysteresis Controller	[118]
Voltage Harmonic Mitigation	Normal	Se APF	9-Level CHB-MLI	Three-Phase				[120]
		APF	11-level CHB	Three-Phase	-	-	LSPWM	[122]
Harmonic current compensation and Reactive power Elimination	Distorted/ Normal	ShAPF	5-level CHB	Three-Phase	average power theory	-	CPS-PWM	[123]
-do-	Normal	ShAPF	3-level DC-MLI/ CHB	Single-Phase	-	-	Hysteresis controller	[79]
-do-	Normal	ShAPF	5-level CHB	Three-Phase	SRF Theory	-	Triangular-periodical current controller	[125]
-do-	Normal	ShAPF	CHB	Three-Phase	-	-	MC-PWM	[126]
-do-	Normal	ShAPF	11-level CHB	Three-Phase	-	-	TCPS-PWM	[127]
-do-	Normal	ShAPF	5-level CHB	Three-Phase	p-q Theory	-		[128]

-do-	Normal	ShAPF	FC-MLI	Three-Phase	sigma-delta modulator	-		[129], [130]
-do-	Normal	ShAPF	3-level CHB	Single-Phase	Predictive Current Control	-	Multi sampled Modulation	[80]
-do-	Unbalanced loading/ Voltage sag	ShAPF	CHB	Three-Phase	p-q theory	-	-	[131]
-do-		ShAPF	7-level CHB	Three-Phase Four-Wire	-	-	-	[132]
Harmonic current compensation and Reactive power Elimination, Balancing of supply currents	Unbalanced loading	ShAPF	-	Three-Phase	p-q theory	-	-	[133]
Harmonic current compensation and Reactive power Elimination	Normal	ShAPF	FC-MLI	Three-Phase	-	-	PSPWM, PODPWM, PDPWM, Sub-harmonic PWM	[134]
-do-	Normal	ShAPF	CHB	Single-Phase	Single-Phase p-q theory+ resonant controller	-	-	[82]
-do-	Normal	ShAPF	-	Three-Phase		-	regular and multi sampled PSC-PWM	[135]
-do-	Normal	ShAPF	5-level CHB	Three-Phase	p-q theory	-	SVM	[136]
-do-	Normal	ShAPF	MMI	Three-Phase	PI-MRI controller+ p-q theory	-	PDPWM	[137]
Voltage	Normal/d	Se APF	CHB	Three-Phase	SRF theory	-	-	[139]

Harmonic Mitigation	ynamic load and balanced three-phase fault							
-do-	Normal	HyAPF	5-level DC-MLI	Three-Phase	p-q theory	-	Hysteresis current control	[138]
Harmonic current compensation and Reactive power Elimination	Normal	ShAPF	CHB	Three-Phase	frequency domain analysis	GA	Selective Harmonic Elimination	[140]
Harmonic current compensation and Reactive power Elimination, Neutral current compensation	Normal	ShAPF	3-level, 4-leg FC-MLI	Three-Phase four-Wire	-	-	3DPWM	[141]
Harmonic current compensation and Reactive power Elimination	Normal	ShAPF	CHB	Three-Phase	-	-	IDPWM	[142]
Harmonic voltage and current compensation , Reactive power Elimination	Normal	UPQC	13-level MMI	Three-Phase	-	-	-	[143]
Harmonic	Normal	ShAPF	DC-MLI	Single-Phase	-		-	[83]

current compensation and Reactive power Elimination								
-do-	Normal	ShAPF	3 H-bridge topology (THB)	Three-Phase	-	-	-	[144]
-do-	Normal	ShAPF		Single-Phase	asymmetrical and conservative power theory+ kalman filter based PLL	-	-	[84]
-do-	Normal	Se APF	5-level CHB			-	-	[145]
-do-	Normal	Hy APF		Single-Phase	unified constant frequency integration	-	-	[85]
-do-	Normal	ShAPF	5-level DC-MLI	Three-Phase	Sliding mode control	-	-	[146]
-do-	Normal	ShAPF	FC-MLI	Three-Phase Four Wire	p-q theory	-	-	[147]
-do-	Normal	ShAPF	7-level Hybrid CHB (2^{s-n})	Three-Phase Four Wire	-	-	Unipolar CD-PWM	[148]
-do-	Normal	ShAPF	MMI	Three-Phase	Decoupled control+ repetative controller+PR controller		-	[150]
-do-	Normal	ShAPF	3-level	Three-Phase			SVM	[149]
-do-	Normal	ShAPF	5-and 7-level CHB-MLI	Three-Phase Four-wire		-	-	[151]
-do-	Normal	ShAPF	Star and Delta 7-level CHB-MLI	Three-Phase Four-wire	PLL based control	-	CDPWM	[152]
-do-	Normal	ShAPF	CHB-MLI	Three-Phase	SRF	-	Triangular	[153]

							carrier current controller	
-do-	Normal/Unbalanced loading	ShAPF	DC-MLI	Three-Phase	SRF	-	-	[154]
-do-	Normal	ShAPF	Asymmetric CHB-MLI	Three-Phase	-	-	-	[155]
-do-	Normal	ShAPF	5,7,9-level CHB-MLI	Three-Phase	i_d-i_q theory	BFO	-	[156]
-do-	Normal/ distortion in supply	ShAPF	1-Phase CHB-MLI	Single-Phase	PLL using ADALINE+PR controller+ single-Phase p-q theory	ADAL-INE	-	[86]
-do-	Normal	ShAPF		Three-Phase	SRF+ p-q theory		-	[157]
-do-	Normal	ShAPF	3 H-Bridge Topology (THB)	Three-Phase Four Wire	i_d-i_q theory	PSO	-	[158]
-do-	Normal / unbalanced load/ distorted supply	ShAPF	4-leg, 5-level CHB-MLI	Three-Phase Four Wire	Self tuning filter	Fuzzy	Carrier based PWM	[146]

[ShAPF: Shunt active filter, SeAPF: series Active Filter, HyAPF: Hybrid Active Filter]

2.2.4 Applications and Practical Implementations of MLI based APF

MLI based APFs can be a better cost-worthy and long term solution for medium-voltage and high-power distribution system. With progression of current civilization and development, industrial drive system increases its rating depending on various applications. Medium-voltage and high-power grid also suits these applications with development of power electronics devices. MLI based filters are mainly used for reactive power and voltage and/ or current harmonic minimization, power factor improvement, neutral current and supply current balancing, better voltage regulation with minimization of the effect of voltage sag, swell into the supply system [41-131]. MLI based APFs found their applications in various fields as depicted in literature. FC-MLI based shunt APFs with zero-voltage switching are used in EDS Maglev system [97], whereas one novel topology based MLI [105], [118] is used at electric ship propulsion system (high power ASD). Multiple VSI based structure with single DC bus is applied for power quality improvement in arc furnaces [109]. MLI based single-phase APF, MLI based three-phase APF found their application in aerospace industries and aircrafts [80], [84], [135]. Renewable energy integration with existing grid also becomes popular in recent scenario. Solar and wind power are major sources of renewable energy production which are variable in nature. Variability affects grid-tied PV and wind so proper active and reactive power management is required for appropriate gird connectivity and its operation. MLI based APFs can provide well suited solution in large-scale renewable energy integrated grid scenario. 3-level CHB is used for renewable energy integration in [130] where as in [105], five-level inverter found its application for grid-tied PV system. A detailed study for CHB inverter based large-scale grid-tied PV system is done in [13] which suggest its possibility to replace two-level inverter. Active as well reactive power can be transferred to existing grid with proper control theory. ABB, Toshiba, Siemens, General Electric and Rockwell automations are leading manufacturers of MLI for different medium to high-voltage commercial applications [62]. Available experimental lower-scale prototypes, described in literatures, are discussed in Table 2.4. Table tries to give idea about required hardware components, scaling as per laboratory prototype and use of different high-speed controllers for executing control theories perfectly.

Table 2.4 Comparative study of hardware/ software implementation of MLI based SAPF

Power Electronic Switch /components used	Type/Level	Processor used	Simulation tool used	Cited by
IGBT	3-Phase	dSPACE 1103	-	[88]
IGBT (IRG4PH40K)	3-Phase, 5-level	dSPACE 1103	-	[93]
IGBT	3-Phase	TMS320C32PCMA	-	[97]
-	1-Phase	TMS320C32	-	[74]
-	3-Level	-	SABER	[101]
IGCT	3-Phase	dSPACE 1103	-	[104]
-	1-Phase	-	PSCAD 4.0	[75]
-	3-Phase	Real Time Digital Simulator	-	[105]
IGBT	3-Phase	DSP -320C6701 with FPGA Xilinx Virtex	-	[106]
-	1-Phase	Fixed point DSP unit	-	[76]
-	3-Phase	-	PSCAD 4.0	[107]
-	3-Phase	DSP-TMS320F240 based dSPACE	-	[108]
PM50CSD120 Intelligent Power Module consists IGBTs	1-Phase	FPGA	NI LabVIEW 4.0	[79]
IGBT based 30 kVA system	3-Phase, 3- level	FPGA+ Xilinx	-	[110], [112]
30 kVA system	3-Phase, 5- level	TMS320F2812	-	[111]
-	3-Phase, 4-Wire	dSPACE 1103	MATLAB/Simulink	[114]
-	3-Phase	-	Advanced Continuous Simulation Language	[118]
-	3-Phase, 4 wire, 3-level	FPGA	-	[119]
-	3-Phase,		MATLAB/ Simulink	[121],[122]

	5,7,11 level			[123],[126]
-	1-Phase	FPGA/DSP	PSIM	[78]
-	1-Phase, 3-level		PSCAD/ EMTDC	[79]
-	3-Phase		PSCAD/ EMTDC	[70]
-		Texas C6713 DSK coupled with FPGA	-	[80]
10 kVA IGBT Module	3-Phase, 4-Level	-	-	[76]
-	3-Phase, 5-Level CHB	Texas C6713 DSK coupled with FPGA	-	[77]
IGBT	3-Phase, 5-Level CHB	dSPACE 1103	MATLAB/Simulink	[78]
10 kVA, 450 V, Infineon IGBT(600V/30A)	3-Phase, 4 wire	TMS320F2812 DSP	-	[83]
Semikron SEMIX202GB12E4S and SEMIX453GB12E4S		F28335 Microprocessor	MATLAB/Simulink	[84]
-	3-Phase, 4 wire	-	MATLAB/Simulink	[148]
2KVA, IGBT (SK1000MLI066T)	3-Phase, 3-level	STARTAN-3A DSP trainer kit which includes Xilinx XC3SD1800A-FG676-4	MATLAB/Simulink	[149]
IGBT with driver card 2SD315AI-33	1-Phase CHB	DSP TMS320C6726 from Texas Instrument	-	[86]
-	3-Phase CHB	RT-Lab with SPARTAN-3 FPGA chip and OP5142 board	MATLAB/Simulink	[156],[158]

2.3 SCOPE OF WORK AND AUTHOR'S CONTRIBUTION

Power quality (PQ) becomes an attractive choice among electrical engineers and researcher community as large scale grid integration takes place in existing distribution scenario. Conventional as well as non-conventional energy integration is major areas of interest while solving different problems related to distribution sector [44-50]. At the same instant, usage of power electronic converter based loads are increasing in nature as per industry demand. Medium-voltage and high-power motor drive system is an essential component in any process control industries. These kinds of loads create major amount of problems in distribution system as it draws non-linear current from source [3-4]. Low power factor, generation and propagation of current harmonics, excessive amount of neutral current are major drawbacks due to the usage of non-linear and unbalanced loading. These kinds of PQ problems can raise serious concern due to issue like malfunctioning of electrical and protection equipments, overheating of line, transformer winding and cables etc [5-6]. Therefore, researchers found solutions with the help of combination of different passive elements, called passive filters. However, passive filters are having limitation of size, space required, fixed compensation etc. Finally, active filters are designed to get rid of these issues. Shunt, series and hybrid are different types of active power filter available in literature. Among these, SAPF system takes care of current related PQ problems [7].

High power, medium- to high voltage distribution sector is growing in current distribution sector as large scale non-conventional as well as conventional energy is integrated in this sector. At the same time, large number of electric motor drives (AC as well as DC) found its application in process control to automation industries. Normally, two-level inverters are primary and foremost component in SAPF system in case of low-voltage distribution sector. However, these inverters face great challenges in medium-to-high power distribution sector due to limitations like high voltage and current rating among power electronic switches, higher dv/dt and di/dt rating, use of different switching combinations, and use of large line-frequency transformer etc. Therefore, multilevel inverters (MLIs) are automatic choice in power sector in medium to high voltage and high power scenario as they are having distinct advantages like low dv/dt and di/dt, low voltage and current rating etc. So, MLI based SAPF configuration turns out to be a great

solution for mitigating distribution sector related different PQ problems [8]. Among all available topologies, cascaded H-bridge multilevel inverter becomes automatic choice in case of medium-voltage SAPF application as it does not require any active source and at the same time, it is modular in structure.

A significant amount of researches are already being carried out in the area of control mechanism and reference current generation. Researchers are proposed many control algorithms related to SAPF applications. However, current control is one of the main parts of control algorithm where improvement can be made for better steady-state as well as transient performance. Therefore, in this thesis, efforts have been made to analyze, design and develop high performance control algorithm for five-level CHB-MLI based SAPF under normal/ distorted source voltage conditions. Efforts have been made for presenting a cost effective and robust solution in order to mitigate current harmonics and reactive power in case of medium-voltage and high-power distribution system. A five-level CHB-MLI based SAPF is used by author with proposed control technique in three-phase and three-wire system.

Performance of the filtering unit and nature of source current mainly depends on current control loop of control algorithm. Conventionally, proportional-integral controllers are used in current control loop for AC current controllability but, it suffers from severe problems namely magnitude and phase error in steady-state conditions. Therefore, an advanced current controller is proposed which consists of a new breed of compensator called proportional-resonant compensator for CHB-MLI based SAPF in order to maintain zero steady-state current error. However, it is found that resonant compensators have limitations during real-time applications. Therefore, PI-vector-proportional-integral (VPI) compensator based current control strategy is also proposed for CHB-MLI based SAPF in order to nullify steady-state source current error in case of real-time applications. This controller shows excellent selective harmonic elimination capability thereby steady-state current error is nullified. Particle-swarm optimization (PSO) technique is used for tuning the PI-VPI compensator gain parameters in order to fill the gap for proper tuning methodology of compensator gains. PSO approach operates with a cost function by minimizing source current total harmonic distortion and steady-state error of current control loop.

Most of the control theories available in literature are not tested in distorted, unbalanced supply and/or unbalanced loading conditions. An improved synchronous reference frame theory based control algorithm is proposed for solving current related power quality problems. This proposed control is a complete solution in case of balanced and/or unbalanced loading condition in existing distribution system. This control algorithm is equally effective in case of distorted and/or unbalanced supply voltage condition due to the use of advanced PLL. An advanced PLL having dc and harmonic rejection capability is presented for proper tracking of frequency and phase angle even if source voltage is polluted. Finally, an attempt has been made to integrate single-phase CHB-MLI based SAPF for active and reactive power management in grid-tied PV application.

In this thesis, the main contributions made by the author are summarized as follows:

1. A widespread review on MLI based APF is presented by assessing its potential to replace two-level inverter based SAPF in medium-voltage distribution sector. Different possible configurations, control techniques, selection of power semiconductor switches and their different applications are reviewed comprehensively to identify current research gaps in existing system.

2. Implementation of PR compensator based control algorithm

- PR compensator based current controller is developed for five-level MLI based SAPF control. PR compensator based modified SRF control algorithm is proposed for five-level CHB-MLI based active filtering application in order to acquire better steady-state source current response.
- Stability of the proposed control theory is checked and analyzed with the help of root-locus analysis.
- PR compensator based advanced current controller is used in current control loop to introduce infinite gain at selected frequency.
- Exhaustive simulations are carried out to investigate the performance of three-phase five-level CHB-MLI based SAPF unit under steady-state and transient state conditions for voltage and current type of non-linear loading.
- Various performance parameters such as THD profile of input current, load current, power factor etc. are observed before and after compensation.

- Various experimental results are obtained using dSPACE 1104 real-time controller with different non-linear conditions with single-phase five-level CHB-MLI based SAPF.

3. Implementation of modified control technique using particle swarm optimization (PSO) assisted PI-VPI compensator based advanced current control

- PI-vector proportional-integral (VPI) compensator based current controller is designed in order to maintain superior SAPF performance during its operation. This compensator is able to mitigate high-frequency components from current control loop and therefore, source current of sinusoidal wave shape is obtained in case of SAPF operations.
- A systematic methodology is presented for tuning PI-VPI compensator parameters using PSO technique. This proposed methodology is consisted of three main steps i.e. tuning of PI compensator constant parameters using bode-plot technique, followed by tuning of VPI compensator constant parameters using frequency response method. Finally, PSO optimization has been used for fine tuning of these parameters by minimizing source current steady-state error and source current THD.
- The proposed control algorithm performance applied to three-phase five-level CHB-MLI based SAPF is tested with diode bridge rectifier with R-L and R-C loading condition. This control effectiveness is also tested with unbalanced loading.
- Hardware prototype of single-phase five-level CHB-MLI based SAPF is designed and developed in laboratory. Proposed control is adopted for single-phase applications. Necessary changes have been made and dSPACE 1104 is used for implementation of this control algorithm.

4. Design and development of advanced PLL based control algorithm

- Advanced synchronous reference frame is proposed in order to solve current related power quality problems in case of balanced/ unbalanced loading condition,
- Advanced PLL has been used for mitigation dc and harmonic component from control loop in available/distorted source voltage conditions,

- A detailed systematic bode-plot based approach has been presented for designing system constant parameters,
- Stability of advanced PLL has been checked with transfer function and Routh-Hurwitz criteria,
- Closed loop control is performed using root-locus analysis,
- MATLAB/ Simulink platform has been used for implementation of advanced PLL based proposed control algorithm,
- dSPACE 1104 has been used for real-time implementation of single-phase five-level CHB-MLI based SAPF with voltage/ current type of non-linear loading under available/distorted supply voltage condition.

5. Implementation of single-phase five-level CHB-MLI based SAPF for grid-tied PV application

- CHB-MLI based filtering approach can provide transformer-less interconnection of converters, gives cost-worthy solution and provides better power quality. Therefore, single-phase CHB-MLI based transformer less grid-tied PV system is proposed with so that system can supply active as well as reactive power in day time and can act as SAPF during night time.
- PV array with boost converter is used as DC voltage source of each H-Bridge of CHB, where P and O MPPT algorithm decides the switching pattern of boost converter for improving efficiency of the proposed system. A detailed mathematical modeling of the proposed system has been presented.
- The proposed system is simulated in MATLAB/ Simulink. The effectiveness of the proposed control algorithm is testing in different operating conditions such as with different non-linear loading conditions including current and voltage type of non-linear loading. The algorithm is also tested under distorted supply voltage conditions. Various results obtained from simulations show efficacy of the proposed system.

2.4. CONCLUSION

This chapter is concerned with the detailed classification and different applications of MLI based APF. This paper also presents a thorough comparative

analysis of different MLI topologies in the area of active filtering. Single and three-phase topologies are reviewed significantly and a relative analysis of different topologies is presented. Well known control strategies are analyzed and comparison based on their performance is discussed thoroughly. At the end, its possibilities, challenges and potential capacity for advanced research to improve the performance of MLI based APF is presented.

A lot of research is done in the area of series and shunt APF, hybrid filters, their different topologies and control schemes. MLI based APF is gaining its popularity over two-level inverter based APF for the past few years in medium-voltage segment. It is having potential to replace two-level inverter based APF in medium-voltage distribution scenario. A number of researches have been carried out by researchers in the area of different conventional converter topologies and modified converter topologies with minimum number of power electronic switches. Rigorous research need to be done for proper control of MLI based APFs in steady-state as well as in transient condition. One concern about MLI based APF is that, MLI itself has complicated structure, combinations with MLI and other power electronics switches made system more complex to understand and its fault tolerance capacity as well as operating range decreases.

Specific research is also focused on implementing precise control theories in normal as well as distorted source voltage and/or balanced and/or unbalanced loading condition. Meticulous Research is also needed for active and reactive power transfer phenomena while doing renewable energy integration in medium-voltage grid. Despite the above limitations, it can be concluded from the above discussion that, though the MLI topology is having certain limitations but MLI based active filtering can provide better cost-effective solution for medium-voltage and high-power distribution system to mitigate different power quality problems where highly non-linear loads are used.

CHAPTER 3

LABORATORY PROTOTYPE DEVELOPMENT OF CHB - MLI BASED SAPF

List of Published Papers

1. **S. Ray**, N. Gupta, R. A. Gupta, "Prototype Development and Experimental Investigation on Cascaded Five-level Inverter based Shunt Active Power Filter for Large-Scale Grid-tied Photovoltaic," *International Journal of Renewable Energy Research*, Gazi University Press, vol. 8, no. 3, pp. 1800-1811, Sep. 2018.

CHAPTER 3

LABORATORY PROTOTYPE DEVELOPMENT OF CASCADED H-BRIDGE (CHB) - MLI BASED SAPF

[This chapter deals with the system hardware development for a laboratory prototype model of CHB-MLI based SAPF for the experimental verification in subsequent chapters. A prototype model of CHB-MLI has been built in the laboratory. H-bridges are designed with IGBT STGW30NC120HD. A driver circuit is composed of TLP 250 opto-coupler and delay circuit. The dSPACE 1104 is used for real-time generation of CHB-MLI gate pulses for all power electronic switches. The system hardware is composed of H-bridge inverter circuits, driver circuits for IGBTs, voltage and current sensors, signal conditioning circuit, inductors, diode-bridge rectifier based non-linear loading and dSPACE 1104 real-time controller. The complete procedure for building this set-up is described in detail.]

3.1 INTRODUCTION

A laboratory prototype model of CHB-MLI based SAPF is designed and developed for performing the experimentation of the proposed control algorithms as discussed in Chapter 4 to Chapter 6. The general hardware schematic of the developed dSPACE 1104-based five-level CHB-MLI based SAPF is shown in Figure 3.1. Required voltage and current quantities are sensed using voltage and current sensors, respectively. Sensed voltage and current quantities are amplified according to the requirement of analog to digital (ADC) terminal of dSPACE 1104. Closed-loop control algorithm is designed in MATLAB/ Simulink. Real-time workshop is used for generation of optimized C-code for real-time applications. Generated pulses are amplified and isolated with the help of driver circuit. Finally, performance of the proposed prototype is tested with diode-bridge rectifier based resistive-inductive (R-L) and capacitive-resistive (R-C) loading. The CHB-MLI consists of IGBTs with proper snubber arrangement. Two numbers of H-bridges are required for developing five-level of CHB-MLI. This unit is connected to the auto-transformer through coupling inductors. Current sensors (LEM make LA-25P) are used to sense line, load and compensating current. Voltage sensors (LEM make LV-25-1000) are used for measuring dc-link voltage and source voltage. These measured quantities are amplified and isolated with the help of signal amplification

circuit. These amplified signals are fed to the ADC terminals of dSPACE 1104. A DSP dSPACE 1104 real-time controller is used for real-time implementation of projected control algorithms. The proposed control architectures mentioned in Chapter 4 to Chapter 6 are designed in MATLAB/Simulink. The real-time workshop of MATLAB software is utilized for generation of optimized C-code for real-time control algorithm execution. The interface between dSPACE 1104 and MATLAB/ Simulink allows the proposed control algorithm to run in real-time platform [163].

DSP of dSPACE 1104 control card is used to implement the control schemes and to generate the required gate pulses. The control card is composed of master PPC and slave PPC. Master PPC is having 4 analog inputs with 16-bit resolution and other 4 analog inputs with 12-bit resolution. The control card also provides 8 digital to analog pins with 16-bit resolution. It is also having 20 digital input output (IOs) pins. Slave PPC is having 1 number of 3 phase PWM pins and 4 numbers of single-phase PWM pins. This also has 14 numbers of digital I/O channels. DSP TMS320F240 is used for programming in DS1104 unit. This dSPACE is connected to one host PC. Host PC is having intel (R) core (TM) i7-6700 CPU @ 3.4 GHz, 4 GB RAM, 64-bit operating system, X64 based processor with Microsoft windows operating system and Control-Desk 3.7.3 [163].

Uncontrolled rectifiers are designed using 16KSR diodes and with proper heat-sink arrangement. Diode-bridge rectifier with R-L and R-C loading are used while performing the experimental analysis of proposed control algorithms. These loads are required as these loads are able to produce non-linear current in source side.

Finally, five-level CHB-MLI power circuit is connected to the PCC through interfacing inductor. Two numbers of dc-link capacitors are used with different H-bridges at the dc side of inverter circuit. The switching pulse generation procedure should be in such a way that the source current wave shape becomes sinusoidal one with non-linear loading.

This chapter shows the detailed implementation procedure of CHB-MLI based SAPF in real-time scenario with measurement circuitry for interfacing to the dSPACE 1104 which is chosen for implementation of control algorithms.

The developed laboratory prototype is composed of the following parts which includes-

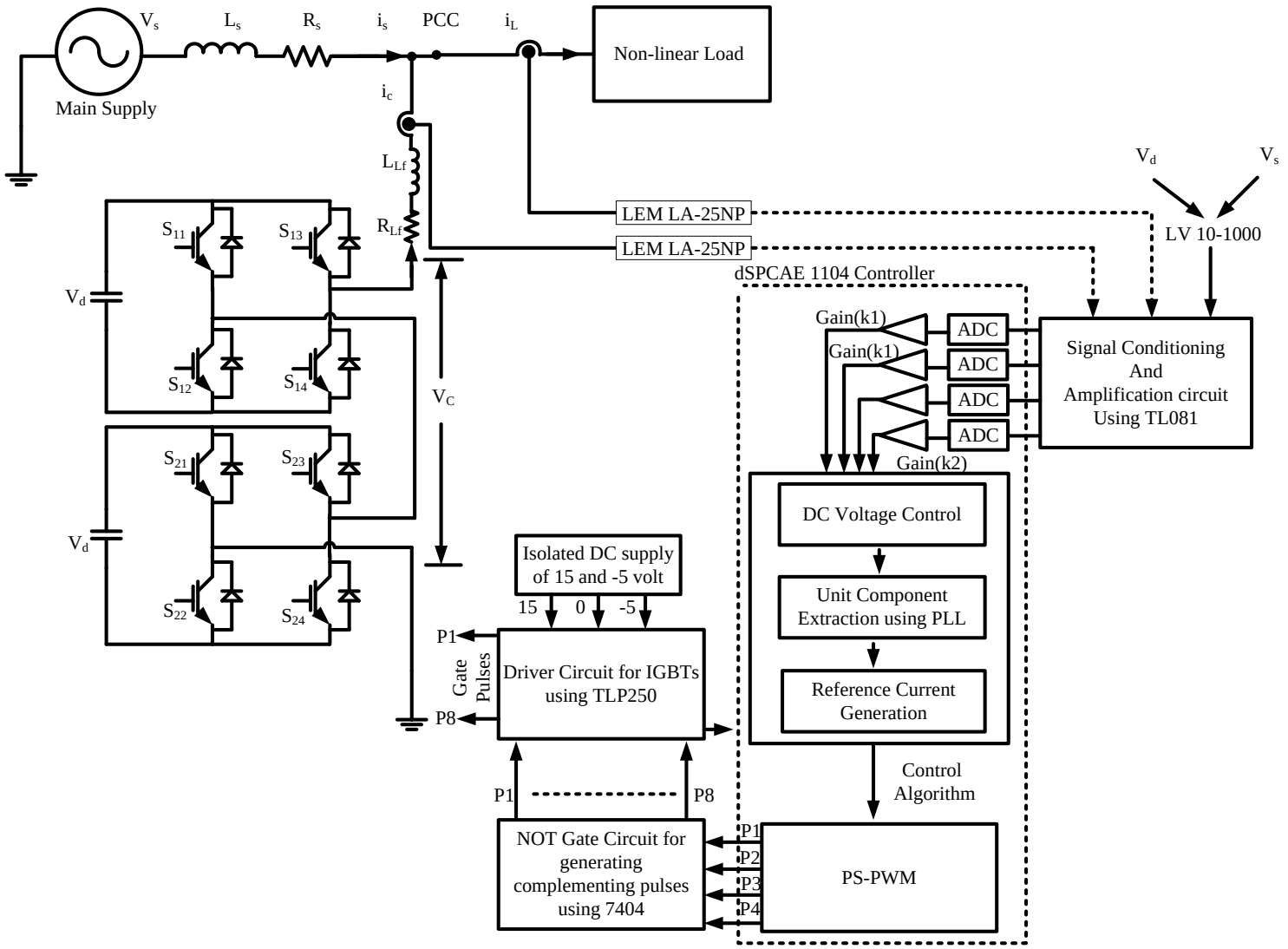


Figure 3.1 Hardware schematic diagram of single-phase five-level CHB-MLI based shunt active power filter

1. Power circuit of five-level CHB-MLI,
2. Non-linear loads,
3. Voltage and current sensors, and signal amplification circuit,
4. Control scheme deployment using dSPACE 1104,
5. Design of gate driver circuit including delay, amplification and isolation.

3.2 DEVELOPMENT OF SYSTEM HARDWARE

The power circuit of five-level CHB-MLI used for laboratory prototype of SAPF unit is presented in Figure 3.1.

3.2.1 Fabrication of Five-level CHB Inverter

Proposed single-phase five-level MLI based SAPF is designed for the compensation of current harmonics related PQ problem in the laboratory, which is depicted in Figure 3.1. This figure gives idea about closed loop operation of single-phase CHB-MLI based active filtering. SAPF unit is connected directly to grid at the point of common coupling (PCC) through coupling inductor (L_{Lf}). Single-phase uncontrolled rectifiers with resistive-inductive and resistive-capacitive circuits are considered as a load in hardware prototype. The proposed SAPF power circuit consists of two main elements namely inverter circuitry and capacitors. Five-level CHB-MLI with IGBT as a power switch is used as inverter unit in which single-phase H-Bridge cells are connected in series manner to produce staircase voltage output. Separate power capacitors are used with each H-Bridge as dc-link capacitors. This modular structure offers transformer-less interconnection to grid. This work deals with three-phase CHB-MLI based SAPF in simulation. However, due to some laboratory constraints and limitations, these control theories are implemented in single-phase CHB-MLI based SAPF system in laboratory condition.

As shown in Figure 3.1, single-phase CHB-MLI circuit consists of eight semiconductor switches. These switches should have self-commutating property; hence IGBTs, MOSFETs or GTOs are the best candidate for it. The four switches are connected in single phase bridge form. This ‘H’ shaped bridge connection is connected in cascaded manner. Each switch should have anti-parallel diodes. These diodes can be in-built in the

semiconductor device or can be connected from outside the switch. An electrolytic DC capacitor needs to be connected between positive and negative rail of one ‘H’ bridge. At the same time, snubber circuit also needs to be used for dv/dt protection to the circuit. Finally, two numbers of ‘H’ bridges are connected in cascaded manner to develop five-level CHB inverter. This structure provides better modularity among other MLIs.

3.2.1.1 Selection of Semiconductor Switch

Selection of semiconductor switch in an electrical circuit depends upon various parameters like v-i characteristics of the device, switching frequency, electrical stress rating, thermal stress rating etc. Voltage and current withstand capability and switching frequency are the most important factors in the selection of a semiconductor switch. SCRs are available with high current and voltage rating but SCR can operate at low frequencies only. Another problem with SCR is that, it requires external commutation circuit. On the other hand IGBTs, MOSFETs and GTOs are self-commutating devices. Also, they can operate at high frequencies. MOSFET can operate at a frequency up to 100 kHz but voltage and current rating is lower than the IGBTs. For medium frequency range of 20 kHz, IGBTs can be used. They are available in high current and voltage rating. CHB-MLI operates at 1 KHz switching frequency. Although thyristor is already available with higher voltage and current rating, but the switch used in CHB-MLI must have self-commutating property hence SCR cannot be used for this operation. High rating IGBTs can be used for the operation of proposed circuit. ST make GW30NC120HD is used as IGBT of required rating for the further experimental analysis [162].

3.2.1.2 Snubber Circuit Design

During transient conditions, voltage across the device can exceed the maximum limit which can damage the switch as well as complete circuit. Therefore, limiting the transient voltage within permissible range is very important factor from the protection point of view. The snubber circuit provides a short term alternative path around the current switching device so that inductive element may discharge safely.

A small resistance with capacitor in series can be used as a RC snubber circuit. Figure 3.2 shows IGBT connected with snubber protection circuit. When a sudden voltage is appeared across the switch, dv/dt triggering may occur as rate of rise of anode

to cathode voltage is higher. With the presence of the snubber circuit, capacitor behaves as short circuit for an instant of high voltage appearance and the voltage across the device become zero. Then, capacitor charges slowly because of presence of parallel path. During the discharging operation of the snubber capacitance, the impedance of the circuit is quite low causing high discharging current. So, a small resistance is used to limit the discharging current of the capacitor.

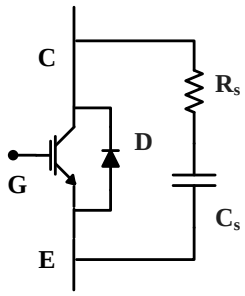


Figure 3.2 Snubber circuit with IGBT

A single-phase 'H-bridge' is designed in the laboratory and this is built in Printed Circuit Board (PCB). The connection diagram of 'H-Bridge' is shown in Figure 3.3 where, four IGBTs are denoted by Q_1, Q_2, Q_3, and Q_4. Proper heat-sink arrangement is done in order to provide proper cooling while running this module continuously. H1, H2, H3, and H4 are connected with Q_1, Q_2, Q_3, and Q_4, respectively. ST make GW30NC120HD is used as IGBT. MUR460s are used as feedback diodes which are denoted as D1, D2, D3, and D4. RC series snubber circuit is used with IGBTs. C_SN_1 and R_SN_1 are connected in series manner and this unit is connected across IGBT Q_1. Snubber circuit across each IGBT are connected in the same manner. Collector (C) terminal of IGBTs Q_1 and Q_3 are connected and Emitter (E) terminal of IGBTs Q_2 and Q_4 are connected. On the other hand, in order to make H-bridge, C terminal of Q_1 is connected to E terminal of Q_4 and, C terminal of Q_3 is connected to E terminal of Q_2. DC-link capacitor is connected between C1 and E4 terminal. Output may be connected in between pins ph1 and ph2. Q1_GT and Q1_ET are connected to gate and emitter terminals, respectively. Amplified and isolated gate pulses for IGBTs are applied to these pins. Other gate pulses are applied in the same fashion i.e. gate pulses for Q_2, Q_3 and Q_4 are given from Q2_GT, Q2_ET; Q3_GT, Q3_ET;

Q4_GT, Q4_ET, respectively. The H-bridge power card used for real-time implementation is shown in Figure A.6 in Appendix A.

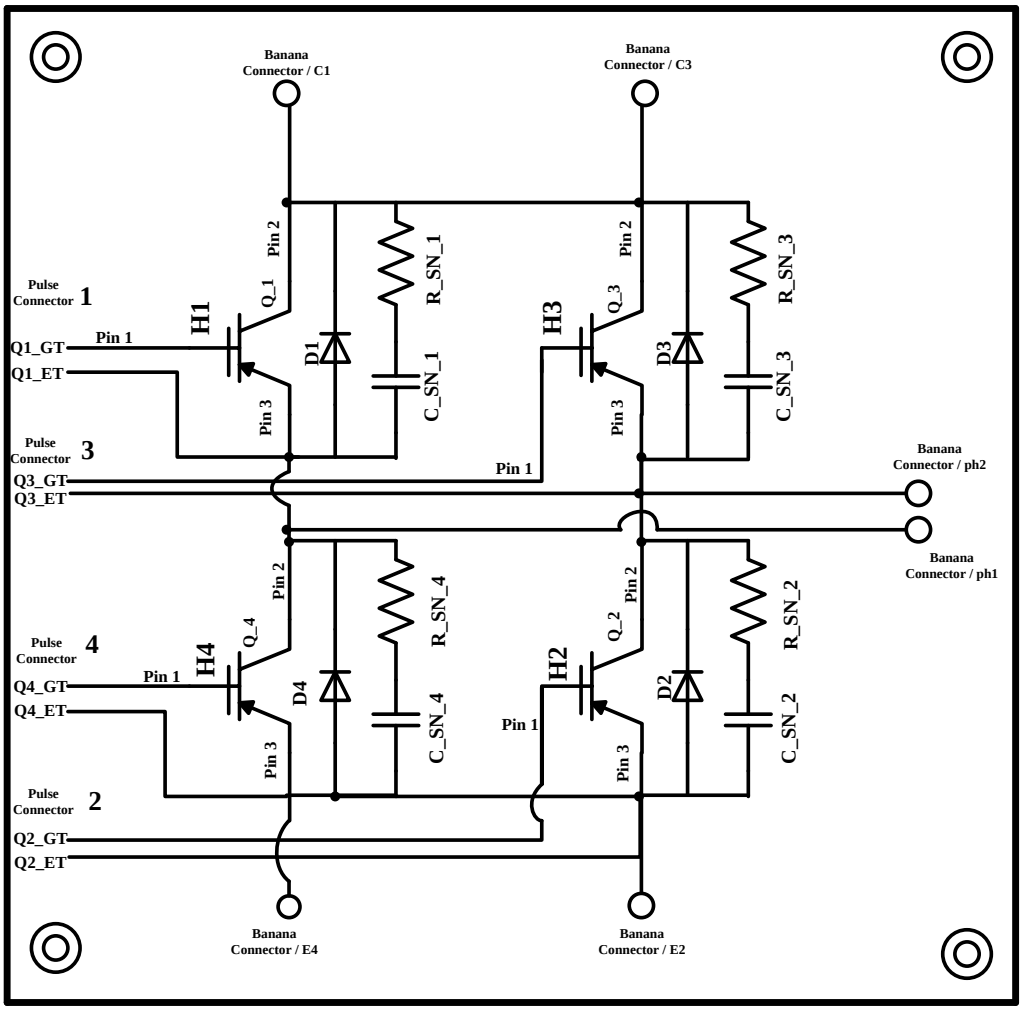


Figure 3.3 H-bridge circuit model

3.2.2 Design of Non-linear Loading

In electrical networks and distribution networks, current-type and voltage-type of non-linear loads are major sources of poor power quality by deviating current wave shape into non-sinusoidal one. Diode-bridge rectifiers with resistive-inductive and resistive-capacitive loading on consumer side are commonly used as non-linear loads for real-time realization. Therefore, a diode-bridge rectifier is built in laboratory by using 16KSR power diode. Terminals of input and output are connected externally for the rest of the circuit connections. The whole module is mounted in a heat-sink module as proper heat-

dissipation is necessary for proper operation of diode-bridge rectifier. Real-time implementation of design of resistive-inductive non-linear loading is shown in Figure A.9 of Appendix A.

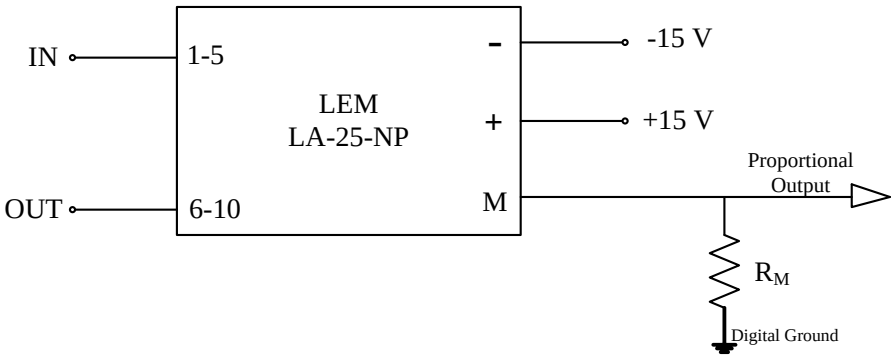
3.2.3 Measurement of Interface Circuit for System Performance

Measurement of various system parameters like supply voltage, load voltage, supply- and load-current, DC-link voltage and their conditioning is required for accurate, reliable and effective control operation. High accuracy, easy to build, linear and fast response are the necessary and important parameter for the measurement circuit. Use of multi-range hall-effect transducers can fulfil these requirements to a great extent. Any control algorithm needs number of voltage and current signals from the circuit. This section describes the different signal conditioning circuit for the implementation of the proposed control algorithms.

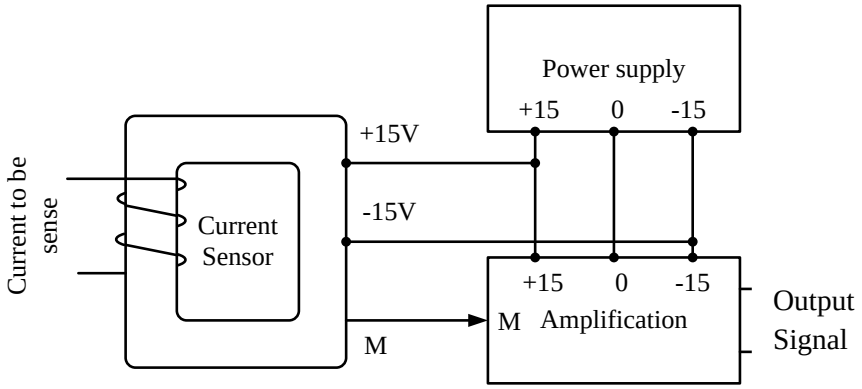
3.2.3.1 Current Sensor Circuit

The current sensors are required to sense the current in the various part of the circuit and generate a proportional signal to the dSPACE 1104 controller in its range. The LEM make hall-effect current transducer type LA 25-NP [160] is used. The main advantages of LA 25-NP are high accuracy, good linearity, optimized response time, no insertion losses, low temperature drift and current overload capability. This current transducer requires ±12V to ±15V DC supply voltage to operate. It is having primary nominal RMS current rating of 25A and can measure 0 to ±25A at the primary side. LA 25NP can be used for the measuring of AC and DC current of the circuit. This current transducer provides galvanic isolation between high voltage primary circuits to the secondary side electronic level low voltage circuit. The circuitry to get the output voltage proportional to the input current is shown in the Figure 3.4 (a) - (b). Figure 3.4 (a) shows schematic diagram of LA 25-NP. This transducer is an instantaneous current output type with isolation capability of 2.5 kV RMS at 50 Hz frequency. This transducer is having five selectable current measurement ranges which are known as primary nominal RMS current. (IPN=5-6-8-12-25 A). The conversion ratio is defined as 1-2-3-4-5:1000. Output signal can be obtained across defined measuring resistance which is denoted by R_M. Figure 3.4 (b) shows detailed connection diagram required for operation. Figure shows

supply of +15V, 0V and -15V is needed for proper procedure. Point 'M' is directly connected to signal amplification circuit. Same power supply may be used for OPAMPs used for signal amplification. The current sensor card used in the study is shown in Figure A.1 of Appendix-A.



(a)



(b)

Figure 3.4 (a) Schematic diagram of current sensor LA 25-NP, and (b) circuit configuration of current sensor circuit with amplification

3.2.3.2 Voltage Sensor Circuit

Generation of desired gate pulse for semiconductor switches require a closed loop control algorithm. Generally, the entire control algorithm depends upon the voltages of various parts of the circuit. Hence, instantaneous voltage measurement or sensing in various parts of the circuit is required. Since the voltage level of the power circuit is high and cannot give to the DSP controller directly, so it is needed to be step down proportionally. The voltage signal can be sensed by a simple combination of resistances

by forming a voltage divider circuit. However, measuring and stepping down the voltage by this method has various problems. In this method the voltages dropped across the resistance causes high level heating. Since number of voltage sensors in the circuit can be high, it causes more energy losses and makes the system less efficient. On the other hand, this method of voltage sensing does not have any electrical isolation between high voltage power circuit and low voltage controlling circuit. Hence, any disturbance in power circuits, noise or any fault can pass to the control circuit directly and may damage or disturb the control circuit.

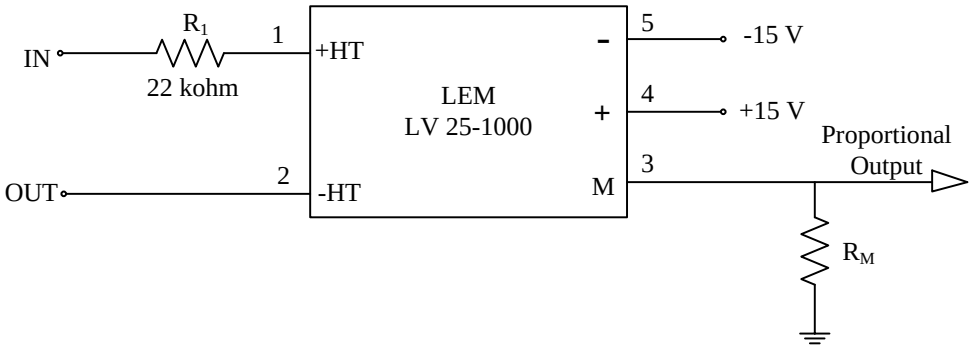
Keeping all this conditions in view, hall-effect voltage sensors are preferable for voltage measurement. In this work, LEM make LV 25-1000 voltage transducer is used for measuring the voltages at different point of the circuit. LV 25-1000 is having many advantages like high accuracy, very good linearity, low response time, low disturbance in common mode, high immunity to external interference and low thermal drift. It has ingrained galvanic isolation between high voltage power circuit and electronic level low voltage control circuit. This transducer requires ±12V to ±15V DC supply to operate. LV 25-1000 can measure DC/AC voltage of level up to 1500V on primary side [161].

Two terminals named as +HV and –HV need to be connected in the circuit where voltage measurement is required. The output voltage from the sensor can be taken from the terminal M. Figure 3.5. (a) - (b) show the circuitry of LV 25-1000. Figure 3.5 (a) shows the circuitry to obtain an output quantity which is proportional to input sensed voltage. Figure 3.5 (b) shows detailed connection diagram required for operation of voltage sensor. Figure shows supply of +15V, 0V and -15V is needed for proper procedure. Point ‘M’ is directly connected to signal amplification circuit. Same power supply may be used for OPAMPs used for signal amplification. The voltage sensor card used in the study is shown in Figure A.2 of Appendix-A.

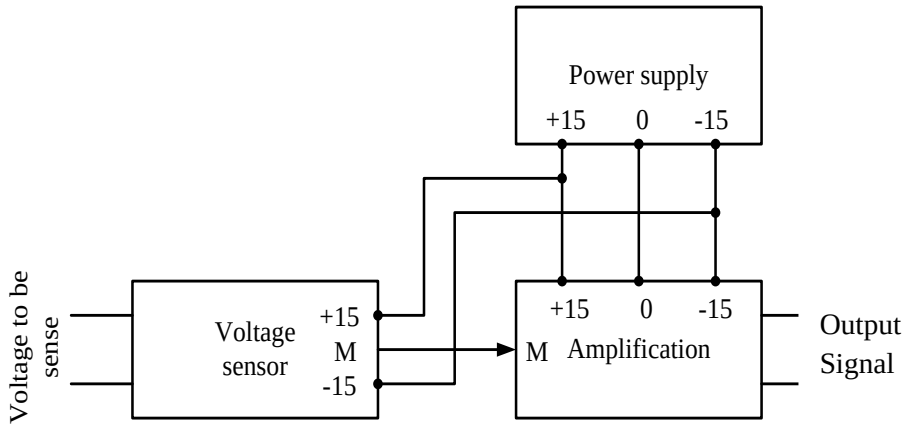
3.2.3.3 Sensor Amplification Circuit

The voltage signal at the output of current and voltage transducer can be higher than 10 V_{p-p} depending upon the various parameters like measured input voltage or current, type of transducer and the method of using the transducer (more number of turns may wound in case of current transducer). The ADCs of most of DSP controller have the

voltage limit of 3.3 to 10 V_{p-p}. Hence, surety of maximum voltage from the transducers is essential for the protection of DSP controller.



(a)



(b)

Figure 3.5 (a) Schematic diagram of voltage sensor LV 25-1000, and (b) circuit configuration of voltage sensor circuit with amplification

Sensor amplification circuit, as shown in Figure 3.6, can be used to control the output voltage of the transducers. It consists of three cascaded op-amp circuits. TL081 op-amp ICs are used in this model. Each IC requires ±15V to operate. The first and third op-amps circuits acts as a buffer to the circuit whereas the second one is used for scaling the output of the amplification circuit. The output of the transducer is given to the 3rd terminal of the first op-amp and the scaled output can be taken from the 6th terminal of the 3rd op-amp based buffer circuit. A 10 kΩ variable resistance is used for the negative feedback of scaling circuit. This variable resistance decides the amplification of the input signal of the circuit. The value of the variable resistance is set such that the output of the amplification circuit should not exceed 10 V_{p-p} for the maximum voltage level of the

power circuit. Once the scaling parameter is done, amplification factor should be calculated by measuring input and output voltages of the amplification circuit in different source voltage and current level. The calculation of amplification factor is required to provide the same amount of gain inside the controller. The voltage and current sensor amplification circuit used for the experimentation is shown in Figure A.3 of Appendix-A.

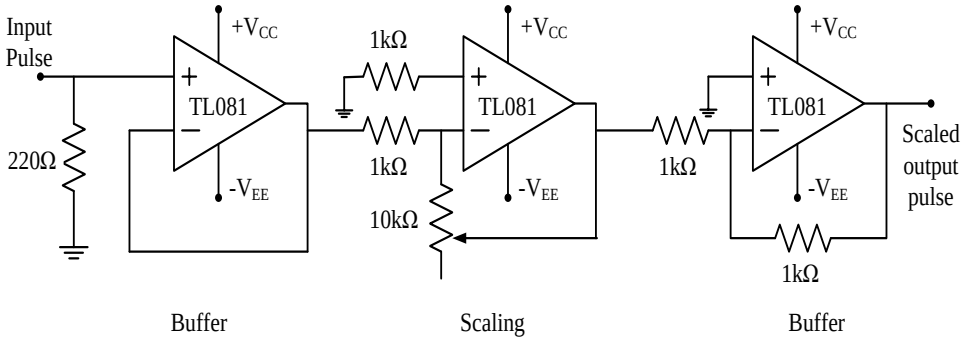
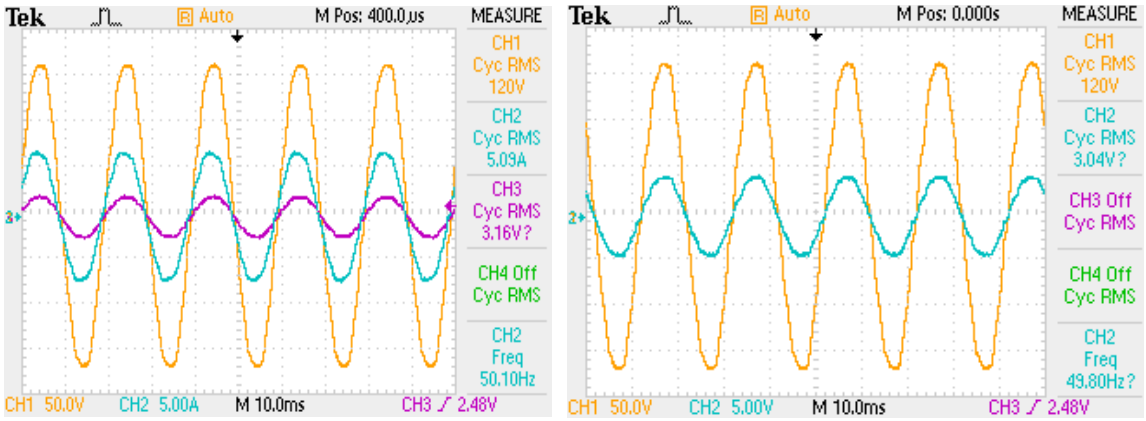


Figure 3.6 Signal amplification circuit

Figure 3.7 (a) and 3.7 (b) show the amplification circuit results with current sensing circuit and the amplification circuit results with voltage sensing circuit, respectively. Figure 3.7 (a) depicts that input to the current sensor is 5.09 A, whereas this quantity becomes 3.16 V after the successful operation of sensor amplification circuit. Figure 3.7 (b) depicts that input to the voltage sensor is 120 V, whereas this quantity becomes 3.04 V after the successful operation of sensor amplification circuit. The calculated amplification factor of current and voltage sensing circuit are 1.69 and 40.46, respectively.



(a) (b)

Figure 3.7 Sensor amplification circuit output of (a) current amplification Circuit, and (b) voltage amplification circuit

3.2.4 Control Scheme Deployment using dSPACE 1104

DSP of dSPACE 1104 control card is used to implement the control scheme, and to generate the required gate pulses. The control card is composed of master PPC and slave PPC. Master PPC is having 4 analog inputs with 16-bit resolution and other 4 analog inputs with 12-bit resolution. The control card also provides 8 digital to analog pins with 16-bit resolution. It is also having 20 digital input output (IOs) pins. Slave PPC is having 1 number of 3 phase PWM pins and 4 numbers of single-phase PWM pins. This also has 14 numbers of digital I/O channels. DSP TMS320F240 is used for programming in DS1104 unit. This dSPACE 1104 is connected to one host PC which is having X64 based processor and Microsoft windows operating system. Control-Desk 3.7.3, MATLAB software and hardware configuration of MATLAB/Simulink are used for programming and implementation of the proposed control schemes.

SIMULINK of MATLAB is an add-on software that enables block diagram based modelling and analysis of linear, nonlinear, discrete, continuous and hybrid systems. Real-time workshop (RTW) is an efficient platform for optimized code source generation. Real-time interface by add-on software of dSPACE provides block libraries for I/O hardware integration of dS1104 R & D controller board and optimized code generation for master and slave processors of the board. dSPACE's control desk is a software tool interfacing with real-time experiment and provides easy and flexible analysis, visualization, data acquisition and automation of the experiment.

The optimized code is automatically generated by RTW of MATLAB in conjunction with RTI of dSPACE. The dSPACE of real-time interface is used to build, download and execute the generated code on the dSPACE 1104 board to obtain signals at CP1104 connector panel. Output signals or any variables in the model can be observed or stored in the control desk. Twelve number of master bit I/Os are configured for outputting the twelve gating signals to isolation board where these are also complimented. The gate pulses are applied to driver circuit given to IGBTs in the CHB-MLI. Figure 3.8 shows the schematic of dSPACE (DS1104) board interfaced with the host PC and real-world plant. This figure depicts detailed implementation procedure of control theories used for this work in MATLAB/ Simulink and its interaction with dSPACE 1104 platform.

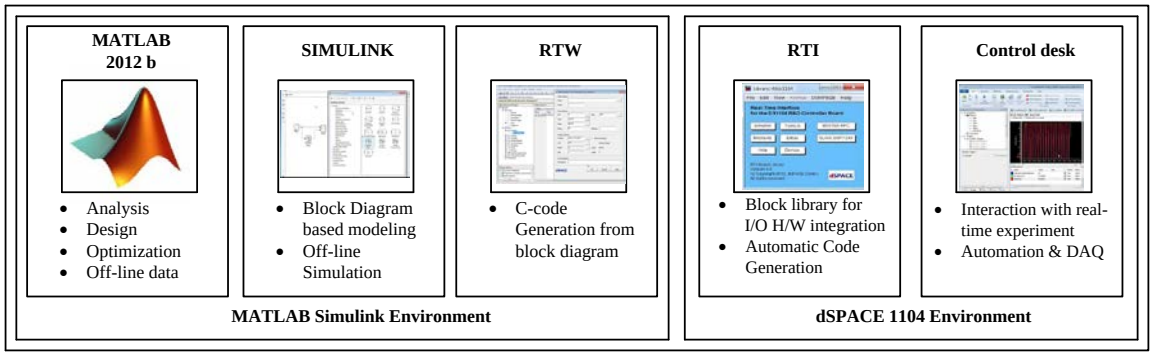


Figure 3.8 Total development environment of dSPACE 1104 with MATLAB

3.2.5 Design of Gate Driver Circuit for CHB-MLI

Gate driver circuit is required in between the real-time controller and the semiconductor switches in power circuit. The purpose of the gate driver circuit is to amplify the pulse generated from the dSPACE 1104 controller. This also provides electrical isolation between control circuit and power circuit, dynamic short circuit protection by using dead band between two switches to the same leg. Various opto-isolator ICs like MCT2E, TLP250, TLP350 etc. are also available as isolation between power and control circuit.

3.2.5.1 Pulse Amplification and Isolation Circuit

The semiconductor devices like MOSFETs require a gate pulse of +12V to trigger the switch, whereas IGBTs require a gate pulse of +15V to turn the switch on and -5 V to turn the switch off. The digital output of the dSPACE 1104 controller is in the order of 0 - 5V. Hence, the voltage level generated by the real-time controller is not sufficient for switching ON the semiconductor switches (IGBTs). The gate driver circuit consists of two parts i.e. isolation and pulse amplification. Opto-coupler IC is normally used to amplify the pulse generated by the controller to the level required by the semiconductor switches.

The current flow in the controller circuit is generally in the rage of 0.2 – 0.5 A, whereas the current level in the power circuit can be high as 10 A – 2 kA. Hence, dSPACE controller needs to be electrically isolated from the power circuit. Among all available opto-coupler ICs, TLP250 is chosen as TLP250 [159] is cost-effective and this TLP can work well in the frequency range of 1 kHz to 10 kHz.

TLP250 is 8 pin DIP package IC. TLP250 can give the gate pulse of 10 - 35V at the output. It provides isolation between power circuit and controller circuit up to 2500V. TLP250 is suitable for the laboratory prototype for moderate voltage level and 25 kHz switching frequency. The internal architecture with schematic diagram for pulse amplification circuit using TLP250 is shown in Figure 3.9.

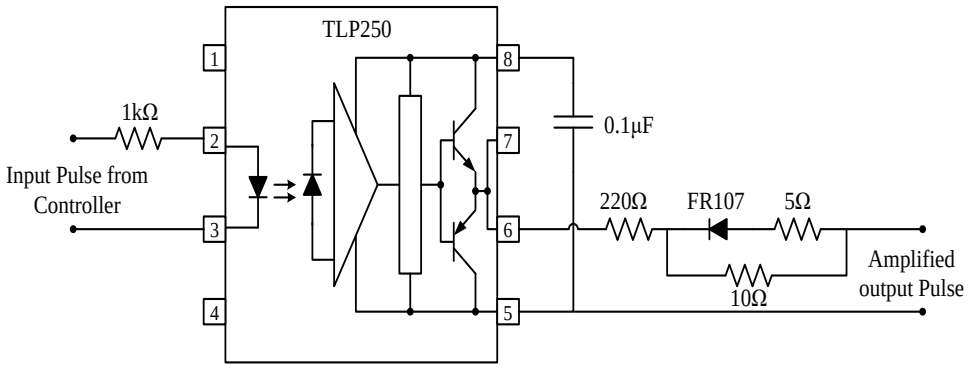


Figure 3.9 TLP 250 based gate pulse amplification and isolation circuit

As shown in Figure 3.9, input pulse from the real-time controller is given between pin number 2 and 3. Pin number 1 and 4 are not connected. 1 kΩ resistance is used at the input of the opto-coupler to limit the current from controller. At the output side, supply is connected between pin number 5 and 8. The voltage level of the supply connected to the TLP is exactly same as the level required to trigger the semiconductor devices i.e. +15V, -5V for IGBTs and +12V, 0V for the MOSFETs. However, this voltage level may be varied according to datasheet of power semiconductor switch. A ceramic capacitor of 0.1μF should be connected from pin number 5 to 8 to stabilize the operation of the high gain amplifier. The output of TLP250 can be taken from pin number 6 or 7. Both the pins are shorted internally. The ground of the output pulse can be taken from pin number 5. The circuit at the output terminal (pin number 6) consists of fast recovery diode FR107, ON resistance of 10 Ω and OFF resistance of 5Ω. This circuit is mainly designed for IGBT's gate pulse. Figure 3.10 shows the amplification of 5 V input pulse to +15 V to -5 V amplified pulse through the opto-coupler circuit. Ground terminal of amplified gate pulses need to be electrically isolated. This isolation is made by using step-down transformer (230V to 15-0-15V, 500 mA). Separate transformers are used for each gate driver circuit. After stepping down of AC voltage, diode-bridge uncontrolled rectifier is used for generating DC voltage. This DC voltage is stabilized by using two capacitors in

series manner. Positive (7815) and negative (7905) voltage regulators are used for generating constant DC voltage of +15V and -5V with respect to ground terminal of transformer secondary. Normally, a high value of resistance needs to be connected in between gate and emitter terminal of IGBT. High value resistance of 18 k, ¼ Watt is attached in between gate and emitter terminal of IGBT for this driver circuit.

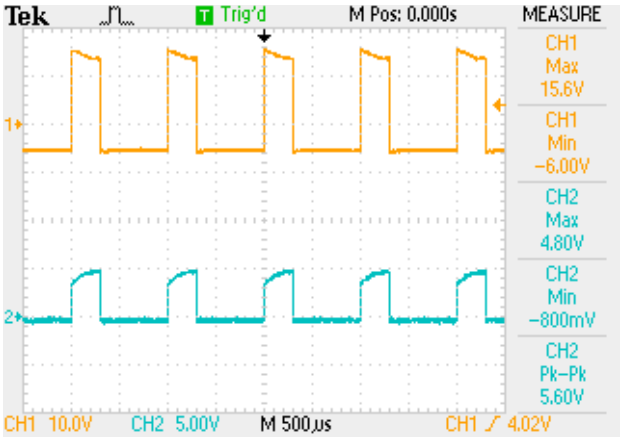


Figure 3.10 Hardware results of gate driver amplification and isolation circuit

3.2.5.2 Dead Band Circuit

Two complimentary gate pulses are given to the two semiconductor switches of the same leg of the bridge. Ideally, the switch should turn-ON and turn-OFF instantly. But, practically it takes some time to turn ON or OFF which is called as switching time. When one of the switches is getting turn ON then other should turn off completely. If both the switches are switched ON at the same instant, then there may be a short-circuit condition. During this interval of time there may be a chance that the both switches start conducting and short circuit the complete leg. It can short the supply or load and may cause for the fault in the circuit. At the same time, every IC and other semiconductor devices need some minor time to respond. But, as the switching frequency is high enough, some delay need to be provided as a precaution of short-circuit condition between two-switches of one leg.

The concept of dead band is one of the best solutions available for this problem. If the pulse of one switch is delayed for a short period of time during rising edge, then the other switch can turn OFF completely. Hence, this problem may be rectified. The

schematic diagram of the dead band circuit is shown in Figure 3.11. It consists of RC circuit to delay the switching ON instant of the pulse.

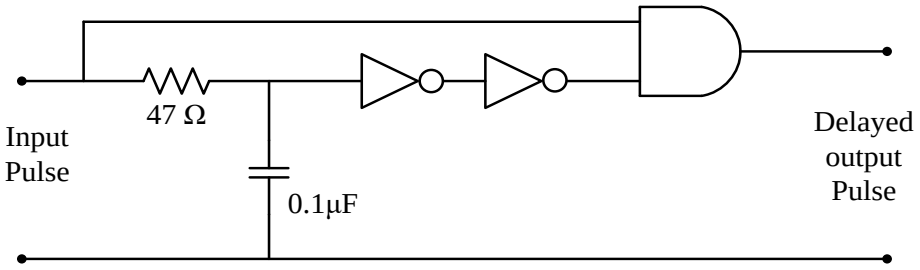


Figure 3.11 Circuit diagram of dead band circuitry

The proposed TLP250 based gate driver circuit with dead band is fabricated in the laboratory to test the effectiveness of the circuit. AND gate IC 7408 and NOT gate IC 7404 is used to fabricate the dead band circuit. Combination of resistance and capacitance decide the amount of dead band required in the circuit. The hardware results of the dead band circuit are given in Figure 3.12. This Figure shows 3 μs dead-band is given between input of opto-isolator and output of opto-isolator. A dedicated driver circuit is designed for two IGBTs where pulse amplification as well as electrical isolation is maintained. At the same time, this driver circuit is able to provide short circuit protection in the help of dead-band circuit. The detailed design of driver circuit is shown in Figure 3.13.

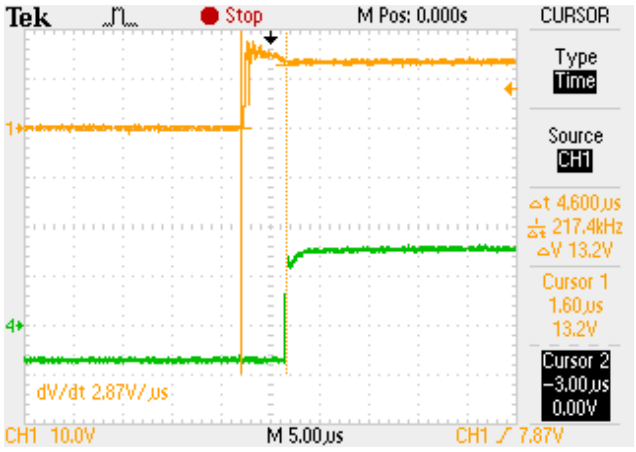


Figure 3.12 Hardware result of dead band circuit

This figure shows driver circuit designed for two numbers of IGBTs in one leg. Resistance and capacitance combination of 7404 and 7408 IC provides required proper dead-band operation. TLP250 provides amplification as well as isolation. Dedicated DC

supplies are also a part of this driver circuit as DC supply of 5V is needed for driving ICs 7404 and 7408. TLP250 requires +15 V and -5V at pin number 8 and 5, respectively. These drive ICs require isolation which is done by using different multi-winding transformers. Input voltage of these multi-winding transformers is 230 V and three numbers of output terminals are present i.e. 15-0-15, 9-0-9 and 15-0-15 V. On and off resistances on the output side of TLP 250 are also provided.

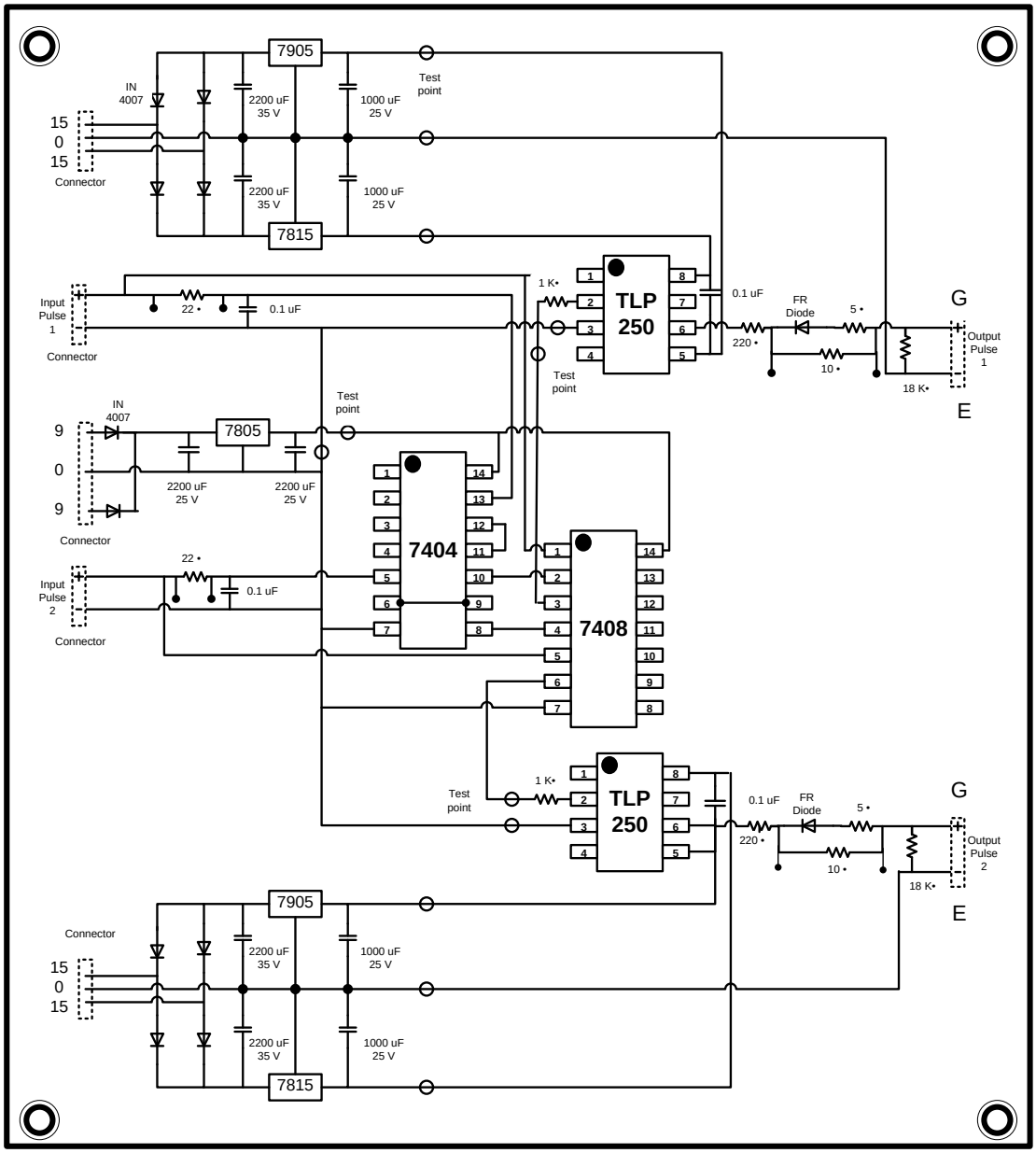


Figure 3.13 Driver circuit developed in the laboratory for two IGBTs of one leg of inverter circuit

3.3 CONCLUSION

A prototype model of five-level CHB-MLI based SAPF is designed and developed in the laboratory using IGBT as power switch. Driver circuit has been designed with TLP- 250 opto-isolator. Delay time is also provided by this driver circuit in order to avoid short circuit condition during its operation. Non-linear loading is designed in laboratory with diode-bridge rectifier and resistive-inductive circuit which acts as current-source type of non-linear loading. On the other hand, voltage-type of non-linear loading is developed using diode-bridge rectifier and resistive-capacitive circuit. Required voltage and current parameters are sensed by using LEM make voltage and current sensors, respectively. These sensed parameters are amplified using signal conditioning circuit. These signals are fed to the DAC of dSPACE 1104 controller. DSP of dSPACE 1104 control card is used to implement the control scheme and in order to generate the required gate pulses.

CHAPTER 4

PROPORTIONAL-RESONANT (PR) COMPENSATOR BASED ADVANCED CURRENT CONTROL STRATEGY

List of Publications

1. **S. Ray**, N. Gupta, R. A. Gupta, "Hardware Realization of Proportional-Resonant Regulator Based Advanced Current Control Strategy for Cascaded H-Bridge Inverter Based Shunt Active Power Filter," *International Transactions on Electrical Energy Systems*, Wiley, Sep. 2018.
   DOI: https://doi.org/10.1002/etep.2714
2. **S. Ray**, N. Gupta, R. A. Gupta, "Modified Three-Layered Artificial Neural Net-work based Improved Control of Multilevel Inverters for Active Filtering," in Proc. *of 7th International Conference on Soft Computing and Problem Solving (SocPros 2017)*, Dec. 2017, Bhubaneswar.

CHAPTER 4

PROPORTIONAL-RESONANT (PR) COMPENSATOR BASED ADVANCED CURRENT CONTROL STRATEGY

[MLI based SAPF is cost-effective and decisive solution for mitigating numerous power quality problems in case of medium-voltage distribution sector. Performance of the filtering unit and nature of source current mainly depends on current control loop of control algorithm. Conventionally, proportional-integral controllers are used in current control loop for AC current controllability but, it suffers from severe problems namely magnitude and phase error in steady-state conditions. This chapter presents an advanced current control loop which consists of a new breed of compensator called proportional-resonant compensator for cascaded H-bridge multilevel inverter based shunt active power filter in order to maintain zero steady-state current error. Stability of proposed current control loop and closed-loop control mechanism is extensively checked and analyzed using transfer function approach and root-locus criteria. A complete mathematical analysis of the proposed control system has been presented and parameters of proportional-resonant regulator are finely tuned using bode-plot technique. The performance of proposed control mechanism is tested using MATLAB/Simulink. A detailed experimental analysis of single-phase five-level CHB-MLI has been carried out to verify effectiveness of the proposed controller over conventional one. Source current waveform becomes sinusoidal and harmonic limits are in compliance with IEEE-519 standard after successful operation of filtering unit.]

4.1 INTRODUCTION

Recently, PQ is becoming a significant element for power engineers and researchers as large number of energy integration are taking place in existing low- to medium-voltage (MV) distribution grid network. Grid-tied and standalone energy is gaining its importance in MV and high-power distribution sector as number of electrical equipments found their application in industries [122, 123]. Maximum numbers of electrical equipments like adjustable electrical drives system, traction drives, arc furnaces etc. are driven by power electronics converter in low- to medium-voltage distribution sector. Non-linear characteristics of the power electronics switches used in the converters are responsible for non-linearity in the existing system. Hence, harmonic contents are introduced in distribution sector due to non-linear behavior of such converter fed loads. Current harmonics, generated by these non-linear loads present in distribution system,

propagated to the source side through point of common coupling (PCC) and pollute the supply current. These current harmonics, in combination with source impedance, generates voltage harmonics, which further affects utility by producing voltage distortion and notches. This voltage and current harmonics create serious problems in distribution side consumers as it results overheating of cables, motors, transformers and mal-operation of various safety devices [34-38]. Such power quality problems results more amount of losses in distribution and transmission sector. High frequency component in the voltage and current waveforms may also cause electromagnetic interference (EMI) in the line. Many national and international regulatory standards are defined like IEEE-519-1992, IEC 61000 etc. in order to describe PQ limits [164-166].

Various custom power devices such as distribution static compensator (DSTATCOM), series-, shunt- and hybrid- APF, unified power quality conditioner (UPQC) etc. are used in order to suppress the drawbacks of conventional passive filters. Shunt APF (SAPF) is a mature technology till date to oppose numerous major PQ concerns like mitigation of current harmonics, reactive power etc. Two-level inverters have been used as a main module of SAPF in low-voltage distribution sector. Two-level voltage source inverters (VSIs) in MV applications face problems related to higher voltage, current and power rating, higher dv/dt and di/dt ratings of switching devices, EMI etc. The use of line-frequency transformer is also becoming cost and space constraint while connecting to the grid.

Multilevel inverters (MLIs) are evolving as major breakthrough in MV systems for their distinctive advantages over conventional inverters like less power and current stress on switches, smaller filter size, better voltage output with lower harmonic distortion, less EMI etc [15]. Three fundamental types of MLIs are projected in literature such as diode-clamped MLI, flying capacitor MLI and CHB-MLIs. Among these topologies, CHB-MLIs reach to higher voltage and power level due to its modular structure [114]. These MLIs accumulate the attention of the researcher community as it found appropriate relevance in high-power & MV industrial drives, STATCOMs, DSTATCOMs, traction drives, large-scale non-conventional energy incorporation etc. Among all these relevant application, CHB-MLI based SAPF is widely demonstrated in

literature and one of the most suitable technologies in present MV distribution sector for reducing PQ problems.

Control theory plays a key role in determining CHB-MLI based SAPF performance. The main objective while designing a control algorithm should be simplicity, robustness and accuracy. Current control plays a significant role for defining current shape and magnitude in case of shunt type active filtering applications. Conventional PI compensators are used for generating accurate reference in case of MLI based SAPF by Waware et al. [124]. This PI compensator gives an effective output in case of dc-link voltage stabilization but, its effectiveness is not satisfactory in case of AC current controllability. It suffers from significant amount of phase and magnitude error in steady-state condition. Presence of harmonic components in the signal could largely deteriorate the quality of reference signal used for phase-shifted pulse width modulation (PS-PWM) technique. This deteriorated reference signal adversely affects the timing of switching. System stability also suffers from large gain of proportional controller. In this context, a synchronous frame based PI controller was proposed by Loh et al. [167]. Minimum steady-state error in three-phase voltage source inverter (VSI) can be acquired by altering stationary reference frame quantities into a dc quantity. However, additional co-ordinate transformation is required to limit increased computational burden by synchronous reference frame PI controller. Therefore, proportional-resonant (PR) controller can be used as a feasible replacement for conventional PI compensator. Stationary frame PR controller was proposed by Zamood *et al.* [168]. This controller is well capable of maintaining almost similar steady-state and transient characteristics compared to synchronous frame PI controller. Stationary to synchronous frame co-ordinate transformation is not required for measured quantities. Loh *et al.* [169] have discussed the use of resonant controllers for selective lower order harmonic component elimination. PR controller provides almost infinite gain at selective frequency for grid connected VSI. The issue of circulating current suppression in high voltage dc (HVDC) application is solved using PR controller by Li *et al.* [170]. PR controller is widely used in case of SAPF applications. PR compensator based SAPF control was proposed by Yuan *et al.* [171] and it gives improved steady-state performance in terms of source current magnitude and phase angle. This control scheme is well capable of enhancing the

effectiveness of the entire system under distorted and/or unbalanced source voltage condition. However, stability of closed loop control is not analyzed by Yuan *et al.* Bojoi *et al.* [172] has proposed an advanced current control strategy comprising PR compensator which needs minimum calculative effort. The problem with this control strategy is that only six lower order harmonics are eliminated from line at a time. However, stability of overall control system and selection of parameters are also not discussed. Lascu *et al.* [173] has analyzed the frequency response of control algorithm which is a parallel combination of PR compensators. Each PR compensator can be tuned at one particular frequency. This scheme is very much feasible for selective harmonic elimination. Still, design of constant parameters will remain a major issue in implementing this system. This controller also suffers from lack of accuracy and computational burden if higher frequency terms are required to be eliminated from the line. According to Trinh *et al.* [174], a combination of PI compensator and vector PI controller is used for harmonic component tracking in case of three-phase SAPF. This control scheme enhances the accuracy of entire system with simpler structures. However, selection of constant parameters and complexity of the control algorithm restricts its use in MLI based SAPF system.

Fukuda *et al.* [175] has proposed robust PR compensator based controller for harmonic current elimination from the distribution sector. However, this compensator is very sensitive in nature to the difference between fundamental and resonant frequency. Also, this system is not effective with variation of frequency of grid voltage. Further, this frequency variation will lead to degradation of stability of the system and perfect tracking capability of the input signal. PR controllers having two integrators minimize the steady-state error with less computational burden. Though, significant error is present in case of real-time applications. Yepes *et al.* [176] has discussed the effect of discretization method in case of different PR controllers. It has been observed that steady-state error increases with the variation of sampling frequency. PI compensators should be replaced by resonant compensator in order to acquire better performance in AC controllability.

Therefore, this chapter presents an advanced current controller based modified synchronous reference frame (SRF) control algorithm in order to get better source current waveform for CHB-MLI based active filtering application. Proportional-resonant

compensator based advanced current controller introduce infinite gain at fundamental frequency. Consequently, the behavior of resonant compensator is similar to an integrator and its infinite gain ensures zero steady-state error in terms of magnitude and frequency. This controller facilitates the system operation with superior performance over conventional controller in terms of sinusoidal reference signal tracking capacity and disturbance rejection capability. Overall closed-loop system stability of the system is also checked and analyzed with transfer function analysis.

4.2 SYSTEM CONFIGURATION

Cascaded H-Bridge Multilevel Inverter (CHB-MLI) can generate high-power and medium-voltage at output terminal with the combination of two or more number of H-Bridges with lower THD compared to two-level inverter. An m level CHB-MLI consists of (m-1) numbers of H-Bridges where each H-Bridge contains separate dc sources. This MLI can generate sinusoidal like waveform even in fundamental switching condition if number of levels are high enough. In case of grid-tied medium-voltage and high-power distribution system, transformer less interconnection can be availed. This CHB-MLI based topology indirectly reduces cost, sizing and space of the set-up.

Figure 4.1 shows five-level CHB-MLI based SAPF for three-phase and three-wire system. The main problem with CHB-MLI is that, more than one number of active sources is required for active power flow whereas in SAPF application only reactive power needs to be compensated. So, DC-link capacitors can be used as an energy source during transient as well as steady state condition. CHB-MLI based SAPF can compensate harmonics as it delivers current with 180 degree out of phase of load current. Source, load and compensating current and source voltage signals are tracked using current and voltage sensors, respectively as per controller algorithm requirement. Control theory generates required reference source current, and finally pulse width modulation (PWM) generates pulses for required IGBTs of CHB-MLI. Computation time, numbers of calculations, reference frame component calculation and its implementation in digital platform are being considered as main factors while considering the complexity of control algorithm. Three-phase and three-wire 11 kV system is considered for simulation study.

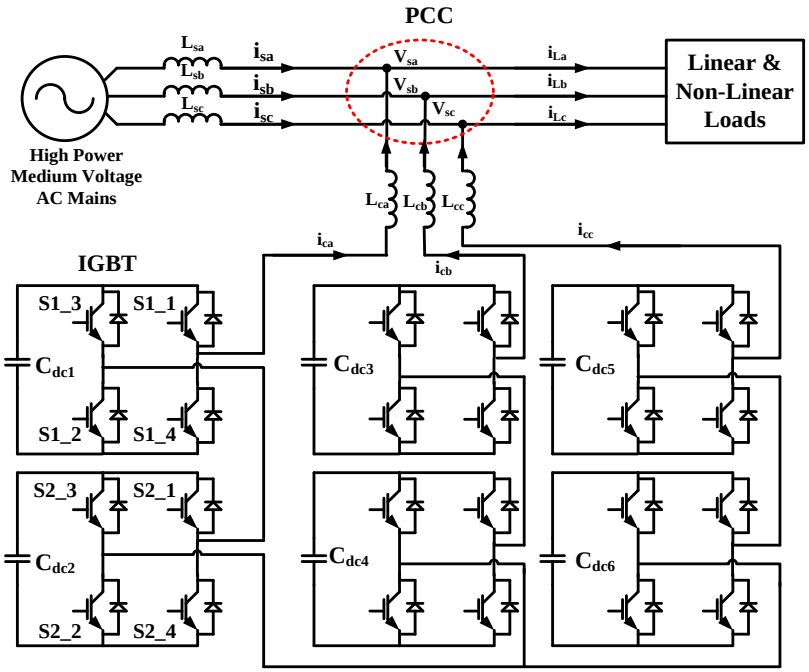


Fig. 4.1 Five-level CHB-MLI based SAPF

4.3 MODELING OF PROPORTIONAL-RESONANT (PR) COMPENSATOR

4.3.1 Introduction

Conventionally, SRF theory is used for reference current generation in case of three-phase SAPF system. The projected modified SRF theory gives better control performance and is easy to implement due to the simplicity of the control algorithm. This theory comprises of a dc-voltage control loop and a current control loop. Transient stability of the system is taken care by the dc-voltage control whereas current control loop decides the amount and quality of the current fed to the existing grid. PI compensator plays a vital role while generating reference current with required magnitude and frequency. The integral section of PI compensator offers infinite gain in dc system. Thereby zero steady-state error is accomplished in case of dc system. Stability of the system does not depend on the proportional part of PI compensator because it is frequency independent. System stability can be examined separately based on proportional and integral parameters. In conventional system, proportional part takes care of transient stability and integral part takes care of steady-state stability. PI compensator based current control loop has been presented by many researchers, though it is having some limitations like steady-state magnitude and phase error, disturbance in system

stability with gain parameter selection etc. Therefore, sinusoidal reference tracking can be enhanced and further inadequacy of PI controllers can be adjusted by using PR compensators.

4.3.2 Modeling and Stability Analysis of PR Compensators

PR compensator [171], as depicted in Figure 4.2, is designed and implemented for CHB-MLI based active filtering application. This compensator can be a viable solution for sinusoidal reference current tracking method with possible minimum magnitude and phase error. The input error signal is multiplied with sine and cosine functions which will shift any higher order harmonic component to dc and double frequency term. Demodulation system, as shown in Figure 4.2, is realized to acquire proper regulation of PI for current controller. Integrator term of PI compensator can serve two purposes i.e. integral action and removal of double-frequency component from the signal. The frequency response of the PI and proposed PR compensator is almost similar in terms of offered bandwidth. Further, transient response of stationary frame PR controller is almost similar to PI compensator regardless of its applications and reference frame. The other main advantages of PR regulator are enumerated below:

a) Infinite gain can be attained by PR controller at a particular frequency. Thereby, zero steady state error can be achieved,
b) It possesses excellent potential to track sinusoidal reference signal,
c) Easy to implement in real-time controllers like DSPs, dSPACE etc.

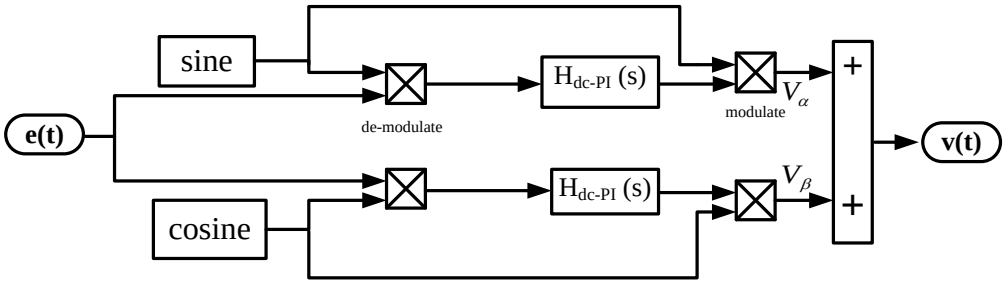


Figure 4.2 Modulation and demodulation of PR compensator [171]

PI compensator is a low-pass type filter in nature. Transfer function of PI compensator is defined by $H_{dc-PI}(s)$. PR controller behaves as a band-pass filter and transfer function of PR regulator is denoted by $H_{PR}(s)$. Output of stationary frame PR controller in time domain can be represented as per Equation 4.1 which is derived from Figure 4.2.

$$v(t) = \{e(t).\cos(\omega t) * h_{dc-PI}(t)\}\cos(\omega t) + \{e(t).\sin(\omega t) * h_{dc-PI}(t)\}\sin(\omega t) = v_\alpha + v_\beta \quad (4.1)$$

Equation 4.1 consists of two terms which are denoted by v_α and v_β.

Two functions F_1 and F_2 are considered for further analysis as per Equation 4.2 and Equation 4.3.

$$F_1(t) \equiv h_{dc-PI}(t) * e(t).\cos(\omega t) \quad (4.2)$$

$$F_2(t) \equiv h_{dc-PI}(t) * e(t).\sin(\omega t) \quad (4.3)$$

Further computation is done in Laplace domain for simplification of calculation. $F_1(s)$ as represented in Equation 4.4 can be found by applying Laplace transform to Equation 4.2.

$$F_1(s) = L[h_{dc-PI}(t) * e(t).\cos(\omega t)]$$

$$F_1(s) = \frac{1}{2}H_{dc-PI}(s)L\left[e(t).\left(e^{j\omega t} + e^{-j\omega t}\right)\right]$$

Therefore,

$$F_1(s) = \frac{1}{2}H_{dc-PI}(s)[E(s + j\omega) + E(s - j\omega)] \quad (4.4)$$

Equation 4.5 represents the Laplace transformation of function $F_2(t)$.

$$F_2(s) = L[h_{dc-PI}(t) * e(t).\sin(\omega t)]$$

$$F_2(s) = \frac{1}{2.j}H_{dc-PI}(s)L\left[e(t).\left(e^{j\omega t} - e^{-j\omega t}\right)\right]$$

Therefore,

$$F_2(s) = \frac{j}{2}H_{dc-PI}(s)[E(s + j\omega) + E(s - j\omega)] \quad (4.5)$$

The more comprehensive form of v_α and v_β can be found out separately by applying Laplace transform to Equation 4.1. These two components are given as per Equation 4.6 and Equation 4.7.

$$v_\alpha = L[h_{dc-PI}(t) * e(t).\cos(\omega t)]\cos(\omega t) = L\{F_1(t).\cos(\omega t)\} = \frac{1}{2}[F_1(s + j\omega) + F_1(s - j\omega)]$$

$$v_\alpha = \frac{1}{2}\left[\frac{1}{2}H_{dc-PI}(s + j\omega)\{E(s + j\omega + j\omega) + E(s + j\omega - j\omega)\} + \frac{1}{2}H_{dc-PI}(s - j\omega)\{E(s - j\omega + j\omega) + E(s - j\omega - j\omega)\}\right]$$

Therefore,

$$v_\alpha = \frac{1}{4}[H_{dc-PI}(s+j\omega)\{E(s)+E(s+2j\omega)\} + H_{dc-PI}(s-j\omega)\{E(s)+E(s-2j\omega)\}] \quad (4.6)$$

and

$$v_\beta = L[h_{dc-PI}(t) * e(t).\sin(\omega t)]\sin(\omega t) = L\{F_2(t).\sin(\omega t)\}$$

$$= \frac{j}{2}[F_2(s+j\omega) - F_2(s-j\omega)]$$

$$v_\beta = \frac{j}{2}\left[\frac{j}{2}H_{dc-PI}(s+j\omega)\{E(s+j\omega+j\omega) - E(s+j\omega-j\omega)\} - \frac{j}{2}H_{dc-PI}(s-j\omega)\{E(s-j\omega+j\omega) + E(s-j\omega-j\omega)\}\right]$$

Therefore,

$$v_\beta = \frac{1}{4}[H_{dc-PI}(s-j\omega)\{E(s)-E(s-2j\omega)\} + H_{dc-PI}(s+j\omega)\{E(s)+E(s+2j\omega)\}] \quad (4.7)$$

Finally, output can be obtained in 's' domain as shown in Equation 4.8. The frequency response of Equation 4.1 and Equation 4.8 is found to be similar for any given $H_{dc\text{-}PI}(s)$. This mathematical analysis also shows the cancellation of double-frequency component in the final stage of the modulator which was previously produced by de-modulation method. This will result into an absence of double-frequency term in the final output waveform.

$$v = v_\alpha + v_\beta = \frac{1}{2}E(s)[H_{dc-PI}(s+j\omega) + H_{dc-PI}(s-j\omega)] \quad (4.8)$$

Equation 4.8 also confirms harmonic content shifting to frequency ω. Equation 4.8 can be rewritten as per Equation 4.9 with the assist of low-pass to band-pass method if reference frequency is greater than signal bandwidth [13].

$$H_{PR} = H_{dc-PI}\left(\frac{s^2+\omega^2}{2s}\right) \quad (4.9)$$

PI compensators can achieve zero steady-state error in case of dc system applications. Therefore, transfer function of ideal PR controllers can be obtained from Equation 4.11 which is basically a function of H_{dc-PI}, as shown in Equation 4.10.

$$H_{dc-PI}(s) = k_P + \frac{k_i}{s} \tag{4.10}$$

$$H_{PR-I}(s) = k_P + \frac{2k_i s}{s^2 + \omega^2} \tag{4.11}$$

Nevertheless, recognition of dc integrator having infinite gain is not possible due to limitation of analog system. Therefore, ideal PI compensator is approximated for its practical use which is shown in Equation 4.12.

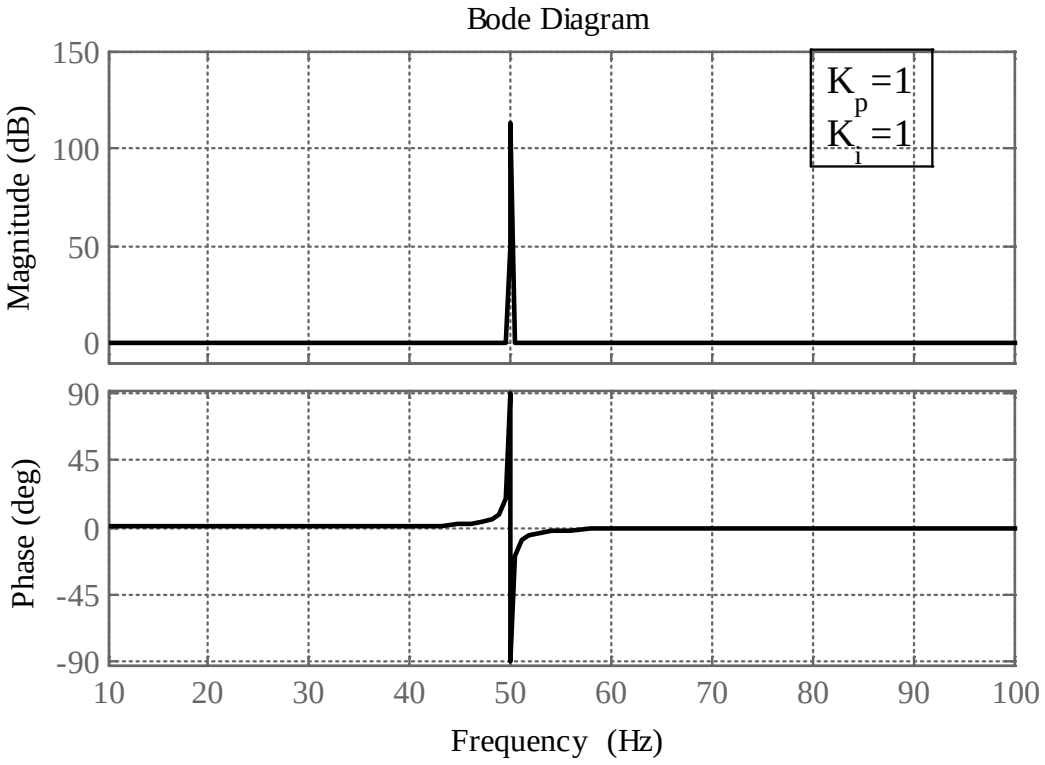
$$H_{dc-PI}(s) = k_P + \frac{k_i \omega_C}{s + \omega_C} \tag{4.12}$$

Consequently, the transfer function of proportional-resonant compensator is calculated as per Equation 4.13 by using the concept of Equation 4.9 which is used for practical applications [13].

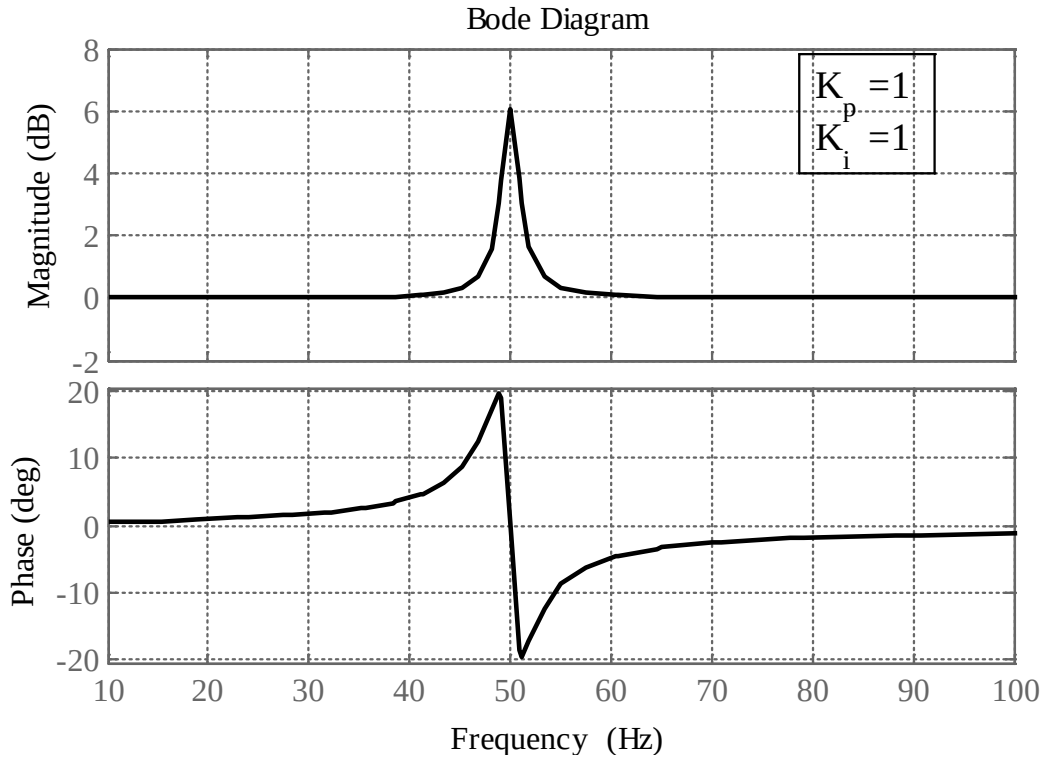
$$H_{PR-NI}(s) = k_P + \frac{2k_i \omega_C s}{s^2 + 2\omega_C s + \omega^2} \tag{4.13}$$

This section shows modelling of proportional-resonant (PR) compensator. The rigorous mathematical analysis demonstrates cancellation of the double frequency components and higher order harmonics from a given signal. The advantages of PR compensator are enumerated over conventional compensator to justify its use in the current control loop of SAPF control system.

Bode-diagrams of open-loop PR compensator transfer functions are plotted for conventional use and for practical purpose and these are shown in Figure 4.3 (a) and 4.3 (b), respectively. Gain is relatively higher at selected fundamental frequency, which is 50 Hz, in case of ideal PR controller as shown in Figure 4.3(a). Significant amount of gain is also present in case of practical application based PR compensator which gives nil magnitude and phase error in steady-state working conditions. The response can be depicted from Figure 4.3 (b). The constants of PR controller need to be tuned according to closed-loop performance requirement. This chapter shows rigorous analysis with PR controller in terms of steady-state performance analysis and closed-loop control stability. It is found that, proportional-resonant controllers are approximated as per Equation 4.13 in case of real-time applications due to limitations in analog circuit and digital signal accuracy [172].



(a)



(b)

Figure 4.3 Bode-plot of proportional-resonant compensator (a) in ideal condition, and (b) in practical condition

Finally, bode-plot technique is employed to show the significant amount of gain present at a particular frequency in case of PR compensator in both ideal condition and practical application.

4.4 DESIGN AND STABILITY ANALYSIS OF PROPOSED CLOSED-LOOP CONTROL SYSTEM

4.4.1. Advanced SRF Theory Composed of PR Compensator

Synchronous reference frame (SRF) theory is a well-known technique for obtaining current reference. Three phase load currents are sensed with the help of current sensors. The sensed load currents are first transformed to alpha-beta component (rotating frame) with the help of Clark's transformation. This is depicted as per Equation 4.14.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{2}/3 \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4.14}$$

Rotating frame components of load currents are further transformed to d-q-0 or synchronous reference frame with the help of park's transformation which can be shown from Equation 4.15.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t & 0 \\ -\sin\omega t & \cos\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} \tag{4.15}$$

Both oscillatory and fundamental component of load current signals are present in this d-q-0 system. Low pass filter of cut-off frequency 5 Hz. is used for extracting DC quantity from these d axis and q axis signals. As, system is balanced one, zero component is not considered for further calculation. For generation of reference component of source current, d-axis and q-axis components are calculated separately. This control of d and q axis component is composed of dc-voltage control loop, and PCC voltage control loop. However, some portion of active power is required for compensating switching losses of inverter unit. DC-link voltage of capacitor is sensed by voltage sensor and it is compared with reference value of dc-link voltage. Error of voltage signal is traditionally passed through PI compensator and finally this component is added with i_{d-DC}. The reference'd' axis current is expressed by Equation 4.16.

$$i_d = i_{d-DC} + i_{loss} \tag{4.16}$$

Generated reference source current should be with phase with source voltage. Therefore, PLL plays a vital role for deciding this factor. Phase angle calculation is done by PLL itself.

Finally, reference source current is converted back to d-q-0 frame to alpha-beta frame first with the help of inverse park transformation as per Eqn. 4.17 and alpha-beta to a-b-c component with the help of Equation 4.18.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{1}{[\sin^2(\omega t) + \cos^2(\omega t)]} \begin{bmatrix} \cos\omega t & -\sin\omega t & 0 \\ \sin\omega t & \cos\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{4.17}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{2}/3 \begin{bmatrix} 2/3 & 0 & \sqrt{2}/3 \\ -1/3 & 1/\sqrt{3} & \sqrt{2}/3 \\ -1/3 & -1/\sqrt{3} & -\sqrt{2}/3 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{4.18}$$

This reference current component is compared with sensed source current signal and error signal is compared with triangular signal with the help of phase-shifted pulse width modulation technique. Generated gate pulses are used for triggering IGBTs of CHB-MLI. The flow-diagram of total control theory along with the operation of PLL is depicted in Figure 4.4. Finally, error current signal is processed through stationary frame PR controller. Further, PS-PWM generates pulses for IGBTs of CHB-MLI. This chapter mainly emphasises on the use of proportional-resonant (PR) controller in advanced control theory under different non-linear loading conditions.

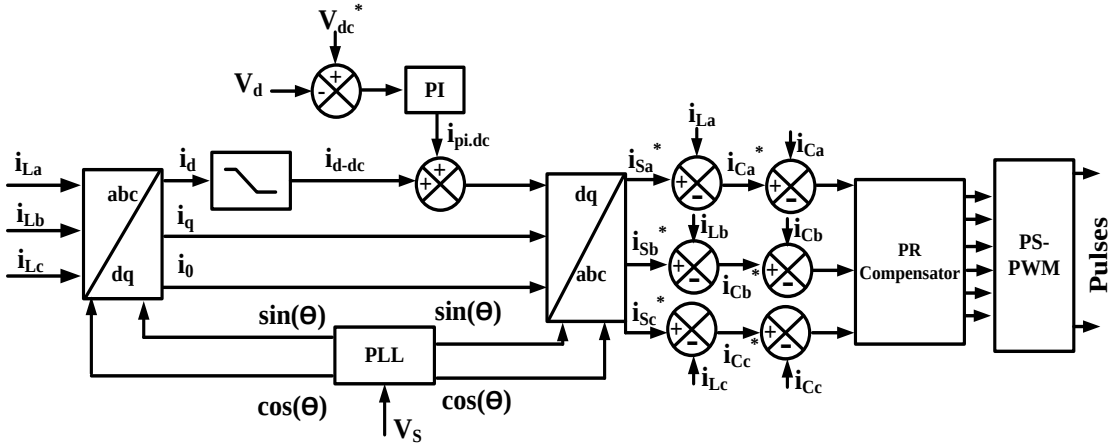


Figure 4.4 SRF based advanced control theory for CHB-MLI based SAPF

4.4.2 Stability Analysis of Proposed Control Algorithm

Closed loop control algorithm for SAPF is demonstrated in Figure 4.5, which comprises of PR compensator based current controller, PS-PWM technique gain and dc-link voltage gain. Average value model of current and voltage is taken into consideration for developing transfer function approach of proposed closed-loop controller. Coupling inductance, source current and load resistance are also taken into consideration for closed-loop transfer function calculation. System stability analysis check is done by linear control system method which is simple and easy to implement i.e. transfer function approach. System stability has been analyzed with Routh-Hurwitz criteria. Bode-plot and nyquist criteria analysis are rigorously performed for proving closed-loop stability of the proposed control method. Figure 4.5 shows closed-loop control system with advanced current controller. Gain K is considered for inverter operation and i_L, i_S are considered as system input and output current, respectively.

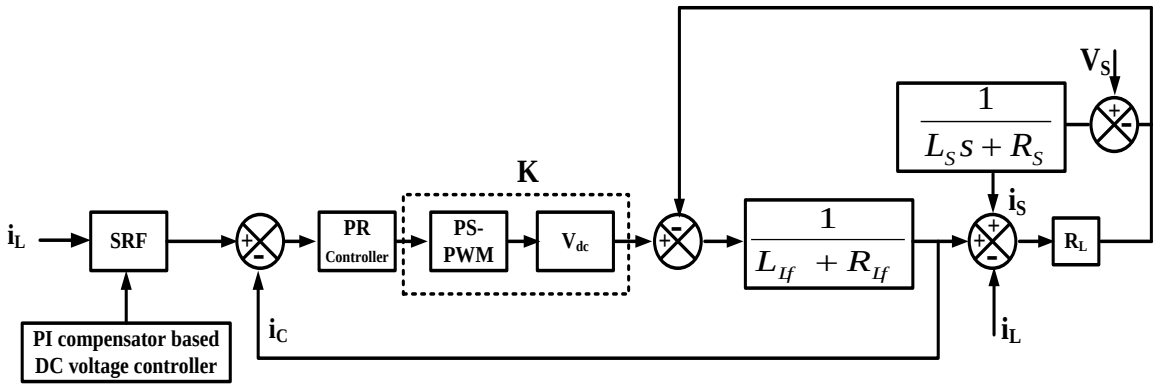
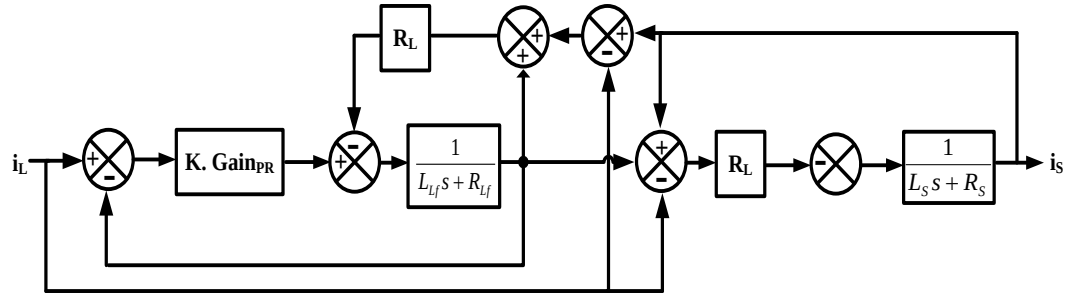
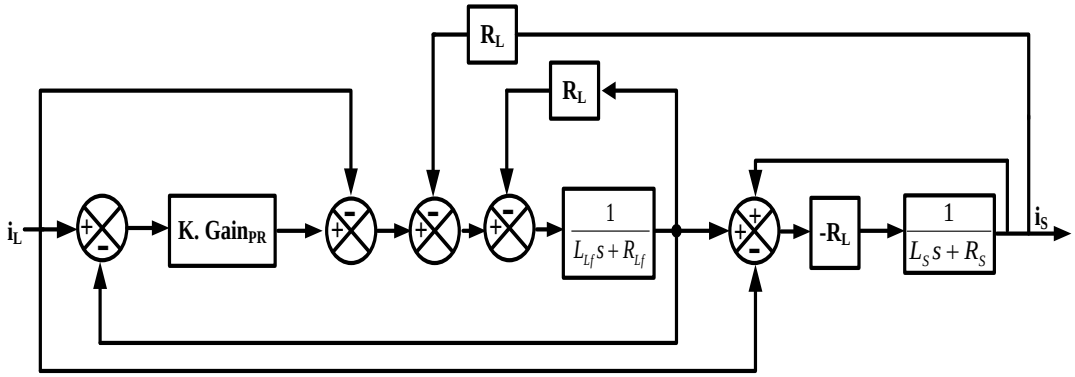


Figure 4.5 Closed-loop control algorithm applied to CHB-MLI based SAPF

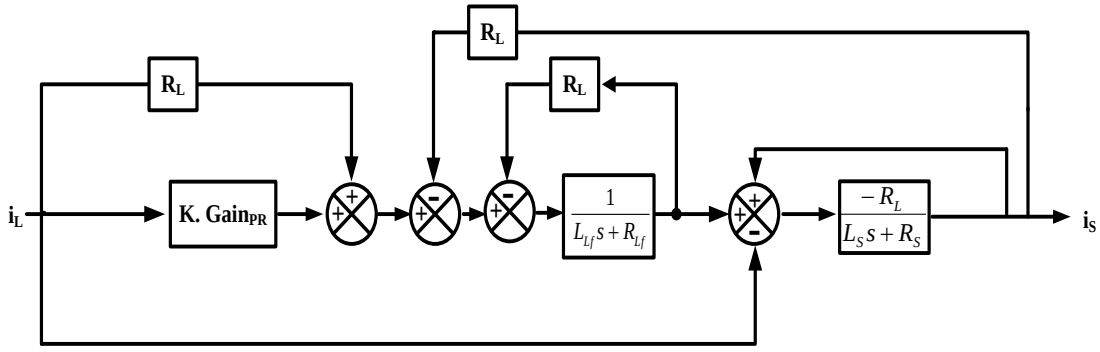
Transfer function of the proposed closed-loop control is found out by applying block-reduction technique. Figure 4.6 (a) - (d) shows detailed analysis of transfer function evolution approach. The derivation of transfer function using simplified closed loop is shown in Figure 4.6 (d). Step by step evaluation of transfer function approach for the proposed control is analyzed with the help of block reduction technique. Simplification of all loops is done by rearranging adder/subtraction block in the proposed closed loop control system. This chapter first shows closed-loop analysis of proposed controller with ideal-PR compensator based controller and then same has been performed with non-ideal PR compensator based current controller.



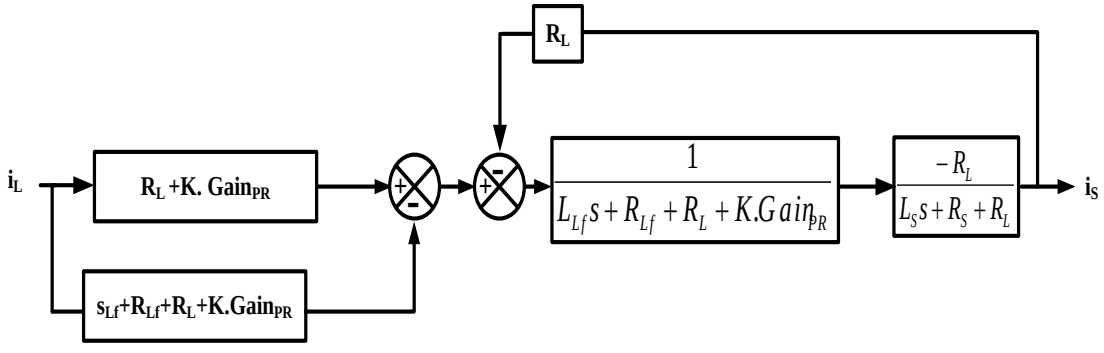
(a)



(b)



(c)



(d)

Figure 4.6 (a) Equivalent loop diagram considering inverter and PS-PWM gain parameter, (b) rearranged loop diagram, (c) simplified loop diagram by rearranging adder blocks, and (d) simplified closed loop diagram by solving feedback loop

Transfer function of PR compensator based closed loop control used for CHB-MLI based SAPF is defined by using Equation 4.19 in ideal condition.

$$\text{T.F.} = \frac{N_{31}.s^3 + N_{21}.s^2 + N_{11}.s + N_{01}}{D_{41}.s^4 + D_{31}.s^3 + D_{21}.s^2 + D_{11}.s + D_{01}} \tag{4.19}$$

where,

$N_{31} = R_L.L_{Lf}$;

$N_{21} = R_L.R_{Lf}$;

$N_{11} = R_L.L_{Lf}.\omega^2$;

$N_{01} = R_L.R_{Lf}.\omega^2$

$D_{41} = L_S L_{Lf}$;

$D_{31} = (R_{Lf}L_S + R_L L_S + KK_P L_S + R_S L_{Lf} + R_L L_{Lf})$;

$D_{21} = \omega^2 .L_{Lf}.L_S + 2KK_i L_S + R_{Lf}R_S + R_S R_L + KK_P R_S + KK_P R_L + R_{Lf}R_L$;

$D_{11} = KK_P L_S\omega^2 + \omega^2 L_S R_{Lf} + \omega^2 R_S L_S + \omega^2 R_S L_{Lf} + 2KK_i R_S + 2KK_i R_L +$

$\omega^2 .L_{Lf}.R_L$;

$D_{01} = KK_P R_S\omega^2 + R_S R_{Lf}\omega^2 + \omega^2 R_L R_S + \omega^2 R_{Lf}R_L + \omega^2 KR_{Lf}R_L + KK_P\omega^2 R_L$

For proportional-resonant compensator based closed-loop control technique, this chapter considers $R_L \rightarrow \infty$ [11]. Thus, transfer function can be rewritten as per Equation 4.20.

$$\text{T.F.} = \frac{N_{37}s^3 + N_{27}s^2 + N_{17}s + N_{07}}{D_{37}s^3 + D_{27}s^2 + D_{17}s + D_{07}} \tag{4.20}$$

where,

$N_{37} = L_{Lf}$;

$N_{27} = R_{Lf}$;

$N_{17} = \omega^2 L_{Lf}$;

$N_{07} = \omega^2 R_{Lf}$;

$D_{37} = (L_S + L_{Lf})$;

$D_{27} = (R_S + KK_P + R_{Lf})$;

$D_{17} = \left(\omega^2 L_{Lf} + 2KK_i\right)$;

$D_{07} = (R + R_{Lf} + KK_P)\omega^2$

By putting values of all declared variables and constants as shown in Appendix I, transfer function becomes

$$\text{T. F.} = \frac{3\text{X}10^{-3}\text{s}^3 + 0.5\text{s}^2 + 295\text{s} + 49298}{3.1\ \text{X}\ 10^{-3}\text{s}^3 + 23.55\ \text{s}^2 + 158685\ \text{s} + 2321936} \tag{4.21}$$

Equation 4.20 shows transfer function of closed loop system having advanced current controller. Table 4.1 shows Routh-Hurwitz (R-H) criteria analysis of advanced current controller with PR compensator which is developed based on Equation 4.21. No sign change is present in the first row of R-H table. Two negative terms are present in the third column but positive term magnitudes are much larger than the negative terms. So this term always appeared as a positive quantity which indicates that there is no sign change in the first column. Hence, closed loop system is stable.

Table 4.1 R-H Table of ideal PR compensator based controller

s^3	$(L_s + L_{Lf})$	$(\omega^2 L_{Lf} + 2KK_i)$
s^2	$(R_s + KK_P + R_{Lf})$	$(R + R_{Lf} + KK_P)\omega^2$
s^1	$(R_s + KK_P + R_{Lf})(\omega^2 L_{Lf} + 2KK_i) - \frac{(L_s + L_{Lf})(L_s + R + KK_P)\omega^2}{(R_s + KK_P + R_{Lf})}$ $= \frac{2KK_i(K_P + R_{Lf}) + \omega^2 KK_i(K_P + L_S) - \omega^2(R_{Lf}L_S + L_{Lf}R)}{(R_s + KK_P + R_{Lf})}$	0
s^0	0	0

Closed-loop stability is also tested with proportional-resonant (PR) compensator based advanced current control loop for practical applications. Transfer function of closed loop control applied to CHB-MLI based SAPF is obtained from simplified closed loop diagram by using linear control system technique as shown in Figure 4.5(h). Transfer function of closed loop control system having practical proportional-resonant compensator is defined by using Equation 4. 22.

$$\text{T. F.} = \frac{N_{32}.s^3 + N_{22}.s^2 + N_{12}.s + N_{02}}{D_{42}.s^4 + D_{32}.s^3 + D_{22}.s^2 + D_{12}.s + D_{02}} \tag{4.22}$$

where,

$N_{32} = R_L L_{Lf}$;

$N_{22} = R_L(R_{Lf} + 2L_{Lf}\omega_C)$;

$N_{12} = R_L(L_{Lf}\omega^2 + 2R_{Lf}\omega_C)$;

$N_{02} = R_L R_{Lf} \omega^2$ and

$D_{42} = R_L L_S L_{Lf}$;

$D_{32} = 2L_S L_{Lf} \omega_C + R_{Lf} L_S + L_S R_L + KK_P L_S + R_S L_{Lf} + L_{Lf} R_L$

$D_{22} = L_S L_{Lf} \omega^2 + 2\omega_C R_{Lf} L_S + 2\omega_C R_L L_S + 2KK_P \omega_C L_S + 2KK_i \omega_C L_S + 2L_{Lf} \omega_C R_S + R_{Lf} R_S + R_L R_S + KK_P R_S + 2L_{Lf} R_L \omega_C + R_L R_{Lf} + KK_P R_L$

$D_{12} = \omega^2 R_{Lf} L_S + \omega^2 R_L L_S + \omega^2 KK_P L_S + \omega^2 L_{Lf} R_S + 2\omega_C R_{Lf} R_S + 2\omega_C R_L R_S + 2KK_P \omega_C R_S + 2KK_i \omega_C R_S + \omega^2 L_{Lf} R_L + 2\omega_C R_{Lf} R_L + 2KK_P \omega_C R_L + 2KK_i \omega_C R_L$

$D_{02} = \omega^2 R_{Lf} R_S + \omega^2 R_L R_S + \omega^2 KR_S K_P + \omega^2 R_{Lf} R_L + \omega^2 KK_P R_L$

For real-time application and for simplification of calculation, $R_L \rightarrow \infty$[11]

Therefore, the transfer function becomes simpler for analysis as shown in Equation 4.23.

$$T.F. = \frac{N_{33}.s^3 + N_{23}.s^2 + N_{13}.s + N_{03}}{D_{33}.s^3 + D_{23}.s^2 + D_{13}.s + D_{03}} \tag{4.23}$$

where,

$N_{33} = L_{Lf}$;

$N_{23} = (R_{Lf} + 2L_{Lf} \omega_C)$;

$N_{13} = \left(L_{Lf} \omega^2 + 2R_{Lf} \omega_C\right)$;

$N_{03} = R_{Lf} \omega^2$

and

$D_{33} = (L_S + L_{Lf})$;

$D_{23} = 2\omega_C L_S + R_S + 2L_{Lf} \omega_C + R_{Lf} + KK_P$;

$D_{13} = \omega^2 L_S + 2\omega_C R_S + \omega^2 L_{Lf} + 2\omega_C R_{Lf} + 2KK_P \omega_C + 2KK_P \omega_C$;

$D_{03} = \omega^2 R_S + \omega^2 R_{Lf} + \omega^2 KK_P$

By putting values of all declared variables and constants, the transfer function becomes

$$T.F. = \frac{3\ X\ 10^{-3}.s^3 + 0.554.s^2 + 304.7.s + 49298}{3.1\ X10^{-3}.s^3 + 4.7163.s^2 + 13233.7502.s + 459511} \tag{4.24}$$

Table 4.2 depicts R-H criteria analysis of advanced current controller employing practical purpose proportional-resonant compensator which is developed based on

Equation 4.23. No sign change is present in the first row of R-H table as negative terms get cancelled out after calculation in third row. Therefore, there is no sign change in the first column. Hence, this calculation implies that closed loop system is stable with practical proportional-resonant type of controller.

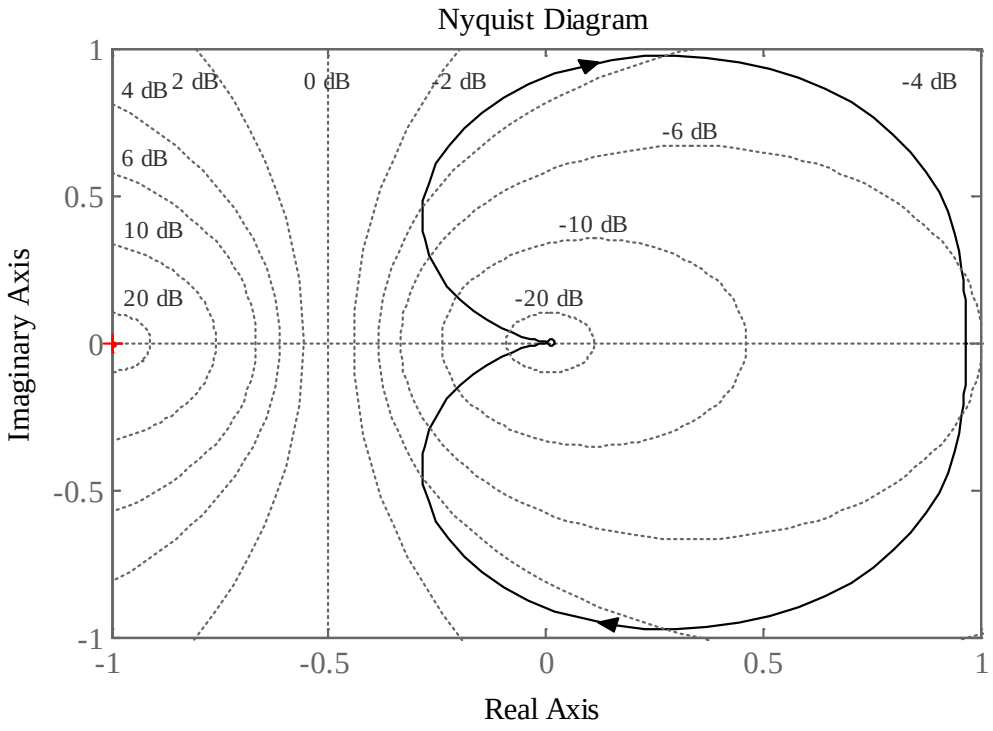
Table 4.2 R-H Table of practical purpose PR compensator based controller

s^3	$(L_S + L_{Lf})$	$(\omega^2 L_S + 2\omega_C R_S + \omega^2 L_{Lf} + 2\omega_C R_{Lf} + 2KK_P\omega_C)$
s^2	$(2\omega_C L_S + R_S + 2L_{Lf}\omega_C + R_{Lf} + KK_P)$	$(\omega^2 R_S + \omega^2 R_{Lf} + \omega^2 KK_P)$
s^1	$(\omega^2 L_S + 2\omega_C R_S + \omega^2 L_{Lf} + 2\omega_C R_{Lf} + 2KK_P\omega_C)$ $\frac{(2\omega_C L_S + R_S + 2L_{Lf}\omega_C + R_{Lf} + KK_P) - (\omega^2 R_S + \omega^2 R_{Lf} + \omega^2 KK_P)(L_S + L_{Lf})}{(2\omega_C L_S + R_S + 2L_{Lf}\omega_C + R_{Lf} + KK_P)}$	0
s^0	0	0

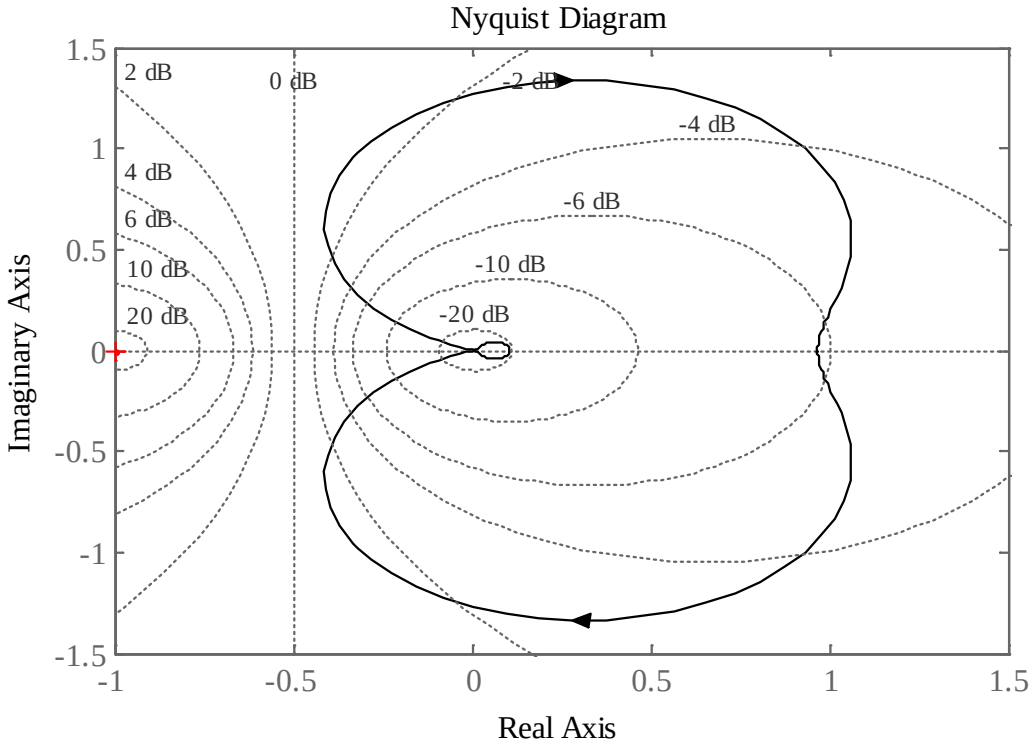
Nyquist plot is important because closed-loop analysis of the proposed system can also be predicted using nyquist plot. Stability can be checked and analyzed from the nyquist plot based on the position of (-1, 0) point. Equation 4.21 and 4.24 are used for checking nyquist stability of the proposed system. Equation 4.25 is used for calculating nyquist stability where, P denotes number of poles in the right-hand side of the s-plane, Z denotes number of zeros in the right-hand side of the s-plane of open-loop transfer function and N denotes anti-clockwise encirclement.

$$P - Z = N \tag{4.25}$$

Nyquist plot of open-loop transfer function for proposed control algorithm is shown in Figure 4.7 (a) and 4.7 (b) which are obtained from Equation 4.21 and 4.24 in case of proportional-resonant compensator for both the conditions. Number of encirclement (N) around (-1, 0) point is zero and open loop pole lying right hand side of s plane is zero. Therefore, $0 - Z = N = 0$. So, $Z = 0$ where, Z denotes close loop pole in right hand side of s-plane. Consequently, no pole lies in the right hand side of s-plane of closed loop transfer function. Hence, it can be concluded from the above detailed analysis from nyquist and R-H criteria that the open and closed-loop system is stable for both ideal and practical purposed PR compensator based current control applied to SAPF.



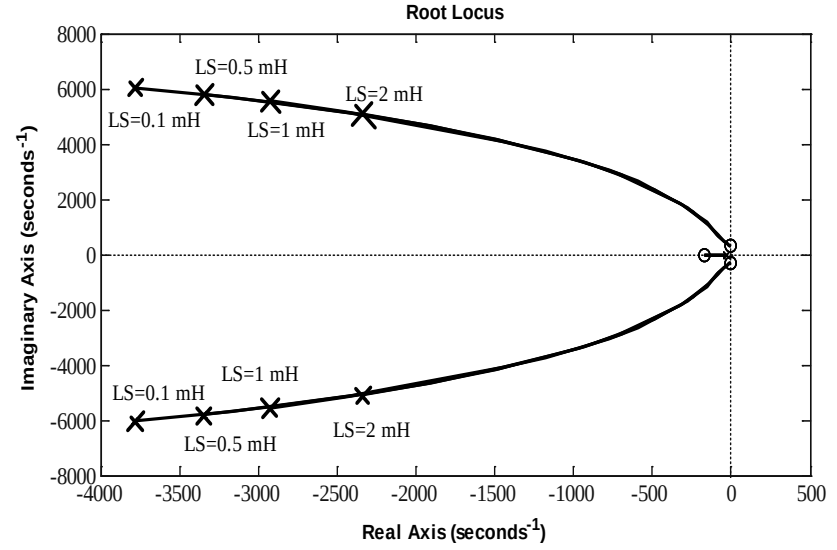
(a)



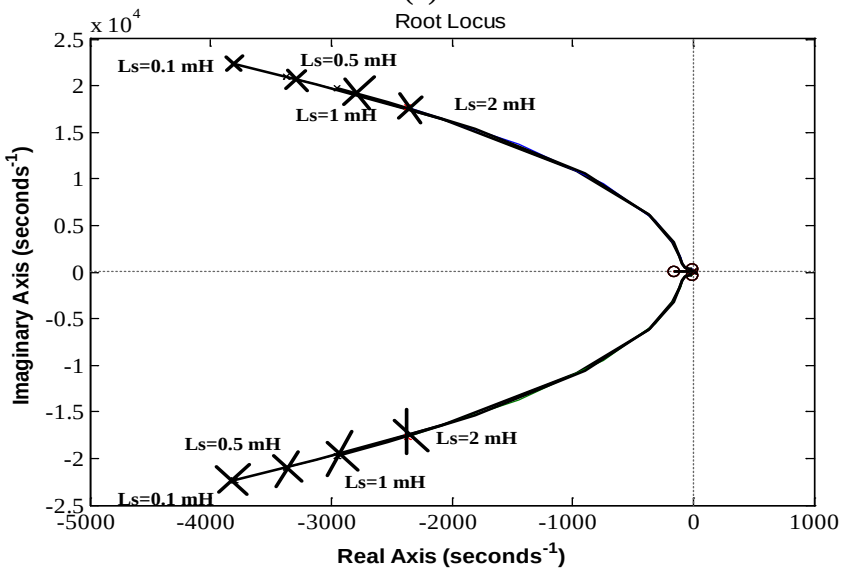
(b)

Figure 4.7 Nyquist diagram of (a) ideal PR compensator based advanced current controller, and (b) practical purpose PR compensator based advanced current controller

Root-locus for advanced current controller employing proportional-resonant compensator for both the conditions are plotted in Figure 4.8 (a) and 4.8 (b), respectively.



(a)



(b)

Figure 4.8 Root-locus diagram with variation of grid impedance in case of (a) ideal PR compensator based control, and (b) practical purpose PR compensator based control

All poles in the left-hand side of the s-plane in both the cases are calculated from Equation 4.20 and Equation 4.23. From the above root-locus analysis, the system is observed to be stable. Effect of stability is also checked with the variation of grid side impedance which shows the relation between inverter and load current. Source inductance is varied from 0.1 to 2 mH and its root-locus diagram is plotted. Both the

figures show that damping factor decreases with increase in magnitude of L_S. Therefore, system behavior tends to be oscillatory in nature. This section shows rigorous closed-loop stability analysis of the proposed controller with proportional-resonant compensator based advance current controller. Bode-plot, nyquist analysis and R-H criteria method have been used for analyzing the system stability.

4.4.3 Design of Current Controller Constants

Selection of controller parameters plays a significant role for improving system behavior. Therefore, controllers need to be tuned in a proper way. Controller parameters are properly tuned in this chapter for CHB-MLI based SAPF system using Bode-plot based mathematical approach, proposed by Angelico et al. [177]. A simplified mathematical model is designed separately for advanced current controller and dc voltage controller.

Equation 4.26 can be written by using the values of K_P mentioned in Equation 4.11 in case of ideal PR controller.

$$H_{PR-I}(s) = k_i\left(T_i + \frac{2s}{s^2+\omega^2}\right)$$

Therefore,

$$H_{PR-I}(s) = k_i\left(\frac{T_i.s^2+\omega^2.T_i+2s}{s^2+\omega^2}\right) \quad (4.26)$$

Equation 4.26 can be rewritten by putting the value of ω as per Equation 4.27.

$$H_{PR-I}(s) = K_i\left[\frac{T_i.s^2+2.s+98696.04.T_i}{s^2+98696.04}\right] \quad (4.27)$$

Gain of advanced current control loop is represented by Equation 4.27, which can be calculated from Figure 4.9.

$$G_1(s) = K_{PS-PWM}.\frac{V_d}{L_{Lf}s+R_{Lf}} \quad (4.28)$$

Equation 4.28 can be rewritten as per Equation 4.29 by putting values of all variables as per requirement of closed-loop stability.

$$G_1(s) = \frac{6800}{(3X10^{-3})+0.35} \times 5.33X10^{-4} = \frac{3.6244+j.0}{0.35+j.\omega.3X10^{-3}} \quad (4.29)$$

The required parameter θ_G can be calculated from Equation 4.24 and its value is calculated as per Equation 4.25.

$$\theta_G = \tan^{-1}\left(\frac{0}{3.6244}\right) - \tan^{-1}\left(\frac{3X10^{-3}X12566}{0.35}\right) = -89.46^{\circ} \quad (4.30)$$

Required phase margin for compensated system is 70° according to $C'(s).G_1(s)$, where $C'(s)$ is denoted by $(T_i.s + 1/s)$.

Consequently, total angle required for $C'(s).G_1(s) = -180^{\circ} + 70^{\circ} = -110^{\circ}$

$$\text{As, } \angle G_1(s) + \angle C'(s) = -110^{\circ}$$

Therefore,

$$\angle C'(s) = -110^{\circ} + 89.46^{\circ} = 20.54^{\circ} \quad (4.31)$$

For current controller, $T_i = \tan(\angle C'(s) + 90^{\circ})/\omega_G = \tan(90 - 20.54)/\omega_G$

Bode diagram of $G_1(s)$ is plotted and ω_G can be calculated at 89.4 degree and its value is 9.36×10^3. Finally T_i can be found from Equation 4.32, which is required for further calculation of constants.

$$T_i = \tan 69.46/9.36 \times 10^3 = 2.6689/9.36 \times 10^3 = 2.85 \times 10^{-4} \quad (4.32)$$

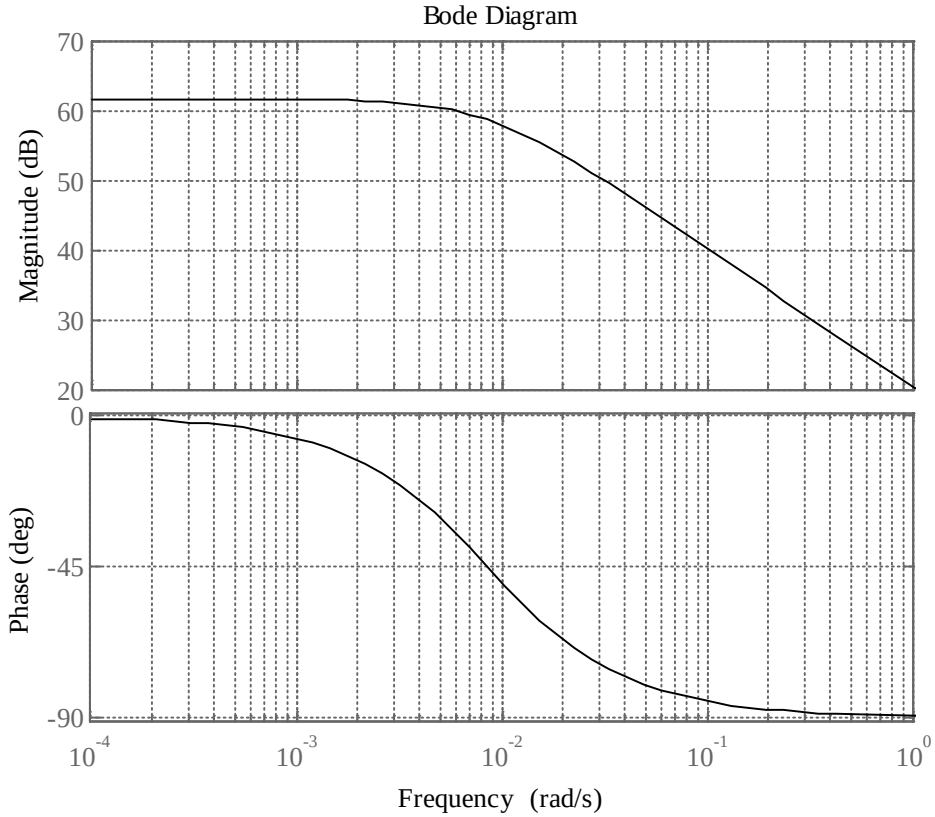


Figure 4.9 Bode plot of $G_1(s)$

Equation 4.33 is formed by multiplying Equation 4.11 and Equation 4.28, which is needed for further calculation.

$$H_{PR-I}(s).G_1(s) = K_i\left[\frac{2.85 \times 10^{-4}s^2 + 2s + (98696.04 \times 2.85 \times 10^{-4})}{s^2 + 98696.04}\right].\left(\frac{3.6244}{0.35 + 3 \times 10^{-3}s}\right)$$

Therefore,

$$H_{PR-I}(s).G_1(s) = K_i\left[\frac{1.032 \times 10^{-3}.s^2 + 7.2488.s + 101.918}{3 \times 10^{-3}.s^3 + 0.35.s^2 + 296.08.s + 34543.614}\right] \quad (4.33)$$

Bode-plot of Equation 4.33 is required for further calculation and it is shown in Figure 4.10 (a). Bode-plot shows that gain of uncompensated system is -86.8 dB whereas system gain is 9.42×10^3. Hence, controller needs to provide a gain of 86.8 dB in order to cross 0 dB of $C'(s).G_1(s)$ according to maintain system stability.

So, integration constant is found out with the help of Equation 4.34.

$$K_i = 10^{(86.8/20)} = 21877.6162 \quad (4.34)$$

The value of proportional constant for ideal PR compensator is found from Equation 4.35.

$$K_P = K_i.T_i = 6.235120 \quad (4.35)$$

Same procedure is applied for designing constant parameters for practical purpose proportional-resonant regulator. Open-loop transfer function of proportional-resonant regulator in this condition is shown as Equation 4.36.

$$H_{PR-N.I}(s) = K_P + \frac{2.K_i.\omega_c.s}{s^2 + 2.\omega_c.s + \omega^2} = K_i\left[T_i + \frac{20.s}{s^2 + 20.s + 98696.04}\right]$$

Therefore,

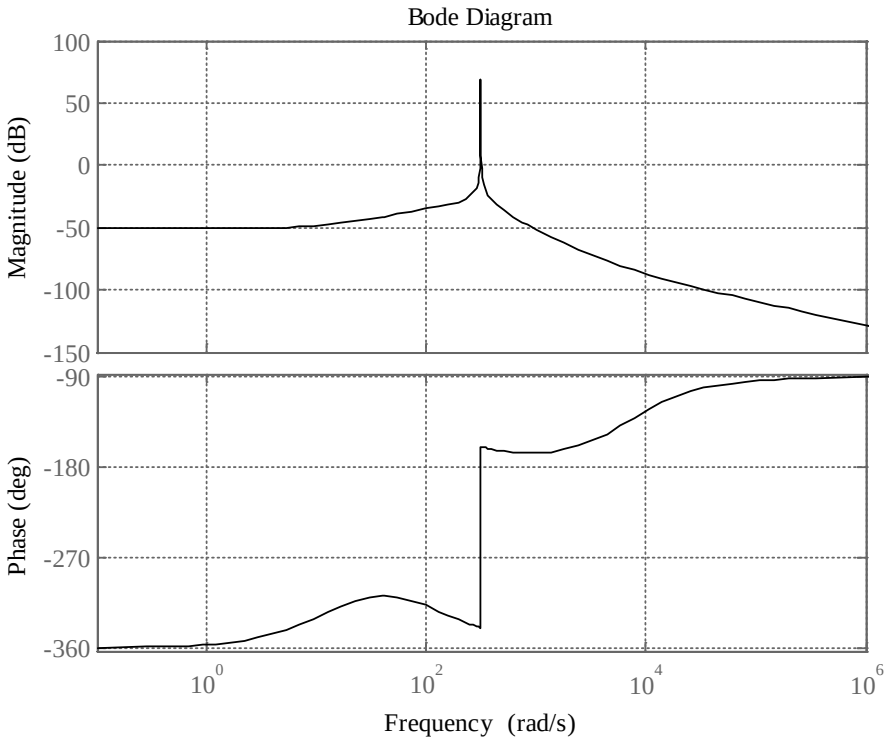
$$H_{PR-N.I}(s) = K_i\left[\frac{2.85 \times 10^{-4}.s^2 + 20.0057.s + 28.1283}{s^2 + 20.s + 98696.04}\right] \quad (4.36)$$

Equation 4.37 is formed by multiplying Equation 4.12 and Equation 4.36.

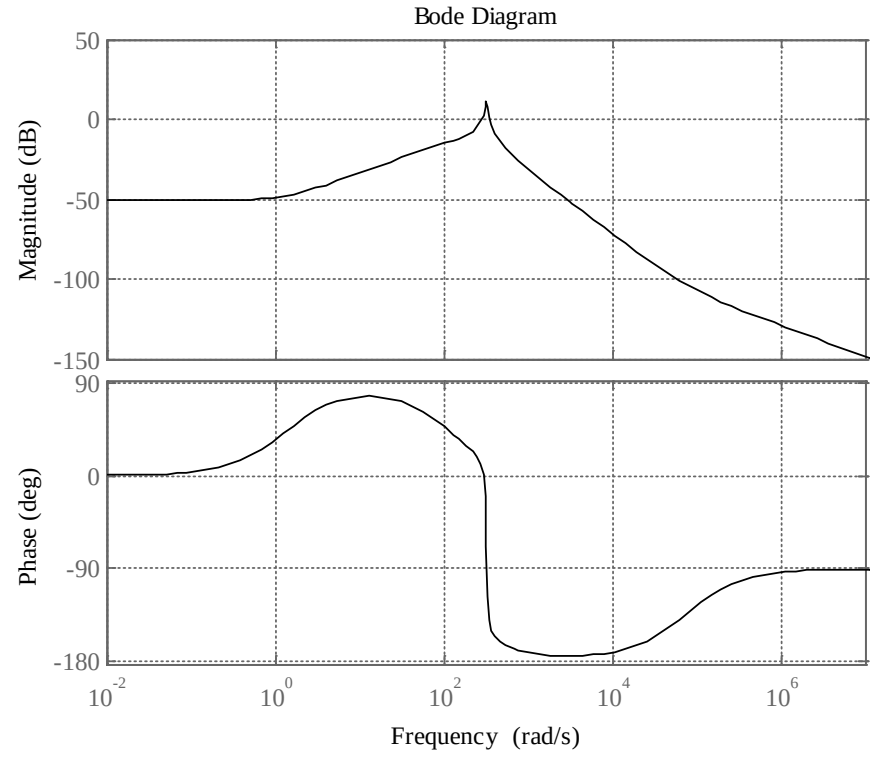
$$H_{PR-N.I}(s).G_1(s) = K_i\left[\frac{2.85 \times 10^{-4}.s^2 + 20.0057.s + 28.1283}{s^2 + 20.s + 98696.04}\right].\left[\frac{3.6244}{0.35 + 3 \times 10^{-3}.s}\right]$$

Therefore,

$$H_{PR-N.I}(s).G_1(s) = K_i\left[\frac{1.0329 \times 10^{-3}.s^2 + 72.50865.s + 101.948}{3 \times 10^{-3}.s^3 + 0.41.s^2 + 303.08812.s + 34543.614}\right] \quad (4.37)$$



(a)



(b)

Figure 4.10 Bode-plot diagram of advanced current controller transfer function (a) ideal PR compensator based current control loop, and (b) non-ideal PR compensator based current control loop

Bode-diagram of Equation 4.37 is plotted and shown in Figure 4.10 (b). Bode plot shows that the gain of uncompensated system is -71 dB where system gain is $9.36 \text{ X } 10^3$. Hence, the controller needs to provide a gain of 71 dB in order to cross 0 dB of $C'(s).G_2(s)$. So, proportional and integration constants of the proposed PR controller can be calculated from Equation 4.38 and Equation 4.39.

$$K_i = 10^{(71/20)} = 3548.133 \tag{4.38}$$

$$K_P = K_i.T_i = 2.85X10^{-4} \times 3548.133 = 1.0112 \tag{4.39}$$

This section portrays the bode-plot based performance parameter selection method for both ideal- and non-ideal PR compensator based advanced current controller keeping stability of the system in mind. These obtained parameters for PR compensator are further used for simulation study and hardware implementation of proposed control algorithm.

4.5 PERFORMANCE EVALUATION OF PROPOSED CONTROL USING MATLAB

The performance of the proposed controller is checked and analyzed using MATLAB/Simulink under different non-linear loading conditions for three-phase and three-wire system. Simulation results are presented in both steady-state as well as in transient condition, with voltage and current type of non-linear loading conditions. As three-phase source voltage considered for this study is balanced one, only voltage and current waveforms related to phase 'A' is considered for further study for better representation. Similar type of waveforms can be observed for phase 'B' and 'C', respectively.

4.5.1 Uncontrolled Rectifier and R-L Loading

Source voltage of phase 'A' (V_{Sa}), source current of phase 'A' (I_{Sa}), load current of phase 'A' (I_{La}), compensating current of phase 'A' (I_{Ca}), dc-link voltage (V_d), inverter output voltage (V_C) waveforms of CHB-MLI based SAPF with advanced current controller under R-L loading are shown in Figure 4.11. It can be depicted from this figure that the proposed control algorithm applied to MLI based SAPF is successfully able to mitigate current harmonic component and compensate reactive power. After successful operation

of this unit, source current becomes sinusoidal and in-phase with respective phase of source voltage. Five-level voltage is generated at the inverter output terminal which ensures proper operation of MLI unit. DC-link voltage is maintained constant during its operation. It can be depicted from figure that, source current is properly sinusoidal even though the load current is still non-linear in nature. Compensating current is shown in the figure to show the amount of current being fed by the inverter unit into the grid.

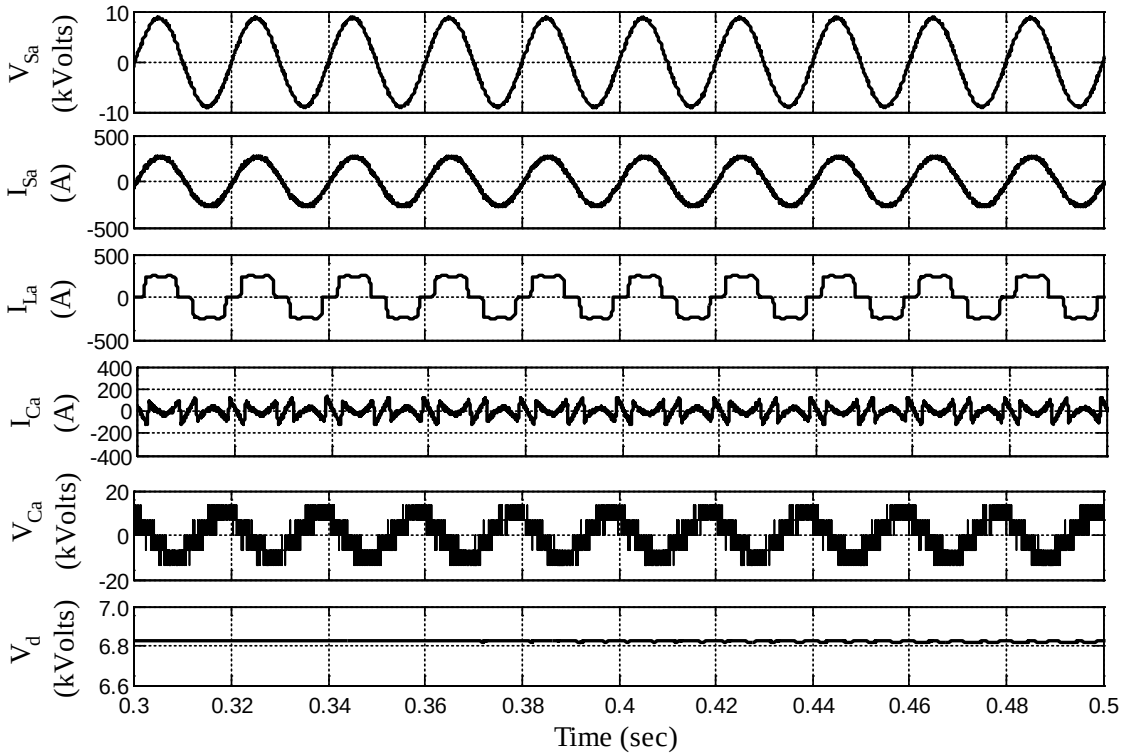


Figure 4.11 Steady-state simulation results of CHB-MLI based SAPF with PR compensator based advanced current controller under R-L loading condition

Figure 4.12 (a) – (b) shows the THD spectrums of source current before and after compensation. Source current THD is reduced from 26.92% to 3.31% after interconnection of MLI based SAPF with grid. Calculated gain parameters are successfully applied to the proposed control algorithm. Power factor also improved in the source side as reactive power demand decreases.

Performance of the proposed control algorithm is not only tested in steady-state condition, the control efficacy is also tested in load changing conditions. Performance of the proposed control algorithm is designed and tested extensively under load changing

condition. Figure 4.13 and Figure 4.14 show the load perturbation response of the MLI based SAPF unit for increment and decrement of load current, respectively.

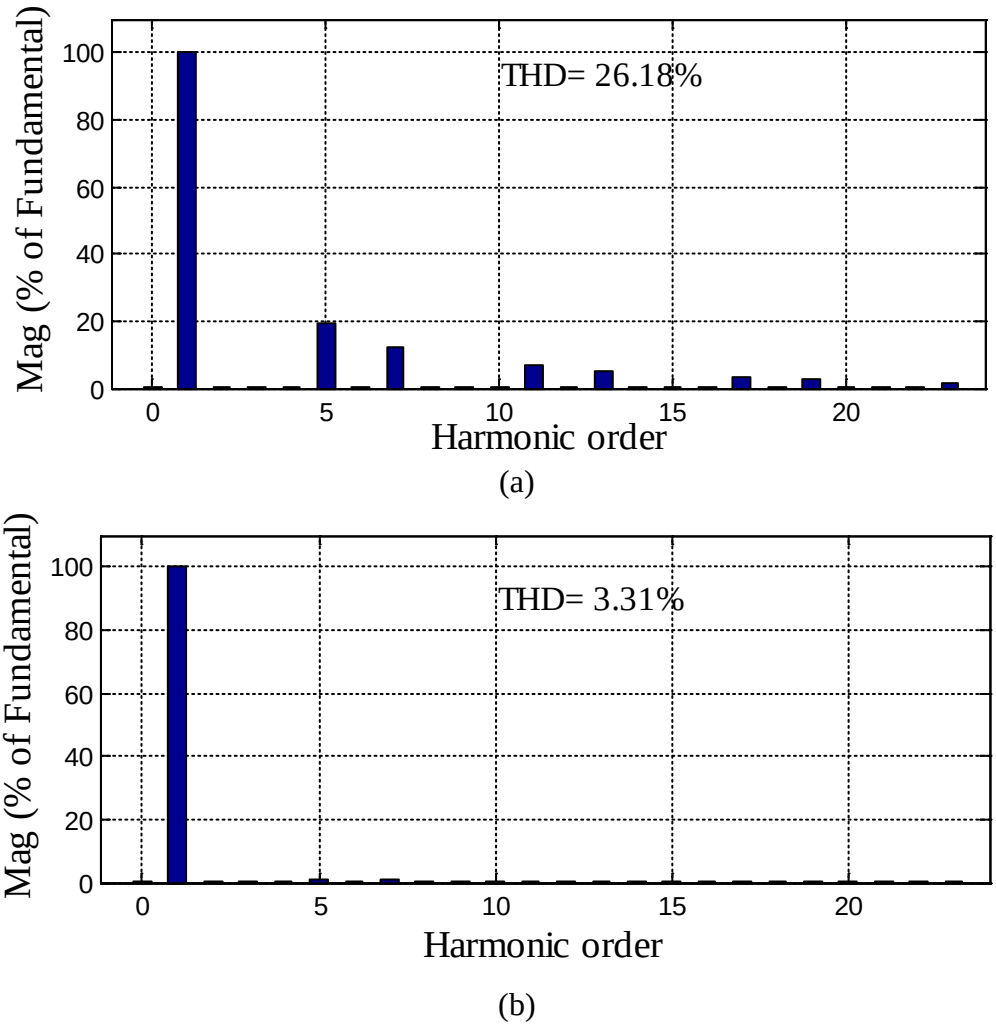


Figure 4.12 THD profile of source current with R-L load (a) before compensation, and (b) after compensation

Load current is increased from 200 A to 250 A at an instant t=0.9 sec while load current is decreased from 250A to 200A at an instant of t=1.5 sec. Only phase 'A' current is shown in figures due to the balanced load current. It can be seen from Figure 4.13 and Figure 4.14 that compensated source current transition is occurring smoothly during load changing conditions. A dip in dc-link voltage is also noticed from its mentioned reference value in order to release the excess amount of energy during the load increment condition. DC-link voltage got stabilized after 0.05 sec. of time span while incrementing load current. A rise in dc-link voltage is also noticed from its mentioned reference value in order to absorb the excess amount of energy during the load decrement condition. DC-

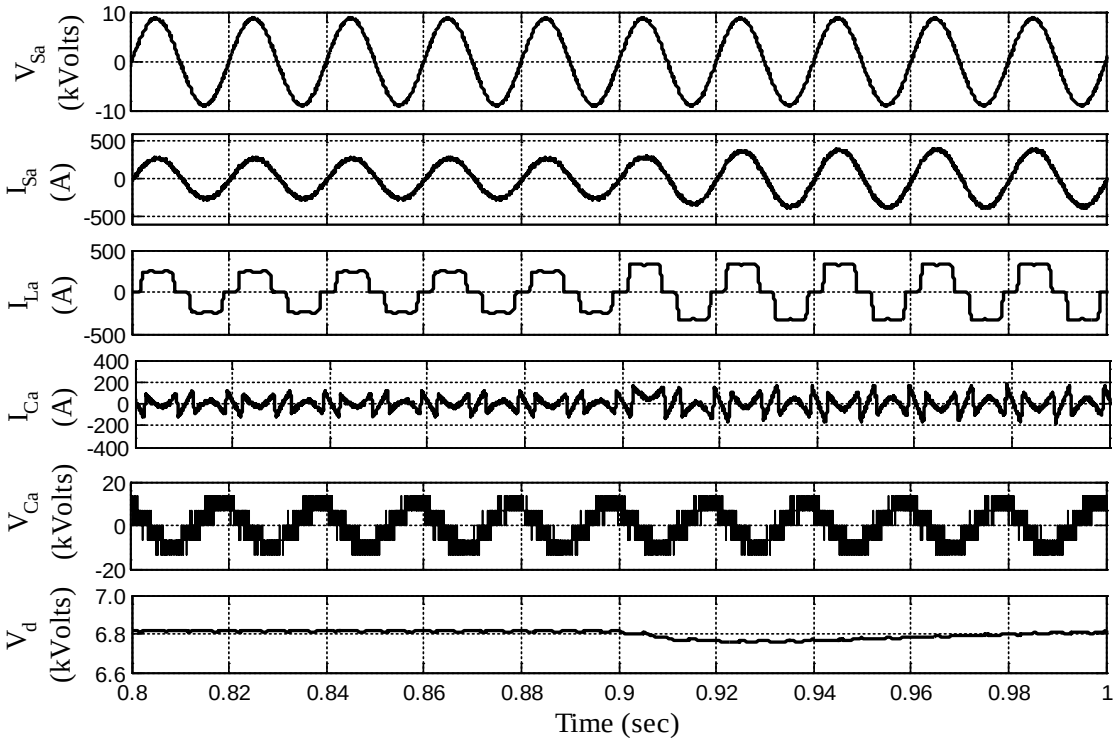


Figure 4.13 Transient performance of MLI based SAPF during load increment with R-L loading condition

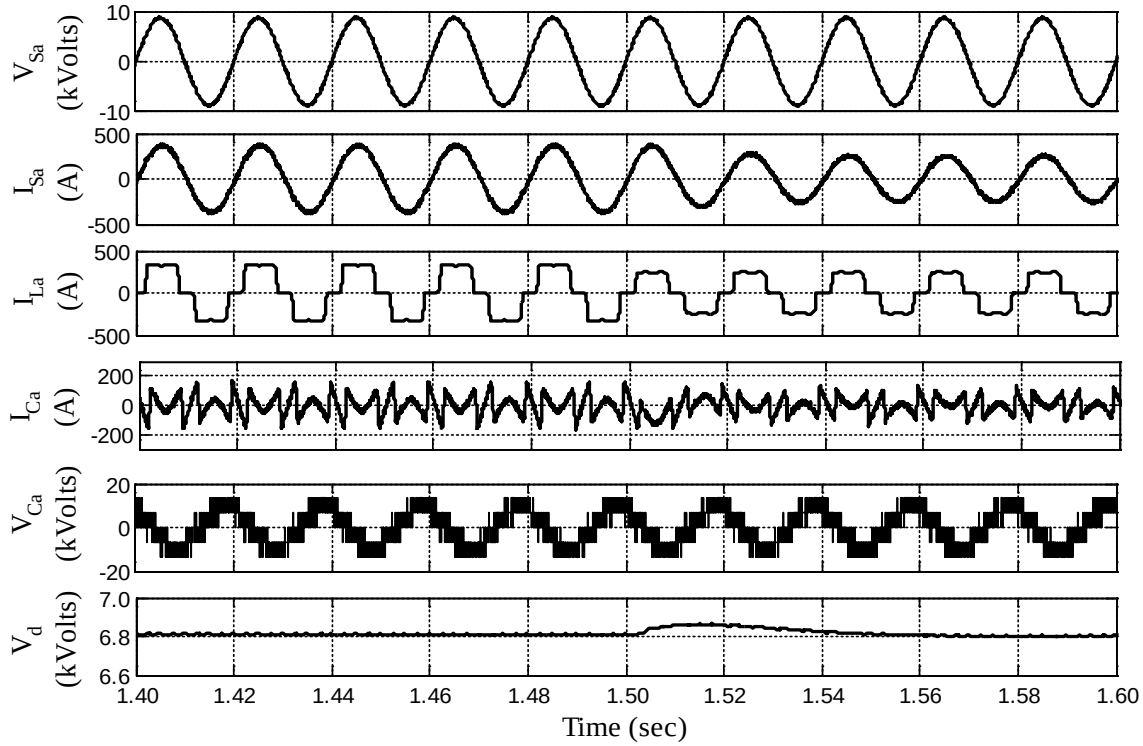
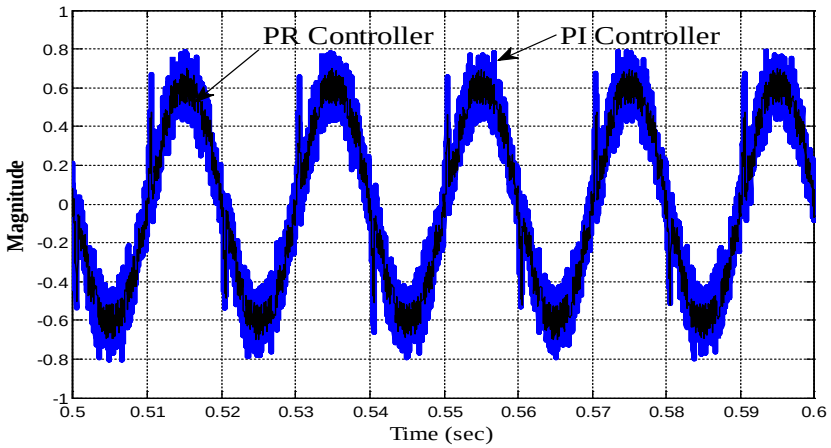


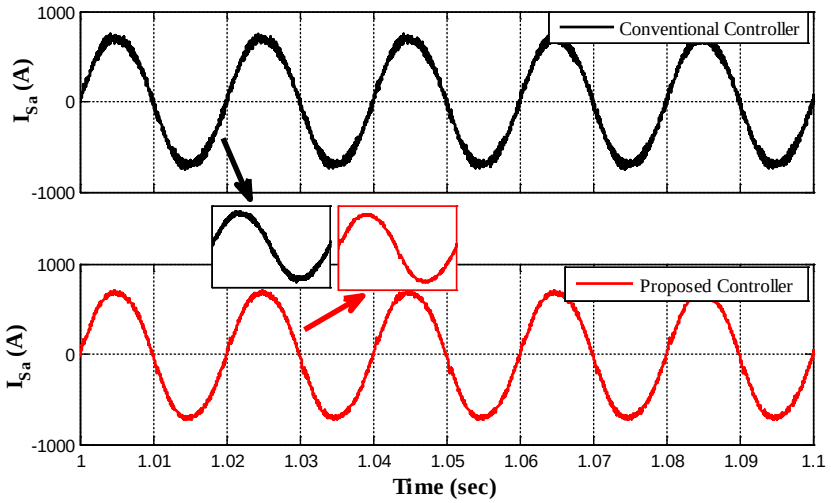
Figure 4.14 Transient performance of MLI based SAPF during load decrement with R-L loading condition

link voltage got stabilized after 0.06 sec. of time span while decreasing load current. It can be depicted from both the figures that source current transition is smooth with change in load current. Source current maintains its sinusoidal shape while load current is rich in harmonic content. So it can be concluded that, MLI based SAPF is able to filter out the harmonic component present in the load current successfully in steady-state as in load changing conditions.

Figure 4.15 (a) – (b) shows comparative analysis of conventional and advanced controller based SAPF system. Figure 4.15 (a) shows error signal for both the control techniques which will be further compared with phase-shifted triangular carrier wave.



(a)



(b)

Figure 4.15 Performance comparison of proposed controller with conventional current controller for MLI based SAPF system (a) error signal magnitude comparison, and (b) source current wave shape comparison

PR-compensator based controller produces sine waveform with minimum phase and magnitude error as compared to PI compensator based current controller. As a result, the quality of current fed to the grid through PCC is further improved in steady-state condition with advanced controller as seen from Figure 4.15 (b). Source current THD is an important parameter for checking the quality of current fed through the converter. The quality of source current is improved with proposed control technique in steady-state condition as shown in Table 4.3. Comparative analysis of proposed and conventional control algorithm with different non-linear loading conditions has been tabulated in Table 4.3.

4.5.2 Uncontrolled Rectifier and R-C Loading

The performance of the proposed controller is also checked with R-C type of non-linear loading. V_{Sa} , I_{Sa} , I_{La} , I_{Ca} , V_d , V_{Ca} waveforms of CHB-MLI based SAPF with advanced current controller under R-C loading are shown in Figure 4.16. After successful operation of this unit, source current becomes sinusoidal and in-phase with respective phase of source voltage.

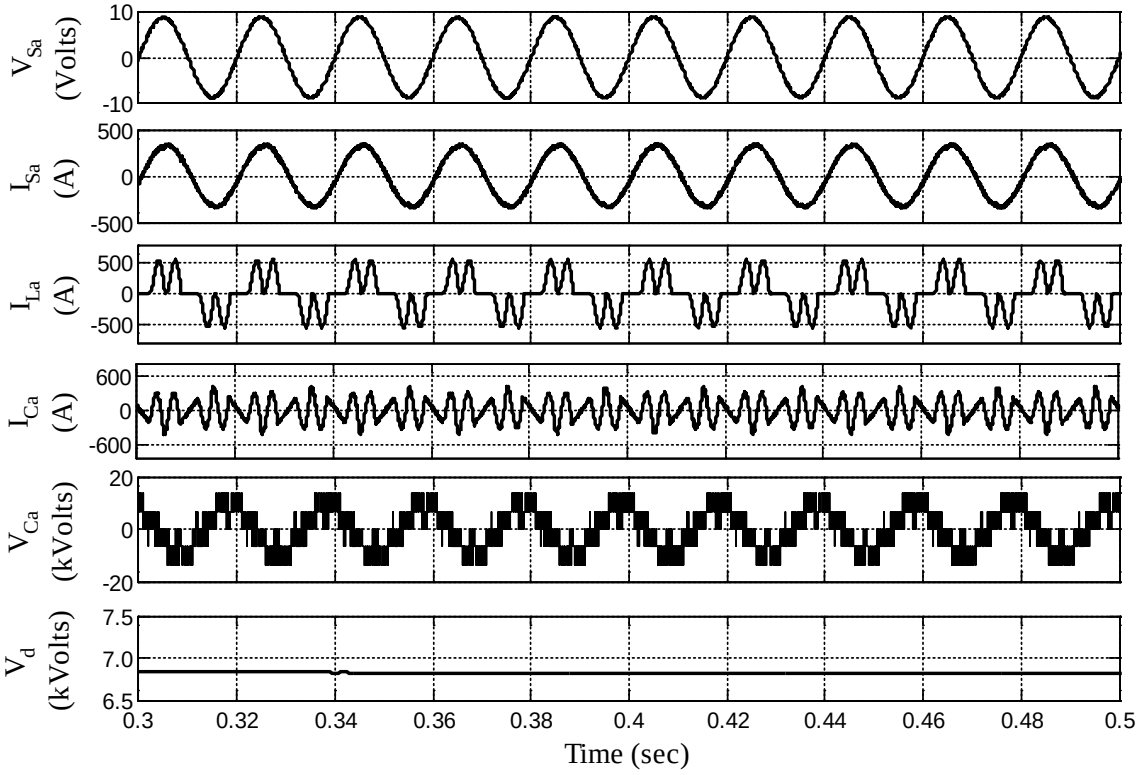
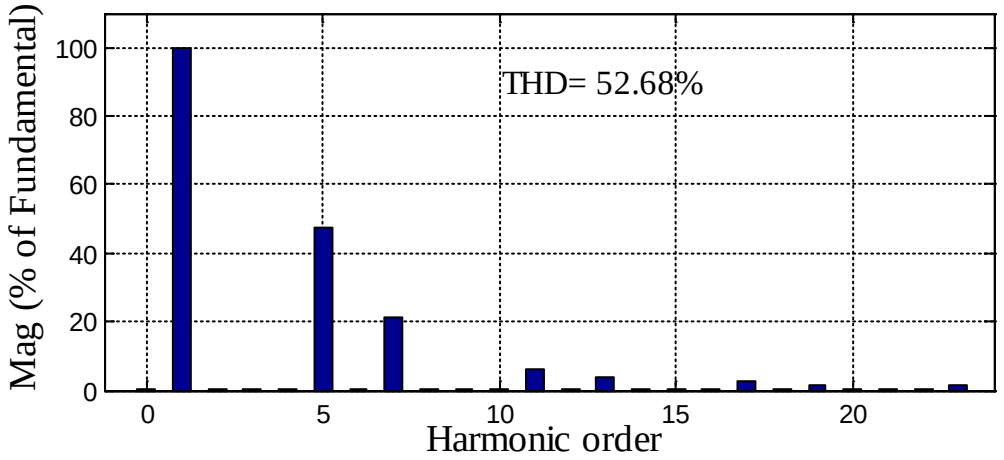


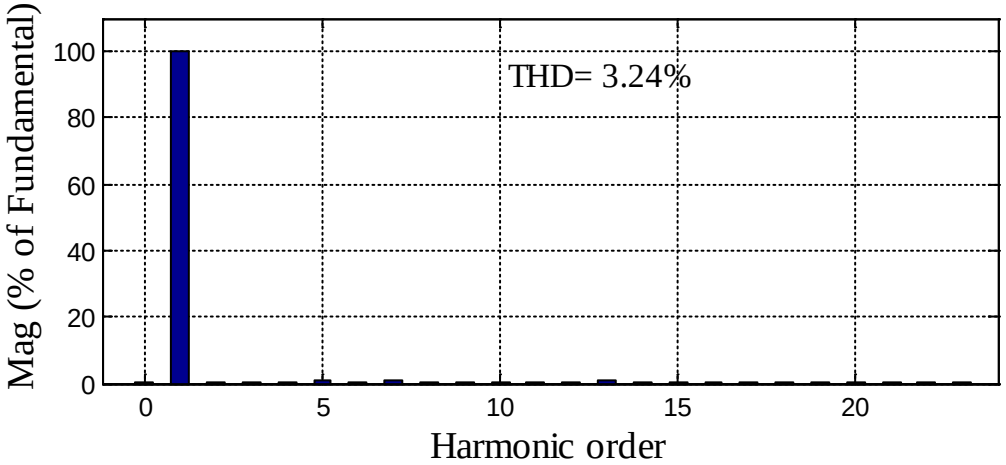
Figure 4.16 Steady-state simulation results of CHB-MLI based SAPF with advanced current controller under R-C loading condition

It can be depicted from this figure that the proposed control algorithm applied to MLI based SAPF is successfully able to mitigate current harmonic component and compensate reactive power with voltage-type non-liner loading condition.

Figure 4.17 (a) – (b) shows the THD spectrums of source current before and after compensation. Source current THD is reduced from 48.16% to 3.24% after interconnection of MLI based SAPF with grid. Calculated gain parameters are successfully applied to the proposed control algorithm. Power factor also improved significantly in the source side as reactive power demand decreases. Performance of modified control algorithm is designed and tested extensively under load changing condition.



(a)



(b)

Figure 4.17 THD profile of source current with R-C loading (a) before compensation, and (b) after compensation

Figure 4.18 and Figure 4.19 show the load perturbation response of the MLI based SAPF for increment and decrement of load current, respectively.

Load current is increased from 200 A to 250 A at an instant t=0.9 sec. while load current is decreased from 250A to 200A at an instant of t=1.5 sec. Only phase 'A' current is shown in figures due to the balanced load current. It can be seen from Figure 4.18 and Figure 4.19 that compensated source current transition is occurring smoothly during load changing conditions within 0.06 second time span. A dip/rise in dc-link voltage is also noticed from its mentioned reference value in order to release/ absorb the excess amount of energy during the load changing condition. It can be depicted from both the figures that source current transition is smooth with change in load current. Source current maintains its sinusoidal shape while load current is rich in harmonic content. So it can be concluded that, MLI based SAPF is able to filter out the harmonic component present in the load current successfully in steady-state as in load changing conditions under R-C non-linear loading condition.

Table 4.3 shows detailed comparative investigation of usual and proposed control algorithm applied to SAPF under R-L and R-C non-linear loading conditions. Non-linear source current THD is 26.92% with R-L loading whereas THD becomes 3.31% after operation of SAPF unit with proposed control algorithm. Power factor also improved from 0.90 to 0.997. Steady-state source current magnitude error is nil with respect to source current reference. Same has been examined with R-C type of non-linear loading conditions and results have been tabulated in Table 4.3. The results are compared with conventional algorithm applied to CHB-MLI based SAPF system. The detailed analysis shows system effectiveness with proposed controller in terms of percentage THD, power factor, steady-state source current magnitude and phase error under both R-L and R-C type of non-linear loading conditions. A comprehensive analysis of proposed and conventional control algorithm performance is analyzed with R-L and R-C load with ideal and practical purpose based PR compensator. Results show that proposed controller performance is almost similar in case of ideal and practical-purpose PR compensator. Based on simulation and comparative analysis as mentioned in Table 4.3, it can be concluded that the proposed controller gives better performance in terms of quality of current supplied to the grid.

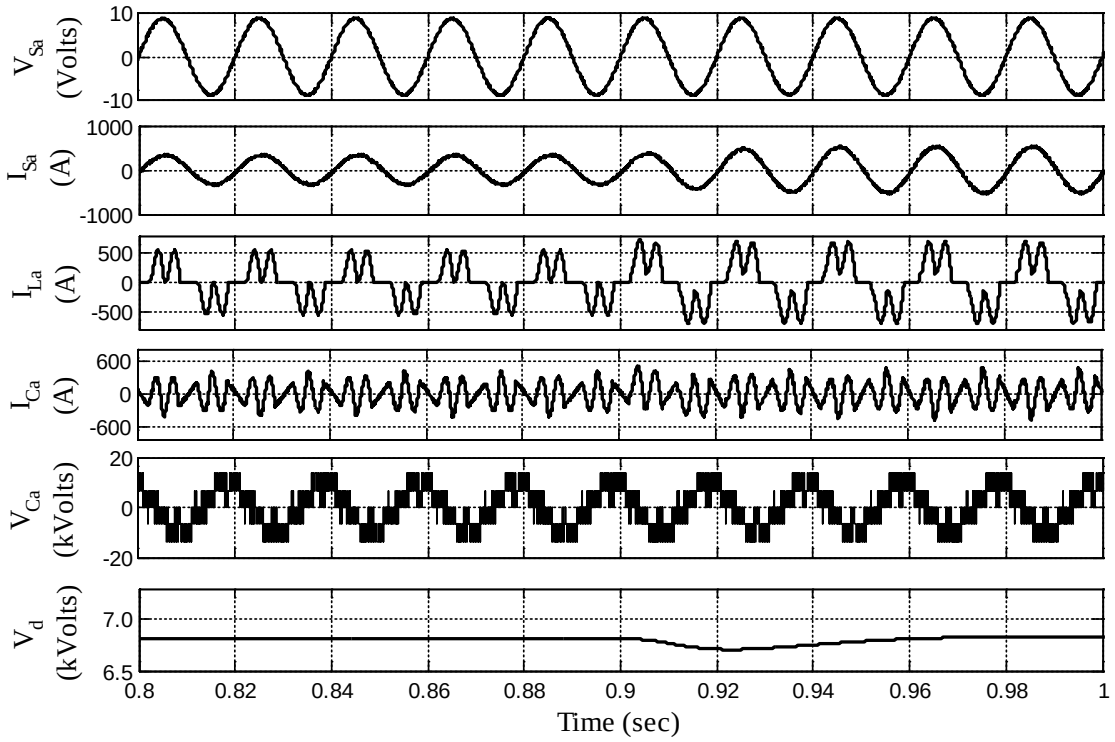


Figure 4.18 Transient performance of MLI based SAPF during load increment with R-C loading condition

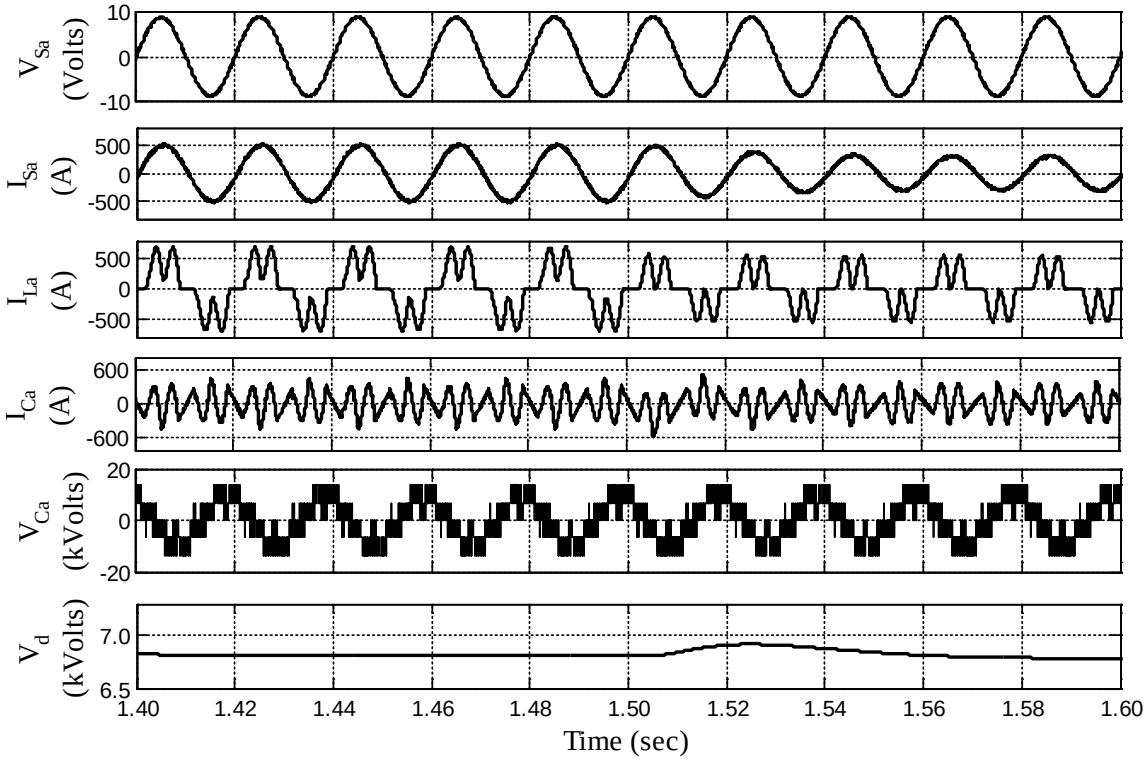


Figure 4.19 Transient performance of MLI based SAPF during load decrement with R-C loading condition

Table 4.3 Comparative analysis of conventional and proposed control algorithm

Parameters Considered	Conventional Control Algorithm [123], [124]		Proposed Control Algorithm			
			With ideal PR		With practical PR	
With diode bridge rectifier and R-L loading						
THD of source current (%)	Before	After	Before	After	Before	After
	26.92	3.76	26.92	3.31	26.92	3.33
Power factor	Before	After	Before	After	Before	After
	0.9	0.97	0.9	0.997	0.9	0.997
Steady-state source current magnitude error (%)	6.71		Nil		Nil	
With diode bridge rectifier and R-C loading						
THD of source current (%)	Before	After	Before	After	Before	After
	48.16	3.58	99.7	3.24	99.7	3.28
Power factor	Before	After	Before	After	Before	After
	0.9	0.96	0.9	0.9958	0.9	0.996
Steady-state source current magnitude error (%)	10.85		Nil		Nil	

4.6 HARDWARE IMPLEMENTATION OF PROPOSED CONTROL USING dSPACE 1104

Prototype of single-phase five-level CHB-MLI based SAPF system is designed at laboratory scale level due to laboratory constraints. The power circuit used for laboratory prototype is shown in Figure 3.1. Advanced control technique applied for three-phase system has been modified for application in single-phase MLI based SAPF system due to some limitations in real-time controller during hardware implementation. Single-phase SRF theory [11] based control technique is used for reference current generation due to its effectiveness and better performance in SAPF system. The measured load current signals are transformed from 'abc' reference frame to synchronous reference frame ('dq') which is known as park's transformation. PLL continuously check the frequency of grid voltage end extract phase angle information which is required for Park's and Inverse Park's transformation. Two fictitious components of load current are i_α and i_β where i_β is delayed by 90^0 to i_α. A low-pass filter is used for fundamental current component extraction and harmonic current rejection. Loss component of the circuit is supplied by a dc-PI compensator for dc-link voltage regulation. The flow diagram of modified single-phase SRF control theory is shown in Figure 4.20. Reference signal is generated by comparing source and load current signal. This signal is compared with measured compensating current signal. Finally, error current signal is processed through stationary

frame PR controller. Further, PS-PWM generates pulses for IGBTs of CHB-MLI. This chapter mainly emphasises on the use of PR compensator in advanced control theory under different non-linear loading conditions.

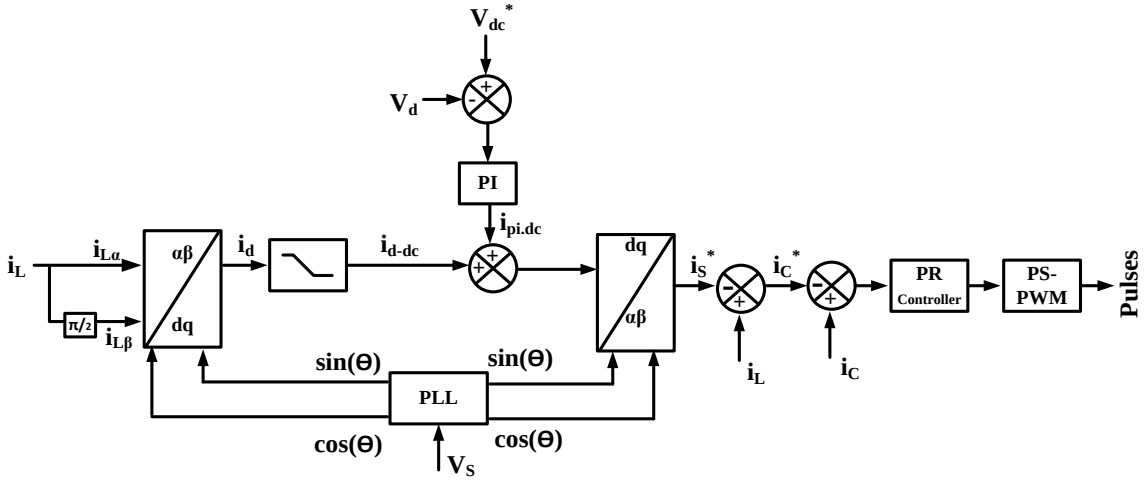


Figure 4.20 Proposed control theory for five-level single-phase CHB-MLI

Conventional and advanced current controller based algorithm is designed and executed in dSPACE 1104 real-time controller. Fixed frequency voltage supply is used for experimental analysis. H-bridge single-phase inverters are fabricated with IGBTs in the laboratory. IGBT STGW30NC120HD is used as power electronic switch which is capable of withstanding 1200V voltage and 30A of current during its operation. Two H-bridges are connected in series manner to make five-level cascaded H-Bridge. MUR460 is used as feedback diode with each IGBT in anti-parallel manner. Driver card is designed for isolation and amplification purpose. Gate pulses are provided to IGBT gate terminal through these driver cards for switching on and off of power electronic switches. The designed driver card is capable of providing delay as well as protection to the circuit. Combination of AND gate (7408) and NOT gate (7404) have been used to provide delay. Delay timing can be changed by the changing the value of resistance and capacitance. Opto-coupler TLP 250 is used to cater two major purposes namely pulse amplification and isolation between power and driver circuit. A high value of resistance between gate and emitter terminal in the driver card ensures rejection of unwanted turn-on. Pulse generated from dSPACE controller is fed to the driver circuit and +5V pulse is amplified to +15V and -5V as per the requirement of the IGBTs. Voltage and current sensors are used to measure source voltage, load current, source current and compensating current. LEM make LV 25-1000 and LA 25-NP are used as voltage and current sensors,

respectively. IC TL081 is used for signal conditioning and amplification and further these amplified signals are fed to ADC of dSPACE 1104 controller. Scaling and gain factors are calculated properly as it is important to restore voltage and current signals into its actual value. These feedback signals are processed through designed control algorithm and subsequently gate pulses are generated through PS-PWM switching technique as shown in Figure 4.21. A detailed laboratory prototype based analysis has been carried out. Hardware results of proposed topology are presented for the validation of the simulation results. Tektronix make 2014B DSO is used to analyze different voltage and current signals. The detailed laboratory prototype photograph of single-phase five-level CHB-MLI based SAPF is shown in Appendix-A.

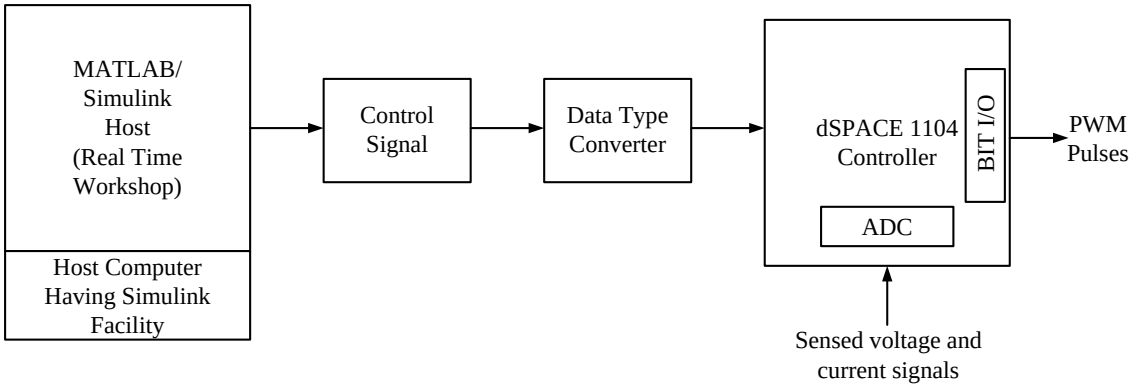


Figure 4.21 Block diagram of co-simulation between dSPACE 1104 and MATLAB

4.6.1 Uncontrolled Rectifier and R-L Loading

Steady-state MLI based SAPF waveforms (V_S, I_S, I_L, I_C, V_C and V_d) of the proposed system are depicted in Figure 4.22 (a) - (d). Figure 4.22 (a) shows waveform of sinusoidal V_S and non-linear I_S due to the presence of diode-bridge rectifier based resistive-inductive load into the existing system. Figure shows that source current is in phase with source voltage. Therefore, unity power factor at the source side is maintained. It is observed that there is significant reduction of phase error with advanced controller. Five-level inverter output is generated and shown in Figure 4.22 (b). Figure 4.22 (c) shows V_S, I_S, I_L, I_C, and V_d waveform during the steady-state operation of MLI based SAPF unit. Inverter output voltage is also plotted for the sake of explanation of converter operation. Effectiveness of the proposed control algorithm is also tested under load

changing conditions. Figure 4.22 (d) shows that dc-link voltage of capacitor is constant during the steady-state operation of inverter.

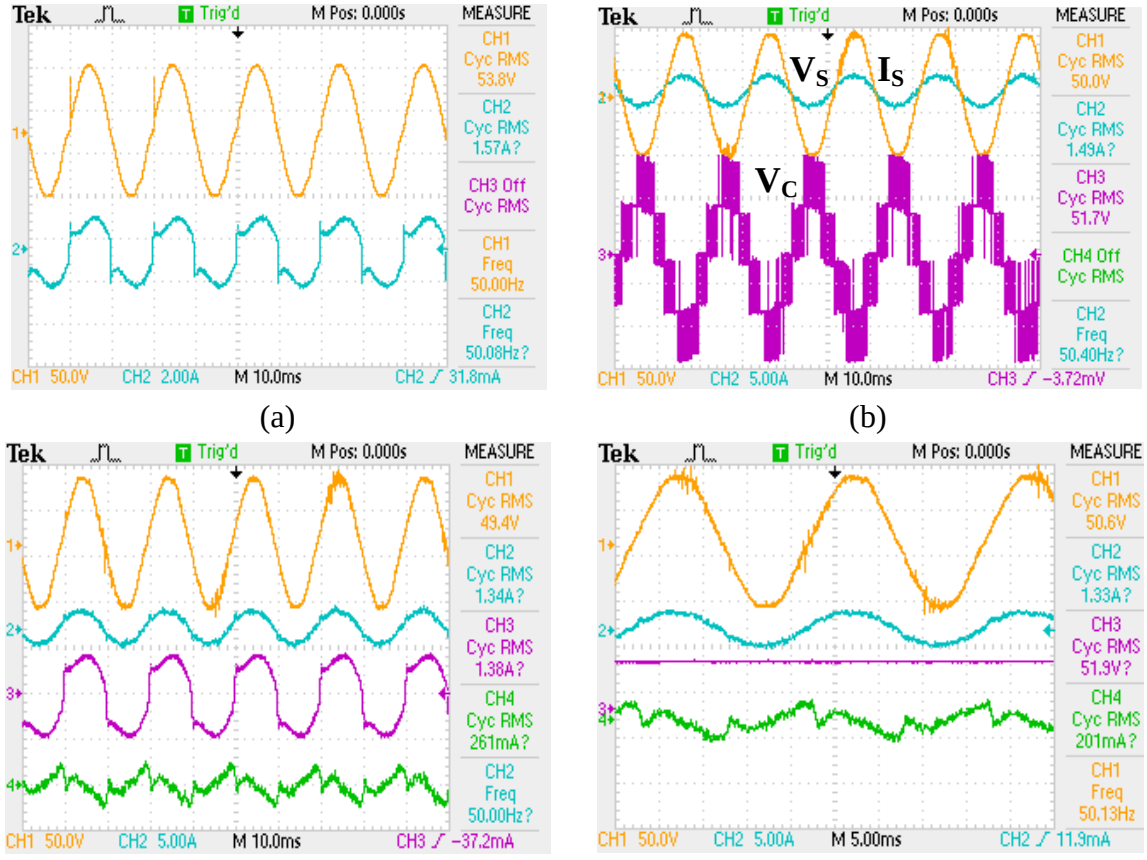
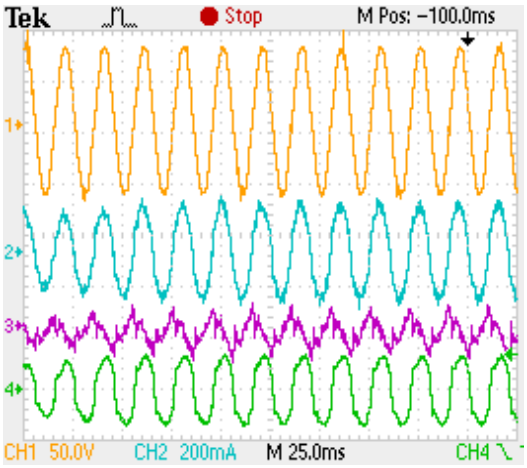


Figure 4.22 Experimental waveforms of CHB-MLI based SAPF with proposed controller under R-L loading (a) V_S and non-linear source current (I_S) (CH1: 50 V/ div., CH2: 5 A/ div.), (b) MLI voltage waveform with source voltage (CH1: 50 V/ div., CH2: 5 A/ div., CH3: 50 V/ div.), (c) V_S, I_S, I_L, I_C waveform in steady-state (CH1: 50 V/ div., CH2: 5 A/ div., CH3: 2 A/ div., CH4: 2A/div.), and (d) V_S, I_S, V_d, I_C waveform (CH1: 50V/div., CH2: 5 A/ div., CH3: 50 V/ div., CH4: 2A/ div.)

Figure 4.23 (a) shows the change in magnitude of source current and source voltage waveforms with step-increase in loading. It can be depicted from figure that source current and compensating current transition is smooth. Load is decreased after some time and the waveform of V_S, I_S, I_C and I_L is depicted in Figure 4.23 (b). Load current is varied from 1 A to 2 A. Source current still remains sinusoidal even with the load changing condition. Source current transition is smooth in case of load decrement. Both the figures ensure the effectiveness of the proposed algorithm in load changing conditions with R-L type of non-linear loading.



(a)

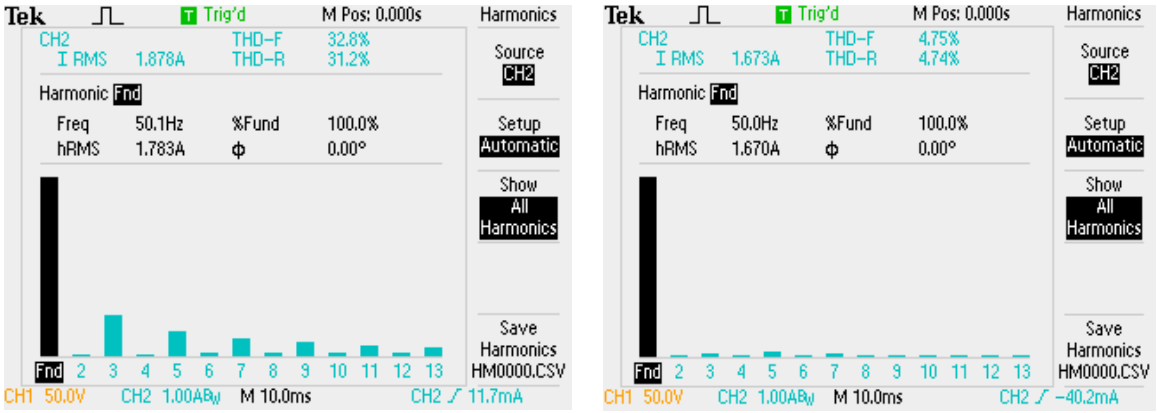
(b)

Figure 4.23 Experimental waveforms of CHB-MLI based SAPF with proposed controller under R-L loading (a) V_S, I_S, I_L, I_C waveform with step-increment of loading, and (b) V_S, I_S, I_L, I_C waveform with step-decrement of loading (CH1: 50V/div., CH2: 200 mA/div.)

Source current THD due to non-linear loading is 32.6% as shown in Figure 4.24 (a). THD of source current becomes 4.74% as shown from Figure 4.24 (b). Source current THD is well under the defined international standards after the successful operation of SAPF unit. The proposed control applied to CHB-MLI gives satisfactory performance under steady-state and transient condition and measured percentage THD value is also as per IEEE defined international standard.

4.6.2 Uncontrolled Rectifier and R-C Loading

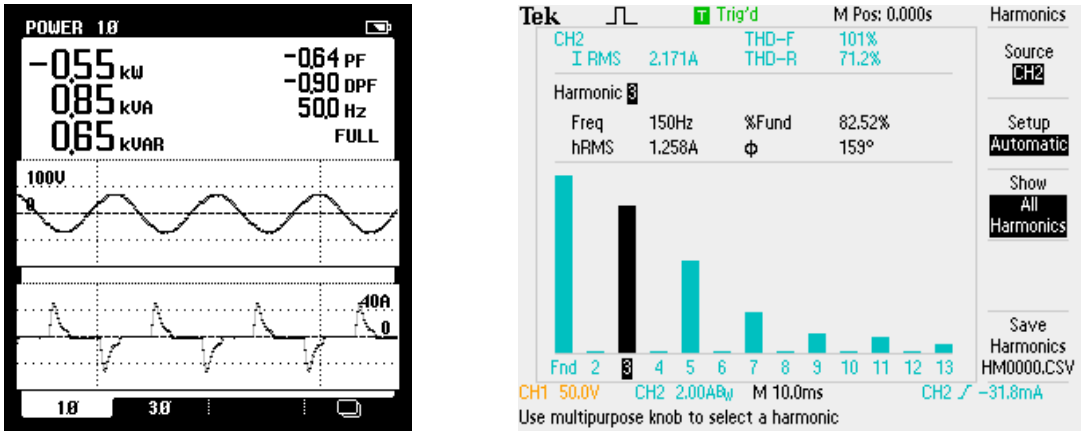
Effectiveness of the proposed control algorithm not only tested with R-L type of non-linear loading, it is also tested with diode-bridge rectifier and R-C loading conditions.



(a) (b)

Figure 4.24 THD of source current with R-L loading (a) before compensation, and (b) after compensation

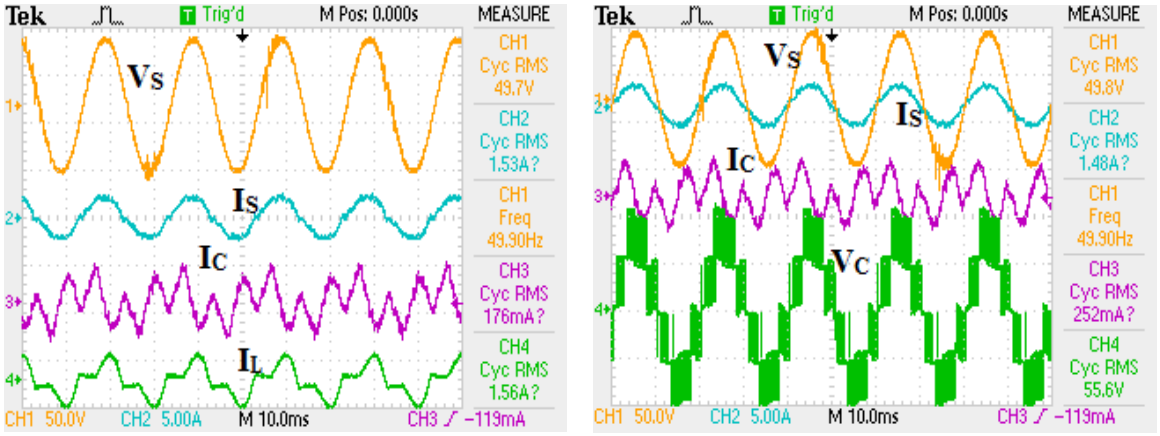
Figure 4.25 (a) shows the waveform of sinusoidal source voltage and non-linear source current which is due to R-C type of loading. THD of non-linear source current is 101% as shown in Figure 4.25 (b).



(a) (b)

Figure 4.25 Performance of five-level CHB-MLI based SAPF with R-C loading (a) V_S and non-linear I_S, and (b) THD of I_S before SAPF operation

MLI based SAPF is switched on and performance of the proposed controller under steady-state condition is shown in Figure 4.26 (a) - (b). Source-voltage, source-current, compensating current, load current are shown for the sake of explanation. It can be shown from the figure that MLI unit supplies compensating current successfully in order to make source current wave shape sinusoidal even though load current is still rich in harmonic content. Figure 4.25 (b) shows that source current is in phase with source voltage which ensures unity power factor operation.



(a) (b)

Figure 4.26 (a) V_S, I_S, I_L and I_C during steady-state condition, and (b) V_S, I_S, I_C and MLI output waveform with R-C loading (CH1: 50V/div, CH2: 5 A/ div., CH3: 5 A/div.)

THD of source current becomes 3.93% from 101% after successful operation of MLI based SAPF unit as shown in Figure 4.27, which is maintained according to IEEE-519 standard.

Figure 4.27 THD of I_S after SAPF operation with R-C loading

Controller effectiveness of the proposed controller is again compared with the conventional controller [8, 9] based SAPF system with resistive-capacitive loading condition. The detailed comparative analysis between these two controllers is shown in Table 4.4. Table shows comparative analysis between traditional and proposed control theories. Table depicts improvement in the power factor of source side from 0.90 to 0.95 with conventional controller whereas power factor improves up to 0.984 with proposed controller. The THD in current waveform of proposed controller are shown in Figure 4.23 (d) and 4.27 for proving the effectiveness of the proposed controller over conventional one. The detailed experimental analysis demonstrates that the advanced

current controller can generate current with better quality compared to conventional current controller. Therefore, proposed controller shows excellent performance over conventional controller in case of filtering application.

Table 4.4 Comparative analysis of conventional and proposed control algorithm in Hardware

	Conventional Control [123]	Proposed Control
with R-L loading		
Power factor after compensation	0.95	0.977
THD after compensation	4.98	4.75
with R-C loading		
Power factor after compensation	0.952	0.973
THD after compensation	4.52	3.93

4.7 CONCLUSION

A five-level CHB-MLI based SAPF with modified synchronous reference frame control theory composed of PR compensator in current control loop has been simulated and experimentally verified for current harmonics elimination and reactive power compensation under non-linear loading environment. Output current waveform can be improved by providing zero magnitude and phase error in steady state condition through PR regulator based advanced controller. A complete mathematical analysis of stationary frame PR controller has been developed and selection of constant parameters has been carried out using bode-plot technique. The transfer function approach has been used to check the stability of closed-loop control system comprising PR compensator based advanced current controller. Stability of entire system is analyzed and also checked using R-H criteria. Finally, a detailed mathematical model shows the change in system characteristics with the variation of grid impedance. A diverse range of simulations has been carried out under different loading conditions. Results obtained from simulation prove that the proposed control technique is effective and gives better performance than the conventional control in both steady-state and transient conditions for mitigating current related PQ problems. A laboratory prototype is also developed and tested to validate the simulation results using dSPACE 1104 controller. The proposed advanced controller has shown its effectiveness in terms of AC current tracking error reduction and efficient current harmonics elimination in MLI based filtering applications.

CHAPTER 5

PSO ASSISTED PI- VECTOR-PROPORTIONAL-INTEGRAL (PI-VPI) COMPENSATOR BASED CONTROL STRATEGY

List of Publications

1. **S. Ray**, N. Gupta, R. A. Gupta, "Cascaded vector resonant controller based novel active filtering using multilevel inverter based shunt active power filter," *Journal of Electric Systems*. **(In Press)**
2. **S. Ray**, N. Gupta, R. A. Gupta, "Comparative Analysis of Conventional and Modified Peak-detection Based Control Technique for Cascaded H-Bridge Multilevel Inverter based Shunt Active Power Filter," in Proc. *of IEEE International Conference on Innovations in Power and Advanced Computing Technologies (i-PACT2017)*, Apr. 2017, Vellore, pp. 1-6.

CHAPTER 5

PSO ASSISTED PI- VECTOR- PROPORTIONAL-INTEGRAL (PI-VPI) COMPENSATOR BASED CONTROL STRATEGY

[CHB-MLI based SAPF is an efficient solution for mitigating harmonic component from source current in case of medium-voltage distribution system. Source current wave shape mainly depends on the accuracy of current control loop in closed-loop control algorithm applied to CHB-MLI based SAPF. Normally, proportional-integral (PI) or resonant compensators are used in current control loop for shaping source current wave shape. However, PI compensator is having problem associated with steady-state error and resonant compensators have limitations during real-time applications. Therefore, this chapter presents PI-vector-proportional-integral (VPI) compensator based current control strategy for CHB-MLI based SAPF in order to nullify steady-state source current error. This controller shows excellent selective harmonic elimination capability thereby steady-state current error is nullified. Mostly, frequency selection based methods are used for selecting compensator gain parameters. But, this technique leads to deficits in accuracy. Therefore, particle-swarm optimization (PSO) technique is used for tuning the PI-VPI compensator gain parameters in order to fill the gap for proper tuning methodology of compensator gains. PSO approach operates with a cost function by minimizing source current total harmonic distortion and steady-state error of current control loop. Double frequency ripple minimization-3φ-power PLL (DFRM-3φ-pPLL) is also proposed for proper phase angle measurement in order to remove error present due to double frequency. Detailed simulated and experimental analysis of proposed system shows effectiveness of projected controller over conventional current controller.]

5.1 INTRODUCTION

Control algorithms of SAPF are responsible for maintaining the wave-shape of source current in steady-state as well as in transient conditions. Many control algorithms for SAPF are already available in literature which gives better performance compared to conventional control algorithms. SAPF control algorithms are mainly comprises of two control loops i.e. dc-link voltage control loop and current control loop. Some amount of energy need to be supplied by the inverter unit in order to maintain dc-link voltage. This energy is required in order to supply active component related to inverter switching losses and other passive component losses. Current control loop adjusts the amount of current need to be injected which indirectly decides the wave shape of source current.

Therefore, current control loop plays major role in SAPF control algorithm for deciding sinusoidal source current wave shape. Hysteresis current controller is commonly used in literature for two-level inverter control. However, change in switching frequency causes problem for selection of power electronic switches in case of multilevel inverters and therefore PWM techniques are normally used for MLIs. M. Waware et al. [123] have used PI compensator in current control loop due to its advantages like easy tuning procedure, and simpler structure. Current control loop comprises of non continuous reference current and a high gain parameter needs to be incorporated in order to ensure proper operation. This high gain indirectly affects the stability of the system. PI compensator also has limitation like presence of steady-state magnitude and phase error while following sinusoidal reference current waveform. Proportional-resonant (PR) compensators are used by researchers in order to nullify the disadvantages associated with PI compensators in current control loop. PR compensators are able to provide infinite gain at selected resonant frequency. Therefore, selected harmonic components from current control loop can be eliminated. This feature makes PR compensator a better solution for SAPF applications. However, use of PR compensator in current control loop causes reduction in stability margin of the system and it is also responsible to create undesired peaks during real-time applications [173]. Therefore, PI-vector proportional-resonant (VPI) compensator based current controller is designed in order to maintain superior SAPF performance during its operation. This compensator is able to mitigate high-frequency components from current control loop and therefore, source current of sinusoidal wave shape is obtained in case of SAPF operations. PI-VPI though produces superior performance but it involves a lot of parameters which need to be tuned properly.

Therefore, one of the tricky tasks is tuning of constant parameters while using PI-VPI compensators in current control loop. Optimal tuning of large number of constant parameters is also important in order to maintain better steady-state current waveform. Thus, researchers face a great challenge for tuning of constant parameters in case of PI-VPI compensator while a large of parameter selection is necessary for selective harmonic component rejection. Most of the researchers have used trial and error method in order to simplify the tuning procedure [179, 181, 182]. A novel approach composed of nyquist criteria and sensitivity function is applied to PI-VPI compensator. Frequency response

based trial and error method is considered by Trinh et al. [183]. However, this method gives approximate solution for tuning of parameters. Fukuda et al. [175] have proposed PI-multi resonant compensator for current control loop in case of single-phase SAPF. However, an appropriate tuning procedure of compensator parameter is not discussed. Most of literatures have not presented a prominent method to tune the constant parameters of PI-VPI compensator.

Therefore, this chapter first present a novel PI-VPI compensator based current controller for CHB-MLI based SAPF application. Furthermore, this chapter also deals with a systematic methodology for tuning PI-VPI compensator parameters using particle swarm optimization (PSO) technique. PSO is becoming an automatic choice for researchers in current scenario because of advantages like quick convergence to best solution, and simpler implementation procedure [178]. This proposed methodology is consisted of three main steps i.e. tuning of PI compensator constant parameters using bode-plot technique, followed by tuning of VPI compensator constant parameters using frequency response method. Finally, PSO optimization has been used for fine tuning of these parameters by minimizing source current steady-state error and source current THD in case of MLI based SAPF applications.

Thus, PI-VPI compensator based current controller for CHB-MLI based SAPF application is discussed in detail in this chapter. An effective methodology has been also proposed for tuning constant parameters of PI-VPI compensator applied to CHB-MLI based SAPF which is also one of the main contributions of this chapter. Furthermore, usefulness of the proposed control technique applied to MLI based SAPF is tested with simulation study. Hardware results also confirm the effectiveness of the proposed controller over conventional control. A comparative analysis is also presented among optimally designed PI-VPI compensator based SAPF with PI compensator based controller in order to justify the usefulness of optimally tuned PI-VPI compensator based controller.

5.2 PROPOSED FIVE-LEVEL CHB-MLI BASED SAPF SYSTEM

H-bridge inverter generates two levels of voltage at the output terminal. Higher number of levels can be created by combining single-phase H-bridge inverters in

cascaded manner. As number of H-bridges increase, output voltage turns to almost sinusoidal. Simultaneously, at output side, total harmonic distortion (THD) of voltage waveform gets reduced. Different number of voltage levels can be created by applying different PWM techniques. Five level CHB-MLI has been used in this chapter as a SAPF unit. Normally, different isolated DC sources are required for different H-bridges. But, in case of SAPF applications, active sources are not required. Therefore, only capacitors of equal magnitude can serve this purpose. No separate active source is required for this purpose. Five level CHB-MLI consists of two number of H-Bridges per phase. One H-bridge contains four number of power electronics switches like IGBTs. One leg contains of two IGBTs. Each IGBT of one leg is switching on such a manner that each switch can be complementary to each other. Combination of switches develop three number of voltage levels i.e. $+V_{dc}$, 0, and $-V_{dc}$ in case of H-bridge. As two numbers of H-bridges are used, five levels of voltages are created. CHB-MLI uses least number of power electronic devices among three multilevel inverters which reduces cost, size and space indirectly. Figure 5.1 shows five-level CHB-MLI based SAPF unit for distribution sector where non-linear loads are used. 11kV three-phase and three-wire system is used in simulation study where L_{Sa}, L_{Sb} and L_{Sc} are source impedance of three different phases, i_{Sa}, i_{Sb} and i_{Sc} are source current, i_{Ca}, i_{Cb} and i_{Cc} are compensating current and i_{La}, i_{Lb} and i_{Lc} are load currents. S1.1, S1.2, S1.3 and S1.4 are four switches of upper H-bridge inverter and S2.1, S2.2, S2.3 and S2.4 are four switches of lower H-bridges in ‘A’ phase. Switching is done in such a manner that switching pulses of S1.1 is complementary to switch S1.4, and switching pulses of S1.2 is complementary to switch S1.3. The same switching pattern is followed through all the H-bridges.

Five-level CHB-MLI based SAPF unit is connected in parallel manner with three-phase grid through interfacing inductor as shown in Figure 5.1. Diode-bridge rectifier with resistive-inductive load or resistive-capacitive type of loading is used as a non-linear load. Three-phase balanced source is considered for further study. The proposed control technique applied to five-level CHB-MLI based SAPF is shown in block diagram manner. DFRM-3φ-pPLL is used for proper phase-angle estimation and double-frequency component effect minimization. Synchronous reference frame (SRF) based theory is used for generating required current reference.

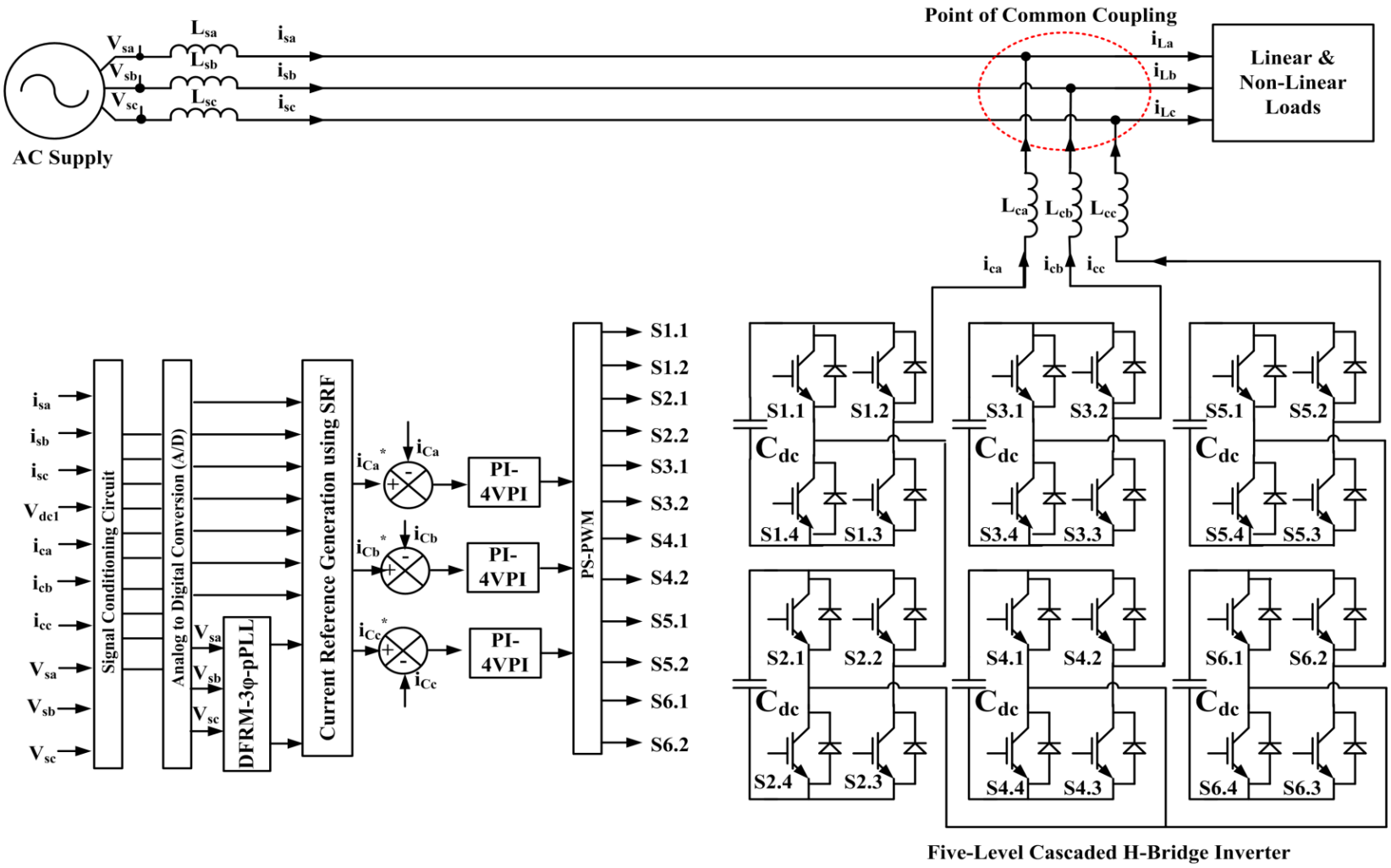


Figure 5.1 Implementation of five-level CHB-MLI based SAPF with proposed control algorithm

5.3 WORKING PRINCIPLE OF PROPORTIONAL INTEGRAL VECTOR PROPORTIONAL INTEGRAL (PI-VPI) COMPENSATOR

Normally, proportional or proportional-integral (PI) compensators are used in fundamental or natural reference frame for the purpose of current control. However, use of PI compensator has restrictions in natural reference frame as control bandwidth is limited. Therefore, PI controllers are not able to control higher frequency components i.e. harmonic component present in current control loop. As a consequence, SAPF may not able to achieve its desired performance by using conventional compensator in natural reference frame. Therefore, in order to achieve this goal, current control loop composed of current compensator must have harmonic component rejection capability. This is possible by providing higher gains at selected high frequency components. Current controller composed of multiple numbers of proportional-resonant (PR) compensators is capable to provide this action. Combination of PR compensators is connected in parallel manner such as each PR compensator can be able to provide higher gain at selected harmonic frequency. The transfer function of multiple PR compensators is depicted as Equation 5.1.

$$G_{M-PR} = \sum_{h=5,7,11,13} K_{ph} + \frac{2K_{rh}s}{s^2 + (h\omega)^2} \tag{5.1}$$

However, in order to regulate fundamental component of current reference along with rejection of harmonic component from current control loop, PI-multiple resonant (MR) is used by researchers [179]. The open-loop transfer function is mentioned as Equation 5.2.

$$G_{PI-MR} = K_{p1} + \frac{K_{i1}}{s} + \sum_{h=5,7,11,13} K_{ph} + \frac{2K_{rh}s}{s^2 + (h\omega)^2} \tag{5.2}$$

Nevertheless, delay-time introduced by hardware components and digital implementation procedure must be taken into consideration while considering system performance. A discretization method is adopted and an extra term is added to PI-MR compensator in order to nullify the effect of delay-time. Therefore, transfer function of discretized PI-MR compensator becomes as shown in Equation 5.3 where PI compensator takes care of fundamental component of reference current.

$$G_{PI-MR} = K_{p1} + \frac{K_{i1}}{s} + \sum_{h=5,7,11,13} K_{ph} + 2K_{rh}.\frac{s.\cos(h\omega_S NT_S) - h\omega_S \sin(h\omega_S NT_S)}{s^2 + (h\omega)^2} \quad (5.3)$$

Figure 5.2 shows bode-plot of open-loop transfer function of PI-MR compensator considering the effect of discretization. It can be depicted from figure that high gains present at unwanted high frequency components in open-loop scenario.

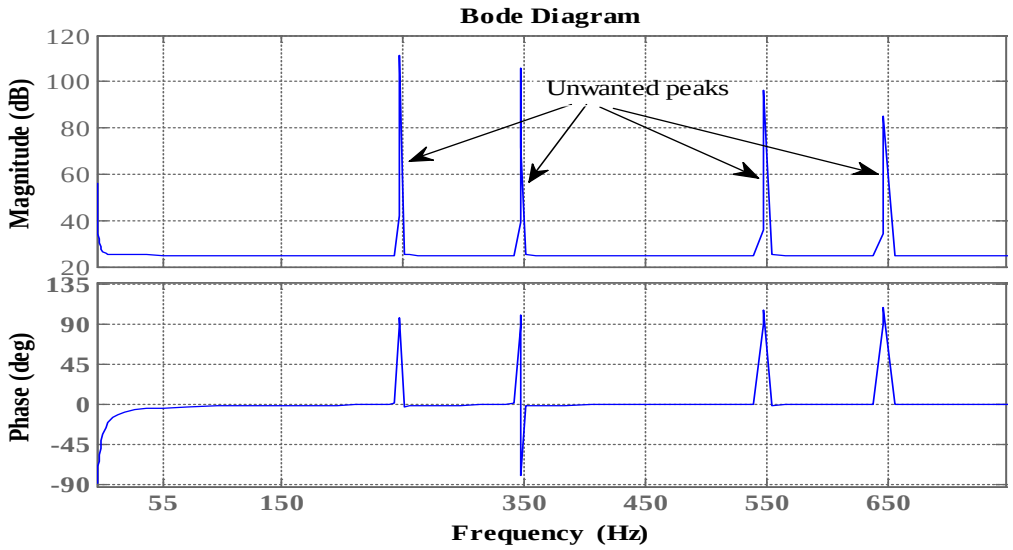


Figure 5.2 Bode-plot of PI-MR controller

However, method proposed in [181] only considers delay-time caused by digital implementation but ignores the effect of SAPF switching and other real-time components. If large number of harmonics needs to be mitigated from current control loop through this compensator, then high gains are appeared in undesired higher frequencies, and margin of stability is reduced [179]. In order to solve this problem, vector-proportional-integral (VPI) controller is proposed in literature [174]. The open-loop transfer function of VPI controller in 's' domain is shown as Equation 5.4.

$$G_{VPI} = \sum_{h=5,7,11,13} \frac{2K_{ph}s^2 + K_{rh}s}{s^2 + (h\omega)^2} \quad (5.4)$$

This compensator is capable to cancel coupling term by choosing resonant gain parameter as shown in Equation 5.5 [174]. Therefore, K_{rh} can be defined as

$$K_{rh} = K_{ph}R_f/L_f \quad (5.5)$$

This compensator is well capable to provide high gain at selected higher frequency even in real-time condition. VPI compensators provide superior performance

with respect to PI-MR compensators in terms of selective harmonic elimination criteria. Therefore, PI-VPI compensator is proposed by Q-N. Trinh et al. in [174] in order to provide regulation over fundamental component and to mitigate selective harmonic component from current control loop. PI-VPI compensator used for this chapter is shown in Figure 5.3. Transfer function of open-loop PI-VPI compensator is given in Equation 5.6.

$$G_{PI-VPI} = K_{p1} + \frac{K_{i1}}{s} + \sum_{h=1\ to\ n} \frac{2K_{ph}s^2 + K_{rh}s}{s^2 + (h\omega)^2} \tag{5.6}$$

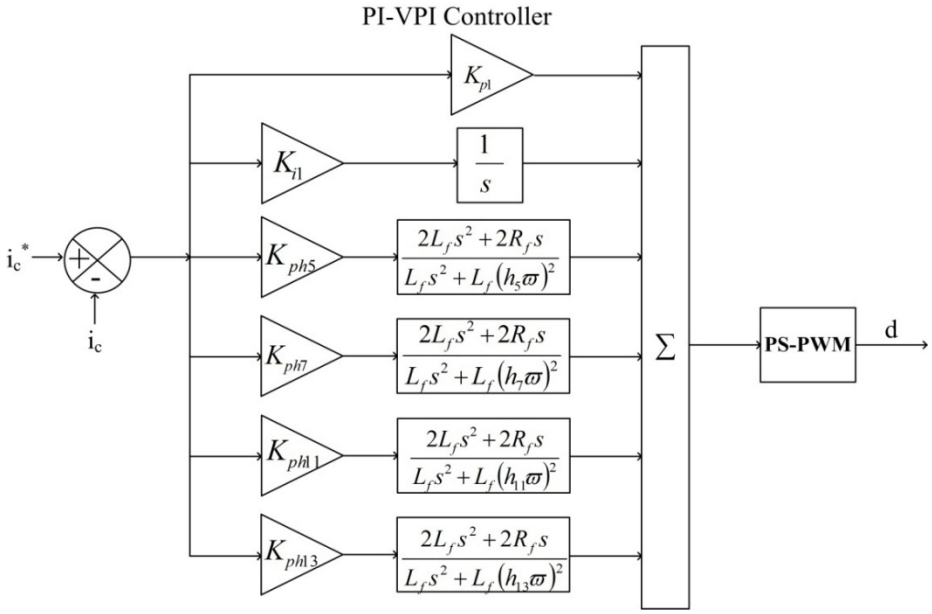


Figure 5.3 PI-VPI compensator applied to CHB-MLI based SAPF

Figure 5.4 depicts bode-plot of open-loop PI-VPI compensator transfer function as compared to bode-plot of open-loop transfer function of PI compensator. Figure shows higher gains present at selected 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic frequency whereas PI compensator gain reduces with higher frequency terms. Figure clearly shows superior performance of PI-VPI compensator over conventional PI compensator in terms of higher gain at higher frequency. Therefore, it can be shown form figure that, PI-VPI compensator provides very high gain at selected higher frequency. This feature also ensures zero amount of steady-state error while compensating non-sinusoidal current. This phenomenon is possible with pole-zero cancellation potential with filter inductor when $K_{rh} = K_{ph}R_f/L_f$.

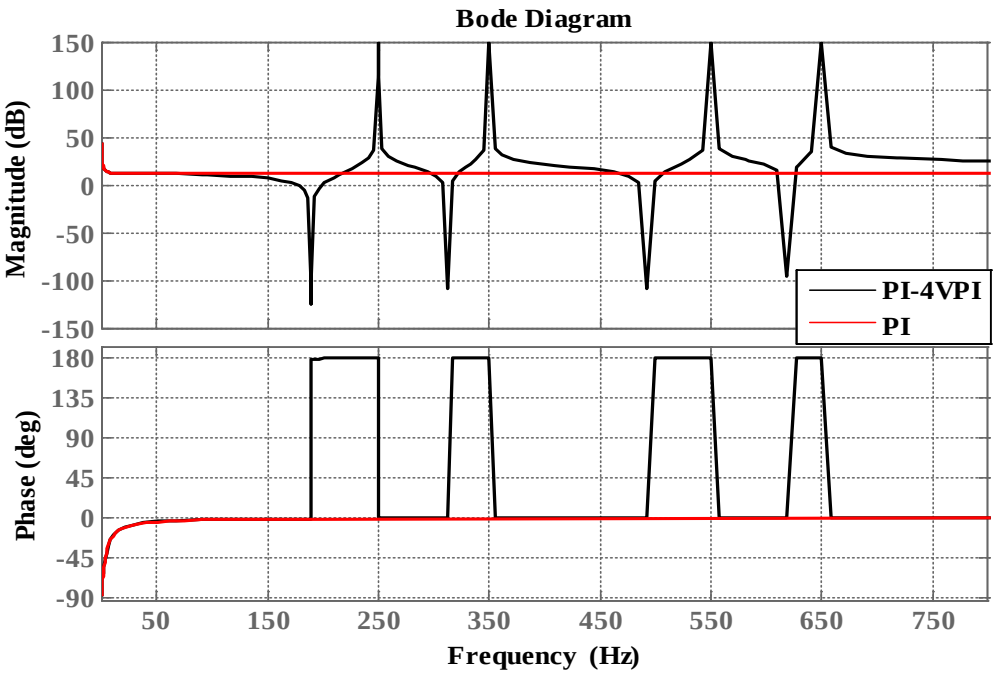


Figure 5.4 Open-loop response of PI-VPI compensator with respect to PI compensator

Open-loop transfer function of PI-VPI compensator for single harmonic component is shown as Equation 5.7.

$$G_{PI-VPI} = K_{p1} + \frac{K_{i1}}{s} + \frac{2K_{ph}s^2 + K_{rh}s}{s^2 + (h\omega)^2} \tag{5.7}$$

Therefore, by putting values of K_{rh} from Equation 5.5 to Equation 5.7 and Equation 5.7 can be written as Equation 5.8. Open-loop transfer function of PI-VPI compensator becomes

$$G_{PI-VPI} = K_{p1} + \frac{K_{i1}}{s} + \frac{2K_{ph}L_f s^2 + 2K_{ph}R_f s}{L_f s^2 + L_f(h\omega)^2} \tag{5.8}$$

Equation 5.8 can be rearranged as Equation 5.9.

$$G_{PI-VPI} = \frac{K_{p1}L_f s^3 + K_{p1}L_f(h\omega)^2 s + K_{i1}L_f s^2 + K_{i1}L_f(h\omega)^2 + 2K_{ph}L_f s^2 + 2K_{ph}R_f s}{L_f s^3 + L_f(h\omega)^2 s} \tag{5.9}$$

Finally, Equation 5.9 can be rearranged as per Equation 5.10. This equation shows open-loop transfer function of PI-VPI compensator for single harmonic component rejection.

$$G_{PI-VPI} = \frac{K_{p1}L_f s^3 + (K_{i1}L_f + 2K_{ph}L_f)s^2 + [K_{p1}L_f(h\omega)^2 + 2K_{ph}R_f]s + L_f K_{i1}(h\omega)^2}{L_f s^3 + L_f(h\omega)^2 s} \tag{5.10}$$

However, in this work, PI-VPI compensator is considered for rejecting 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonic components. PI-VPI compensator for these harmonic components rejection is written as Equation 5.11.

$$G_{PI-VPI} = K_{p1} + \frac{K_{i1}}{s} + \sum_{h=5,7,11,13} \frac{2K_{ph}s^2 + K_{rh}s}{s^2 + (h\omega)^2} \tag{5.11}$$

5.4 IMPROVED CLOSED-LOOP CONTROL SCHEME FOR ACTIVE FILTERING

Improved closed loop control scheme for CHB-MLI based SAPF consists of mainly two control loops i.e. current control loop and DC-link voltage control. Current control loop shapes source current with proper magnitude and phase angle, while, DC-link voltage control loop supplies the required active power in order to maintain proper SAPF operation. Figure 5.1 shows the complete control in block diagram manner which is applied to five-level CHB-MLI based SAPF.

5.4.1 Current Reference Generation Technique

Load current components are sensed through current sensors and transformed to alpha-beta component (rotating frame) with the help of Clark's transformation as shown in Equation 4.14. Rotating frame components of load currents are further transformed to synchronous reference frame with the help of park's transformation which can be shown from Equation 4.15.

Phase locked loop (PLL) performs matching of frequency with existing grid and it supplies phase information which is required for park's and inverse park's transformation. In this chapter, proposed DFRM-3φ-pPLL is used for proper phase angle information extraction from three-phase sensed grid voltage. Generated double-frequency component degrades PLL and system performance. Therefore, double frequency component need to be removed from PLL. The proposed DFRM-3φ-pPLL is able to cancel double frequency component which is described in the next sub-section.

Loss component is contributed by DC-link voltage regulation which is done by PI controller. The diagram of SRF theory based control is shown in Figure 5.5. Reference

source current signal is generated in the final stage of the algorithm according to Equation 4.18 and PS-PWM generates required gate pulses. Both oscillatory and fundamental component of load current signals are present in this d-q-0 system. Low pass filter of cut-off frequency 10 Hz. is used for extracting DC quantity from these d axis and q axis signals. As, system is balanced one, zero component is not considered for further calculation. DC-link voltage of capacitor is sensed by voltage sensor and it is compared with reference value of dc-link voltage. Error of voltage signal is traditionally passed through PI compensator and finally this component is added with i_{Ld-dc}. Finally, reference source current is converted back to d-q-0 frame to alpha-beta frame first with the help of inverse park transformation as per Equation 4.17 and alpha-beta to a-b-c component with the help of Equation 4.18. This reference current component is compared with sensed source current signal and error signal is compared with triangular signal with the help of phase-shifted pulse width modulation technique. Generated gate pulses are used for triggering IGBTs of CHB-MLI. The flow-diagram of total closed-loop control theory is depicted in Figure 5.1 and reference current computation technique is shown in Figure 5.5. Finally, error current signal is processed through PI-VPI controller. Further, PS-PWM generates pulses for IGBTs of CHB-MLI. This chapter mainly emphasises on the use of PI-VPI compensator in advanced control theory under different non-linear loading conditions.

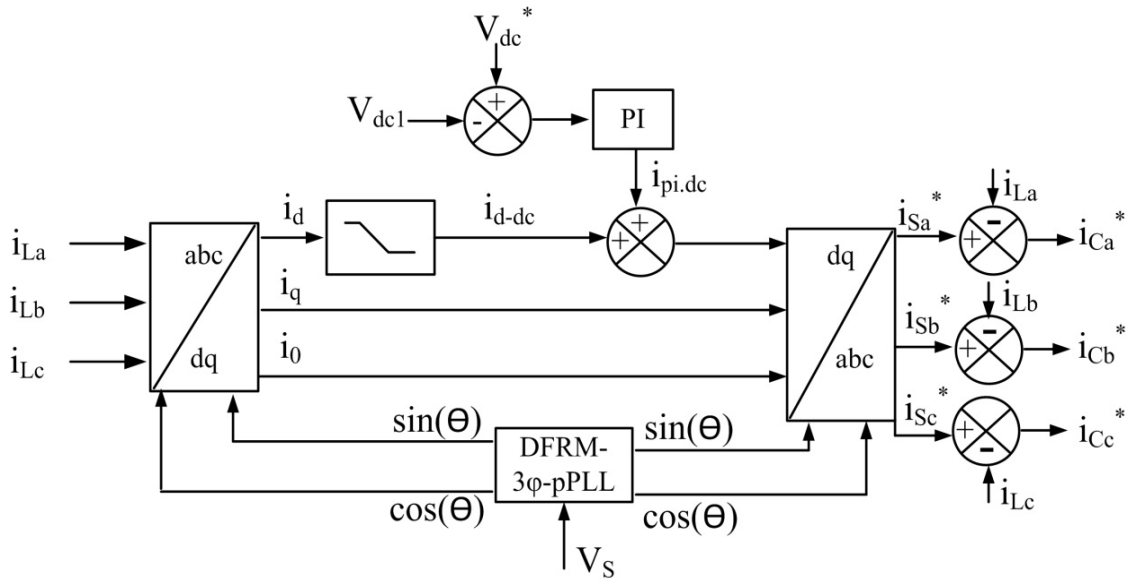


Figure 5.5 Current reference generation technique with proposed DFRM-three-phase-pPLL

5.4.2 Closed-loop Performance of PI-VPI Compensator based Current Controller

Closed-loop control algorithm stability analysis is an important concern while applying modified control algorithm to CHB-MLI based SAPF. Therefore, in this subsection, detailed closed-loop analysis of proposed controller which is composed of PI-VPI compensator based current controller is performed. Figure 5.6 shows closed-loop control technique of proposed control technique applied CHB-MLI based SAPF composed of PI-VPI compensator based current control technique.

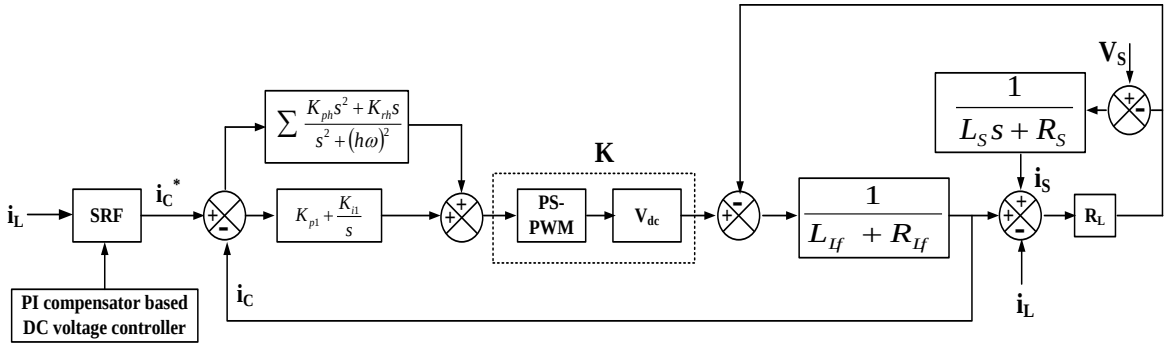


Figure 5.6 Closed-loop control of proposed SAPF control technique

This sub-section shows detailed closed loop transfer function analysis. Closed-loop transfer function of the proposed controller is depicted in Equation 5.12.

$$G_{CL.PI-4VPI} = \sum_{h=5,7,11,13} \frac{N_{74}s^4 + N_{73}s^3 + N_{72}s^2 + N_{71}s^1 + N_{70}s^0}{D_{75}s^5 + D_{74}s^4 + D_{73}s^3 + D_{72}s^2 + D_{71}s^1 + D_{70}s^0} \qquad (5.12)$$

where,

$N_{74} = {L_f}^2 R_L;$

$N_{73} = R_f R_L L_f;$

$N_{72} = R_L {L_f}^2 (h\omega)^2;$

$N_{71} = R_L R_f L_f (h\omega)^2$

$D_{75} = {L_f}^2 L_S;$

$D_{74} = L_f R_f L_S + R_L L_f L_S + KK_{p1} L_f L_S + 2\left(R_S {L_f}^2 + R_L {L_f}^2\right);$

$D_{73} = L_S {L_f}^2 (h\omega)^2 + KK_i L_f L_S + 2KK_{ph} L_f L_S + L_f R_f R_S + R_L L_f R_S + R_L L_f R_f + KK_{p1} L_f R_S + KK_{p1} R_L L_f;$

$$D_{72} = R_f L_f L_S (h\omega)^2 + R_L L_f L_S (h\omega)^2 + KK_{p1} L_f L_S (h\omega)^2 + 2KK_{ph} R_f L_S + R_L (h\omega)^2 {L_f}^2 + KK_{i1} R_S L_f + KK_{i1} L_f R_L + 2KK_{ph} L_f R_S + 2KK_{ph} L_f R_S;$$

$$D_{71} = KK_{i1} L_f L_S (h\omega)^2 + R_f L_f R_S (h\omega)^2 + R_f L_f R_S (h\omega)^2 + KK_{p1} L_f R_S (h\omega)^2 + 2KK_{ph} R_f R_S + R_f L_f R_L (h\omega)^2 + KK_{p1} L_f R_S R_L (h\omega)^2 + 2KK_{ph} R_S R_f R_L;$$

$$D_{70} = KK_{i1} L_f R_S (h\omega)^2 + KK_{i1} L_f R_L (h\omega)^2$$

Closed-loop transfer function of proposed CHB-MLI based SAPF control scheme is finally depicted as Equation 5.13 after simplification as $R_L \to \infty$.

$$G_{CL.PI-4VPI} = \sum_{h=5,7,11,13} \frac{{L_f}^2 s^4 + L_f R_f s^3 + {L_f}^2 (h\omega)^2 s^2 + R_f L_f (h\omega)^2 s}{D_{65} s^5 + D_{64} s^4 + D_{63} s^3 + D_{62} s^2 + D_{61} s^1 + D_{60} s^0} \qquad (5.13)$$

where,

$$N_{64} = {L_f}^2;$$

$$N_{63} = L_f R_f;$$

$$N_{62} = {L_f}^2 (h\omega)^2;$$

$$N_{61} = R_f L_f (h\omega)^2;$$

$$D_{65} = \left({L_f}^2 + L_S L_f\right);$$

$$D_{64} = \left(KK_{p1} L_f + L_f R_f + R_S L_f\right);$$

$$D_{63} = \left[L_S L_f (h\omega)^2 + {L_f}^2 (h\omega)^2 + KK_{i1} L_f + 2KK_{ph} L_f\right];$$

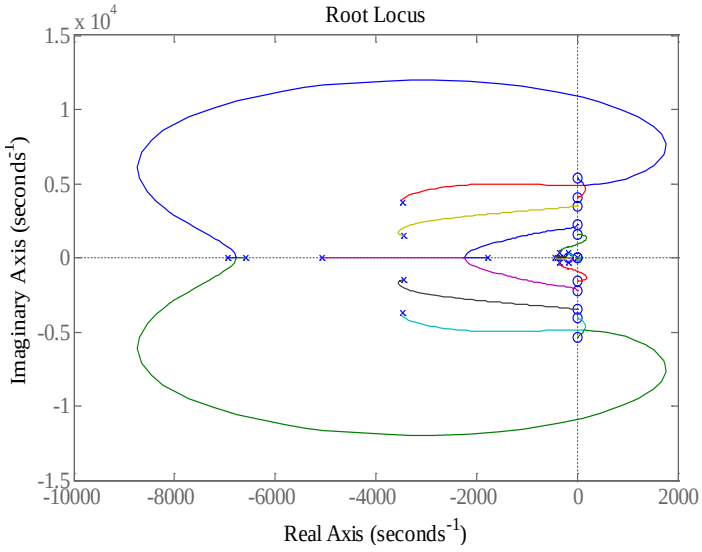
$$D_{62} = \left({L_f}^2 + L_S L_f\right);$$

$$D_{61} = \left[R_S L_f (h\omega)^2 + R_f L_f (h\omega)^2 + KK_{p1} L_f R_S (h\omega)^2 + 2KK_{ph} R_f R_S\right];$$

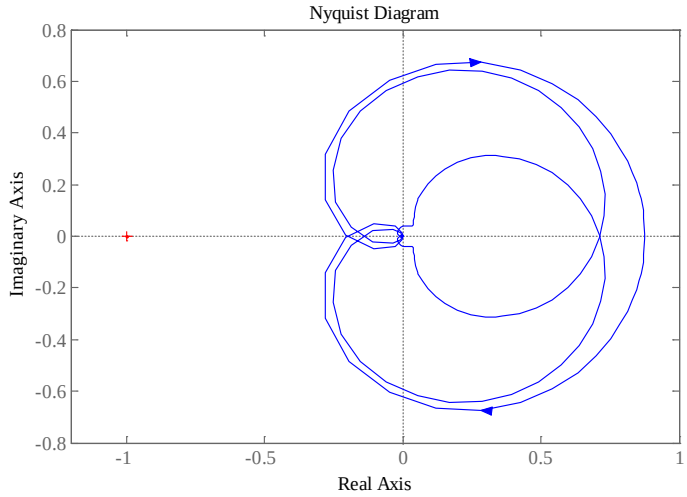
$$D_{60} = KK_{i1} L_f (h\omega)^2$$

Stability of the proposed closed-loop controller needs to be checked thoroughly. Therefore, root-locus analysis is considered as an effective technique for checking system closed-loop stability. It can be depicted from Figure 5.7 (a) that all poles lie in the left-hand side of imaginary axis. Root-locus diagram shows that closed-loop system is

perfectly stable. Nyquist plots, as shown in Figure 5.7 (b), also confirms the same as no encirclement is present around (-1, 0) point.



(a)



(b)

Figure 5.7 (a) Root-locus plot of closed-loop transfer function and (b) nyquist plot of closed-loop transfer function

Figure 5.8 shows bode-diagram of proposed closed-loop current controller composed of PI-VPI compensator. The figure shows that proposed current controller is able to provide unity gain at fundamental frequency and at the same point of time rejection of higher frequency component from existing signal. Selected resonance frequencies i.e. 250, 350, 550 and 650 Hz components are successfully eliminated from existing signal. This phenomenon leads to zero amount of steady-state error in reference

signal. Figure 5.9 shows impact of gain parameter selection in closed-loop operation of proposed current controller.

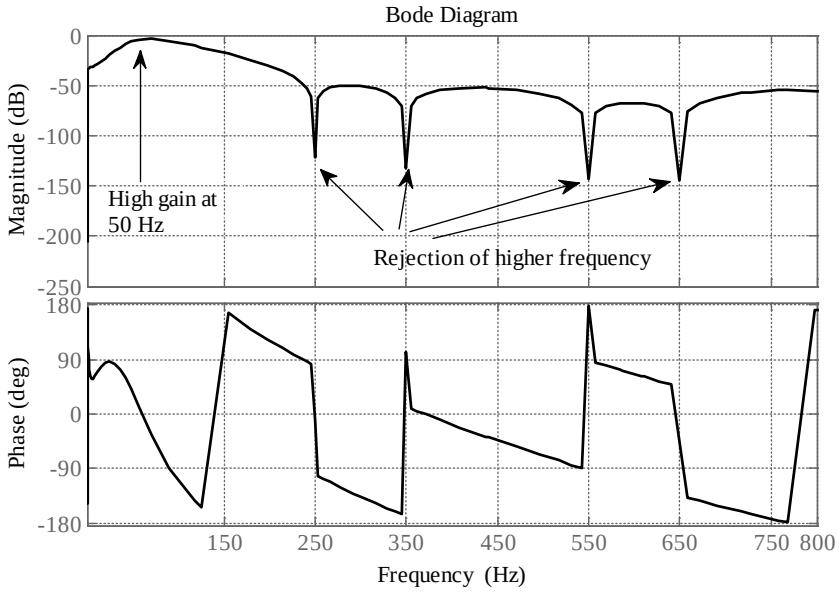


Figure 5.8 Bode-plot of closed-loop proposed controller transfer function

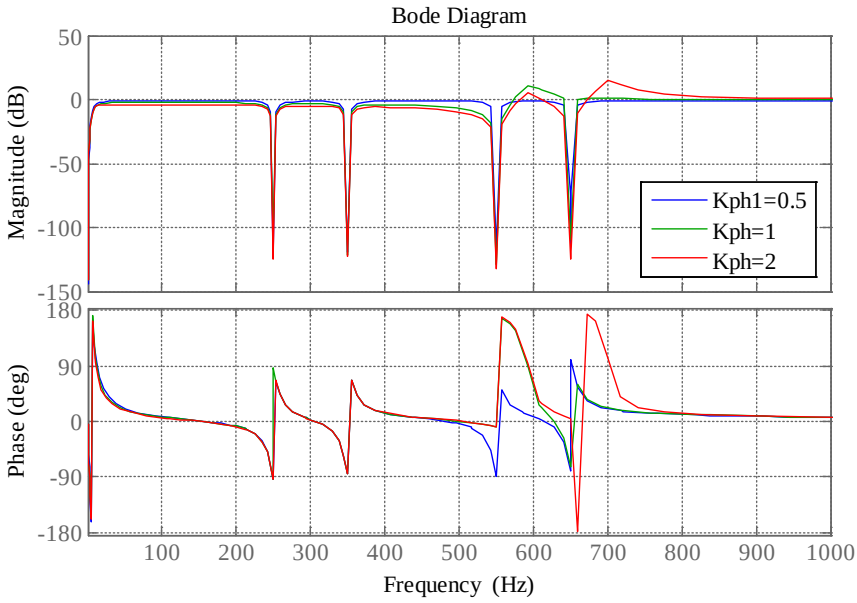


Figure 5.9 Bode-plot of closed-loop proposed controller transfer function with variation of gain parameters

Performance of current controller needs to be checked with variation of controller parameter K_{ph} as this parameter is a deciding factor of SAPF system performance. Selectivity of harmonic compensation increases with a smaller value of K_{ph} but dynamic response of the system reduces drastically. In contrast, system dynamic performance

improves with larger value of K_{ph} but at the cost of steady-state system performance degradation. Therefore, gain parameters need to select in such a way that steady-state performance should satisfy the main criteria and dynamic stability should not be compromised at the same time. Figure shows bode-plot of close-loop control with different K_{ph} values. It can be depicted from figure that controller is able to provide satisfactory performance in terms of harmonic component rejection with change of gain parameter.

As shown in this chapter, gain parameters for PI-VPI compensator are selected on the basis of $K_{rh}=K_{ph}/L_f$. It can be seen that K_{rh} is dependent on line parameter L_f. This inductance may change with different operating conditions including source voltage and source current. If inductance is changed, then the gain parameter K_{rh} will be also changed. Therefore, robustness of the system is also checked with different inductance parameters. Figure 5.10 shows bode-plot of closed-loop current controller with change in line inductance. Figure shows that system steady-state performance remains unchanged even if L_f is changed. Still, controller is able to filter out 250, 350, 550, 650 Hz components from signal. This figure also confirms the robustness of the proposed PI-VPI compensator based current controller with the variation of line impedance.

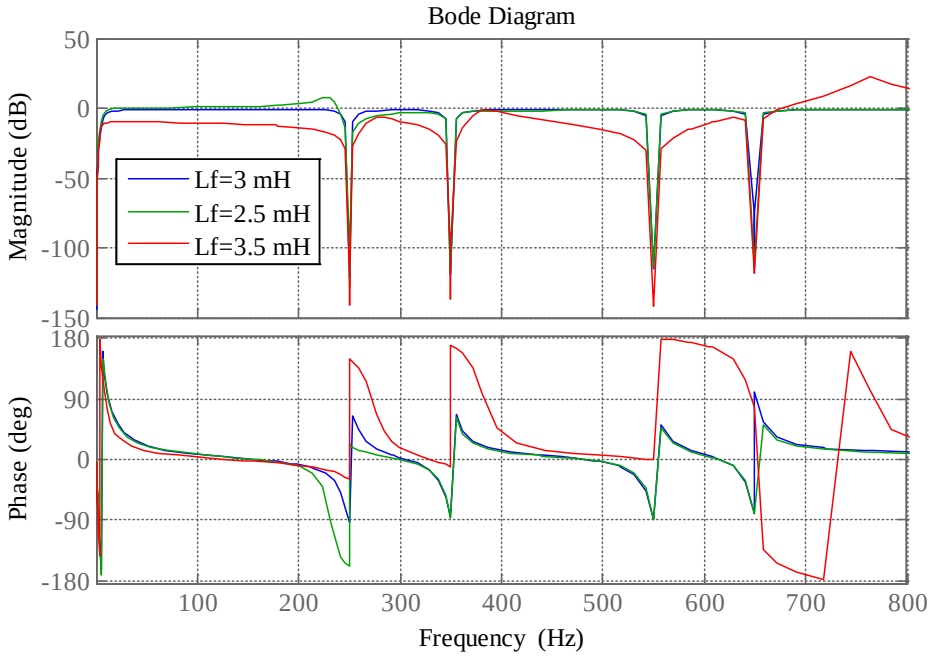


Figure 5.10 Bode-plot of closed-loop proposed current controller transfer function with variation of line impedance

Impact of Proposed Current Controller on DC-link Voltage Control Loop

Proposed PI-VPI compensator introduces four numbers of peaks in frequency response as seen from bode-plot of PI-VPI compensator compared to PI compensator. Gain parameters of PI-VPI compensators need to be properly tuned otherwise it may affect the stability of DC-link voltage control loop. From Figure 5.1 and Figure 5.6, the block diagram of DC-link voltage control can be drawn as Figure 5.11.

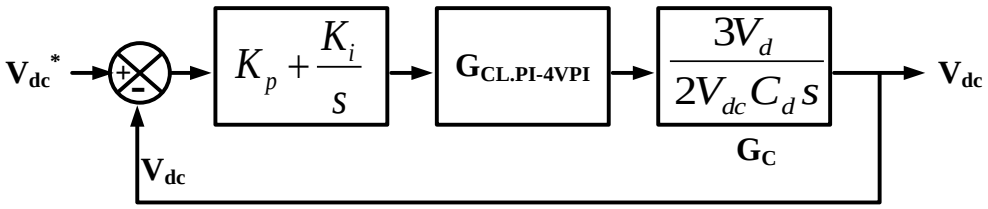


Figure 5.11 DC-link voltage control loop

DC-link voltage control closed-loop transfer function is expressed as Equation 5.14.

$$G_{CL.DC} = \frac{G_{PI-dc}(s)G_{CL.PI-VPI}(s)G_C(s)}{1 + G_{PI-dc}(s)G_{CL.PI-VPI}(s)G_C(s)} \quad (5.14)$$

Figure 5.12 shows bode-plot of closed-loop DC-link voltage control loop transfer function which shows the effect of proposed PI-VPI compensator based current controller in DC-link voltage control loop.

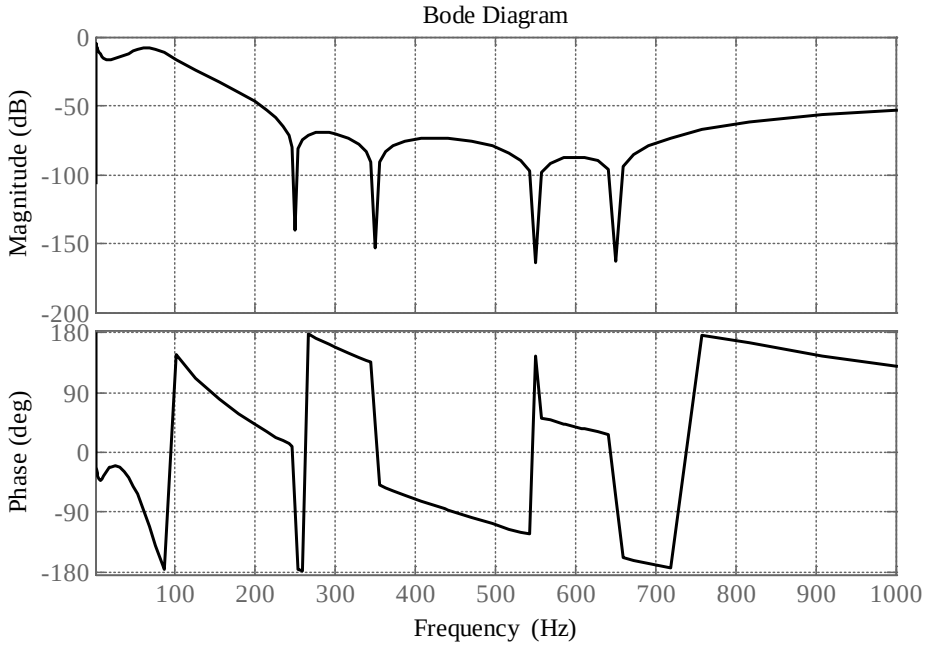


Figure 5.12 Bode-plot of closed-loop DC-link voltage control

Figure shows closed loop transfer function maintains zero amount of phase shift at lower frequency range. Higher frequency rejection does not affect dc-link voltage loop as magnitude of transfer function is always below 0 dB. Therefore, it can be stated that the proposed controller does not harm the stability of DC-link voltage control loop.

5.4.3 DFRM-3φ-pPLL Structure

Phase angle and line frequency information are important parameters while connecting CHB-MLI based SAPF unit to grid. PLL is normally used as most suitable technique for extracting phase angle information from grid voltage as this method is simple to implement, and robust in nature. PLLs are mainly closed-loop feedback control system, where PLL is used for exact measurement of frequency and phase angle. PLL structure mainly consists of three main blocks namely phase detector block, loop filter and voltage controlled oscillator (VCO). PI controllers are normally used as loop filter and integrator is used as VCO. A lot of PLLs are used in the literature for extracting phase angle information. Changes are made mainly in phase detection section to make PLL suitable for different source voltage conditions. Normally, PLLs are sensible for grid voltage variations where double frequency oscillations appeared in estimated frequency. DFRM-3φ-pPLL Structure is proposed in this chapter in order to counter these above mentioned problems. This unique structure is able to provide perfect double frequency ripple minimization from estimated frequency. The proposed DFRM block is shown in Figure 5.13 (a) and structure of proposed PLL is shown in Figure 5.13 (b).

The proposed PLL structure is able to provide perfect cancellation of double frequency component from estimated signal. S. Golestan et al. [180] has proposed modified power-based PLL for single-phase grid-tied system. In this chapter, this idea has been extended to three-phase–DFRM-pPLL system for cancellation of double-frequency component in three-phase grid-tied system. Three-phase voltage quantities may be transformed into d-q-0 quantities as per Equation 5.15.

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \cos(\hat{\theta} - 2\pi/3) & \cos(\hat{\theta} + 2\pi/3) \\ \sin(\hat{\theta}) & \sin(\hat{\theta} - 2\pi/3) & \sin(\hat{\theta} + 2\pi/3) \end{bmatrix} \begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} \quad (5.15)$$

where, three-phase voltage quantities can be shown as Equation 5.16.

$$\left.\begin{aligned} V_a(t) &= V\sin(\theta t) \\ V_b(t) &= V\sin(\theta t - 2\pi/3) \\ V_c(t) &= V\sin(\theta t + 2\pi/3) \end{aligned}\right\} \tag{5.16}$$

Values of Equation 5.16 are placed in Equation 5.15 and finally three-phase voltage is converted into equivalent d-q-0 system which can be shown as per Equation 5.17.

$$\left.\begin{aligned} v_d(t) &= {}^{V}/_{3}\left[2\sin(\theta - \hat{\theta}) + \sin(\theta + \hat{\theta})\right] \\ v_q(t) &= -{}^{V}/_{3}\left[\sqrt{3}/2\,.\sin(\theta + \hat{\theta}) - 1/2\cos(\theta + \hat{\theta}) + 3\cos(\theta + \hat{\theta})\right] \end{aligned}\right\} \tag{5.17}$$

Considering $\theta - \hat{\theta} = \theta_e$, it can be noted that,

$$\theta + \hat{\theta} = \theta_e + 2\hat{\theta} \tag{5.18}$$

Therefore, Equation 5.17 can be rewritten as Equation 5.19 and Equation 5.20.

$$v_d(t) = {}^{V}/_{3}\left[2\sin\theta_e + \sin\theta_e\cos 2\hat{\theta} + \cos\theta_e\sin 2\hat{\theta}\right] \tag{5.19}$$

$$\begin{aligned} v_q(t) = {}^{V}/_{3}\big[&2\cos\theta_e + \sqrt{3}/2\,.\sin\theta_e.\cos 2\hat{\theta} \\ &+ \sqrt{3}/2\,.\cos\theta_e.\sin 2\hat{\theta} + 1/2\,.\sin\theta_e\sin 2\hat{\theta} - 1/2\,.\sin\theta_e.\sin 2\hat{\theta}\big] \end{aligned} \tag{5.20}$$

Terms ($V\cos\theta_e$ and $V\sin\theta_e$) of Equation 5.19 and Equation 5.20 are almost equivalent to a dc quantity for a small angle difference θ_e. These equations again shows dependency of double-frequency component terms on these dc quantities. Therefore, it is very much easy to cancel these double-frequency terms by injecting double-frequency terms of same magnitude but of opposite angle into v_d and v_q. This PLL is composed of two main elements namely DFRM block and amplitude compensation block. For reduction of complexity, LPF is considered as first order filter as shown in Equation 5.21.

$$LPF(s) = \frac{\omega_P}{s + \omega_P} \tag{5.21}$$

where, ω_p is the cut-off frequency of LPF. Figure 5.13 (a) shows the proposed DFRM block for three-phase application. Perfect cancellation of double-frequency terms can be done with the help of this block. In order to analyze this proposed DFRM block, the mathematical expressions of v_d and v_q are derived in Laplace domain. From Equation 5.19 and Figure 5.13 (a), $\overline{v_d}$ can be written as Equation 5.22 and $\overline{v_q}$ can be written as Equation 5.23.

$$\overline{v_d} = \frac{\omega_P}{3(s+\omega_P)} . \mathcal{L}\left[2v_d - \overline{v_d}\cos 2\hat{\theta} - \overline{v_q}\sin 2\hat{\theta}\right] \tag{5.22}$$

$$\begin{aligned}\overline{v_q} = \frac{\omega_P}{3(s+\omega_P)} . \mathcal{L}\big[&2v_q - \sqrt{3}/2 . \overline{v_d}\cos 2\hat{\theta} - \sqrt{3}/2 . \overline{v_q}\sin 2\hat{\theta} \\ &- 1/2 . \overline{v_q}\cos 2\hat{\theta} - 1/2 . \overline{v_d}\sin 2\hat{\theta}\big]\end{aligned} \tag{5.23}$$

where, $\mathcal{L}$ denotes Laplace operator.

Equation 5.22 and Equation 5.23 can be rearranged as per Equation 5.24 and Equation 5.25 by multiplying both sides with one operator $(s + \omega_P)$.

$$s\overline{v_d} = \omega_P . \mathcal{L}\left[2/3 . v_d - \overline{v_d}\left(1 + 1/3 . \cos 2\hat{\theta}\right) - \overline{v_q} . 1/3 . \sin 2\hat{\theta}\right] \tag{5.24}$$

$$\begin{aligned}s\overline{v_q} = \omega_P . \mathcal{L}\big[&2/3 . v_q + 1/2 . \overline{v_q}\cos 2\hat{\theta} - 3\overline{v_q} - 1/2 . \overline{v_d}\sin 2\hat{\theta} \\ &- \sqrt{3}/2 . \overline{v_d}\cos 2\hat{\theta} - \sqrt{3}/2 . \overline{v_q}\sin 2\hat{\theta}\big]\end{aligned} \tag{5.25}$$

Equation 5.24 can be rearranged for further calculation as per Equation 5.26.

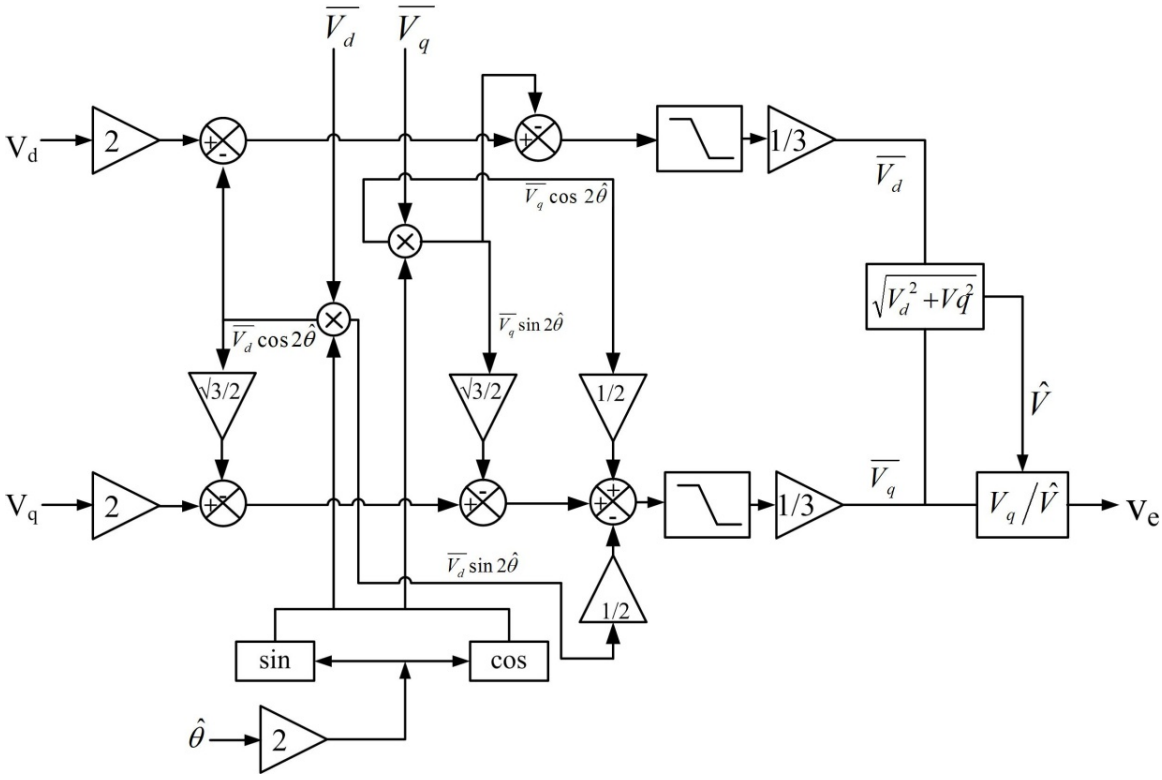
$$\begin{aligned}s\overline{v_d} = \omega_P . \mathcal{L}\big[&4/9 . V . \sin\theta_e + 2/9 . \cos 2\hat{\theta} . V \sin\theta_e + 2/9 . \sin 2\hat{\theta} . V \cos\theta_e \\ &- \overline{v_d}\left(1 + 1/3 . \cos 2\hat{\theta}\right) - 1/3 . \overline{v_q} . \sin 2\hat{\theta}\big]\end{aligned} \tag{5.26}$$

and

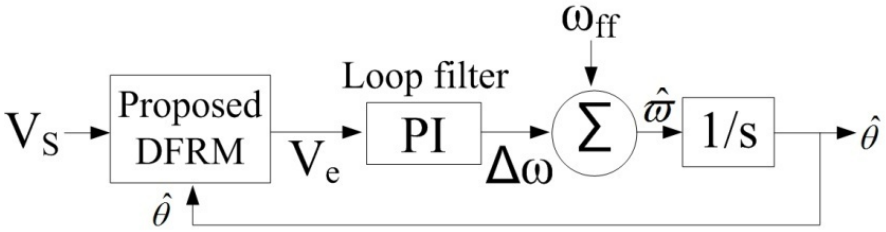
$$\begin{aligned}s\overline{v_q} = \omega_P . \mathcal{L}\big[&1/3\sqrt{3} . \cos 2\hat{\theta} . V \sin\theta_e + 1/3\sqrt{3} . \sin 2\hat{\theta} . V \cos\theta_e \\ &+ 4/9 . V \cos\theta_e - 1/9 . \cos 2\hat{\theta} . V \cos\theta_e + 1/9 . \sin 2\hat{\theta} . V \sin\theta_e \\ &+ 1/2 . \overline{v_q} . \cos 2\hat{\theta} - 3\overline{v_q} - 1/2\,\overline{v_d} . \sin 2\hat{\theta} - \sqrt{3}/2 . \overline{v_d} . \cos 2\hat{\theta} \\ &- \sqrt{3}/2 . \overline{v_q} . \sin 2\hat{\theta}\big]\end{aligned} \tag{5.27}$$

Finally, Equations 5.26 and 5.27 are transformed to Equation 5.28 for showing proper double-frequency component cancellation with a constant term 'ω_P'. Equation 5.28 is a linear time-variant system which is having two numbers of inputs namely 'V_d' and 'V_q'. The double-frequency terms decreases to zero and solution ultimately converges to $V\sin\theta_e$ and $V\cos\theta_e$.

$$\begin{aligned}&\begin{bmatrix}\dot{\overline{v_d}} \\ \dot{\overline{v_q}}\end{bmatrix} \\ &= \omega_P \begin{bmatrix} -1/3 . \cos 2\hat{\theta} & -1/3 . \sin 2\hat{\theta} \\ -\left(1/2 \sin 2\hat{\theta} + \sqrt{3}/2 \cos 2\hat{\theta}\right) & -\left(3 + \sqrt{3}/2 . \sin 2\hat{\theta} - 1/2 . \cos 2\hat{\theta}\right)\end{bmatrix}\begin{bmatrix}\overline{v_d} \\ \overline{v_q}\end{bmatrix} \\ &+ \omega_P \begin{bmatrix} 4/9 + 2/9 . \cos 2\hat{\theta} & 2/9 . \sin 2\hat{\theta} \\ 1/3\sqrt{3} . \cos 2\hat{\theta} + 1/9 . \sin 2\hat{\theta} & 1/3\sqrt{3} . \sin 2\hat{\theta} + 1/9 . \cos 2\hat{\theta}\end{bmatrix}\begin{bmatrix} V \sin\theta_e \\ V \cos\theta_e\end{bmatrix}\end{aligned} \tag{5.28}$$



(a)



(b)

Figure 5.13 (a) DFRM-3φ-pPLL structure and (b) proposed PLL structure

5.5 GAIN PARAMETER CALCULATION OF PI-VPI COMPENSATOR

The performance of PI-VPI compensator in current control loop is checked by transfer function approach in order to design the gain parameters. Closed-loop transfer function is denoted by Equation 5.12. As $R_L \rightarrow \infty$; transfer function becomes Equation 5.13 as a simpler form. In Equation 5.13, gain parameters i.e. K_{p1}, K_{i1}, K_{ph5}, K_{ph7}, K_{ph11}, K_{ph13} needs to be tuned properly in order to get best solution. Normally, gain parameters K_{p1} and K_{i1} do not affect harmonic compensation ability from current control loop. These constant parameters regulate fundamental frequency component of source current.

Therefore, normally, K_{p1} and K_{i1} are made constant in order to make design of the compensator simpler. Parameter K_{ph5}, K_{ph7}, K_{ph11} and K_{ph13} are tuned as per frequency-response characteristics. Different gain parameters are set according to high frequency component elimination criteria of above said compensator. Q. C. Trinh et al. [174] show controller selective harmonic elimination performance in terms of gain of the controller. It is shown that, PI-VPI compensator produces high gain at selected frequencies with zero amount of phase shift; regardless of selection of gain parameter K_{ph}. Study also shows better selectivity and steady-state performance with lower value of gain parameter K_{ph}. However, selection of K_{ph} to a too small value affects dynamic performance of SAPF system. Therefore, all the constant parameters need to be tuned carefully in order to get good steady-state as well as good transient response. Till date, systematic design procedure of gain parameters is an issue which needs to be solved. Furthermore, if number of gain parameters is more, then design is a difficult task by this method. Therefore, this chapter shows a systematic design procedure of selecting gain parameters.

5.5.1 Particle Swarm Optimization Technique

A number of meta-heuristic approaches have been presented in literatures [182] for different engineering applications. Among these algorithms, PSO, proposed by Kennedy et al., is one of the emerging optimization techniques available for finding out best possible solution with simpler approach [178]. The concept of PSO depends on the movement and social behavior of flocks, birds etc. PSO is becoming an automatic choice for researchers in current scenario because of advantages like quick convergence to best solution, and simpler implementation procedure. Flowchart of PSO algorithm for optimal gain parameter selection is shown in Figure 5.14. In order to start this optimization procedure, initial conditions of each particle need to be defined. A flock is considered for a given problem and this flock helps to determine the optimal solution for a mentioned objective function. The minimization/ maximization of objective function depend on the experience of the flock and solution defined for each time. Particles will identify this information and the analogy is tested each time. This phenomenon decides the best possible solution locally. All particles will perform this exercise and finally a global best solution is found among these locally best solutions. Each particle reshuffles their

position in order to maintain this above said condition. This concept is useful for finding out the newer position of particles as well as velocity of each particle. Newer position of each particle is defined as per Equation 5.29.

$$x_{k+1}{}^{i} = x_{k}{}^{i} + v_{k+1}{}^{i} \tag{5.29}$$

Updated velocity of each particle is defined as follows:

$$v_{k+1}{}^{i} = v_{k}{}^{i} + c_1 r_1 \left(p_{k}{}^{i} - x_{k}{}^{i}\right) + c_2 r_2 \left(p_{k}{}^{g} - x_{k}{}^{i}\right) \tag{5.30}$$

Right-hand side of this equation is composed of three terms. First term defines previous velocity of the particle whereas second and third terms help to define the amount of change in velocity of the particles. These two terms will decide the direction of particles. Particle will follow the same direction until boundary condition if these two terms are absent. Finally, the main aim of these particles is convergence of its best possible solution within a minimum span of time. PSO is basically one of the simplest approaches present in the literature for finding out the optimal solutions for a given problem. This code can be implemented in m-file of MALTAB software with few lines of coding.

Step-1: Initial conditions for each particle need to be selected. Velocity and position of each particle are generated arbitrarily within the permissible range. Current searching point is set as p_{best} for each particle. G_{best} is selected as best possible solution of p_{best}.

Step-2: The value of given objective function is calculated for each particle. This process helps for evaluating the searching point of each particle. If the newly found objective function value is better solution than previously mentioned p_{best}, then the older p_{best} value will be replaced by current value. If the locally best value is better solution than the current global best value, then global best solution will be also updated.

Step-3: Searching point will be updated in searching space as per Equation 5.29 and Equation 5.30.

Step-4: If the iteration number mentioned during the program is already achieved, then the iteration will stop. Otherwise, it will continue its operation in loop.

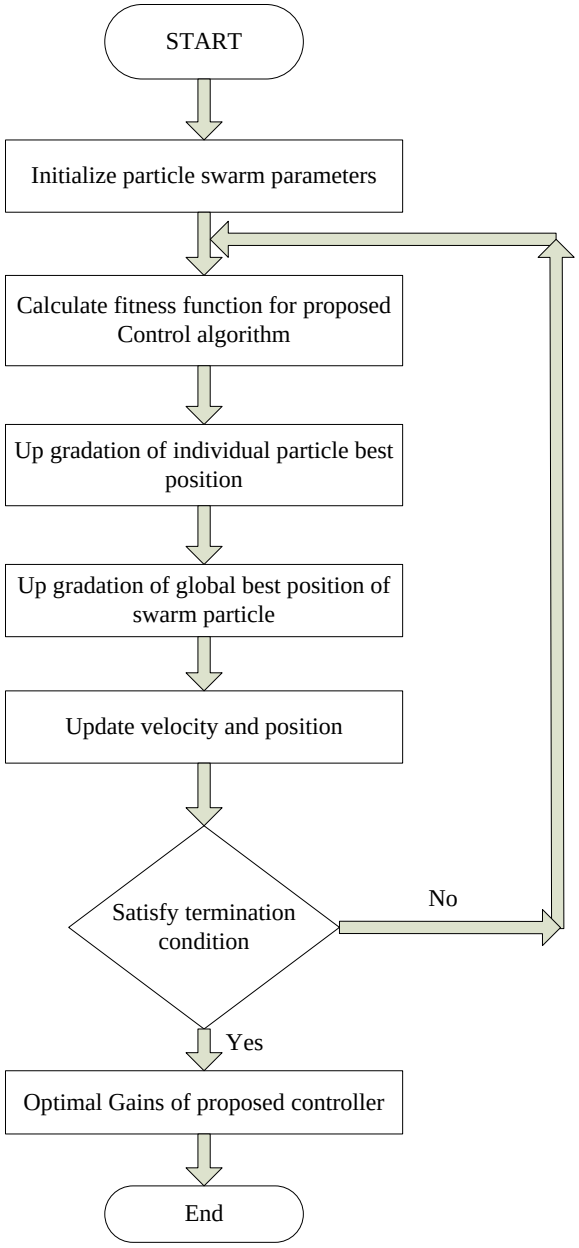


Figure 5.14 Particle swarm optimization algorithm

5.5.2 Proposed Methodology for Finding out Optimal Gain Parameters

This section deals with the detailed procedure which is adopted for tuning PI-VPI gain parameters optimally. The proposed methodology is shown in Figure 5.15. PSO is used as a platform for finding out optimal gain parameters. For PSO application, two things need to be defined carefully i.e. a consistent search range for defined variables which need to be optimized and a cost function as per application. The search range needs to be defined properly in order to ensure best solutions for better system

performance. This search results in global best solution. Solutions may be locally best if this search space is not well defined. Even it may be possible that solution prescribed by the algorithm found not so satisfactory. Thus, firstly, PI compensator gain parameters are tuned using bode-diagram technique. Then, VPI compensator gain constants are selected based on bandwidth selection which is based on frequency response process. These gain constants are selected for initial search condition. Range of search space is well defined based on user defined criteria. The detailed procedure is shown as follows.

A. PI compensator gain parameter selection [177]

CHB-MLI based SAPF system transfer function is defined as

$$G_{CHB-MLI-SAPF} = \frac{K_{PS-PWM}.V_d}{L_f s + R_f} \tag{5.31}$$

and PI compensator transfer function is defined in 's' domain as

$$G_{PI}(s) = K_{p1} + K_{i1}/s \tag{5.32}$$

This PI compensator gain parameters are tuned using frequency response methodology through bode-plot. Phase margin and zero decibel gain cross over frequency are main design specifications while designing these parameters. Thus, following steps are used for finding out PI compensator gain parameters.

1) Phase angle of CHB-MLI based SAPF system is calculated, which is represented as Equation 5.31, at zero decibel gain cross-over frequency. This much phase angle delay must be provided by the compensator in order to maintain design specification.

2) PI compensator is designed as depicted in Equation 5.33.

$$G_{PI}(s) = K_{p1}\left(1 + \frac{1}{T_i s}\right) = \frac{K_{p1}}{T_i}\left(\frac{T_i s + 1}{s}\right) = K_{i1}\left(\frac{T_i s + 1}{s}\right) \tag{5.33}$$

This compensator is added with CHB-MLI based SAPF system for adjusting the required phase margin needed by selecting T_i.

3) Bode diagram of the system composed of compensator and CHB-MLI based SAPF system is plotted and amplification factor is calculated at specified frequency.

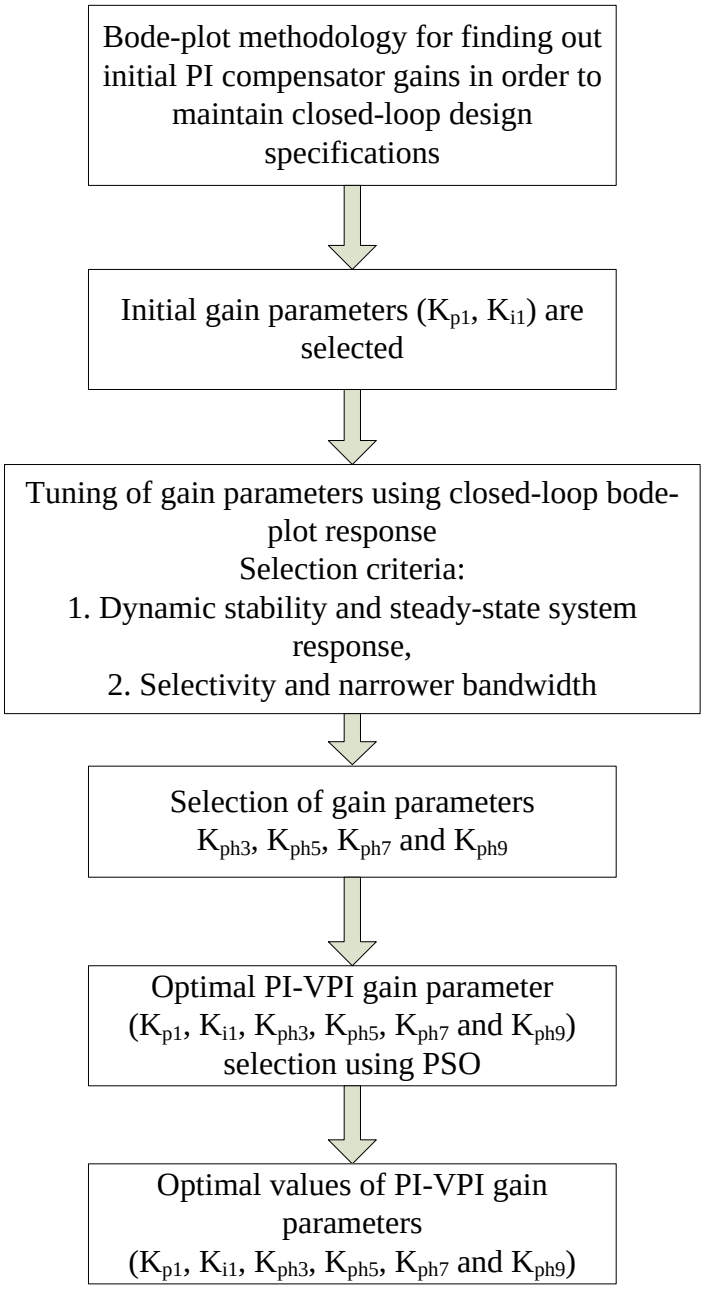


Figure 5.15 Proposed methodology for finding out optimal solutions

4) Compensator should provide this amplification in accordance to design specifications. It can be done by adjusting open-loop gain K_{i1} so that the curve of compensated system should cross 0 db at crossover frequency.

5) As K_{i1} is already decided, K_{p1} is found out by applying Equation 5.34.

$$K_{p1}=K_{i1}.T_i \tag{5.34}$$

B. VPI compensator gain parameter selection

The first round of VPI compensator gain parameters is obtained using bode-plot and frequency response criteria. Current compensator is added with CHB-MLI-based system in series and closed-loop transfer function is obtained with inverter average model as per Equation 5.31. Gain parameters for above mentioned compensator are calculated as per required control performance. Bode-diagram of closed-loop system is plotted as shown in Figure 5.9 with different K_{ph} values. Study shows high amount of gain present at selected harmonic frequency for each K_{ph}. However, it can be noted that, with reduction of gain parameter constant, bandwidth also becomes narrower. SAPF system achieves better steady-state performance with smaller K_{ph}. Selectivity also increases with lesser value of gain parameter [183]. Furthermore, system dynamic performance reduces if these values are not well set. Therefore, this compensator gain parameters need to be tuned perfectly in order to get better steady-state as well as dynamic response.

C. PSO optimization based proposed technique for finding out optimal gain parameters

In order to start this optimization procedure, initial conditions of each particle need to be defined. For this particular problem, six-dimensional search space is defined and each particle is fixed by using position and velocity vectors. Particles modify their movements according to their experience and their adjacent particle knowledge. Each particle moves around search space and memorize the finest positions for them, called P_{best}. These particles communicate among them and able to find the best possible solution for this problem.

The initial conditions of PI-VPI compensator are defined by using methods discussed in previous section. Proper search range needs to be defined in order to get best solutions with less time. Methodology considered for obtaining maximum and minimum search range is based on bode-plot based selection criteria. Though frequency response procedure does not guarantee best solutions for parameter selection, it can be noticed that, initial search conditions can be found out by this method. Once gain parameters K_{p1}, K_{i1}, K_{ph5}, K_{ph7}, K_{ph11} and K_{ph13} are defined, search space is also defined as

$$K_{j.max} < K_j < K_{j.min} \tag{5.35}$$

The algorithm finds newer position based on the velocity and position information as mentioned in Equation 5.29 and Equation 5.30 [178].

The objective function is determined according to the criteria such as minimum steady-state error as well as less total harmonic distortion in source current. These two criteria are most important to determine SAPF system performance. Integral square error (ISE) technique is used for analyzing the system response with an objective function.

The main aim of this proposed controller is to maintain minimum error in source current magnitude and phase during real-time operative condition. This proposed algorithm perfectly finds the values of constant parameters of the PI-VPI compensator. These obtained values are further used for simulation as well as for hardware validation of proposed control technique.

5.6 PERFORMANCE ASSESSMENT OF PROPOSED CONTROL USING MATLAB/ SIMULINK

The required three-phase power circuit consists of five-level CHB-MLI based SAPF. Suitable control algorithm composed of proposed PI-VPI compensator based current controller is implemented in MATLAB/Simulink software. The performance of proposed system is rigorously checked with voltage- and current-type of non-linear loading. Simulation results of proposed system during steady-state and transient conditions are presented in this subsection. Three-phase and three-wire balanced system is considered for further study. Three-phase voltage and current waveforms have been presented to show the effectiveness of the proposed system.

5.6.1 Uncontrolled Rectifier and R-L Loading

Three-phase source voltage (V_S), three-phase source current (I_S), three-phase load current (I_L), compensating current of phase 'A' (I_{Ca}), dc-link voltage (V_d), inverter output voltage of phase 'A' (V_{Ca}) waveforms of five-level CHB-MLI based SAPF with proposed PI-VPI current compensator based closed-loop controller under R-L type of non-linear loading are shown in Figure 5.16. Figure shows that the proposed control algorithm is able to provide current harmonic content in phase opposition perfectly in order to make source current sinusoidal during steady-state condition. Therefore, MLI

based SAPF is successfully able to compensate reactive power and maintains unity power factor. After successful operation of MLI based SAPF unit, source current becomes sinusoidal and in-phase with respective phase of source voltage.

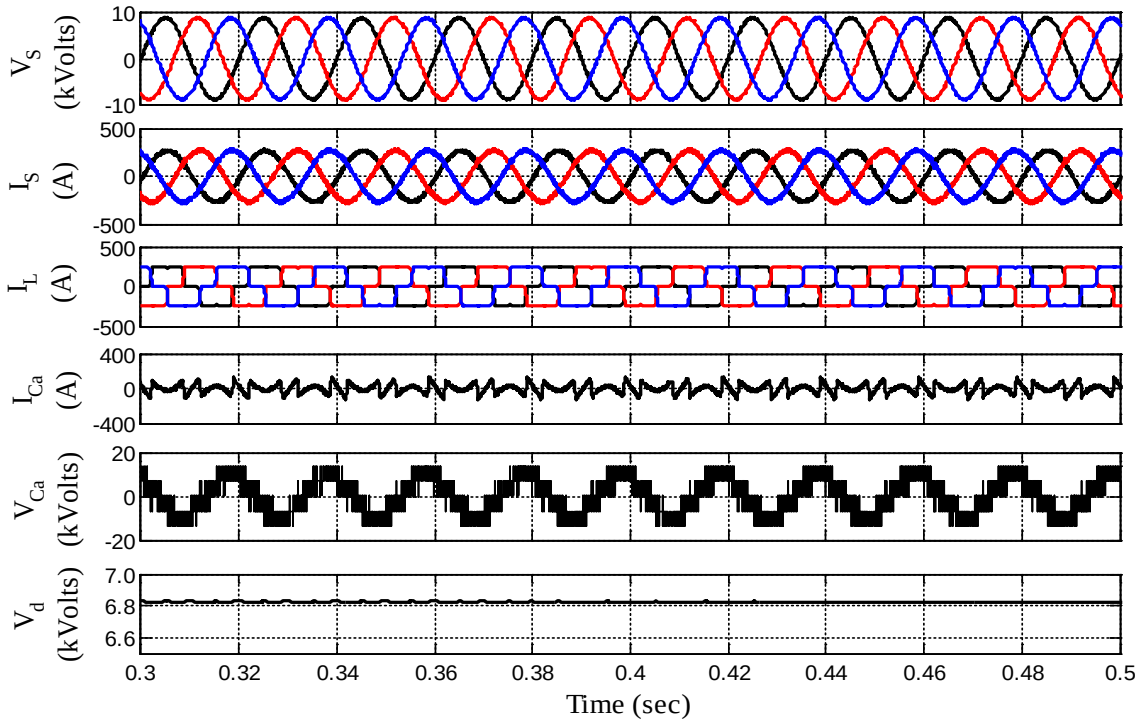


Figure 5.16 Steady-state performance of CHB-MLI based SAPF with proposed control strategy with R-L loading

Figure 5.17 and 5.18 show the THD spectrums of source current before and after compensation. Source current THD is reduced from 26.92% to 2.08% after interconnection of MLI based SAPF with grid. Calculated optimized gain parameters are successfully applied to the proposed PI-VPI compensator based controller. Power factor is also improved from 0.9 to 0.998 in the source side as reactive power demand decreases.

Performance of proposed control algorithm is not only tested in steady-state condition, the control technique applied to CHB-MLI based SAPF is tested with load changing condition also as load may be changed frequently in distribution sector. Figure 5.19 and Figure 5.20 show the load perturbation response of the CHB-MLI based SAPF with proposed PI-VPI compensator based control algorithm for increment and decrement of load current, respectively.

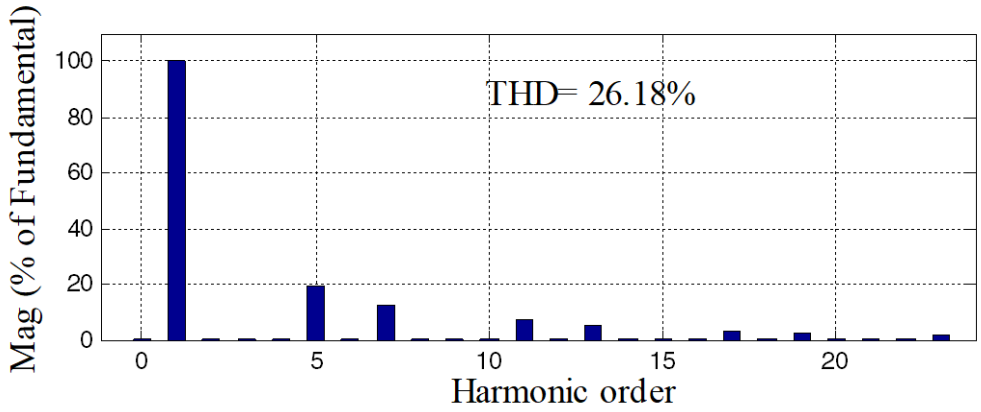


Figure. 5.17 THD of source current before source current compensation with R-L loading

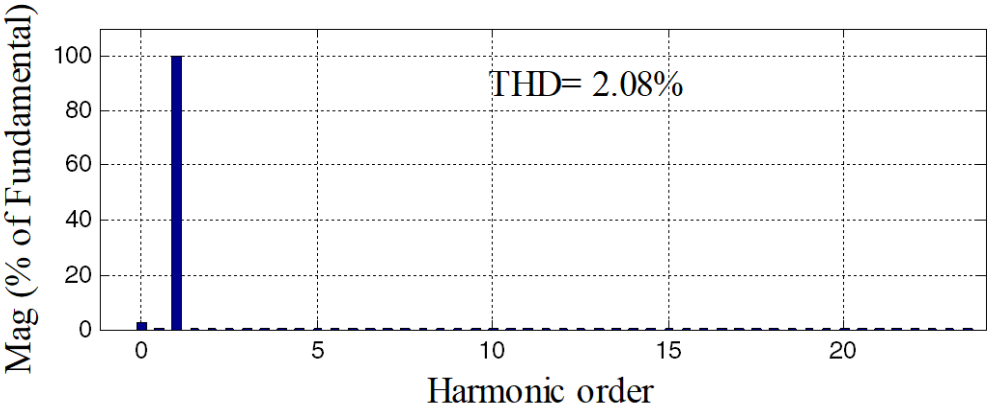


Figure. 5.18 THD of source current after source current compensation with R-L loading

Load current is increased from 200 A to 250 A at an instant t=0.9 sec while load current is decreased from 250 A to 200 A at an instant of t=1.5 sec. Three-phase balanced voltage (V_S), I_S, I_L, V_{Ca}, V_d is shown in both the figures. Compensating current of only phase 'A' (I_{Ca}) is shown in figures due to the balanced loading arrangement. It can be seen from Figure 5.19 and Figure 5.20 that compensated source current transition is occurring smoothly during load changing conditions within three cycles of time span. A dip in dc-link voltage is also noticed from its reference value in order to release the excess amount of energy during the increment of loading condition. A rise in dc-link voltage is also noticed from its reference value in order to absorb the excess amount of energy during decrement in the loading condition. Steady-state and transient response proves system effectiveness with R-L type of non-linear loading condition.

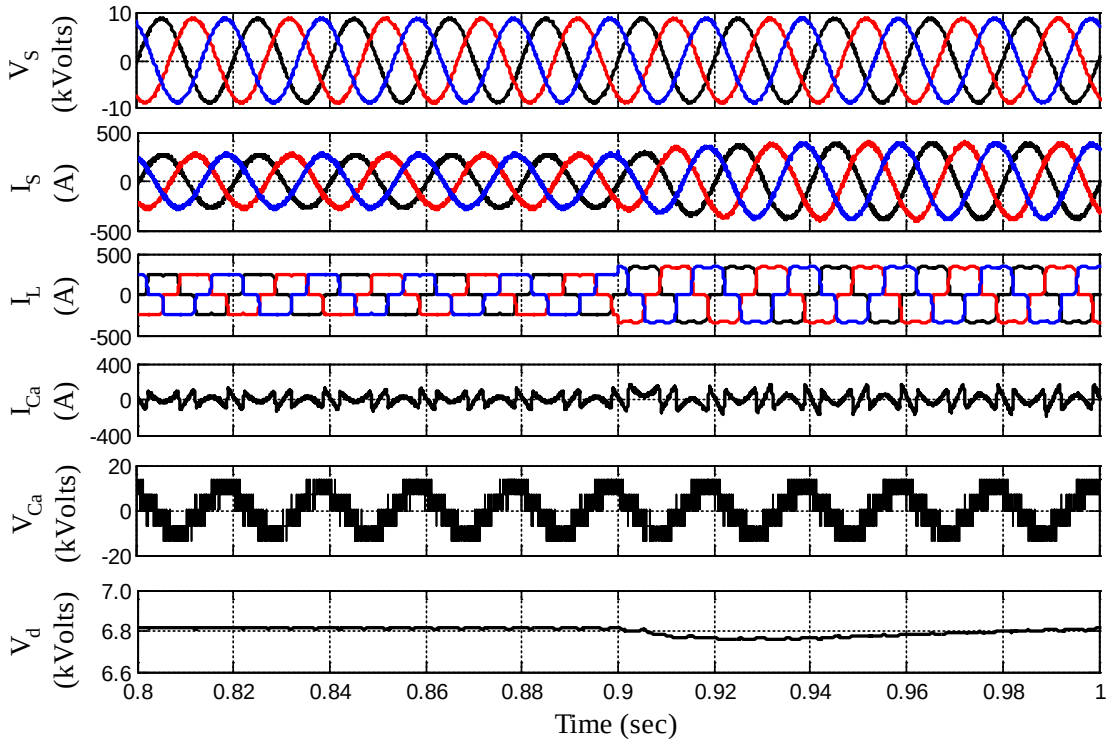


Figure 5.19 Transient-state performance of CHB-MLI based SAPF with proposed control strategy during load increment with R-L loading

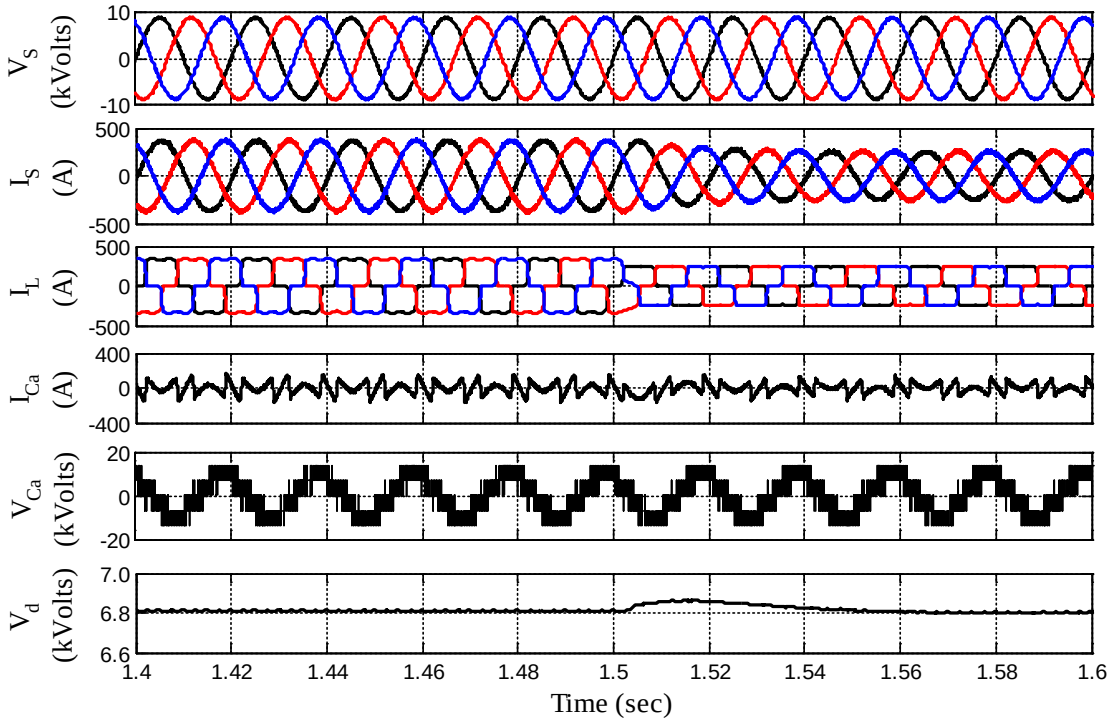


Figure 5.20 Transient-state performance of CHB-MLI based SAPF with proposed control strategy during load decrement with R-L loading

PI-VPI compensator based controller produces sine waveform with minimum phase and magnitude error as compared to PI compensator based current controller. As a result, the quality of current fed to the grid through PCC is further improved in steady-state and transient condition with proposed controller. The performance of the proposed control technique is not only tested with R-L loading condition, but also it is tested with R-C loading conditions in the next subsection.

5.6.2 Uncontrolled Rectifier and R-C Loading

The performance of the proposed controller is also checked with R-C type of non-linear loading. Steady-state V_S, I_S, I_L, I_{Ca}, V_d, V_{Ca} waveforms of five-level CHB-MLI based SAPF with proposed current controller under R-C loading are shown in Figure 5.21. It can be depicted from this figure that the proposed control algorithm applied to MLI based SAPF is successfully able to mitigate current harmonic component and compensate reactive power with voltage-type non-liner loading condition. After successful operation of this unit, source current becomes sinusoidal and in-phase with respective phase of source voltage.

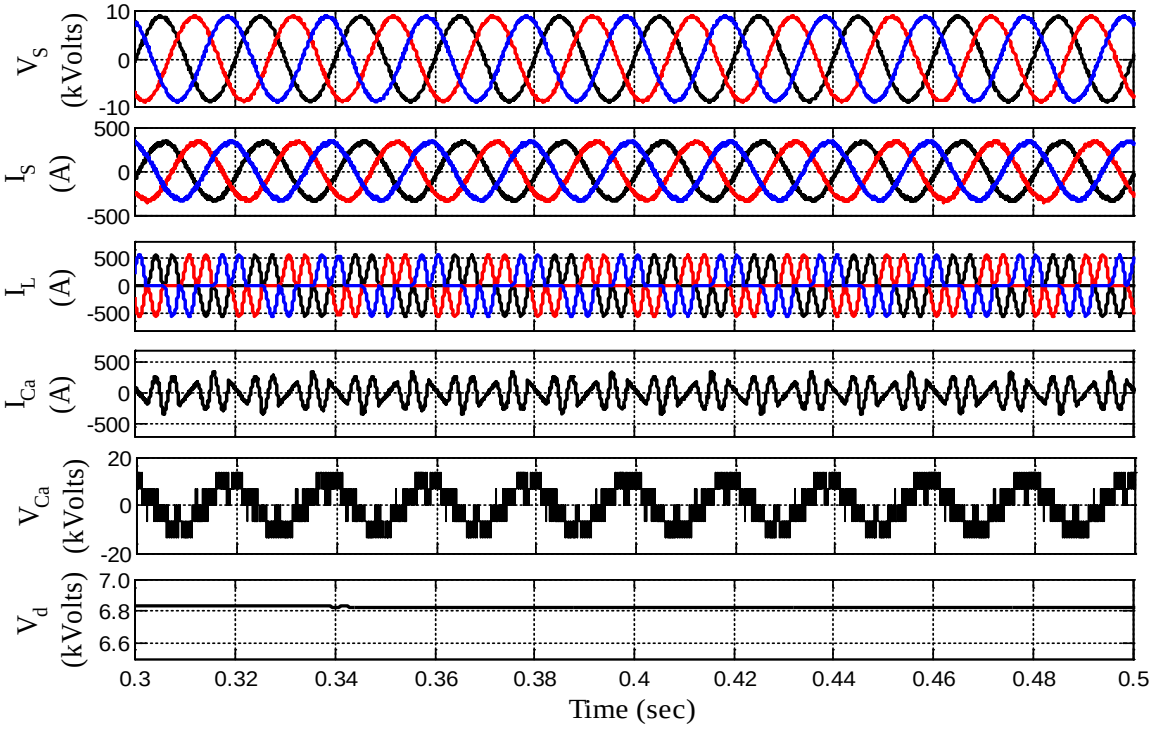


Figure 5.21 Steady-state performance of CHB-MLI based SAPF with proposed control strategy with R-C loading

Figure 5.22 and 5.23 show the THD spectrums of source current before and after compensation. Source current THD is reduced from 49.82% to 2.06% after interconnection of MLI based SAPF with grid. Calculated gain parameters are successfully applied to the proposed control algorithm. Power factor also improved from 0.90 to 0.997 in the source side as reactive power demand decreases.

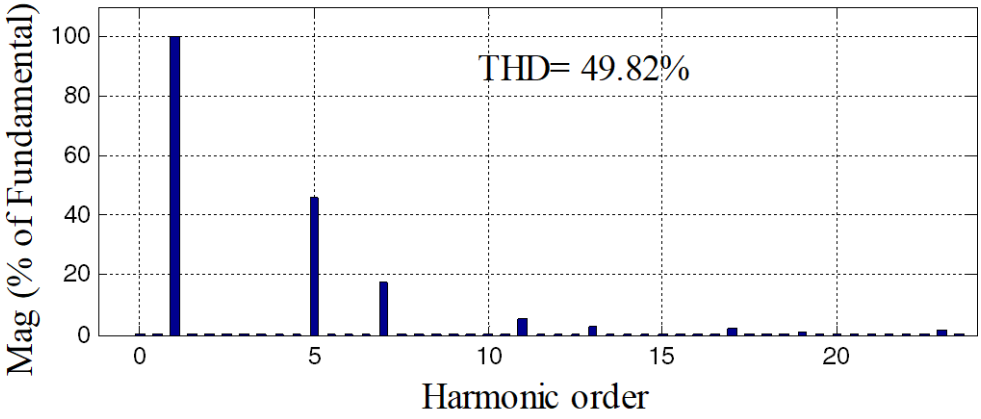


Figure. 5.22 THD of source current before source current compensation with R-C loading

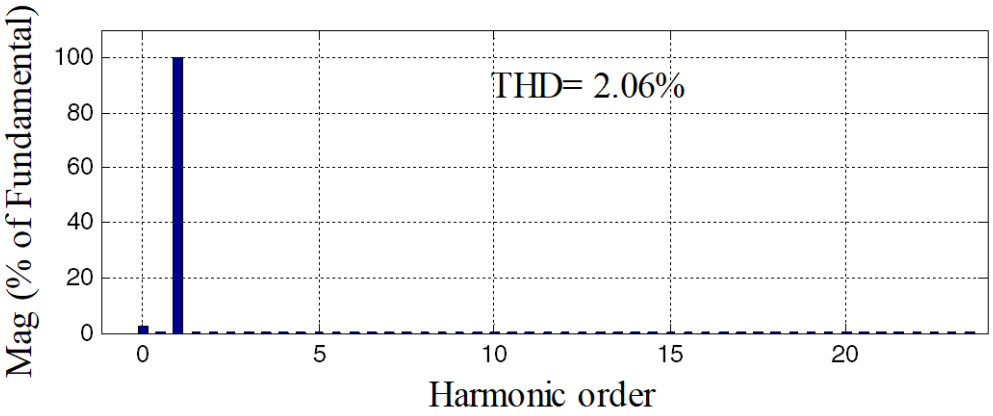


Figure. 5.23 THD of source current after source current compensation with R-C loading

Performance of modified control algorithm is designed and tested extensively under load changing condition. Figure 5.24 and Figure 5.25 show the load perturbation response of the MLI based SAPF for increment and decrement of load current, respectively.

Load current is increased from 200 A to 250 A at an instant t=0.9 sec. while load current is decreased from 250 A to 200 A at an instant of t=1.5 sec. It can be seen from Figure 5.24 and 5.25 that compensated source current transition is occurring smoothly.

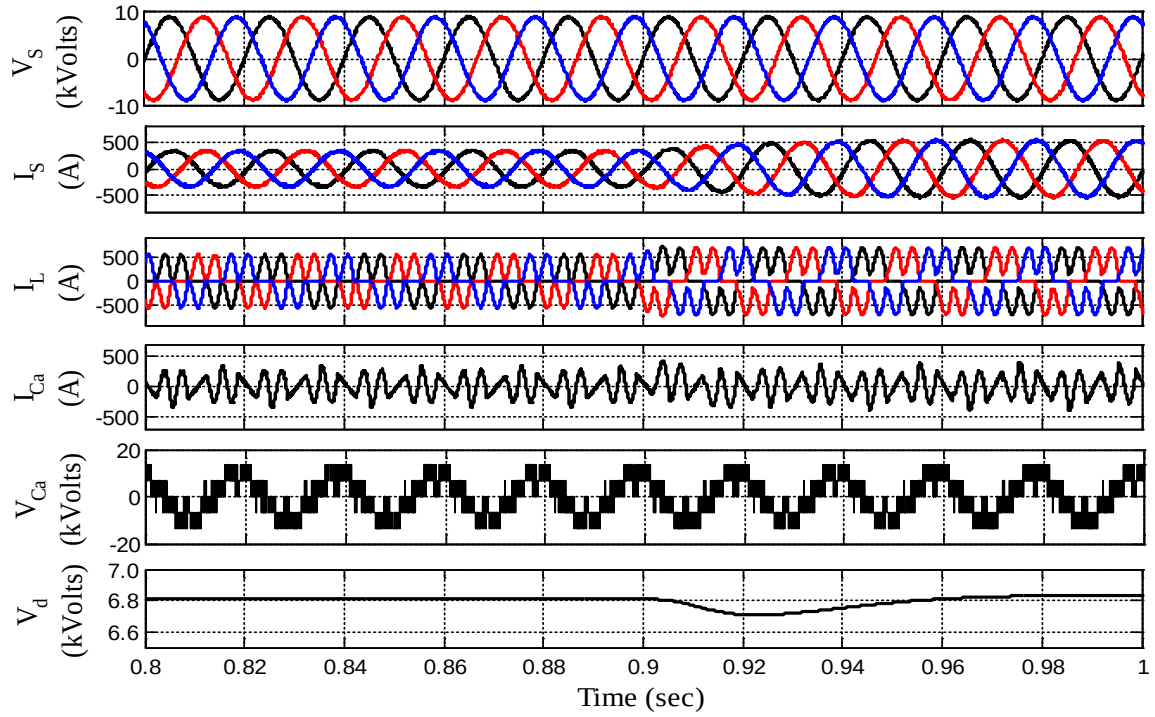


Figure 5.24 Transient-state performance of CHB-MLI based SAPF with proposed control strategy during load increment with R-C loading condition

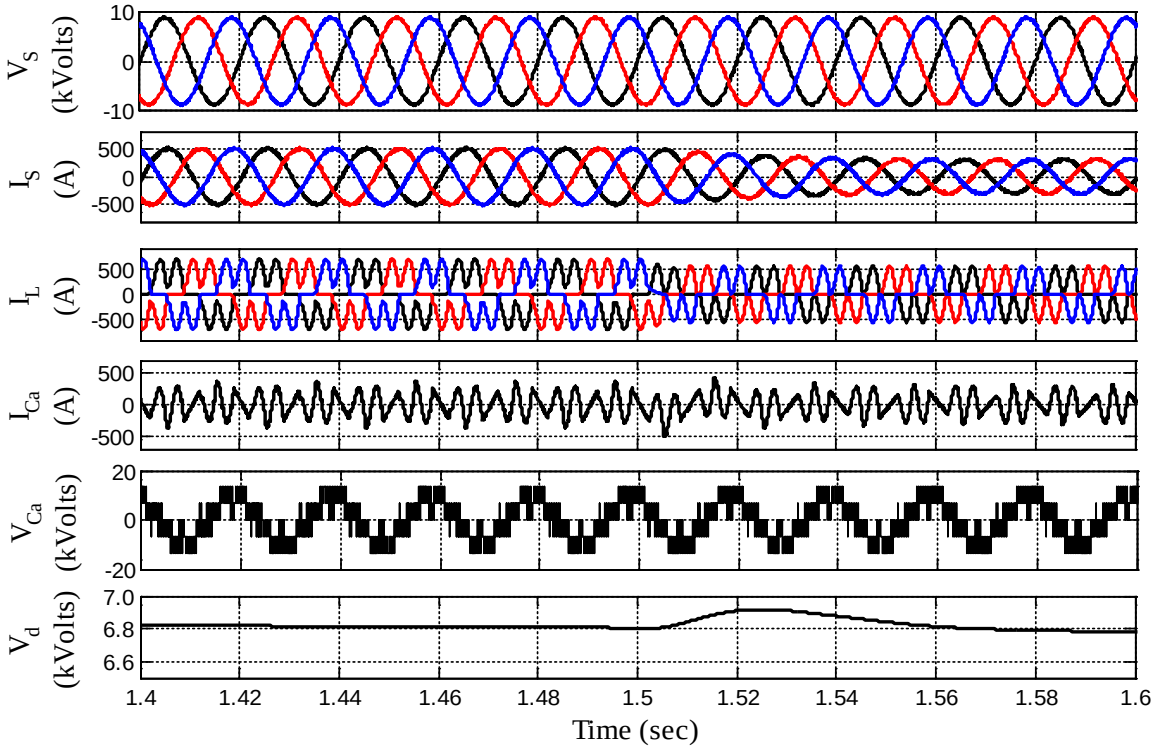


Figure 5.25 Transient-state performance of CHB-MLI based SAPF with proposed control strategy during load decrement with R-C loading

A dip/rise in dc-link voltage is also noticed from its mentioned reference value in order to release/ absorb the excess amount of energy during the load changing condition and settled within 0.06 second of time span.

Table 5.1 shows detailed comparative investigation of proposed control algorithm applied to SAPF under R-L and R-C non-linear loading conditions with PI-VPI compensator based control algorithm applied to CHB-MLI based SAPF. Non-linear source current THD is 26.18% with R-L loading whereas THD becomes 2.08% after operation of SAPF unit with proposed control algorithm. Power factor also improved from 0.90 to 0.997. Steady-state source current magnitude error is nil with respect to source current reference. Same has been examined with R-C type of non-linear loading conditions and results have been tabulated in Table 5.1. The detailed analysis shows system effectiveness with proposed controller in terms of percentage THD, power factor, steady-state source current magnitude and phase error under both R-L and R-C type of non-linear loading conditions.

Table 5.1 Comparative analysis of conventional and proposed control algorithm

Parameters Considered	Conventional Control Algorithm [123], [124]		Proposed Control Algorithm With PI-VPI compensator	
With diode bridge rectifier and R-L loading				
THD of source current (%)	Before	After	Before	After
	26.18	3.76	26.18	2.08
Power factor	Before	After	Before	After
	0.90	0.97	0.90	0.997
Steady-state source current magnitude error (%)	6.71		Nil	Nil
With diode bridge rectifier and R-C loading				
THD of source current (%)	Before	After	Before	After
	49.82	3.58	49.82	2.06
Power factor	Before	After	Before	After
	0.90	0.96	0.90	0.996
Steady-state source current magnitude error (%)	10.85		Nil	Nil

A comprehensive analysis of proposed and conventional control algorithm performance is analyzed with R-L and R-C load with PI-VPI compensator. Based on simulation and comparative analysis as mentioned in Table 5.1, it can be concluded that the proposed controller gives better performance in terms of quality of current supplied to the grid.

5.7 EXPERIMENTAL VALIDATION OF PROPOSED CONTROL USING dSPACE 1104

Prototype of single-phase five-level CHB-MLI based SAPF system is designed at laboratory scale level due to laboratory constraints. The power circuit used for laboratory prototype is shown in Figure 3.1. Advanced control technique applied for three-phase system has been modified for application in single-phase MLI based SAPF system. Single-phase SRF theory [123, 124] based control technique is used for reference current generation due to its effectiveness and better performance in SAPF system. The measured load current signals are transformed from 'abc' reference frame to synchronous reference frame ('dq') which is known as park's transformation. PLL continuously checks the frequency of grid voltage end extract phase angle information which is required for Park's and Inverse Park's transformation. Two fictitious components of load current are i_α and i_β where i_β is delayed by 90^0 to i_α. A low-pass filter is used for fundamental current component extraction and harmonic current rejection. Loss component of the circuit is supplied by a dc-PI compensator for dc-link voltage regulation. The flow diagram of modified single-phase SRF control theory is shown in Figure 5.26. Reference signal is generated by comparing source and load current signal. This signal is compared with measured compensating current signal. Finally, error current signal is processed through PI-VPI compensator. The experimental analysis mainly aims for proving the effectiveness of PI-VPI compensator over conventional one.

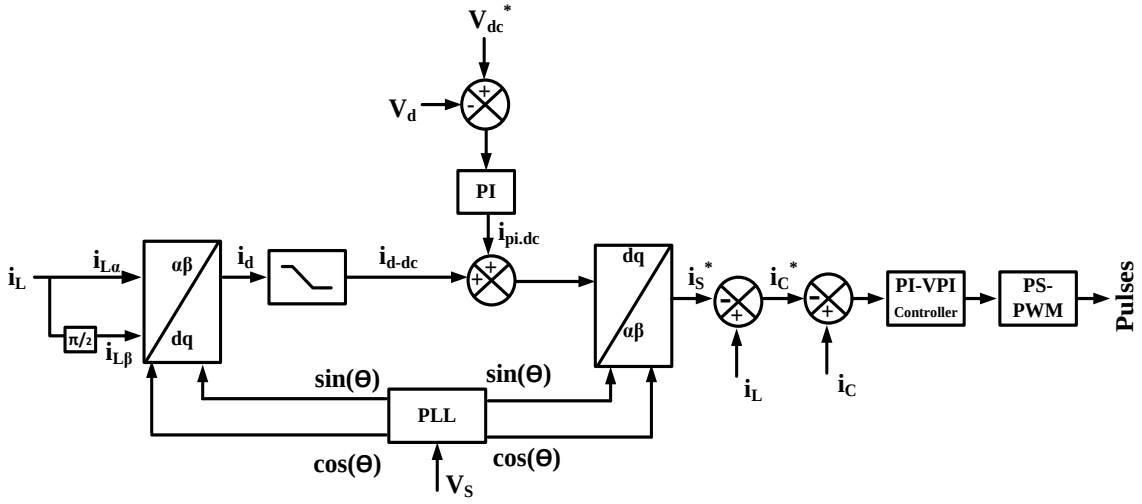
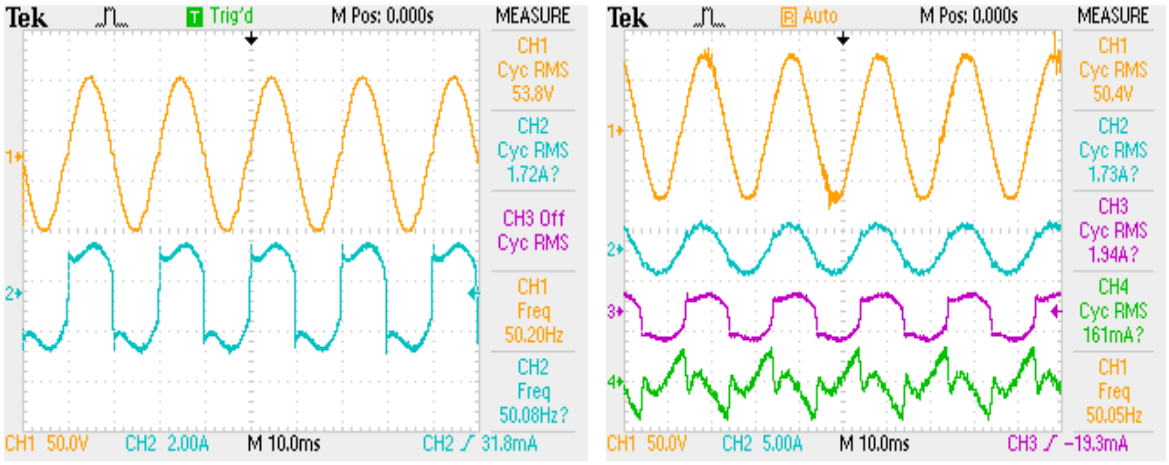


Figure. 5.26 Proposed PI-VPI compensator based SRF control algorithm for single-phase CHB-MLI

Conventional and advanced current controller based algorithm is designed and executed in dSPACE 1104 real-time controller. Fixed frequency voltage supply is used for experimental analysis. A detailed laboratory prototype based analysis has been carried out. Hardware results of proposed topology are presented for the validation of the simulation results.

5.7.1 Uncontrolled Rectifier and R-L Loading

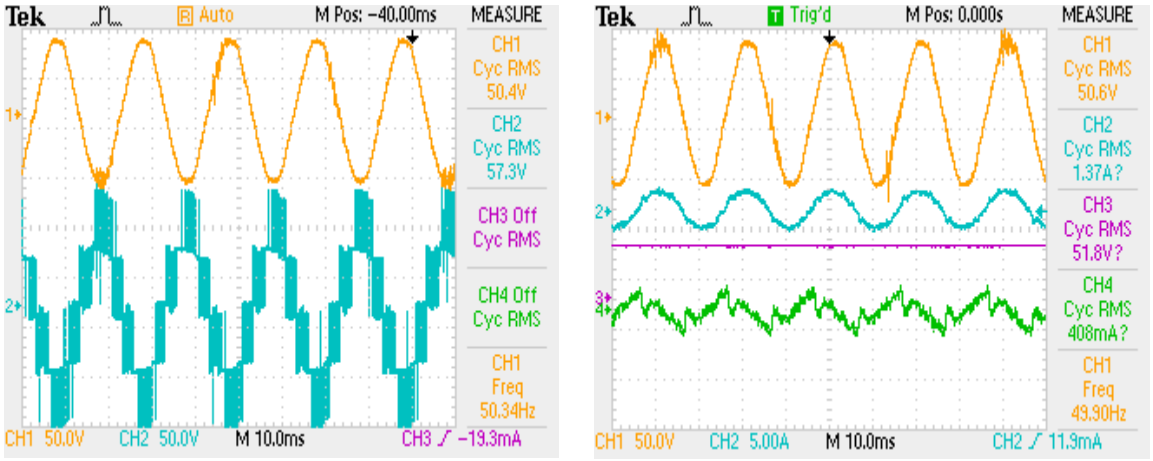
Steady-state MLI based SAPF waveforms (V_S, I_S, I_L, I_C, V_C and V_d) of the proposed system are depicted in Figure 5.27 (a) - (b). Figure 5.27 (a) shows waveform of sinusoidal V_S and non-linear I_S due to the presence of diode-bridge rectifier based resistive-inductive load into the existing system. Figure 5.27 (b) shows that source current is in phase with source voltage. Therefore, unity power factor at the source side is maintained. It is observed that there is significant reduction of phase error with advanced controller. Figure 5.27 (b) shows V_S, I_S, I_L, and I_C waveform during the steady-state operation of MLI based SAPF unit.



(a) (b)

Figure 5.27 Steady-state performance of MLI based SAPF with proposed controller under R-L loading (a) V_S with non-linear I_S, and (b) V_S, I_S, I_C, I_L waveform after compensation (CH1: 50V/div., CH2: 2A/div., CH3: 5A/div., CH3: 5A/div., CH4: 5A/div.)

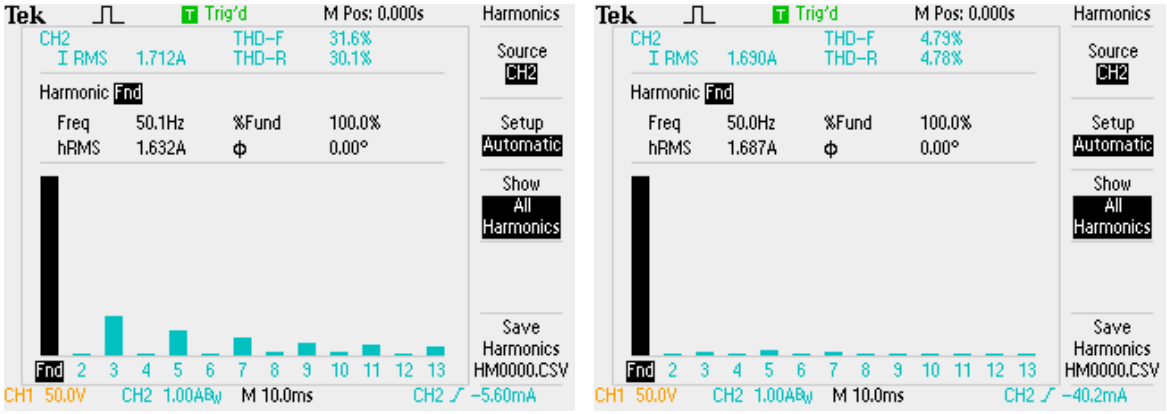
Inverter output voltage is also plotted for the sake of explanation of converter operation. Five-level inverter output is generated and shown in Figure 5.28 (a). Figure 5.28 (b) shows that dc-link voltage of capacitor is constant during the steady-state operation of inverter. Sinusoidal source current with unity power factor is produced in steady-state.



(a) (b)

Figure 5.28 Performance of MLI based SAPF with R-L loading (a) five-level MLI output voltage, and (b) V_S, I_S, V_d, and I_C steady-state waveform

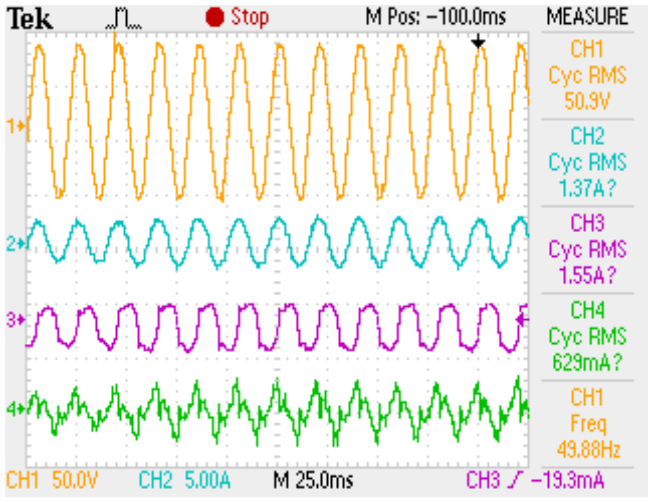
Source current almost maintains its sinusoidal shape during its operation which can be seen from above mentioned figures. Source current THD was 31.60% due to presence of non-linear loading which is shown in Figure 5.29 (a). However, after successful operation of SAPF unit, source current THD becomes 4.79% which is acceptable as per IEEE standard which can be seen from Figure 5.29 (b).



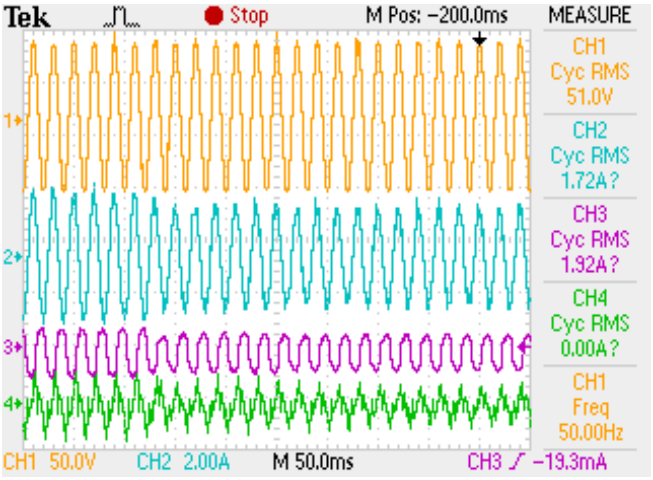
(a) (b)

Figure 5.29 THD profile of source current with R-L loading condition (a) before Compensation, and (b) after compensation

Effectiveness of the proposed control algorithm is also tested under load changing conditions. Load is first increased and corresponding V_S, I_S, I_C, and I_L waveforms are shown in Figure 5.30 (a). Source current transition is smooth when load current is increased. In the same manner, when load is decreased, waveforms show good transition response and corresponding V_S, I_S, I_C, and I_L waveforms are shown in Figure 5.30 (b).



(a)



(b)

Figure 5.30 Transient performance of CHB-MLI based SAPF with proposed controller under R-L loading condition (a) load increment, and (b) load decrement

SAPF performance is also tested when SAPF unit is switched off from grid. Figure 5.31 shows that transition of source current is smooth when SAPF unit is switched off. Compensating current which is supplied by the inverter unit also becomes zero while inverter unit is detached from grid.

5.7.2 Uncontrolled Rectifier and R-C Loading

SAPF performance is not only tested with R-L loading condition, it has been tested with R-C loading conditions also. Steady-state MLI based SAPF waveforms of the proposed system with R-C type of non-linear loading are depicted in Figure 5.32 (a)-(b).Figure 5.31 (a) shows waveform of sinusoidal V_S and non-linear I_S due to the

presence of diode-bridge rectifier based resistive-capacitive loading into the existing system.

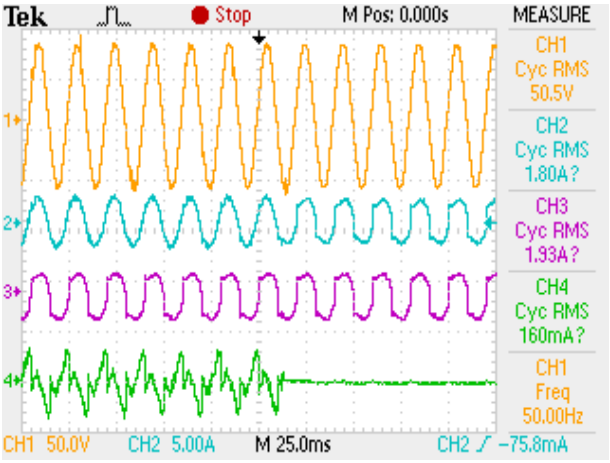
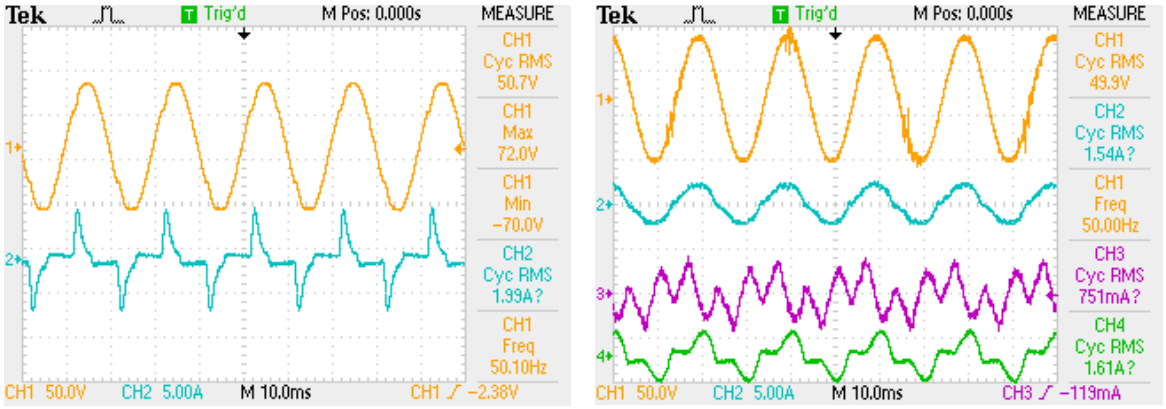


Figure 5.31 Transient performance of CHB-MLI based SAPF during switching off condition

Figure 5.32 (b) shows steady-state SAPF performance in terms of V_S, I_S, I_C, and I_L. that source current is in phase with source voltage. Therefore, unity power factor at the source side is maintained. It is observed that there is significant reduction of phase error with advanced controller. Figure 5.32 (b) shows V_S, I_S, I_L, and I_C waveform during the steady-state operation of MLI based SAPF unit.



(a) (b)

Figure. 5.32 Steady-state performance of CHB-MLI based SAPF with proposed control algorithm under R-C loading condition (a) V_S with non-linear I_S, and (b) V_S, I_S, I_C, and I_L steady-state waveform (CH1: 50V/div., CH2: 5A/div., CH3: 5A/div., CH4: 5A/div.)

Figure 5.33 shows that after the successful operation of SAPF unit, I_S becomes in phase with V_S, therefore it is maintaining unity power factor in the source side. Inverter

output voltage is also plotted for the sake of explanation of MLI operation. Five-level inverter output is generated which can be seen from Figure 5.33.

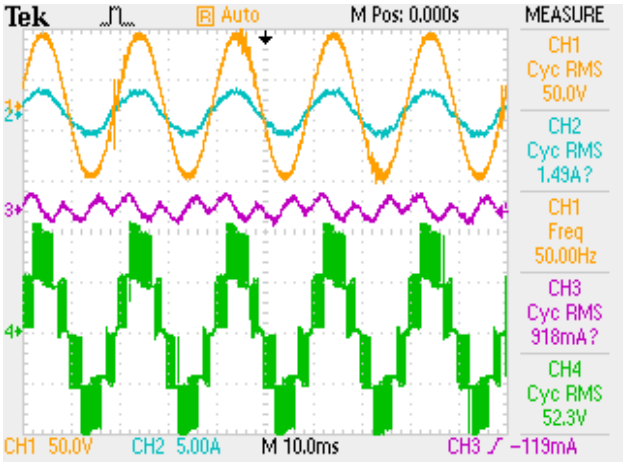
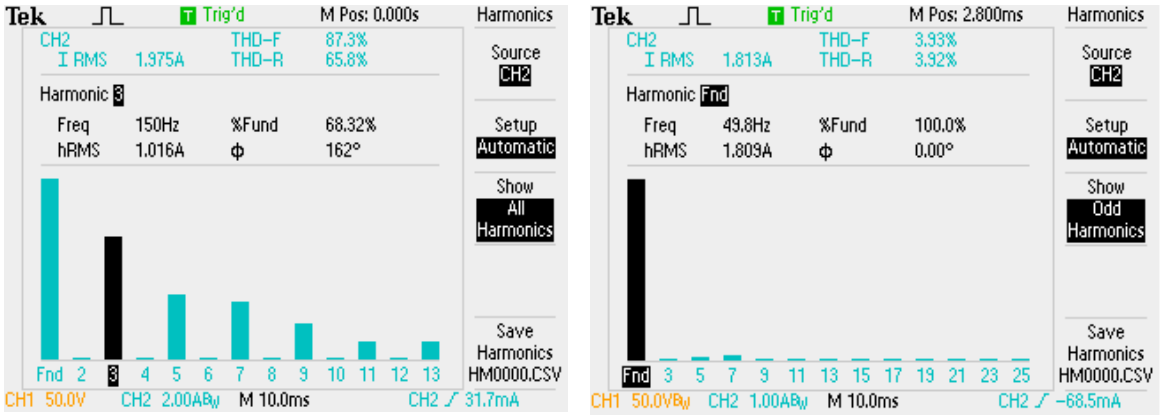


Figure 5.33 Steady-state performance of MLI based SAPF including inverter voltage with R-C loading

Source current THD was 87.30% due to presence of R-C type of non-linear loading which is shown in Figure 5.34 (a). However, after successful operation of MLI based SAPF unit, source current THD becomes 3.93% which can be seen from Figure 5.34 (b).

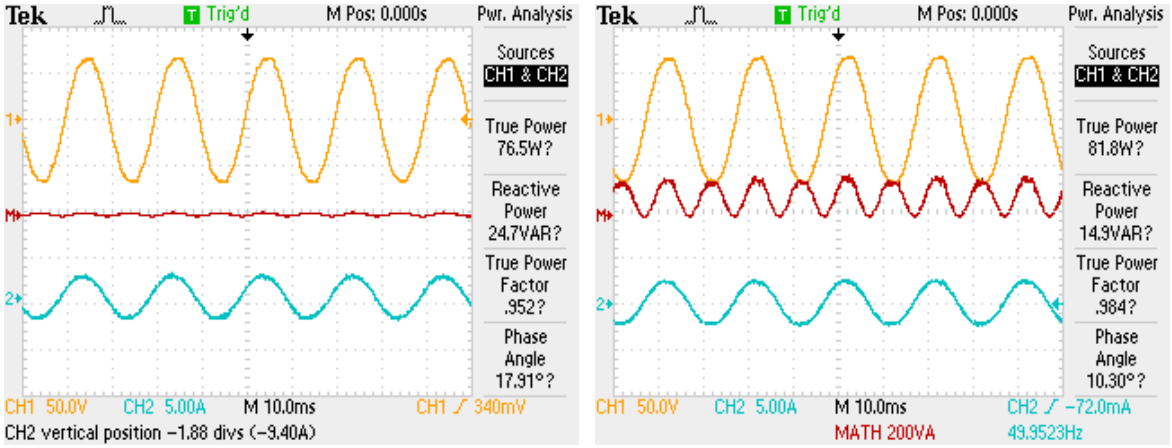


(a) (b)

Figure 5.34 THD of source current under R-C loading condition (a) before Compensation, and (b) after compensation

Controller effectiveness of the proposed controller is again compared with the conventional controller [123, 124] based SAPF system with resistive-inductive loading condition. The detailed comparative analysis between these two controllers is shown in Figure 5.35 (a) - (b). Figure shows comparative analysis between traditional and

proposed control theories in terms of reactive power compensation capability of the control algorithm. Figure depicts that the power factor of source side is improved from 0.85 to 0.952 with conventional controller whereas power factor improves up to 0.984 with proposed controller.



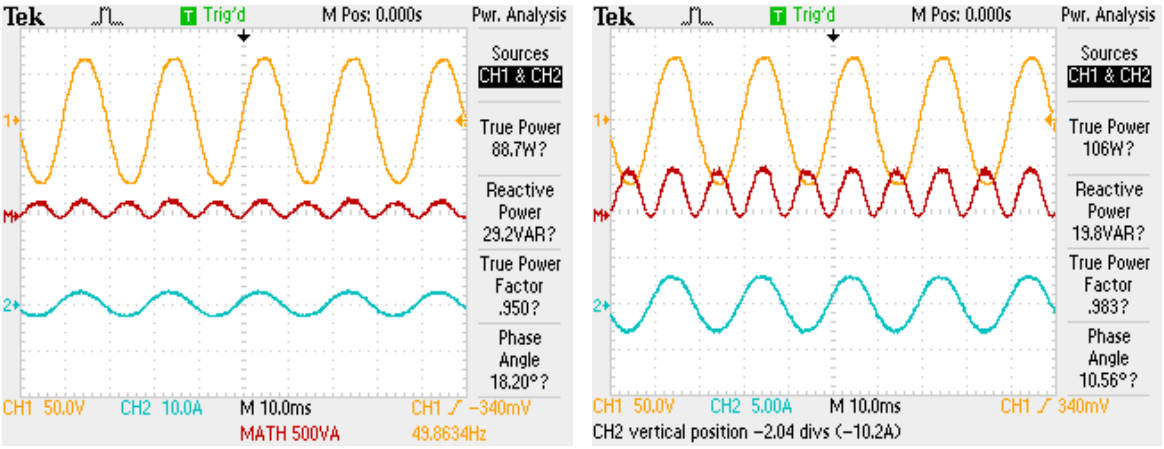
(a) (b)

Figure 5.35 Performance comparison of proposed control algorithm with conventional control in terms of reactive power compensation with R-L load (a) power factor and reactive power with conventional controller, and (b) power factor and reactive power with proposed controller

Reactive power compensation capability is also tested with resistive-capacitive type of non-linear loading. Figure 5.36 (a) - (b) shows comparative analysis between traditional and proposed control theories in terms of reactive power compensation capability of the control algorithm with R-C loading condition. Figure depicts that the power factor of source side is improved from 0.85 to 0.950 with conventional controller whereas power factor improves up to 0.983 with proposed controller.

The proposed control applied to CHB-MLI gives satisfactory performance and measured percentage THD value is also as per IEEE defined international standard both in simulation study as well as in hardware validation. The detailed experimental analysis demonstrates that the advanced current controller can generate current with better quality compared to conventional current controller in terms of source current magnitude with reduced THD and better reactive power minimization. The proposed controller also helps to maintain better power factor during its operation with different non-linear loading.

Therefore, proposed controller shows excellent performance over conventional controller in case of filtering application.



(a) (b)

Figure 5.36 Performance comparison of proposed control algorithm with conventional control in terms of reactive power compensation with R-C load (a) power factor and reactive power with conventional controller, and (b) power factor and reactive power with proposed controller

5.8 CONCLUSION

PI- VPI compensator based novel current control strategy for CHB-MLI based SAPF has been presented in this chapter in order to nullify current harmonic component from source current. This controller shows excellent selective harmonic elimination capability thereby steady-state current error has been removed. Particle-swarm optimization (PSO) based systematic approach is presented for optimal tuning of PI-VPI compensator gain parameters. PSO approach operates with a cost function by considering source current THD and steady-state error of current control loop. Closed-loop control stability is also analyzed with root-locus criteria. Moreover, a comparative performance analysis of proposed optimal tuned current controller is also demonstrated with PI compensator based current controller. Extensive simulation and experimental analysis of proposed system shows superior performance of proposed controller over conventional compensator based current controller. Therefore, it can be concluded that PSO assisted PI-VPI controller is a promising approach for CHB-MLI based SAPF in order to maintain better quality source current with zero steady-state error.

CHAPTER 6

DESIGN OF ADVANCED PLL BASED IMPROVED SYNCHRONOUS REFERENCE FRAME CONTROL ALGORITHM

List of Publications

1. **S. Ray**, N. Gupta, R. A. Gupta, "Mathematical and Experimental Investigation on Advanced PLL for Cascaded H-Bridge Multilevel Inverter in Active Filtering Application," *Electric Power Components and Systems*, Taylor and Francis. **(In Press)**
2. **S. Ray**, N. Gupta, R. A. Gupta, "Improved Single Phase SRF Algorithm for CHB Inverter Based Shunt Active Power Filter under Non-ideal Supply Conditions," in *Proc. of 9th IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov. 2017, Bangalore, pp. 1-6.

CHAPTER 6

DESIGN OF ADVANCED PLL BASED IMPROVED SYNCHRONOUS REFERENCE FRAME CONTROL ALGORITHM

[An improved synchronous reference frame theory based control algorithm is proposed in this chapter for solving current related power quality problems. This proposed control is a complete solution in case of balanced and/or unbalanced loading condition in existing distribution system. This control algorithm is equally effective in case of distorted and/or unbalanced supply voltage condition due to the use of advanced PLL. Performance of conventional PLL degrades to a great extent due to the presence of dc offset and harmonic component in the grid voltage since this will result phase angle and frequency error. Therefore, an advanced PLL having dc and harmonic rejection capability is presented in this chapter. The advanced PLL can track frequency and phase angle accurately even though source voltage is polluted. A detailed mathematical modeling and stability analysis of this PLL is presented using Routh-Hurwitz criteria. A systematic design procedure using Eigen value analysis is proposed for calculating PLL parameters. Closed-loop SAPF control stability is tested using root-locus analysis. An extensive simulation and experimental study of advanced PLL and CHB-MLI based SAPF has been performed under highly distorted source voltage and different non-linear loading conditions to show the effectiveness of the advanced PLL over recently published work. Source current maintains its sinusoidal shape, properly synchronized with grid voltage and having distortion limit in compliance with IEEE-519 standard irrespective of source voltage conditions during the operation of SAPF unit.]

6.1 INTRODUCTION

One significant aspect of harmonic current compensation and reference current generation is the design of the overall control system for CHB-MLI based SAPF. The main concern while designing control algorithm is simplicity, robustness and accuracy. A significant amount of researches are already done in the area of control mechanism and reference current generation. Researchers have proposed many control algorithms related to SAPF applications. However, performance of most of the control theories is not satisfactory in distorted, unbalanced supply and/or unbalanced loading conditions [185-190]. In literatures, peak-detection based control is proposed by Singh et al. [184] but this theory is tested in balanced loading and balanced source voltage condition only. A novel control strategy is proposed in [16] by Silva et al. [181] which can work in distorted source voltage conditions as well as unbalanced loading. However, detailed calculation

and analysis is not shown. A single-phase P-Q theory based control is proposed and implemented by Arya et al. [184] which can takes care of zero voltage regulation and improvement of power factor. However, performance of the algorithm is not tested with distorted and unbalanced supply condition. As per available literatures, potential of most of control theories are not tested in different possible scenarios. So, effectiveness of control algorithm should be tested under distorted source voltage condition also.

Phase-Locked Loop (PLL) plays an important role in case of active filtering applications in maximum number of control algorithms. Maximum number of conventional and modified control theories for single- and three-phase SAPF depends on PLL. S. Arya et al. used software PLL for active filtering applications [184] whereas synchronous-reference frame-PLL (SRF-PLL) is commonly used for synchronization which suffers from double-frequency error. PLL also suffers from accuracy issue in distorted voltage condition. Enhanced-PLL (E-PLL) resolves above mentioned problems to some extent, however presence of dc component may degrade dynamic performance of the system. DC component may be present in the existing system due to offset of DC/ AC voltage sensors, characteristics mismatch among semiconductor switches, dc offset in Analog to Digital converters etc [185-188]. Presence of dc component results low frequency ripple in the PLL loop. It also degrades the performance of amplitude estimation loop. Consequently, several PLLs have been used in literature but removal of dc components has not been taken care of by the most of the researchers. Meticulous research need to be done in this area for better control performance. Labura et al. [185] proposed a PLL structure in order to reject dc offset. This PLL structure used park's transformation for phase angle measurement. Alpha component of the input voltage signal and polluted input voltage is compared and passed through an integrator circuit for removing dc component from the circuit. Golestan et al. [186] proposed SRF-PLL based approach for rejecting dc component from polluted supply. Phase detection scheme of this PLL is also working on the basis 'abc' to 'alpha-beta' transformation. Delayed signal is used for mitigating dc component from polluted input supply. However, computational burden and transformation from 'abc' to 'alpha-beta' frame are major drawbacks of these PLLs. Kulkarni et al. [187, 188] presents an improved version of generalized integrator based PLL (FR-PLL) in order to get rid of dc offset. Two numbers of second order GIs

are connected in cascaded manner and finally ‘alpha-beta’ component is fed to SRF-PLL. At the same instant, bandwidth selection of SRF-PLL affects dynamic response time. An improved E-PLL based approach is designed and used for grid-tied photovoltaic (PV) system to get rid of dc components by Verma et al. [189]. Improved E-PLL is capable of exact measurement of phase angle, fundamental component extraction from polluted signal and DC component removal but its effectiveness is tested only in case of normal condition.

Effectiveness of this PLL [189] should be tested in presence of dc component as well as its performance need to be tested rigorously in highly distorted source voltage condition. At the same instant, its performance is not compared with recently proposed PLLs which are capable of dc component rejection. This PLL is applied for improving control technique of grid connected solar inverter. However, grid connected inverter performance is not tested under distorted supply voltage condition or in presence of dc component. This PLL is yet to be applied in case of MLI based SAPF applications where exact phase measurement is required in order to give better source current compensation and for maintaining near about unity power factor with presence of highly non-linear loading conditions. Still, a proper and effective designing procedure of advanced PLL parameters is missing from literatures. A systematic design procedure of PLL parameters need to be adopted for MLI based SAPF application as performance of SAPF depends on PLL parameters to a great extent.

Therefore, advanced PLL based improved control algorithm is used in this chapter for CHB-MLI based active filtering application. This control algorithm is equally effective in normal as well as distorted source voltage conditions. Projected PLL used in this control theory is having better amplitude and frequency measurement potential along with phase angle detection approach in distorted grid voltage condition as well as in presence of dc component in the existing line. Performance of the PLL is tested rigorously under highly distorted source voltage condition and in presence of dc component. Same has been compared with recently proposed FR-PLL. Theoretical and practical performance of the PLL is tested with source voltage having odd-, even-harmonic and/or dc component. Finally, this PLL has been applied to CHB-MLI based SAPF for mitigating current related PQ problems in MV distribution sector. A detailed real-time performance

analysis of CHB-MLI based SAPF with proposed PLL based control algorithm is tested in different non-linear loading conditions. Transient as well as steady-state behavior of the proposed system shows its effectiveness under highly distorted grid condition as well as with the presence of dc component. Eigen value analysis is used as an effective tool to design of constant parameters for this PLL. In addition, a detailed mathematical modeling of advanced PLL is presented and its rigorous stability analysis has been tested using R-H criteria and bode diagram.

6.2 DESIGN AND DEVELOPMENT OF PROJECTED PLL

PLL plays a significant function for synchronizing inverter unit to grid with required frequency. Working mechanism of PLL depends upon supply voltage condition which affects accuracy of phase angle information and propagation of harmonic content throughout the algorithm. E-PLL, as shown in Figure 6.1 (a), can serve as a better alternative of existing PLL as it can work on distorted supply voltage conditions also. However some limitations of conventional PLL and E-PLL are listed out as follows [13]:

i. Proportional and integration constants of E-PLL can be tuned up to a particular range in terms of stability,
ii. Distortion and noise can affect the system performance,
iii. Presence of dc component results low frequency ripple in the PLL loop which also degrades the performance of amplitude estimation loop,
iv. Performance of PLL is dependent of internal parameter selection,
v. Double-frequency ripple in the loop affects the performance of conventional PLL.

In concern to these aforesaid issues, an advanced PLL algorithm, shown in Figure 6.1 (b), is designed and implemented for MLI based active filtering application. The projected PLL consists of two loops, i.e. amplitude measurement loop and phase angle measurement loop. The phase angle measurement loop guarantees the phase error between reference and input voltage to zero. An integrator is used for checking the power frequency variations. This loop confirms steady state error to zero even in varying frequency conditions. Fundamental component amplitude of input voltage can be calculated from amplitude estimation loop which also ensures the removal of double-frequency error as well as removal of higher frequency components. This PLL consists of one extra branch for mitigating DC components from the PLL loop. Additional integrator

present in that extra branch detects dc component. The estimated dc component finally adds to the output, therefore no dc component is present in the PLL loop while calculating magnitude error. The same has been validated through simulation as well as in hardware results in later section. This PLL though has a simple and robust structure then also it is useful for extracting important information like magnitude, frequency, phase of signal, fundamental component, dc and total harmonic component present from a signal. This PLL can be implemented in digital platform like DSPs, dSPACE 1104 effectively with minimum calculation. Phase tracking is an important aspect for synchronization with utility grid in polluted source voltage condition which is also performed accurately by projected PLL.

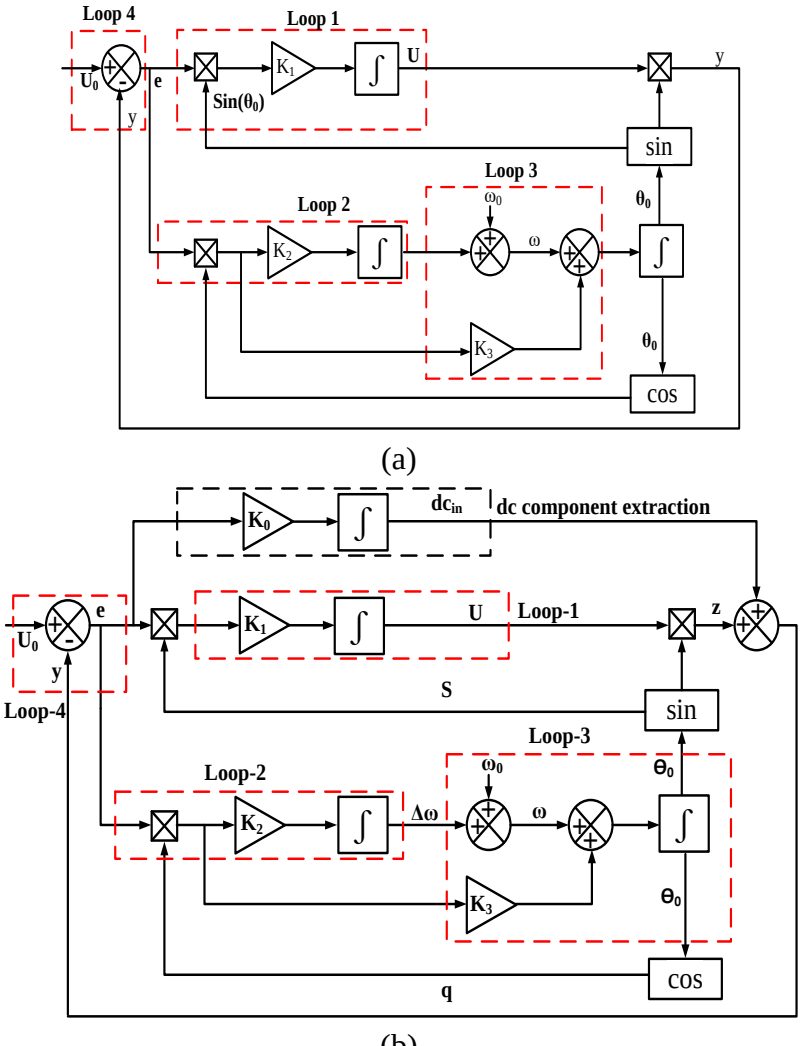


Figure 6.1 (a) E-PLL, and (b) Advanced PLL

6.2.1 Mathematical Modeling using Transfer Function Approach

As the advanced PLL is employed from the concept of E-PLL, the working principle and issues related to E-PLL need to be reviewed. Therefore, in this section, E-PLL is reviewed first briefly and design of advanced PLL is discussed in later subsection.

Review of Enhanced PLL:

In normal supply voltage condition, E-PLL can estimate peak magnitude of an input signal, frequency and phase angle of input signal accurately. The following equations of estimated magnitude (U), frequency ($\Delta\omega_0$) and phase angle (θ_0) can be formulated from Figure 6.1 (a).

$$\dot{U} = K_1 . e . \sin\theta_0 \; ; \quad \Delta\dot{\omega}_0 = K_2 e \cos\theta_0 \; ; \quad \dot{\theta_0} = \omega \; + K_3 e \cos\theta_0 \tag{6.1}$$

The error signal is defined as per Equation 6.2 by solving Loop 4 of Figure 6.1 (a).

$$e = U_0 - y \text{ and } y = U \sin\theta_0 \tag{6.2}$$

Let, input signal contains some dc component which is denoted by dc_{in}. Then the polluted voltage goes through E-PLL structure. Then, input to the E-PLL may be defined as per Equation 6.3.

$$U_0 = U_{in} \sin\theta_A + dc_{in} \tag{6.3}$$

where, θ_A is phase angle of input voltage.

Input to loop 2 of E-PLL is denoted by Equation 6.4 as shown in Figure 6.1(a), which is found by solving the loop.

$$e . \cos\theta_0 = [(U_{in} \sin\theta_A + dc_{in}) - U \sin\theta_0] \cos\theta_0$$

Therefore,

$$\begin{aligned} e . \cos\theta_0 = & \underbrace{(U_{in}/2 . \sin(\theta_A - \theta_0))}_{A} + dc_{in} . \cos\theta_0 \\ & + [\underbrace{- U_{in}/2 . \sin(\theta_A + \theta_0)}_{B} - U/2 . \sin 2\theta_0] \end{aligned} \tag{6.4}$$

At steady state after the successful operation of E-PLL unit, θ_0 will be equal to θ_A and magnitude of U will becomeU_{in}. Therefore, 'B' term will be zero at steady-state. Still dc components and low frequency components are present as depicted from 'A' term of Equation 6.4. Thus PLL experiences a lower frequency ripple as well as it influences calculation related to amplitude estimation.

Design of Advanced PLL:

Advanced PLL improves E-PLL structure capability by removing its main drawback i.e. presence of dc component in the existing loop. Therefore, when dc component is present in the input voltage, advanced PLL can detect and mitigate dc component with another branch comprising integrator as shown in Figure 6.1(b). In the advanced PLL, U, $\Delta\omega_0$, θ_0 and dc_{in} can be represented as follows:

$$\dot{U} = K_1 . e . \sin\theta_0; \quad \Delta\dot{\omega}_0 = K_2 . e . \cos\theta_0; \quad \dot{\theta_0} = \omega_0 + K_3 . e . \cos\theta_0; \quad \dot{dc_{in}} = K_0 . e \tag{6.5}$$

Therefore, error signal consists of a dc and harmonic content which is given by Equation 6.6. This equation confirms mitigation of dc component in the PLL loop.

$$e = Y - dc_{in} - U \sin\theta_0 \tag{6.6}$$

Signal S in Figure 6.1(b) is used for synchronization of phase angle with input signal and its operation is not dependent on input signal magnitude. The speed of dc component estimation loop is determined by K_0. Design parameters, K_2 and K_3 can be selected on the basis of accuracy and estimation process speed. Gain parameters K_0, K_1, K_2, K_3 not only affect steady-state stability but also it is responsible for better dynamic performance of the control system. Therefore, a design procedure of these gain parameters using Eigen value analysis has been presented as a proficient tool which is described in Section 6.2.2.

6.2.2 Selection of Gain Parameters in Advanced PLL

The magnitude of constant parameters K_1, K_2 and K_3 are found from Figure 6.1(a) when dc component is absent. The output of the phase detection circuit is given as Equation 6.7.

$$\begin{aligned} e . \cos\theta_0 &= (U_{in} \sin\theta_A - U \sin\theta) \cos\theta_0 \\ &= (U_{in}/2 . \sin(\theta_A - \theta_0)) - U_{in}/2 . \sin(\theta_A + \theta_0) - U/2 . \sin 2\theta_0 \end{aligned} \tag{6.7}$$

In steady-state condition, U becomes U_i and θ_0 becomes θ_A. Therefore double frequency terms can be omitted.

So, $e . \cos\theta_0$ can be represented as $(U_{in}/2 . \sin(\theta_A - \theta_0))$ and

$$\begin{aligned} e . \sin\theta_0 &= [U_{in} \sin\theta_A - U \sin\theta] \cos\theta_0 \\ &= (U_{in}/2 . \cos(\theta_A - \theta_0)) - U/2 - U_{in}/2 . \cos(\theta_A + \theta_0) \\ &+ U/2 . \cos 2\theta_0 \end{aligned} \tag{6.8}$$

After double frequency term cancellation, it becomes,

$$e.\sin\theta_0 = (U_{in}/2\,.\cos(\theta_A - \theta_0)) - U/2 \tag{6.9}$$

Estimated voltage magnitude, phase angle and frequency are found out from Figure 6.1(a) and loop 1, 2 and 3. These are shown in Equation 6.10.

$$\begin{cases} \dot{U} = K_1.e.\sin\theta_0 = K_1(U_{in}/2\,.\cos(\theta_A - \theta_0)) - K_1.U/2 \\ \dot{\Delta\omega} = K_2.e.\cos\theta_0 = K_2(U_{in}/2\,.\sin(\theta_A - \theta_0)) \\ \dot{\theta_0} = \omega_0 + \dot{\Delta\omega} + K_3.e.\cos\theta_0 = \omega_0 + \Delta\omega + K_3.(U_{in}/2\,.\sin(\theta_A - \theta_0)) \end{cases} \tag{6.10}$$

Three new variables are defined for further calculations which are defined as $\breve{U} = U - U_{in}, \tilde{\omega} = \omega - \omega_{in}, \text{and } \tilde{\theta} = \theta - \theta_{in}$. Equation 6.10 can be rewritten by linearizing and replacing new variables. It can be depicted as per Equation 6.11.

$$\begin{cases} \dot{\breve{U}} = -K_1/2\,.\breve{U} \\ \dot{\tilde{\omega}} = -K_2/2\,.U_{in}.\tilde{\theta} \\ \dot{\tilde{\theta}} = \dot{\omega} - K_3.U_{in}/2\,.\tilde{\theta} \end{cases} \tag{6.11}$$

Amplitude selection loop can be described as a first order system and its time constant is defined by

$$\tau = 2/K_1 \tag{6.12}$$

Equation 6.11 can be rewritten as

$$\begin{bmatrix} \dot{\tilde{\omega}} \\ \dot{\tilde{\theta}} \end{bmatrix} = \begin{bmatrix} 0 & -K_2/2\,.U_i \\ 1 & -K_3/2\,.U_i \end{bmatrix} \begin{bmatrix} \tilde{\omega} \\ \tilde{\theta} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [U_{in}] \tag{6.13}$$

State-space equation of the system can be represented as,

$$[Q] = \begin{bmatrix} s & K_2/2\,.U_{in} \\ -1 & s + K_3/2\,.U_{in} \end{bmatrix} \tag{6.14}$$

So, it can be written as

$$|Q| = s^2 + K_2/2\,.U_{in}.s + K_3/2\,.U_{in} = 0 \tag{6.15}$$

Characteristics equation of $|Q|$ can be written as,

$$q(s) = s^2 + K_2/2\,.U_{in}.s + K_3/2\,.U_{in} = 1 + G(s) \tag{6.16}$$

By comparing Equation 6.15 and 6.16, this can be written as,

$$G(s) = K_3U_{in}/2s + K_2U_{in}/2s^2 \tag{6.17}$$

So, transfer function of the proposed system can be written as,

$$T(s) = (K_3 U_{in} s/2 + K_2 U_{in}/2)/(s^2 + K_3 U_{in} s/2 + K_2 U_{in}/2) \quad (6.18)$$

Equation 6.19 can be written by comparing Equation 6.16 to second order system transfer function and it can be written as Equation 6.19.

$$\begin{cases} \omega_r^2 = K_2 U_{in}/2 \\ 2\zeta\omega_r = K_3 U_{in}/2 \end{cases} \quad (6.19)$$

Advanced PLL loop equations can be depicted as shown in Figure 6.1(b). The same parameters are also estimated for advanced PLL. These are given as Equation 6.20 as follows.

$$\begin{cases} \dot{U} = K_1 . e . \sin\theta_0 \\ \dot{\omega} = K_2 . e . \cos\theta_0 \\ \dot{\theta} = K_3 . e . \cos\theta_0 + \omega_0 \\ \dot{dc_{in}} = K_0 . e \\ e = U_0 - U . \sin\theta_0 - dc_{in} \end{cases} \quad (6.20)$$

By removing double frequency terms, Equation 6.20 can be rewritten as Equation 6.21.

$$\dot{\theta} = K_3 . e . \cos\theta_0 + \omega_0 = (K_3 . U_0 - K_3 . dc_{in})\cos\theta_0 + \omega_0$$
$$\text{and} \quad (6.21)$$
$$\dot{dc_{in}} = K_0 (U_0 - U . \sin\theta_0 - dc_{in})$$

By linearizing Equation 6.21, this can be formed as Equation 6.22.

$$\begin{bmatrix} \dot{\theta} \\ \dot{dc_{in}} \end{bmatrix} = \begin{bmatrix} 0 & -K_3 \\ -K_0 U & -K_0 \end{bmatrix} \begin{bmatrix} \theta_0 \\ dc_{in} \end{bmatrix} + \begin{bmatrix} K_3 \\ K_0 \end{bmatrix} U_0 \quad (6.22)$$

By Eigen value analysis, roots are $-K_0 \pm \sqrt{{K_0}^2 + 4K_0 K_3 U}/2$. In order to maintain stability criteria, Equation 6.23 must be satisfied.

$$\sqrt{K_0^2 + 4K_0 K_3 U} < K_0 \quad (6.23)$$

So, gain constant parameters K_0, K_1, K_2 and K_3 can be found from Equation 6.12, Equation 6.19 and Equation 6.23 which are implemented in advanced PLL for simulation and experimental study. The selection of gain parameters of projected PLL has a great impact on system performance as these gain parameters are selected based on system stability. Therefore, this selection method provides good steady-state and transient performance of advanced PLL.

6.2.3 Stability Analysis using Transfer Function Approach

Transfer function approach has been used for finding out the mathematical modeling of this PLL. Three state variables X_0, X_1 and X_2 are being considered for stability analysis of the projected system. Variable X_1 represents filtered component of polluted signal, X_2 represents orthogonal component of filtered version and X_0 represents low-pass component of polluted signal. Constant parameters α and α_0 define bandwidth of filter circuit. Figure 6.2 (b) - (f) show flow-diagram for these three state variables.

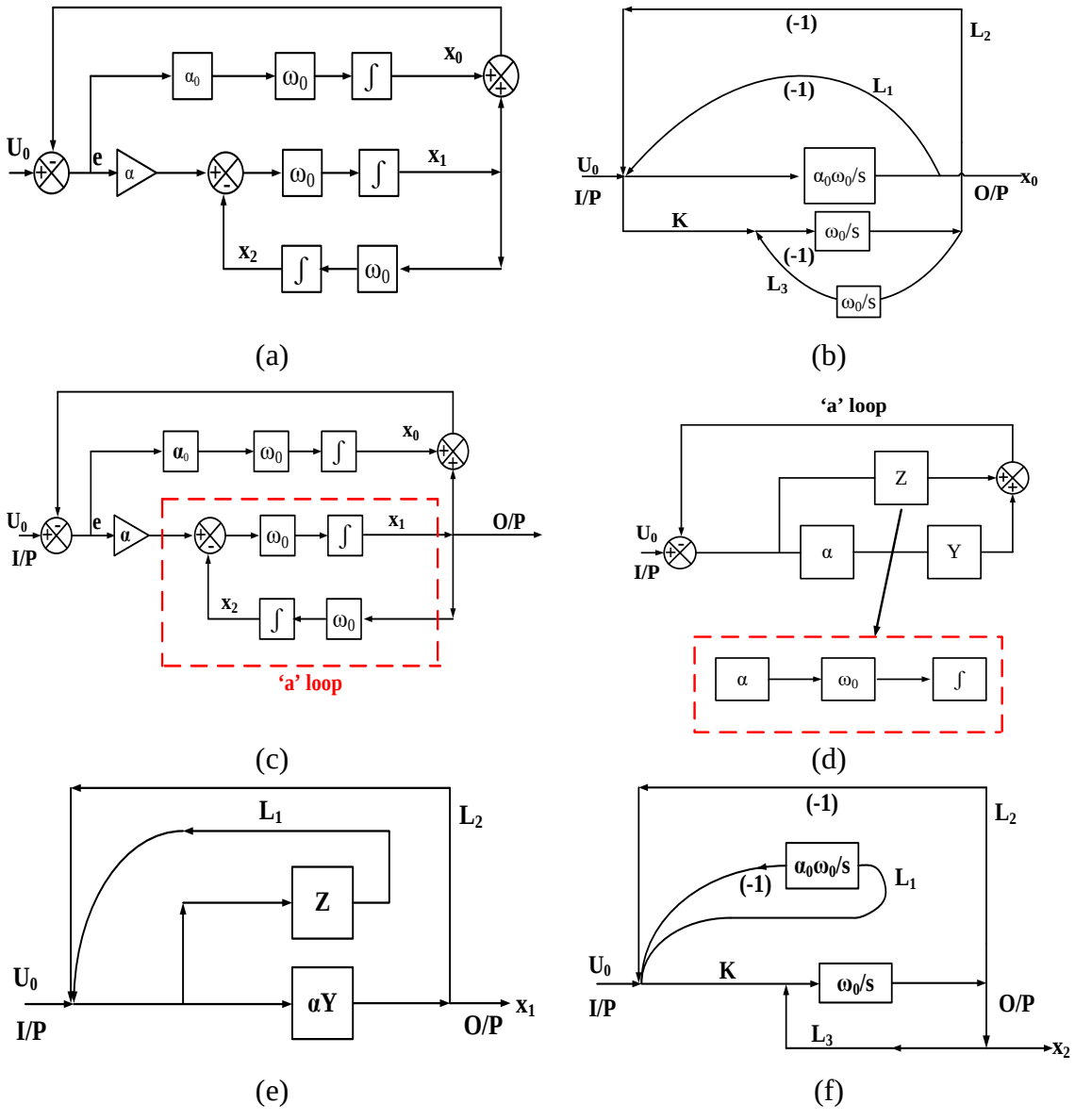


Figure 6.2 (a) SOGI based OSG diagram of advanced PLL, (b) loop diagram for X_0/U_0, (c) rearranged loop diagram for X_0/U_0, (d) simplified loop diagram for X_0/U_0, (e) loop diagram for X_1/U_0, and (f) loop diagram for X_2/U_0

Second-order generalized-integrator (SOGI) based circuit is shown in Figure 6.2 (a). From Figure 6.3 (b), while calculating transfer function $X_0(s)/U_0(s)$, forward path gain can be calculated as $P_1 = \alpha_0.\omega_0/s$ and number of loops present in the circuit is three numbers which can be denoted by L_1, L_2 and L_3. One number of non-touching loop is also present in the circuit. The forward path gains can be calculated as:

$$\left.\begin{aligned} L_1 &= (\alpha_0.\omega_0/s).(-1) = -\alpha_0.\omega_0/s \\ L_2 &= (\alpha).(\omega_0/s).(-1) = -(\alpha.\omega_0/s) \\ L_3 &= (\omega_0/s).(-\omega_0/s) = -(\omega_0^2/s^2) \end{aligned}\right\} \quad (6.24)$$

Transfer function can be calculated according to Mason's Gain formula. $X_0(s)/U_0(s)$ can be calculated with the help of Equation 6.28. Final transfer function can be shown as per Equation 6.25.

$$TF = \frac{\sum P_1\Delta_i}{\Delta}$$

Therefore,

$$\frac{X_0(s)}{U_0(s)} = \frac{(\alpha_0.\omega_0/s).[1-(-\omega_0^2/s^2)]}{1+[\{-(\sum \text{all loops})\} + (\text{sum of product of non}-\text{touching loops})]}$$

$$\frac{X_0(s)}{U_0(s)} = \frac{(\alpha_0.\omega_0/s).(s^2+\omega_0^2/s^2)}{1+[\{-(-\alpha_0.\omega_0/s-\alpha.\omega_0/s-\omega_0^2/s^2)\}+\{(-\alpha_0.\omega_0/s)(-\omega_0^2/s^2)\}]}$$

Hence,

$$\frac{X_0(s)}{U_0(s)} = \frac{\alpha_0.\omega_0(s^2+\omega_0^2)/s^3}{1+[(\alpha_0.\omega_0/s+\alpha.\omega_0/s+\omega_0^2/s^2)+\alpha_0.\omega_0^3/s^3]}$$

$$\frac{X_0(s)}{U_0(s)} = \frac{\alpha_0.\omega_0(s^2+\omega_0^2)}{s^3+(\alpha+\alpha_0)\omega_0.s^2+\omega_0^2.s+\alpha_0.\omega_0^3} \quad (6.25)$$

Using the concept of mason's gain formula, transfer function $X_1(s)/U_0(s)$ is also calculated. Based on Figure 6.2 (c), (d) and (e), forward path gains, touching and non-touching loops are decided. Forward path gain is decided by $P_1 = \alpha Y$. Two numbers of loops are present while calculating transfer function with respect to X_1 and no non-touching loops are present which are demonstrated by Equation 6.26.

$$L_1 = Z*(-1) = -Z,\ L_2 = \alpha Y*(-1) = -\alpha Y \quad (6.26)$$

Two smaller loops are being considered for simplification of the calculation. These are denoted by Y and Z. These two loops are denoted by:

$$Y = \frac{\omega_0/s}{1+\omega_0^2/s^2} = \frac{\omega_0.s}{\omega_0^2+s^2} \text{ and } Z = \alpha_0 * \omega_0/s \tag{6.27}$$

Finally, transfer function is calculated as per Equation 6.28 according to mason's gain formula which is represented by

$$TF = \frac{\sum P_1\Delta_i}{\Delta}$$

$$\text{Therefore,} \quad \frac{X_1(s)}{U_0(s)} = \frac{\alpha Y}{1-(-Z-\alpha Y)} = \frac{\alpha Y}{1+Z+\alpha Y}$$

$$\text{Hence,} \quad \frac{X_1(s)}{U_0(s)} = \frac{\alpha.\omega_0.s/(\omega_0^2+s^2)}{[1+(\alpha_0\omega_0/s)+(\alpha\omega_0 s/\omega_0^2+s^2)]}$$

$$\frac{X_1(s)}{U_0(s)} = \frac{\alpha.\omega_0.s/(\omega_0^2+s^2)}{[s(\omega_0^2+s^2)+\alpha_0\omega_0(\omega_0^2+s^2)+\omega_0.s^2]/s(\omega_0^2+s^2)}$$

$$\frac{X_1(s)}{U_0(s)} = \frac{\alpha.\omega_0.s^2}{s^3+(\alpha+\alpha_0)\omega_0 s^2+\omega_0^2 s+\omega_0^3\alpha_0} \tag{6.28}$$

Transfer function of X_2 with respect to input U_0 is found from Figure 6.2 (f). Forward path gain is represented by $\alpha.\omega_0^2/s^2$. Three numbers of loops (L_1, L_2 and L_3) are present where L_1 and L_3 are non-touching loops.

$$\left.\begin{aligned} L_1 &= -(\alpha_0\omega_0/s) \\ L_2 &= \alpha.(\omega_0/s).(-1) = -\alpha.\omega_0/s \\ L_3 &= \omega_0/s\,.\,\omega_0/s\,.(-1) = -\omega_0^2/s^2 \end{aligned}\right\} \tag{6.29}$$

Therefore, transfer function $X_2(s)/U_0(s)$ may be represented as per Equation 6.30.

$$\frac{X_2(s)}{U_0(s)} = \frac{(\alpha.\omega_0^2/s)}{1-\{-(-\alpha_0\omega_0/s-\alpha.\omega_0/s-\omega_0^2/s^2)\}+L_1.L_3}$$

Hence,

$$\frac{X_2(s)}{U_0(s)} = \frac{\alpha.\omega_0^2/s}{1+\alpha_0\omega_0/s+\alpha.\omega_0/s+\omega_0^2/s^2+\alpha_0\omega_0^3/s^3}$$

Therefore,

$$\frac{X_2(s)}{U_0(s)} = \frac{s.\alpha.\omega_0^2}{s^3+(\alpha+\alpha_0)\omega_0 s^2+\omega_0^2 s+\omega_0^3\alpha_0} \tag{6.30}$$

From Equation 6.25, Equation 6.28 and Equation 6.30, according to Routh-Hurwitz criteria, R-H table of open-loop transfer function is plotted and it is given in Table 6.1. As constants α, α_0 and ω_0 are positive quantity, therefore no sign change is there in the first column of the R-H table. From this, one can clearly conclude that

advanced PLL system is stable. The system stability of advanced PLL is compared with E-PLL with the help of bode plot to prove the effectiveness of the system. From magnitude bode plot, it is seen that, slope of advanced PLL is less compare to E-PLL. System is well capable of handling more sudden changes as gain and phase margin also improves which can be decoded from Figure 6.3.

Table 6.1 R-H table of open loop transfer function of advanced PLL

s^3	1	ω_0^2	0
s^2	$(\alpha+\alpha_0)\omega_0$	$\alpha_0\omega_0^3$	0
s^1	$\frac{(\alpha+\alpha_0)\omega_0^3-\alpha_0.\omega_0^3}{(\alpha+\alpha_0)\omega_0}=\frac{\alpha_0.\omega_0^3}{(\alpha+\alpha_0)\omega_0}$ $=\frac{\alpha_0.\omega_0^2}{(\alpha+\alpha_0)}$	0	0
s^0	0	0	0

Gain margin of the advanced system is more positive than E-PLL based system. Frequency response curve provides information about phase delay. Initially, modified system is starting from zero while E-PLL is starting from -90 degree. This makes the advanced PLL system more stable with respect to E-PLL.

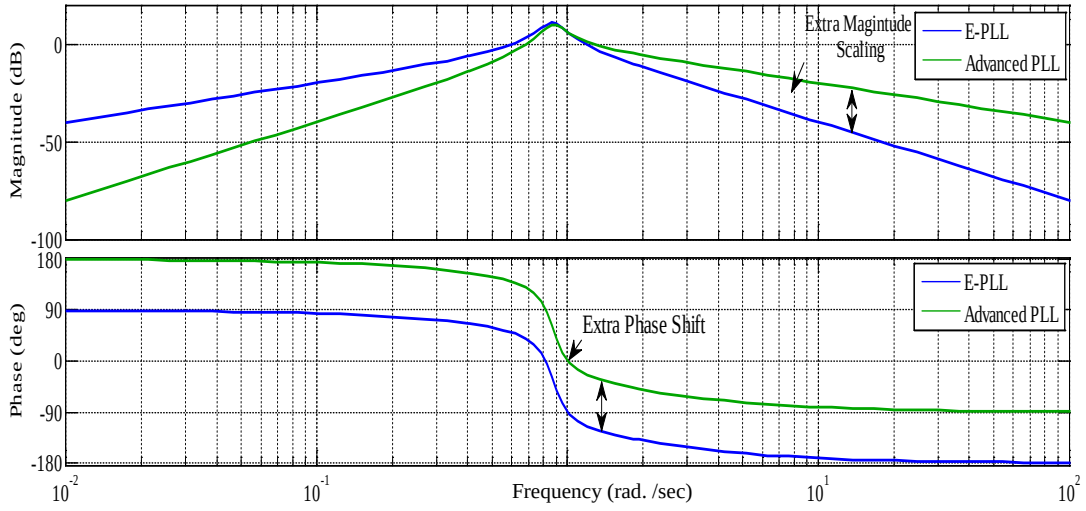


Figure 6.3 Bode plot comparison between E-PLL and advanced PLL

System stability is rigorously checked from the above analysis. Above mathematical and stability analysis of advanced PLL makes this system useful in active filtering applications.

6.3 DESIGN AND DEVELOPMENT OF ADVANCED SYNCHRONOUS REFERECNE FRAME CONTROL ALGORITHM

The proposed control technique can be divided in to four parts i.e. DC-link voltage controller, advanced PLL, sensing and reference current generation circuit and phase-shifted PWM technique. PI compensator is used for stabilizing six DC voltages used for three-phase five-level CHB-MLI. As nature of six voltage profiles are same in nature, tuning of dc-voltages are possible with only one PI compensator. This phenomenon helps to reduce complexity of control algorithm. The proposed control theory is composed of four main sections namely, reference current generation, PLL, DC-link voltage control and PS-PWM technique.

6.3.1 Reference Current Generation

Three phase load currents are being sensed by current sensors and each phase of load current is transferred to dq frame quantity separately with the help of transformation theory as per Equation 6.31.

$$\begin{bmatrix} i_{La\alpha} \\ i_{La\beta} \end{bmatrix} = \begin{bmatrix} i_{La}(\theta) \\ i_{La}\left(\theta - \frac{\pi}{2}\right) \end{bmatrix} \tag{6.31}$$

DC components (active and reactive) of each phase current are extracted by low pass filters which are defined as $i_{da\text{-}dc}$ for phase 'A', $i_{db\text{-}dc}$ for phase 'B', and $i_{db\text{-}dc}$ for phase 'C'. Source voltage waveforms are also being sensed by voltage sensors and passed through advanced phase locked loop circuit, as shown in Section 6.2.1, for generation of fundamental component from distorted and unbalanced supply. Inverter switching loss component is also supplied by dc voltage controller. The error is generated by comparing dc-link reference voltage and dc-link voltage of one capacitor. This error is minimized with PI compensator and the amount ($i_{pi.dc}$) is added to extracted active power component. These components are finally denoted as i_{Tdca}, i_{Tdcb} and i_{Tdcc} for phase 'A', phase 'B' and phase 'C', respectively, as shown in Figure 6.4. As this controller treats three-phase current amount separately, this control is well capable of working in case of unbalanced loading conditions also. Active component is extracted as per Equation 6.32.

$$i_{Tdc} = \sqrt{\frac{3}{2}} \cdot \left(\frac{i_{Tdca} + i_{Tdcb} + i_{Tdcc}}{3} \right) \tag{6.32}$$

Finally, dq components of reference current are converted to αβ component ($i_{\alpha T}$, $i_{\beta T}$) as per Equation 6.33.

$$\begin{bmatrix} i_{\alpha T} \\ i_{\beta T} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{Tdc} \\ i_q \end{bmatrix} \tag{6.33}$$

Two-axis component, α and β component of source current is finally converted to three-phase components which can be seen from Eqn. 6.34.

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{\alpha T} \\ i_{\beta T} \end{bmatrix} \tag{6.34}$$

The reference current generation technique is discussed in this section while advanced PLL and PS-PWM technique are described in later sections. This control can solve two purposes i.e. enhancement of power factor and mitigation of current harmonics. The flow diagram of overall control algorithm is depicted on Figure 6.4. Advanced PLL used in this control algorithm is already described in the previous section.

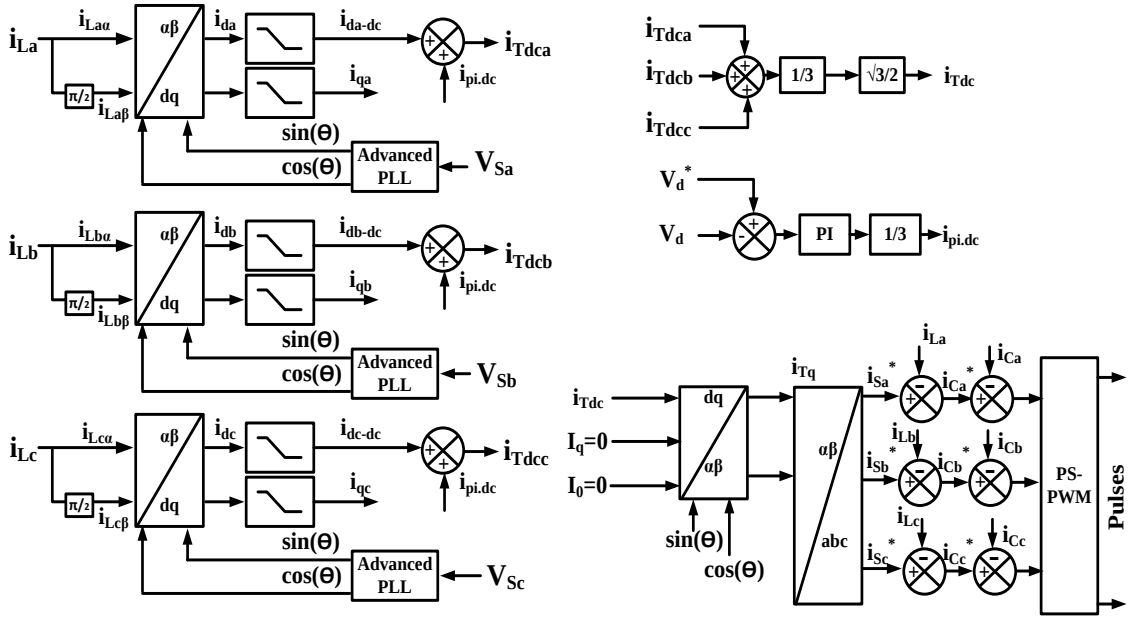


Figure 6.4 Control technique for five-level CHB-MLI based SAPF

6.3.2 DC-link Voltage Control

The exchanged active and reactive power between grid and MLI based SAPF is depicted as

$$p = i_d . v_{sd} \text{ and } q = -i_q . v_{sd} \tag{6.35}$$

DC-link voltages of H-bridges need to be maintained at its reference value for proper operation of SAPF unit. As DC-link voltage behavior of all H-bridges maintain almost same characteristics in steady-state condition, therefore, only one PI compensator is used to operate DC-link voltage at its fixed reference. This implementation also reduces the number of sensors in the MLI based SAPF circuit. Loss component of practical circuit component and losses due to inverter switching are supplied by DC-link voltage regulation. DC-link reference value is compared with actual measured DC-link voltage and is processed through PI compensator. Output of PI compensator can be depicted as Equation 6.36.

$$u_{dc} = K_P(V_d{}^* - V_d) + K_i \int (V_d{}^* - V_d)\, dt \tag{6.36}$$

DC-link voltage control circuit is shown in Figure 6.5. Transfer function of DC-link voltage controller can be obtained from Figure 6.5.

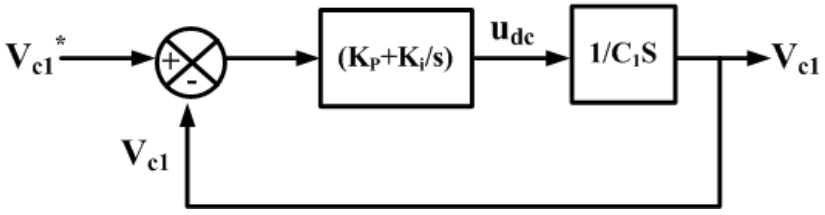


Figure 6.5 Closed-loop circuit of DC-link voltage control

Transfer function of DC-link voltage control circuit is given in Equation 6.37.

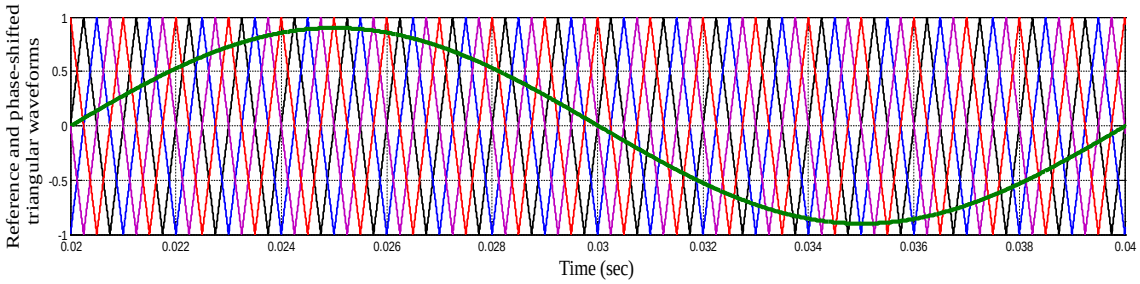
$$G_{dc}(s) = \frac{V_d{}^*(s)}{V_d(s)} = \frac{(K_P s + K_i/s)(1/C_1 s)}{1 + (K_P s + K_i/C_1 s^2)} = \frac{K_P s + K_i}{C_1 s^2 + K_P s + K_i} \tag{6.37}$$

Equation 6.37 can be compared with second order equations and gain parameter constants can be calculated as per Equation 6.38.

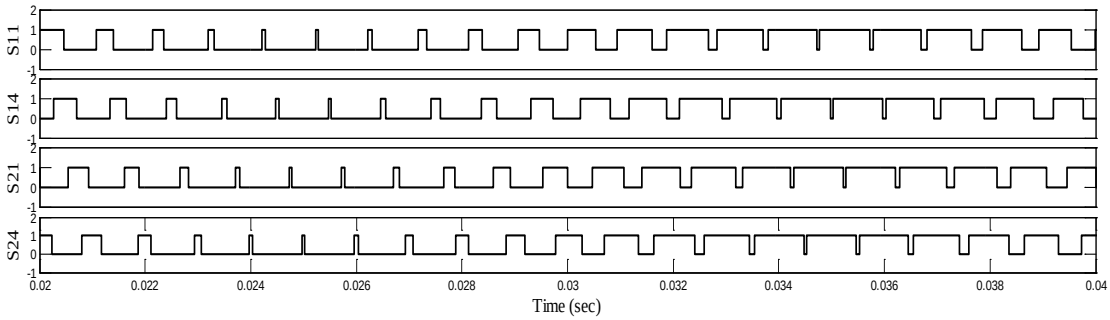
$$\left.\begin{aligned} K_i &= \omega_n{}^2 / C_1 \\ K_P &= 2C_1 \xi \omega_n \end{aligned}\right\} \tag{6.38}$$

6.3.3 Gate Pulse Generation

Modulation technique is an important part of any control scheme. Proposed work has used phase-shifted PWM technique for generating gate pulses of CHB-MLI as this technique helps to distribute power into all modules of inverter unit. This modulation technique allows even amount of power distribution among H-bridge cells as this is very much important for voltage balancing. Four numbers of triangular signals are used as carrier wave. As four numbers of carriers are present, each carrier is phase shifted by 90 degree. If first triangular signal magnitude is lesser than sinusoidal reference signal magnitude, then upper switch of one leg and one H-Bridge is on and else it will be on zero/off condition. The other switch of that particular leg will follow the reverse logic. Similarly, switching of the rest of the three legs will be decided by the same manner. PS-PWM technique working principle along with triangular carrier wave and sinusoidal reference waveform is depicted on Figure 6.6 (a) whereas pulses of switches S11, S14, S21 and S24 are shown in Figure 6.6 (b) for ready reference. Pulse widths are changing in nature according to pulse generation strategy of PWM.



(a)

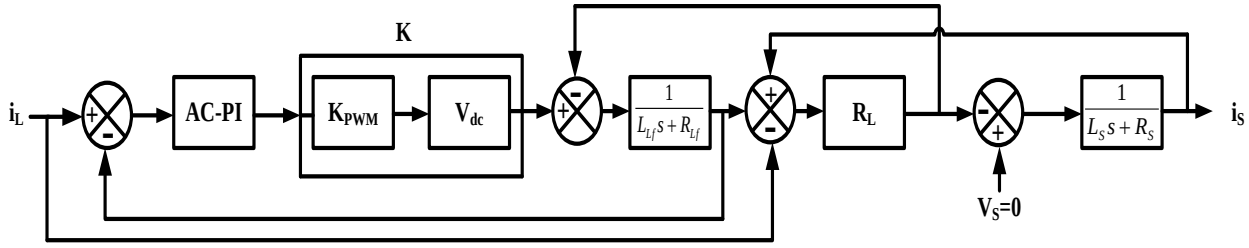


(b)

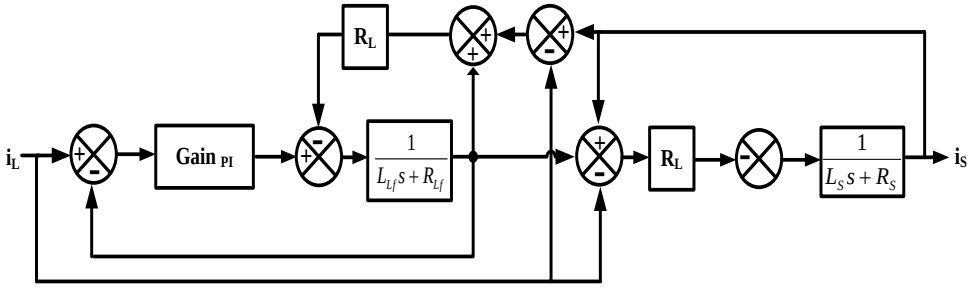
Fig.6.6 (a) PS-PWM technique, and (b) gate pulses for two H-bridges

6.3.4 Stability Analysis of Closed-Loop Control Theory

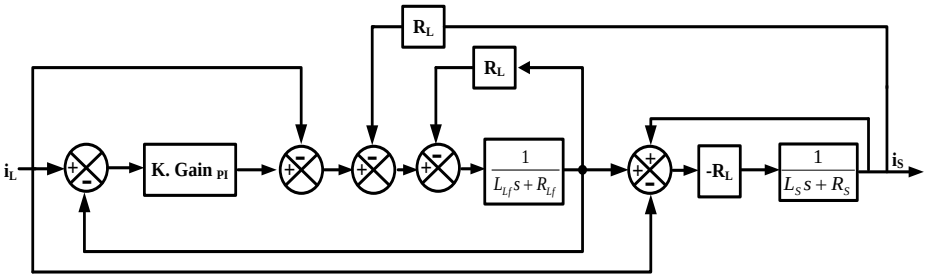
Modified closed-loop control of CHB-MLI based SAPF can be depicted as shown in Figure 6.7 (a) - (d). Figure 6.7 shows block reduction technique based approach while calculating closed-loop transfer function of the proposed control.



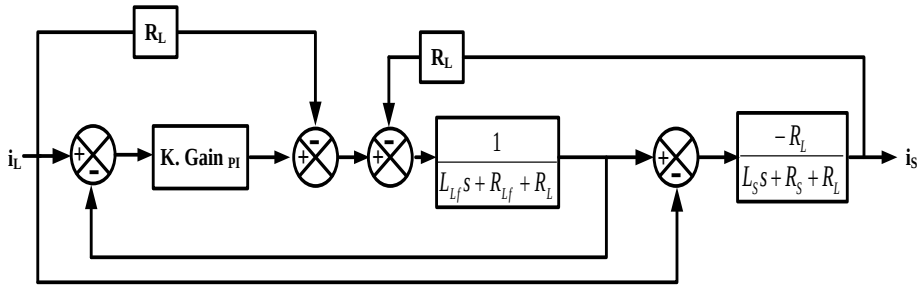
(a)



(b)



(c)



(d)

Figure 6.7 (a) Closed-loop transfer function of control algorithm, (b) equivalent loop diagram considering MLI and PWM gain parameters, (c) rearranged loop diagram, and (d) loop diagram using block reduction technique

Transfer function of the closed loop control is shown as per Equation 6.39.

$$\frac{i_s}{i_L} = \frac{N_{52}s^2 + N_{51}s}{D_{53}s^3 + D_{52}s^2 + D_{51}s + D_{50}} \tag{6.39}$$

where, $N_{52} = R_L L_{Lf}$; $N_{51} = R_L R_{Lf}$;

$D_{53} = L_s L_{Lf}$;

$D_{52} = [(R_s + R_L)L_{Lf} + (R_{Lf} + R_L)L_s + KK_P L_s]$;

$D_{51} = [R_{Lf}(R_s + R_L) + R_L R_s + KK_i L_s + KK_P(R_s + R_L)]$;

$D_{50} = KK_i(R_s + R_L)$

Therefore, transfer function can be derived by considering $R_L \to \infty$ for simplified calculations. The simplified transfer function of closed-loop control is mentioned in Equation 6.40.

$$\frac{i_s}{i_L} = \frac{L_{Lf}s^2 + R_{Lf}s}{(L_s + L_{Lf})s^2 + (R_s + R_{Lf} + KK_P)s + KK_i} \tag{6.40}$$

Transfer function is derived by block diagram reduction technique and its stability is checked with root-locus criteria. Root-locus has been plotted and shown in Figure 6.8. Figure 6.8 shows that poles lie in the left hand side of imaginary axis. It can be concluded that MLI based SAPF control system is composed of advanced PLL is stable one.

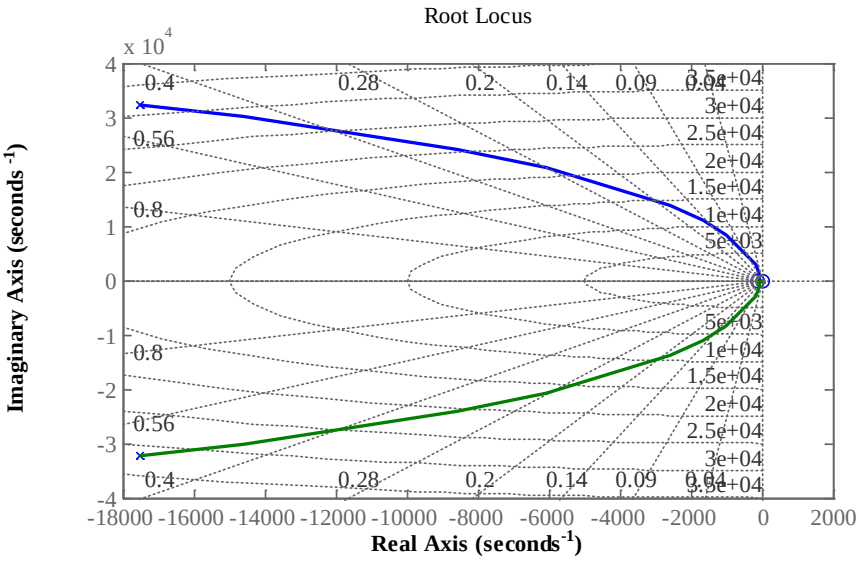


Fig. 6.8 Root-locus diagram of closed-loop modified control for CHB-MLI based SAPF

6.4 IMPLEMENTATION OF MODIFIED SRF THEORY WITH ADVANCED PLL IN MATLAB/ SIMULINK

The performance of the advanced PLL is rigorously tested in different line voltage conditions inclusive harmonic and dc content as shown in Figure 6.9 and Figure 6.10.

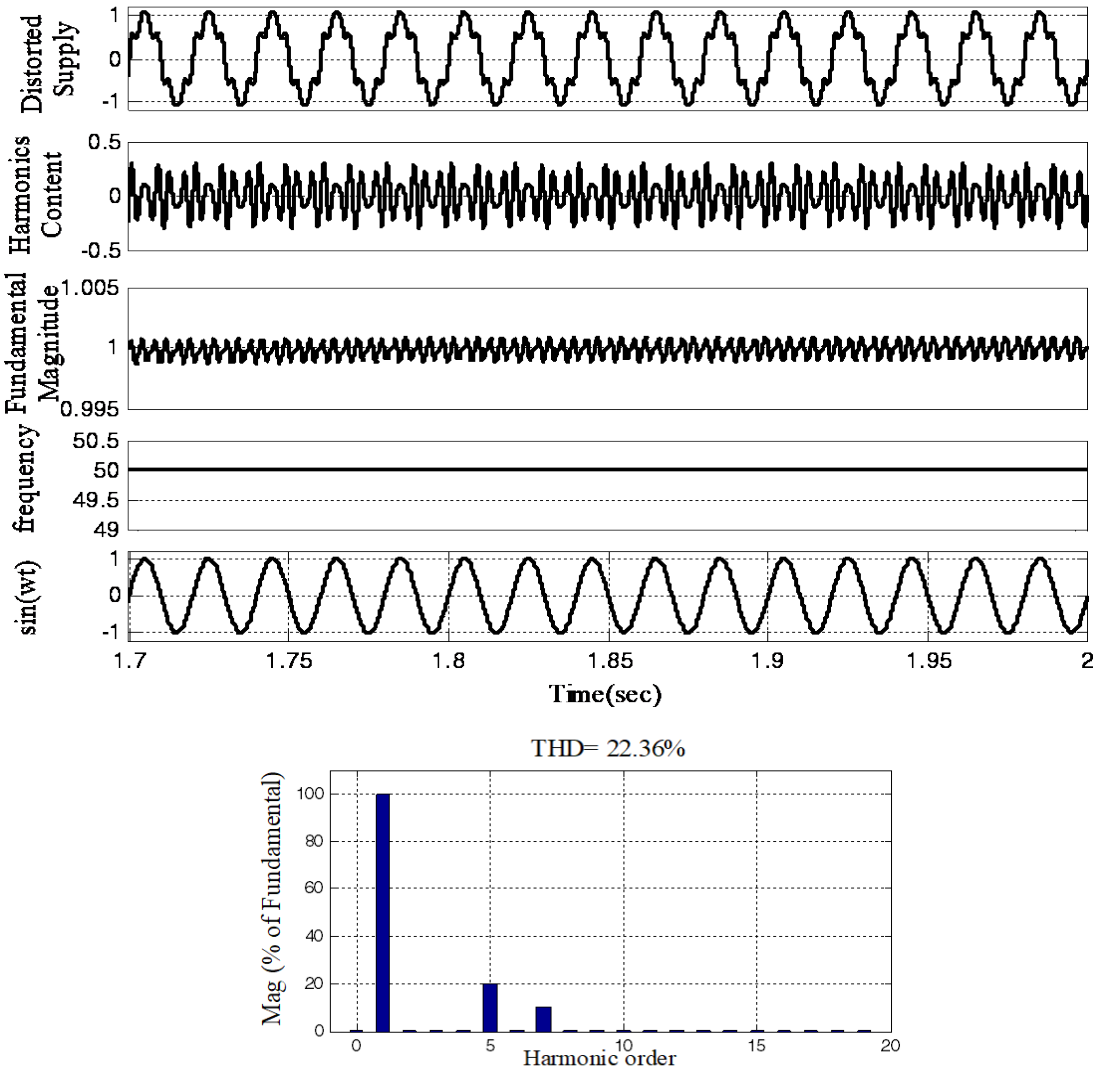


Figure 6.9 Performance of advanced PLL with harmonic injection

The parameters under consideration are frequency, harmonic content, magnitude of fundamental voltage, phase angle with respect to input voltage. Figure 6.9 shows performance of the PLL with input supply voltage having THD of 22.36% where 5^{th} and 7^{th} harmonic content are injected in line. Figure shows that harmonic component is extracted successfully with proper frequency information extraction in distorted source voltage condition. Figure 6.10 shows advanced PLL efficiency during the presence of 0.1

p. u. dc and 22.36% odd harmonic components in input voltage. Figure shows that DC component is extracted from DC component extraction loop of advanced PLL and harmonic component is extracted from harmonic component extraction loop. As a result, PLL performs successfully its phase angle detection and frequency estimation operation. It can be concluded form the steady-state simulation results that advanced PLL is able to generate unit template accurately in distorted line voltage conditions.

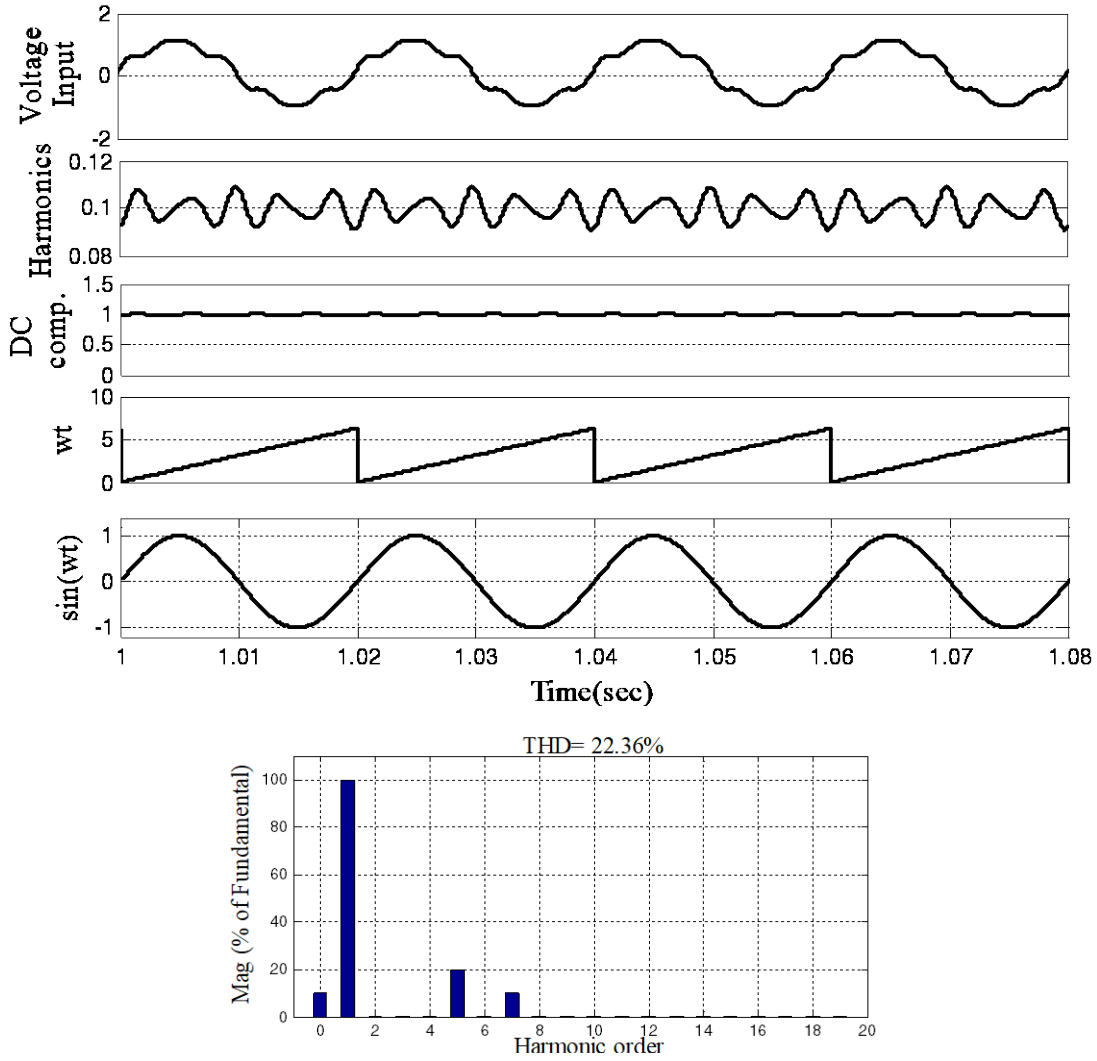
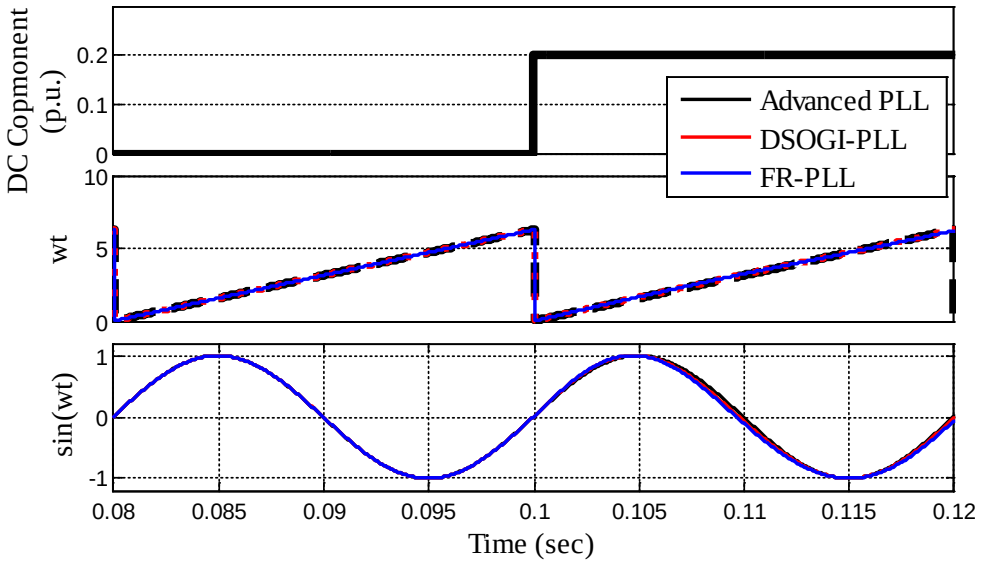


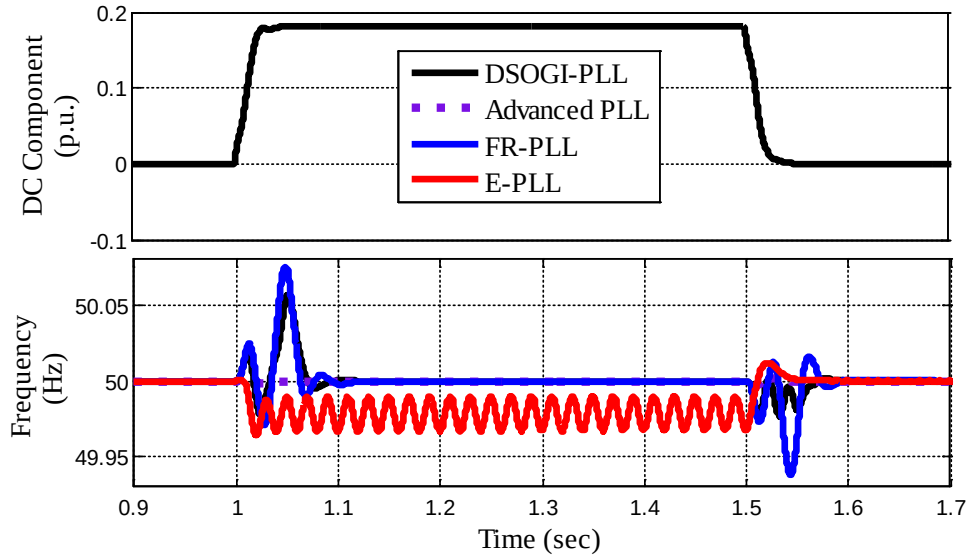
Figure 6.10 Performance of advanced PLL with DC component and odd harmonic injection

However, transient behavior of PLL also plays a vital role while selecting a PLL in grid-synchronization application. Dynamic response of the advanced PLL is examined and compared with several PLLs having harmonic and/or dc rejection capability (E-PLL

[190], FR-PLL [187, 188] and DSOGI-PLL [186]). Figure 6.11 (a) shows advanced-PLL dynamic performance during 20% dc component injection in source voltage. Dynamic response of advanced PLL is having lesser settling time with respect to other PLLs. It is seen from Figure 6.11 (b) that, E-PLL response becomes slightly oscillatory with dc component injection in supply voltage whereas advanced PLL shows very good dynamic response in case of frequency tracking.



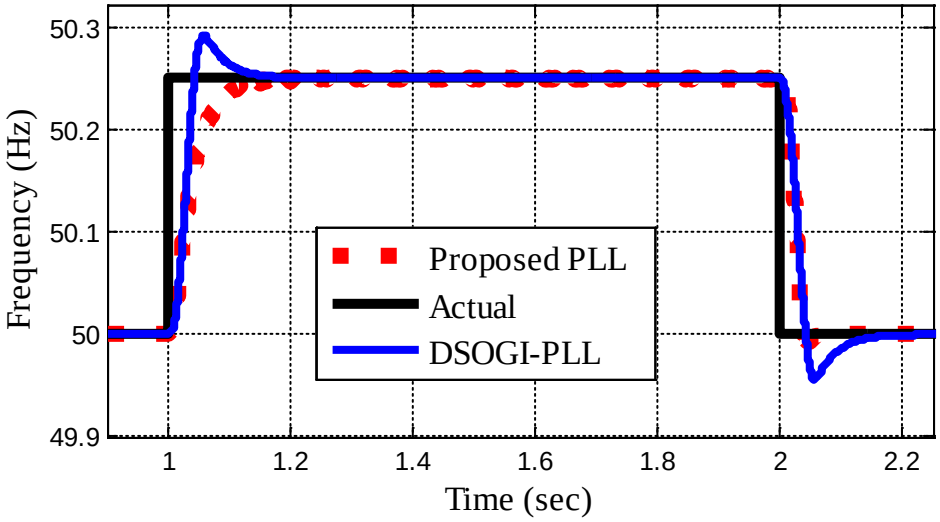
(a)



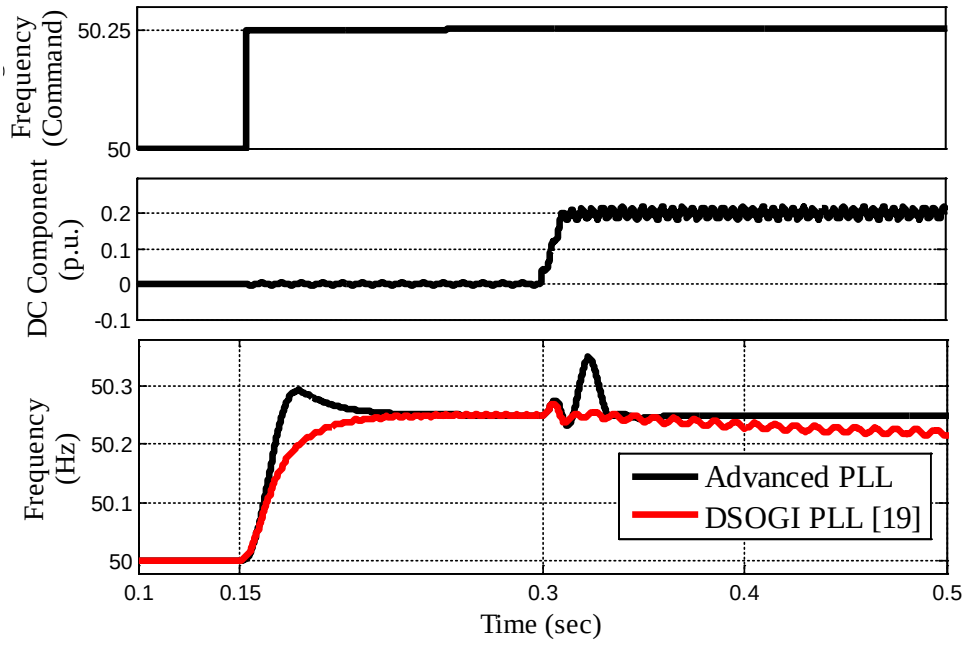
(b)

Figure 6.11 Dynamic performance of advanced PLL (a) with 20% dc injection, and (b) frequency response application and removal of dc component

Step-change of frequency is applied in the supply voltage and Figure 6.12 (a) shows fewer amounts of settling time and peak overshoot with change in supply frequency. PLL performance is also checked with dc component injection in supply voltage as well as with change in supply frequency. It is shown from Figure 6.12 (b) that frequency tracking is accurate with advanced PLL. Detailed simulation results show the effectiveness of the advanced PLL compared to other PLLs.



(a)



(b)

Figure 6.12 (a) Performance of PLL with change in frequency, and (b) with dc component and change in frequency

The overall simulation model of three-phase five-level CHB-MLI based SAPF along with proposed control algorithm is developed in MATLAB/ Simulink environment using SimPowerSystem Blockset. This simulation model consists of a three-phase source, five-level SAPF, voltage and current type non-linear loading, DC-link capacitors, interfacing inductors and proposed control algorithm. Current and voltage signals are sensed with current and voltage measurement block, respectively. Various simulation results are obtained for non-linear loads with different balanced and unbalanced loading conditions. Performance of proposed control algorithm is tested with five-level CHB-MLI based SAPF during steady-state as well as during transient conditions under sinusoidal and distorted supply voltage. Distorted source voltage condition includes the effect of harmonics as well as dc components in supply voltage. The SAPF unit is switched on at t=0.1 sec. for testing SAPF effectiveness in different test conditions.

6.4.1 Uncontrolled Converter with R-L Load and Distorted Supply Voltage

A diode-bridge rectifier with R-L element is considered as current-type non linear loading for this investigation. In this case, source voltage is distorted. The three-phase source and load current is non-sinusoidal due to the presence of non linear loading. Supply voltage contains fifth and seventh harmonics. Presence of DC components in source voltage is also considered in this section.

Simulation under balanced loading condition

Figure 6.13 - 6.15 show simulated performance of three-phase source voltage (V_S), three-phase source current (I_S), compensating currents for phase 'A' (I_{Ca}), DC-link voltage (V_d), inverter output voltage (V_{Ca}) using proposed control scheme for distorted voltage source and balanced non-linear loading conditions. SAPF unit is switched on at t=0.1 sec. At the instant MLI based SAPF unit is switched on, the non-linear source current becomes perfectly sinusoidal from stepped waveform and is perfectly balanced. The total harmonic distortion of three-phase source current reduces from 27.19% and becomes 2.74%, which is in accordance with the IEEE 519-1992 recommended standard. However, non-linear current is still drawn from distribution sector loading. Figure 6.11 shows steady state behavior of V_S, I_S, I_{Ca}, I_{Cb}, I_{Cc}, V_d and V_{Ca} with proposed control algorithm. Figure shows that even if source voltage contains fifth and seventh harmonic

current component, advanced PLL filters out the effect of harmonic content perfectly. Therefore, source current becomes perfectly sinusoidal. Performance is also tested with change in loading conditions. Figure 6.12 shows V_S, I_S, I_{Ca}, V_d and V_{Ca} behavior with increment in loading. It can be seen from figure that DC-link becomes stable after 2 cycles. Transition in source current magnitude is smooth. Figure 6.13 shows V_S, I_S, I_{Ca}, V_d and V_{Ca} behavior with decrement in loading. It can be seen from figure that DC-link becomes stable after 2.5 cycles. Transition in source current magnitude is smooth. Source voltage contains 11.27% of harmonic content. It is seen from both the figures that current transition is smooth with change in loading conditions. DC-link becomes stabilized after having a dip/rise and maintains its reference value. Therefore, source current becomes sinusoidal after switching on SAPF unit in all possible source voltage conditions. It can be depicted from all the results that source current becomes perfectly sinusoidal in all possible distorted source voltage scenarios including steady-state and transient loading conditions.

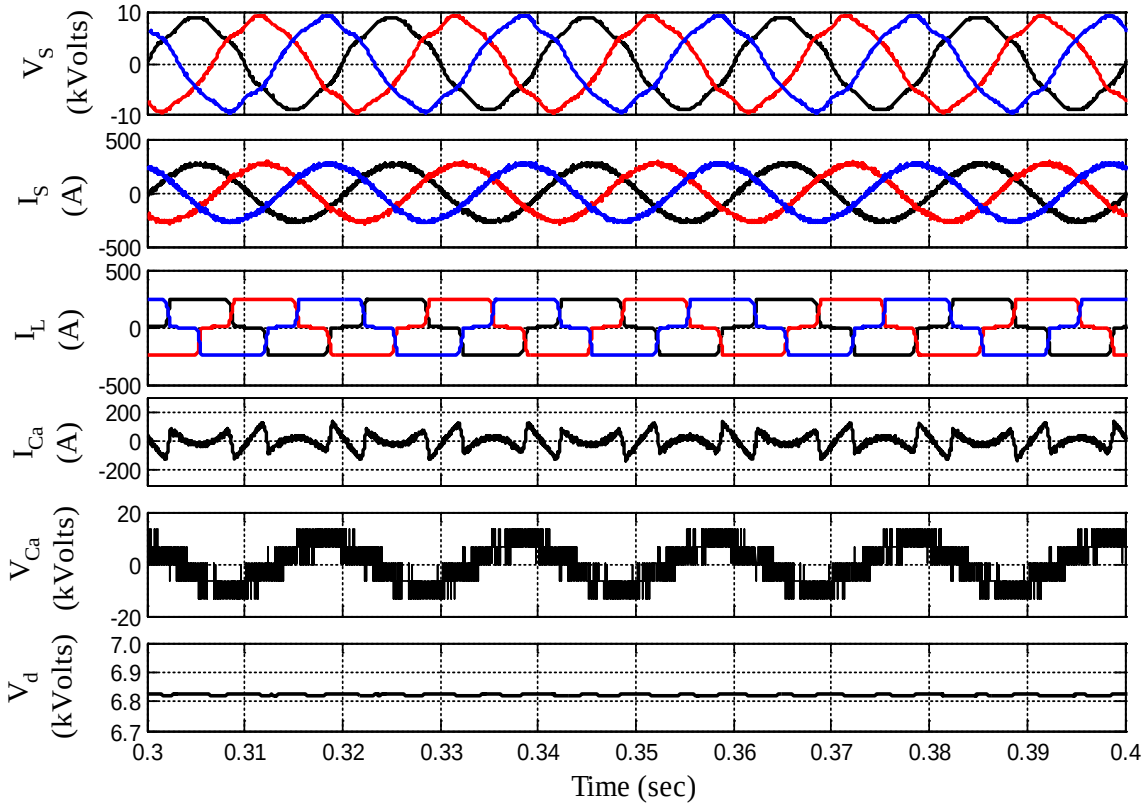


Figure 6.13 Steady-state waveform of CHB-MLI based SAPF with proposed control algorithm under distorted source voltage and balanced R-L loading

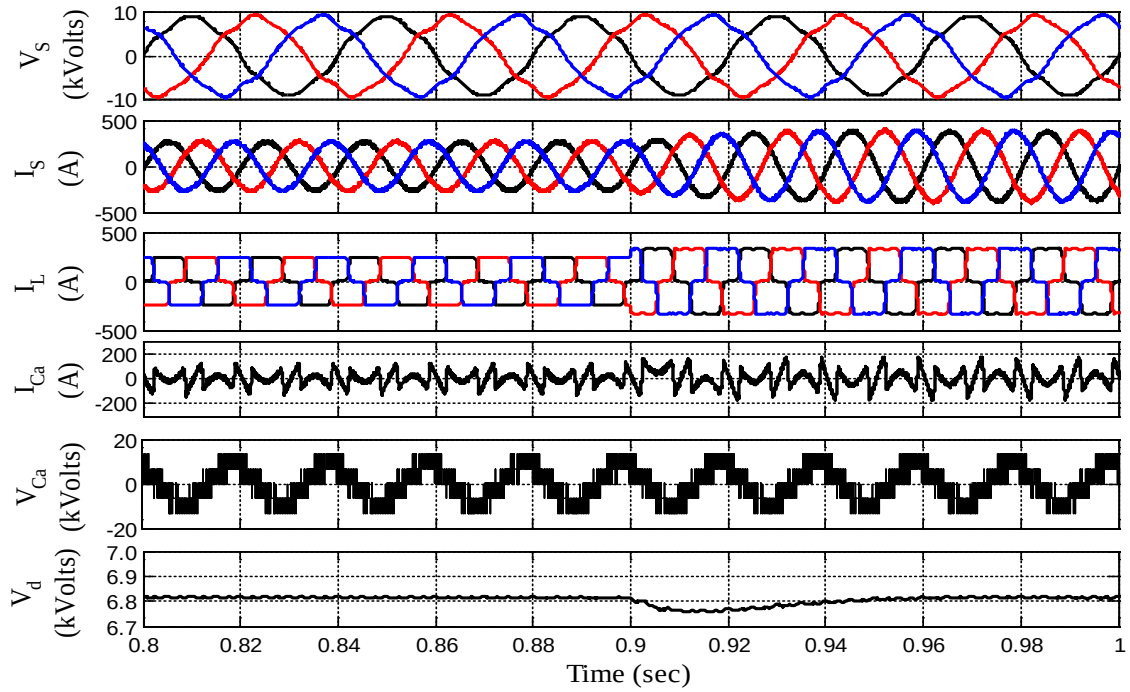


Figure 6.14 Transient response of CHB-MLI based SAPF with proposed control algorithm with load increment under distorted source voltage and balanced R-L loading

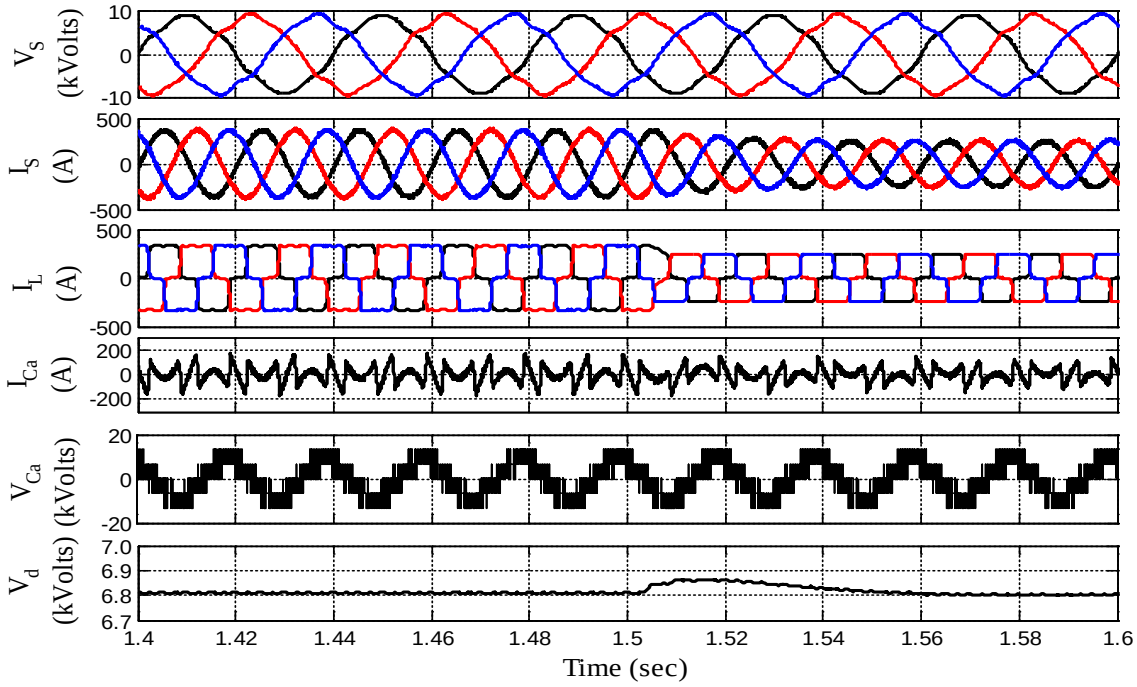


Figure 6.15 Transient response of CHB-MLI based SAPF with proposed control algorithm with load decrement under distorted source voltage and balanced R-L loading

Figure 6.16 sows that the source current is distorted in nature and it can be observed that source current THD is around 27% before connecting MLI based SAPF unit with grid. As soon as SAPF unit is connected to PCC, source current becomes sinusoidal and in-phase with source voltage. Source current THD is reduced from 27.19% to 2.74%. The frequency response of source current after compensation is shown in Figure 6.17.

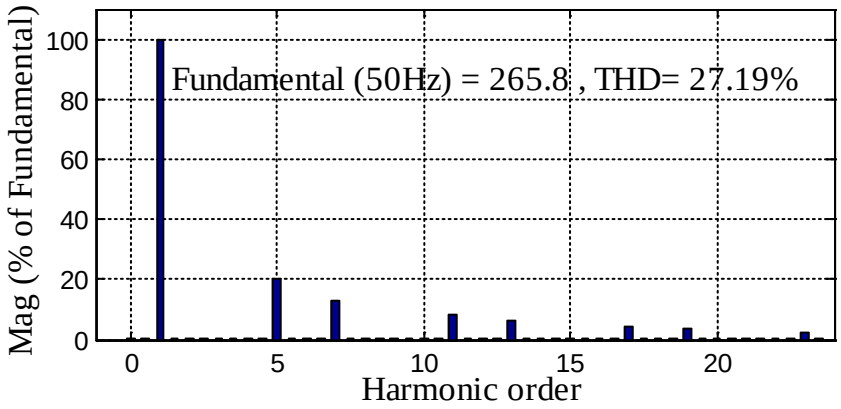


Figure 6.16 THD profile of source current before compensation for R-L loading

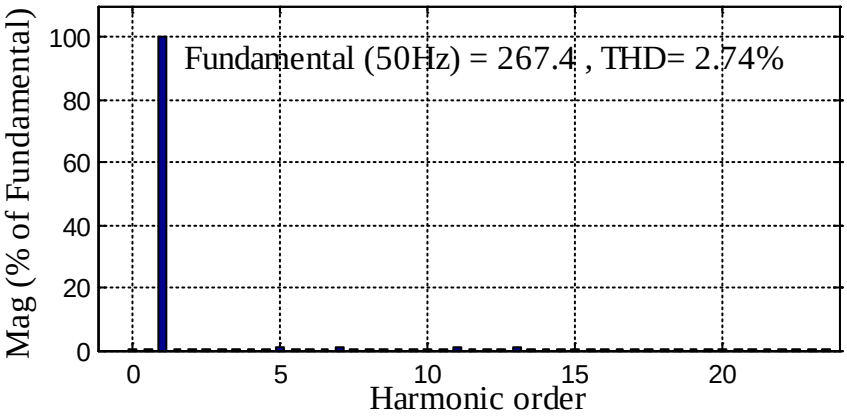


Figure 6.17 THD profile of source current after compensation for R-L loading

Rigorous simulation study has been presented in this subsection and this detailed steady-state, transient analysis show that the response of MLI based SAPF is quite satisfactory during steady-state and transient conditions which include step-increment in loading and step-decrement in loading.

Simulation under Unbalanced Loading Condition

In the previous subsection, steady-state and transient performance of the proposed control scheme is tested with current-type of balanced non-linear loading. Behavior of the proposed control is also tested under unbalanced loading condition. An additional single-

phase uncontrolled converter between two phases has been added with existing loading arrangement. This arrangement makes source current unbalanced one. Simulation study results have been also observed with distorted source voltage conditions including dc and harmonic component. Three-phase load currents are quite unbalanced and having magnitude of 399.3 V_{pp} , 264.6 V_{pp} ,and 396.7 V_{pp} and THD of 21.05%, 26.08% and 16.56% for phase 'A', 'B' and 'C', respectively. It can be observed that source current is also distorted due to the presence of unbalanced resistive-inductive type of non-linear loading and are having similar wave-shape of load currents. MLI based SAPF unit is switched on at t=0.1 sec. Source current THD for phase 'A', 'B' and 'C' becomes below 5% after successful operation of SAPF unit. Source current is also perfectly balanced after connecting SAPF unit to grid. Figure 6.18 shows SAPF system steady-state performance with resistive-inductive loading under distorted source conditions. Load is applied into the existing system at an instant of t=0.9 sec and the SAPF performance is shown in Figure 6.19. Load is again decreased at an instant of t=1.5 sec. Transient-state MLI based SAPF performance is plotted in Figure 6.20 when load is withdrawn from the system. Transient condition waveforms during load increment and decrement confirm the effectiveness of the proposed control algorithm.

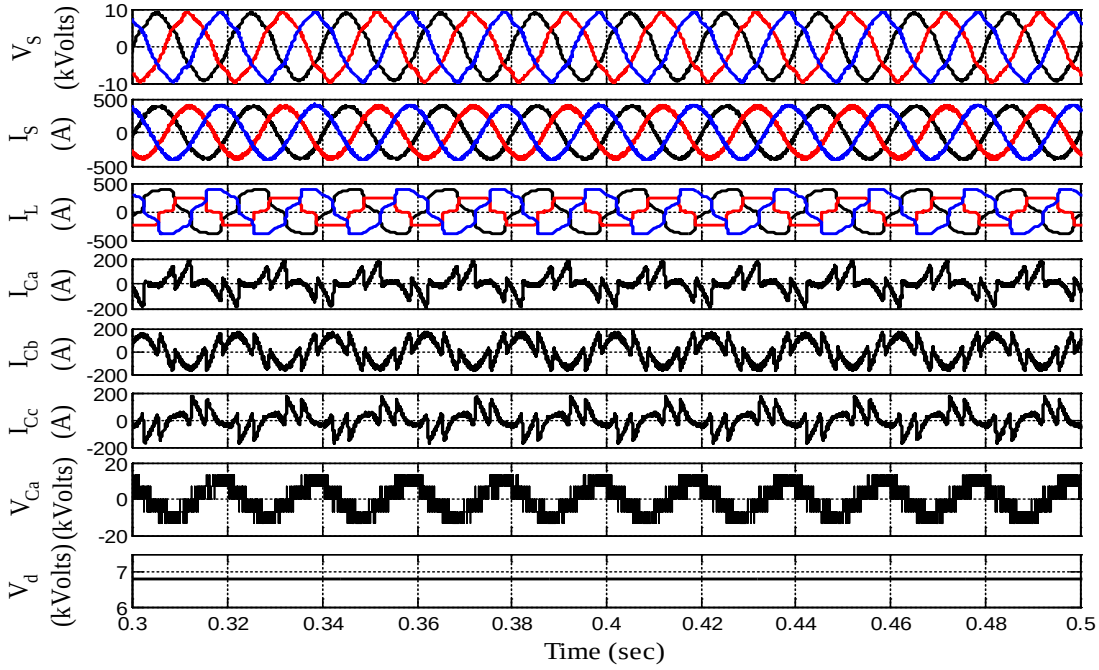


Figure 6.18 Steady-state waveform of CHB-MLI based SAPF with proposed control algorithm with distorted source voltage and unbalanced R-L loading

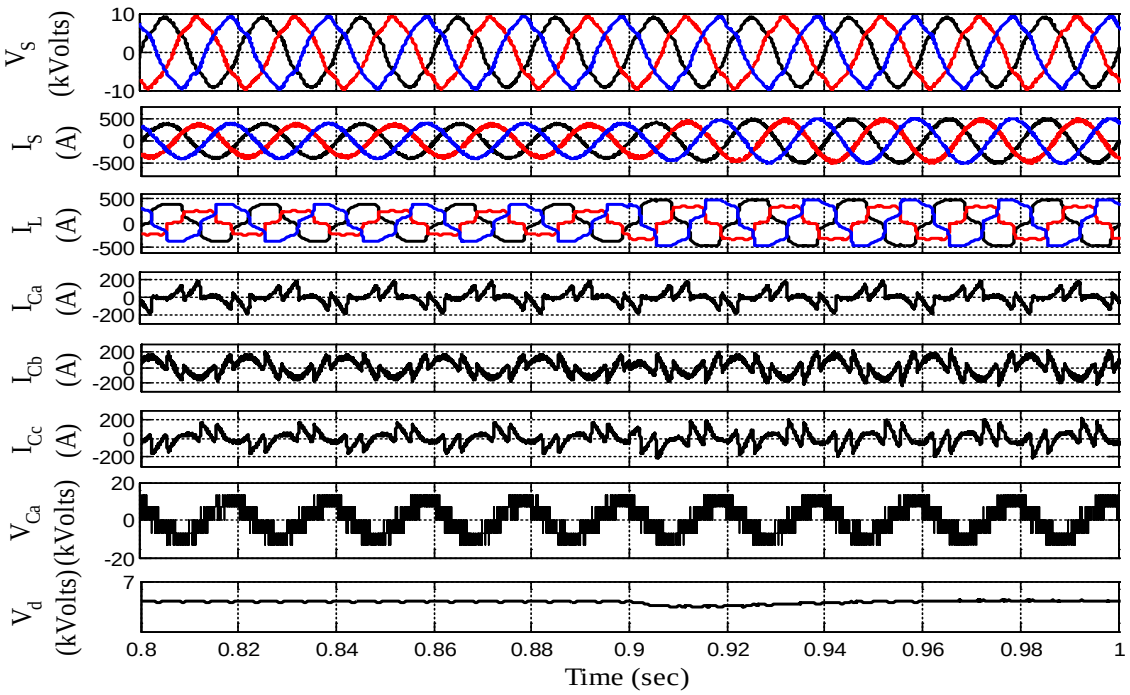


Figure 6.19 Transient response of CHB-MLI based SAPF with proposed control algorithm with load increment under distorted source voltage and unbalanced R-L loading

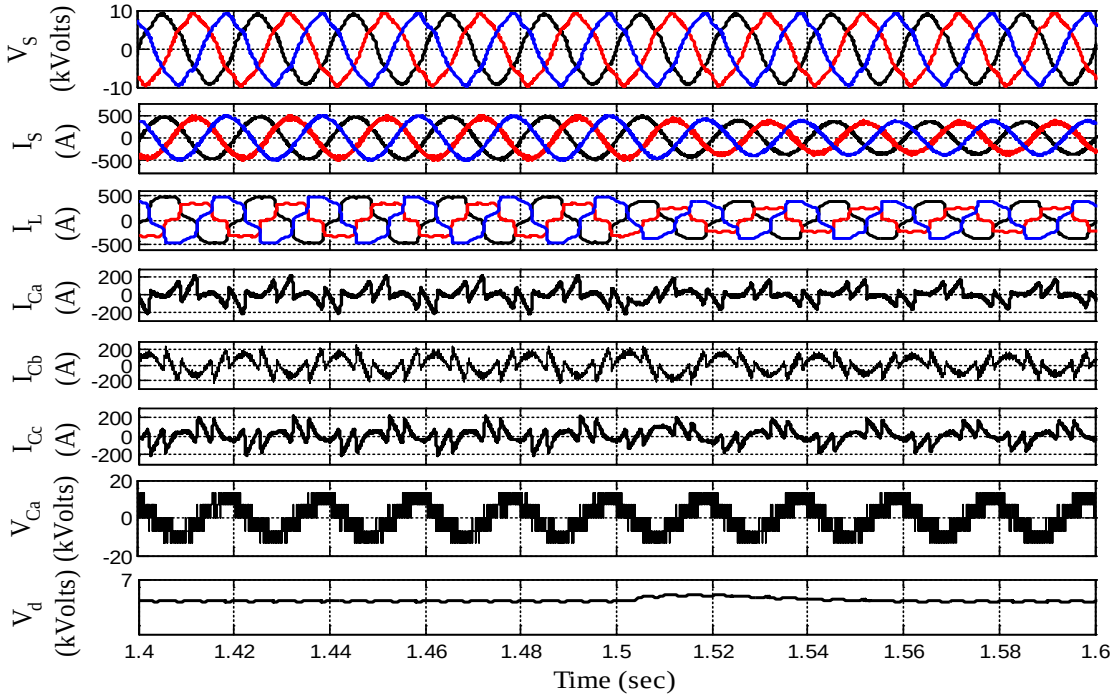
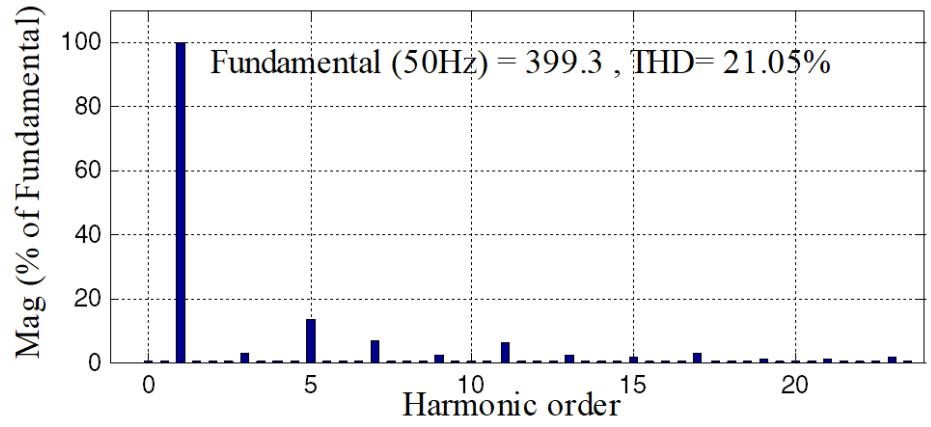
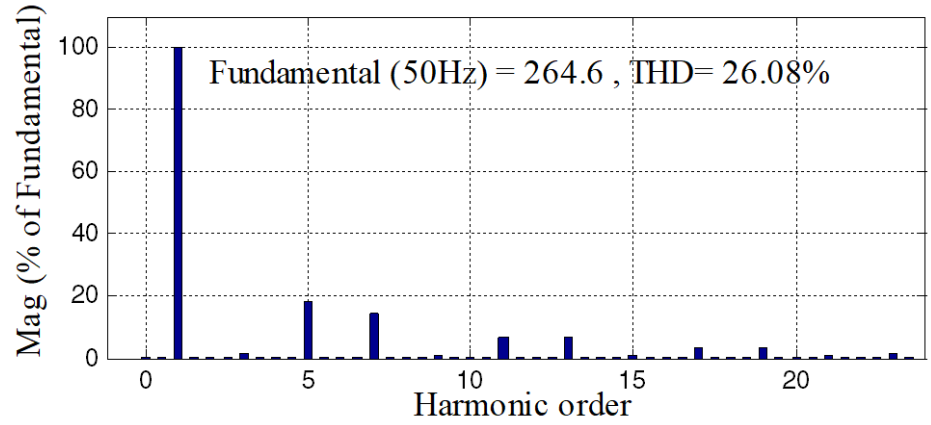


Figure 6.20 Transient response of CHB-MLI based SAPF with proposed control algorithm with load decrement under distorted source voltage and unbalanced R-L loading

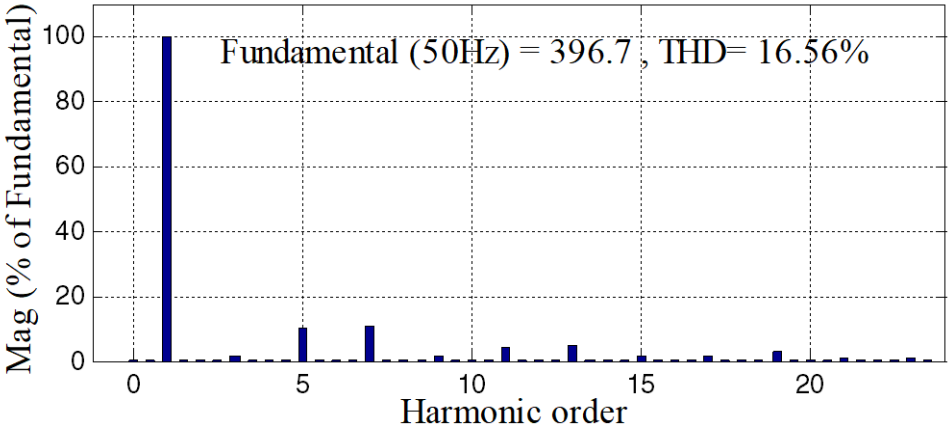
Figure 6.21 depicts unbalanced source current with magnitude and their THDs. The THD of source current is reduced from 21.05% to 2.94% in phase 'A', 26.08% to 3.01%, and 16.56% to 2.91% in phase 'C', respectively.



(a)



(b)



(c)

Figure 6.21 THD profile of source current before compensation for unbalanced R-L loading (a) THD profile of Phase 'A', (b) THD profile of Phase 'B', and (c) THD profile of Phase 'C'

Source current THD for phase ‘A’, ‘B’ and ‘C’ becomes below 5% after successful operation of SAPF unit, as shown in Figure 6.22. This FFT analysis also shows source current is perfectly balanced after connecting SAPF unit to grid.

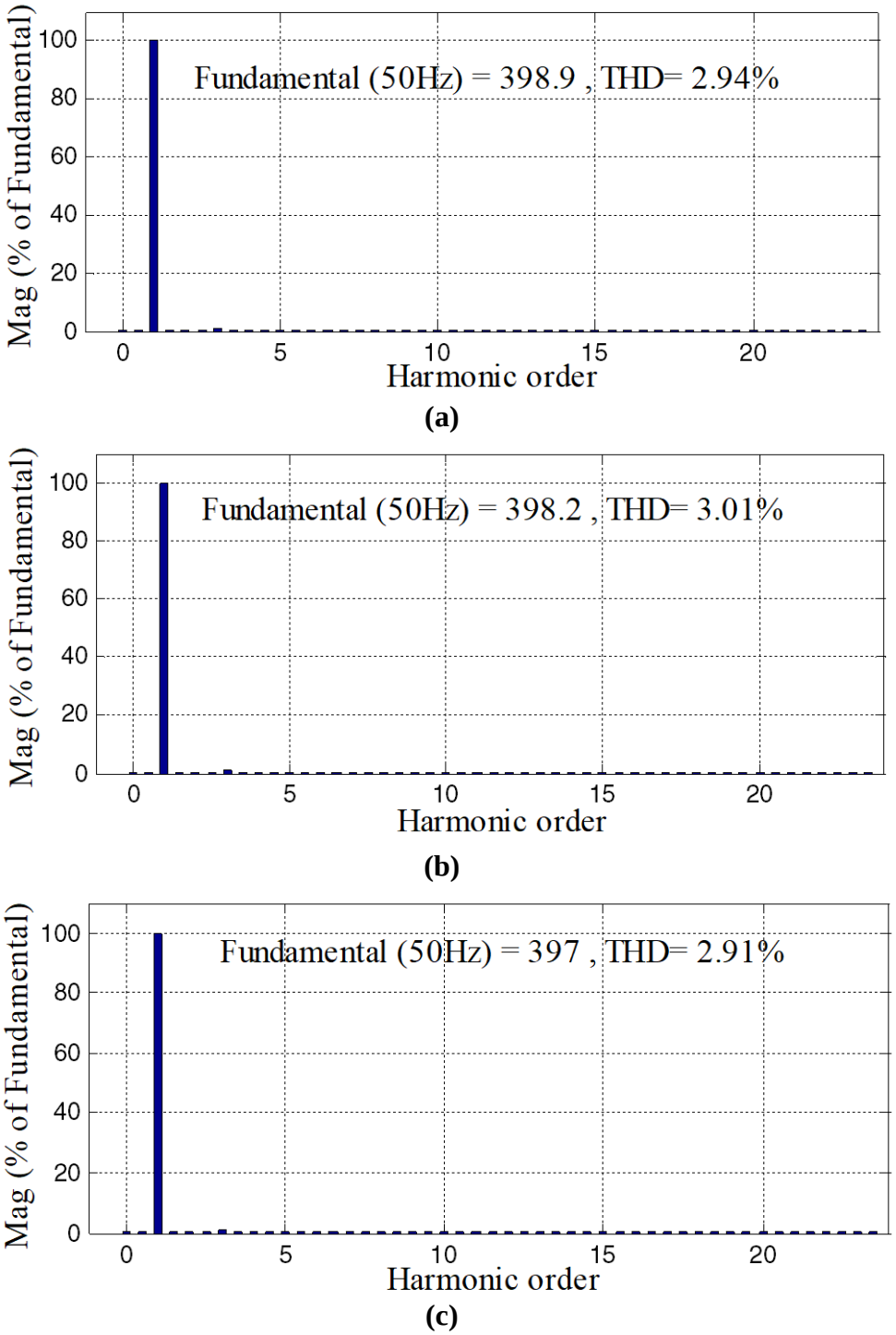


Figure 6.22 THD profile of source current after compensation for unbalanced R-L loading (a) THD profile of Phase ‘A’, (b) THD profile of Phase ‘B’, and (c) THD profile of Phase ‘C’

The effectiveness of the proposed control algorithm is tested with distorted source voltage and with balanced/ unbalanced current-source type of non-linear loading condition. Controller is able to provide good compensation is different possible source voltage and loading conditions. Advanced PLL block is able to provide exact phase angle information even during distorted source voltage conditions. However, effectiveness of the control algorithm should be also tested with voltage type of non-linear loading also.

6.4.2 Uncontrolled Converter with R-C Load and Distorted Supply Voltage

The suitability of five-level CHB-MLI based SAPF should be also investigated for the compensation of reactive power as well as mitigation of current harmonic component. The control algorithm performance is tested with voltage-type of non-linear loading. A diode-bridge rectifier with R-C element is considered as voltage-type non linear loading for this investigation. The three-phase source and load current is non-sinusoidal due to the presence of non-linear loading. However, supply voltage contains fifth and seventh harmonics. Presence of DC components in source voltage is also considered in this sub-section for further investigation.

Simulation under Balanced Loading Condition

Figures 6.23 - 6.25 show simulated performance of V_S, I_S, I_{Ca}, V_d, V_{Ca} using proposed control scheme for distorted voltage source and balanced non-linear loading conditions. SAPF unit is switched on at t=0.1 sec. After SAPF is integrated to grid, the non-linear current becomes sinusoidal and perfectly balanced from discontinuous type of current wave-shape. The total harmonic distortion of three-phase source current is reduced from 71.55% to 2.44%, which is in accordance with recommended standard. However, non-linear current is still drawn from distribution sector loading. The instant MLI based SAPF unit is switched on, I_S becomes sinusoidal from non-linear wave-shape. Figure 6.21 shows steady state behavior of V_S, I_S, I_{Ca}, V_d and V_{Ca} with proposed control algorithm. Figure shows that even if source voltage contains harmonic component with 11.27% THD, advanced PLL filters out the effect of harmonic content perfectly. The algorithm works perfectly fine with distorted source voltage condition as advanced PLL successfully extracts phase angle information. The proposed control algorithm measures

load current of each phase separately and therefore, this control algorithm perfectly capable to maintain its operation during balanced/ unbalanced loading conditions.

Therefore, source current becomes perfectly sinusoidal. Performance is also tested with change in loading conditions. Figure 6.22 shows V_S, I_S, I_{Ca}, V_d and V_{Ca} behavior with increment in loading. It can be seen from figure that DC-link becomes stable after 2 cycles. Transition in source current magnitude is smooth. Figure 6.23 shows V_{Sabc}, I_{Sabc}, I_{Ca}, I_{Cb}, I_{Cc}, V_d and V_C behavior with decrement in loading. It can be seen from figure that DC-link becomes stable after 3 cycles. Transition in source current magnitude is smooth even though the source voltage contains almost 11% of harmonic content. It is seen from both the figures that current transition is smooth with change in loading conditions. DC-link becomes stabilized after having a dip/rise and maintains its reference value. Therefore, source current becomes sinusoidal after switching on SAPF unit. It can be depicted from all the results that source current becomes perfectly sinusoidal in all possible distorted source voltage scenarios.

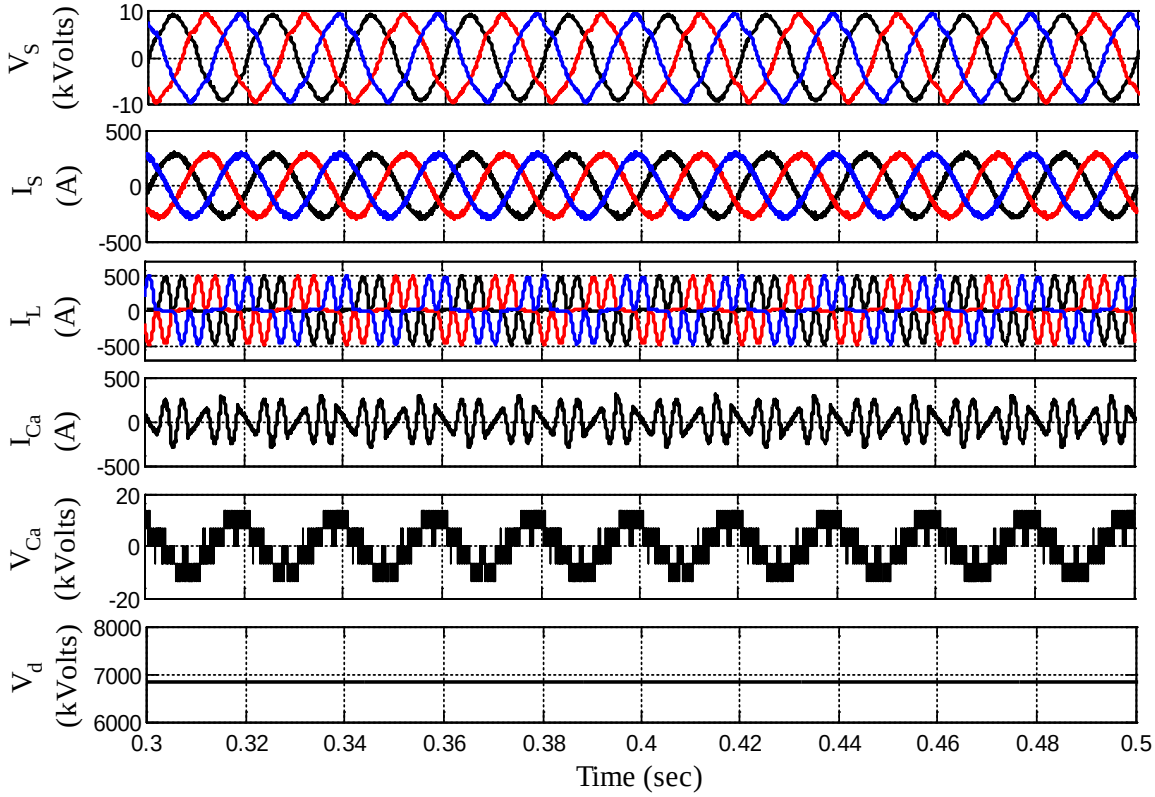


Figure 6.23 Steady-state waveform of CHB-MLI based SAPF with proposed control algorithm under distorted source voltage and balanced R-C loading

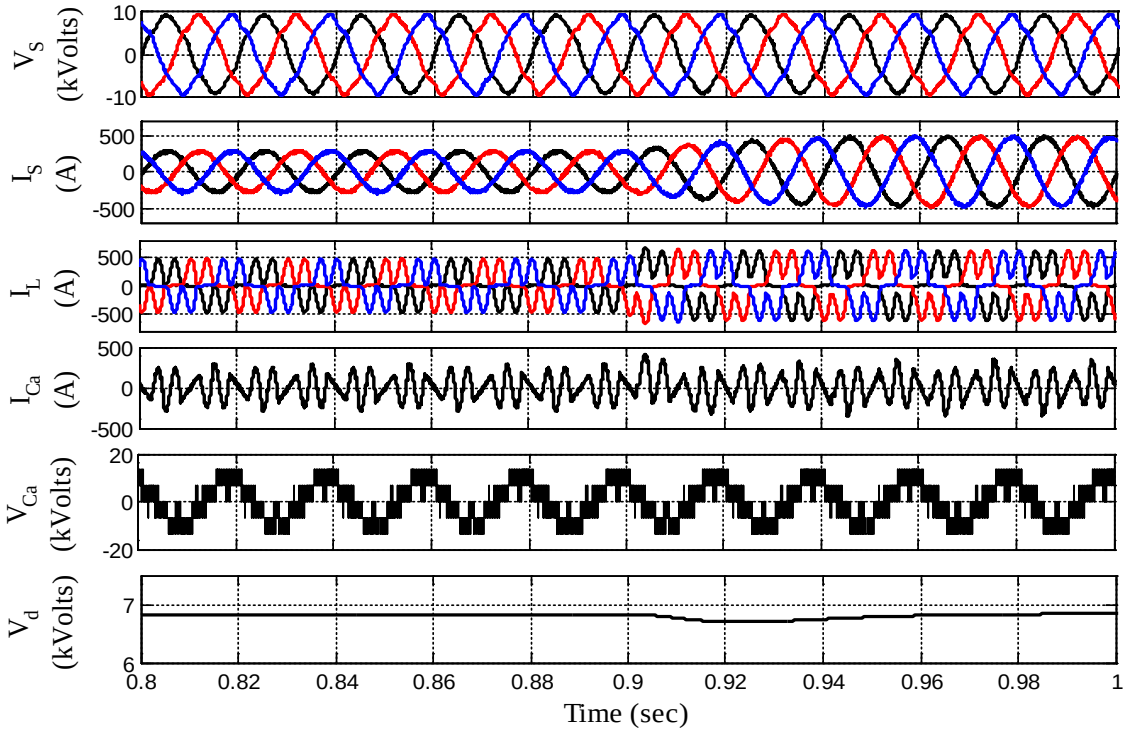


Figure 6.24 Transient response of CHB-MLI based SAPF with proposed control algorithm with load increment under distorted source voltage and balanced R-C loading

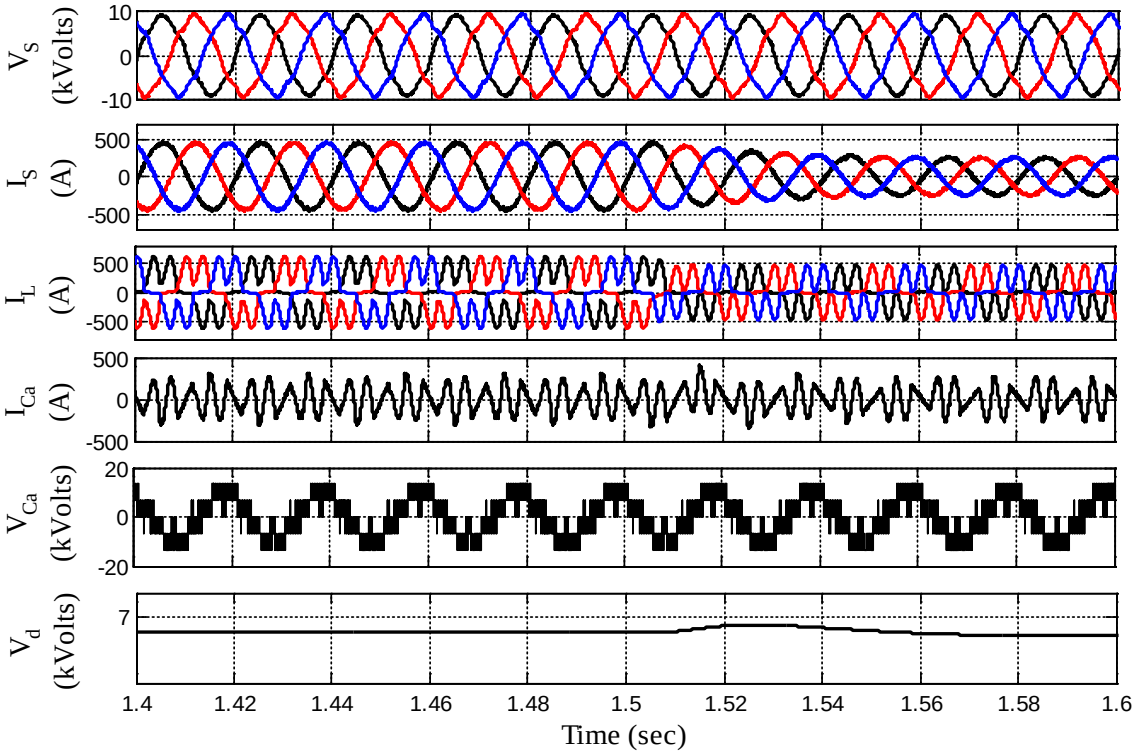


Figure 6.25 Transient response of CHB-MLI based SAPF with proposed control algorithm with load decrement under distorted source voltage and balanced R-C loading

Figure 6.26 sows that the source current is distorted in nature and it can be observed that source current THD is around 71% before connecting MLI based SAPF unit with grid. As soon as SAPF unit is connected to PCC, source current becomes sinusoidal and in-phase with source voltage. Source current THD is reduced from 71.55% to 2.44%. The frequency response of source current after compensation is shown in Figure 6.27.

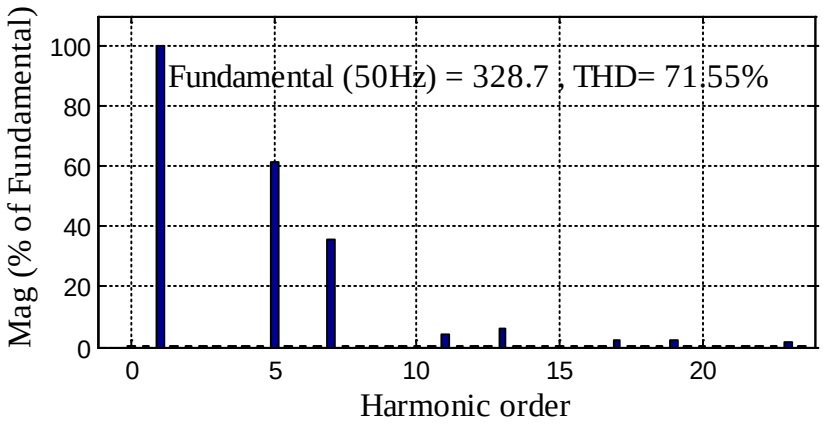


Figure 6.26 THD profile of source current before compensation for R-C loading

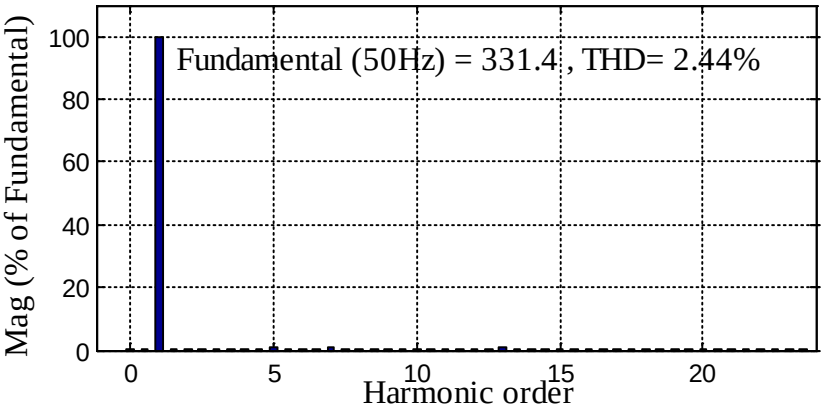


Figure 6.27 THD profile of source current after compensation for R-C loading

Thorough simulation study with R-C type of loading has been presented in this subsection with balanced loading condition, and this detailed analysis show that the response of MLI based SAPF is quite satisfactory during steady-state and transient conditions which include step-increment in loading and step-decrement in loading.

Simulation under Unbalanced Loading Condition

Behavior of the proposed control is also observed under unbalanced loading condition in this subsection. An additional single-phase uncontrolled converter with resistive load between two phases has been added with existing loading arrangement.

This arrangement makes source current unbalanced one. SAPF unit is switched on at t=0.1 sec. Three-phase load currents are quite unbalanced and having magnitude of 330 V_{pp} , 181.2 V_{pp} ,and 340.5 V_{pp} and THD of 42.94%, 82.81% and 46.34% for phase 'A', 'B' and 'C', respectively. It can be observed that source current is also distorted due to the presence of unbalanced resistive-capacitive type of non-linear loading and are having similar wave-shape of load currents. MLI based SAPF unit is switched on at t=0.1 sec. Source current THD for phase 'A', 'B' and 'C' becomes below 5% after successful operation of SAPF unit. Source current is also perfectly balanced after connecting SAPF unit to grid. Steady-state performance of MLI based SAPF with resistive-capacitive loading is depicted on Figure 6.28. Five-level voltage is generated at inverter output terminal. Source current becomes sinusoidal even if load current is highly distorted. Load is increased at an instant of t=0.9 sec and corresponding transient behavior of SAPF unit is shown in Figure 6.29. Again, load is decreased at an instant of t=1.5 sec. and related waveforms are shown in Figure 6.30. Transient-state waveforms show system effective performance as source current transition is smooth enough for judging efficacy of the proposed system.

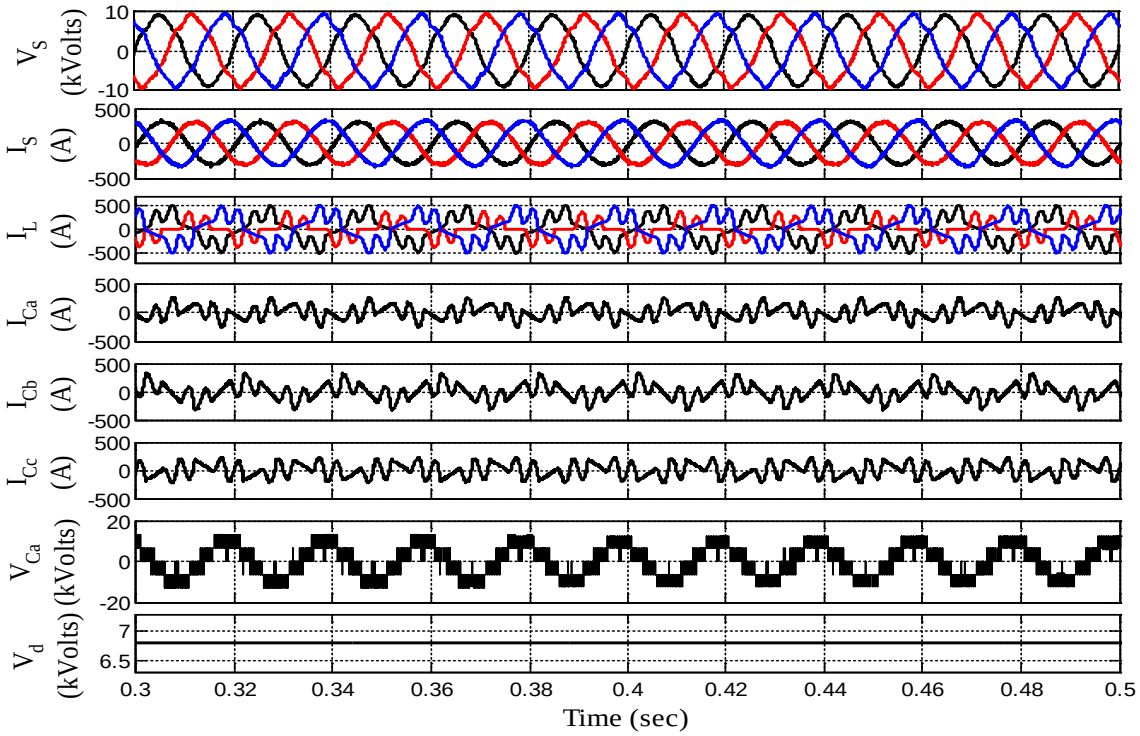


Figure 6.28 Steady-state waveform of CHB-MLI based SAPF with proposed control algorithm under distorted source voltage and unbalanced R-C loading

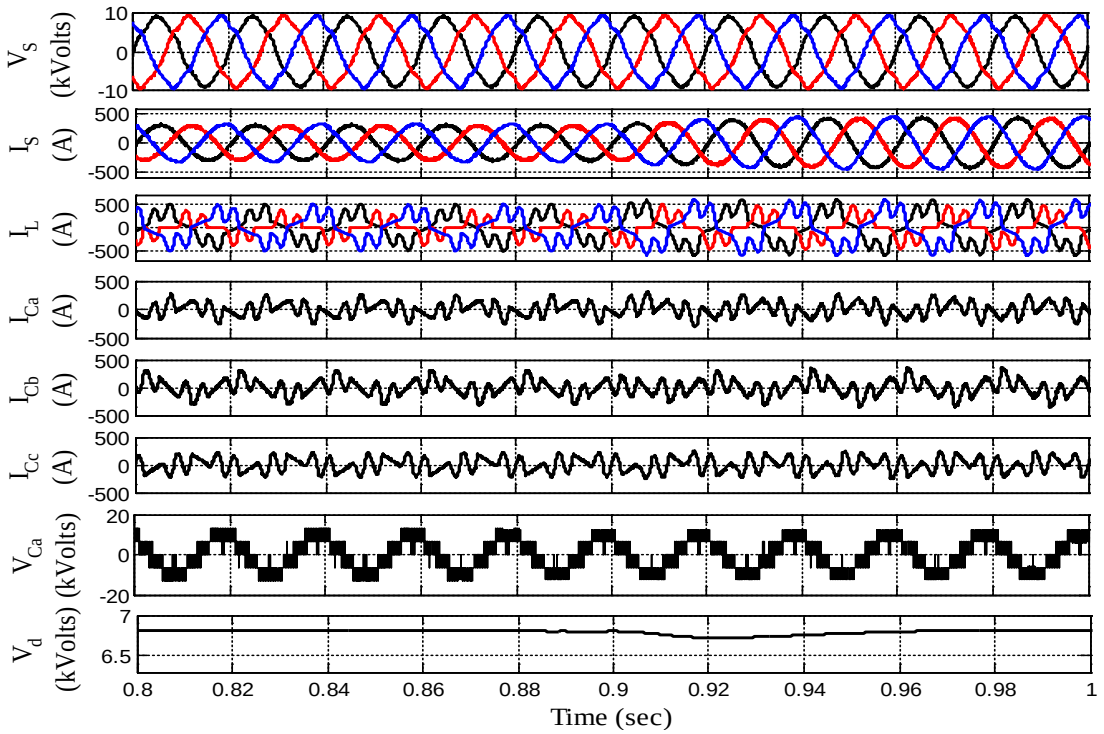


Figure 6.29 Transient response of CHB-MLI based SAPF with proposed control algorithm with load increment under distorted source voltage and unbalanced R-C loading

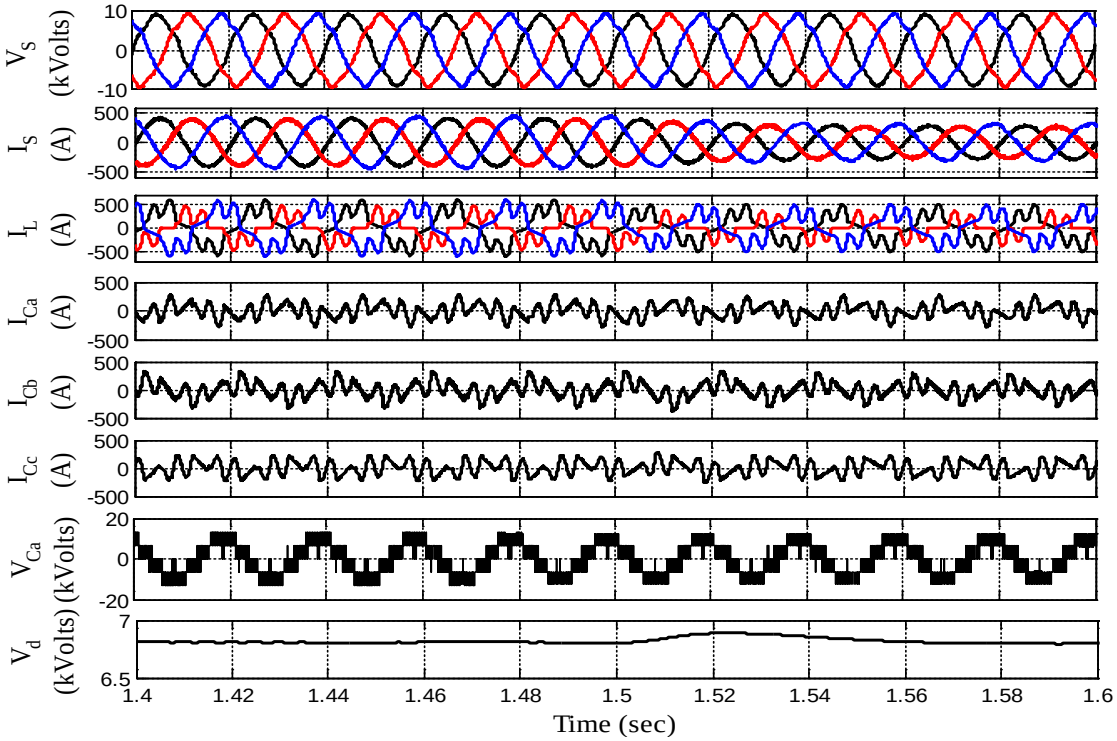
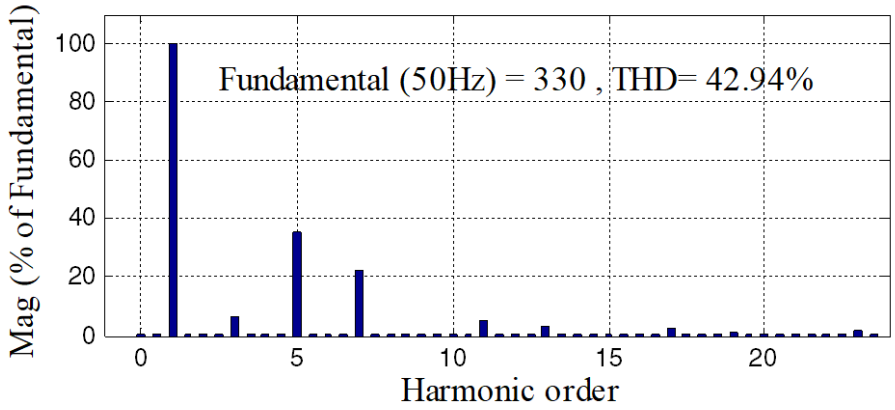
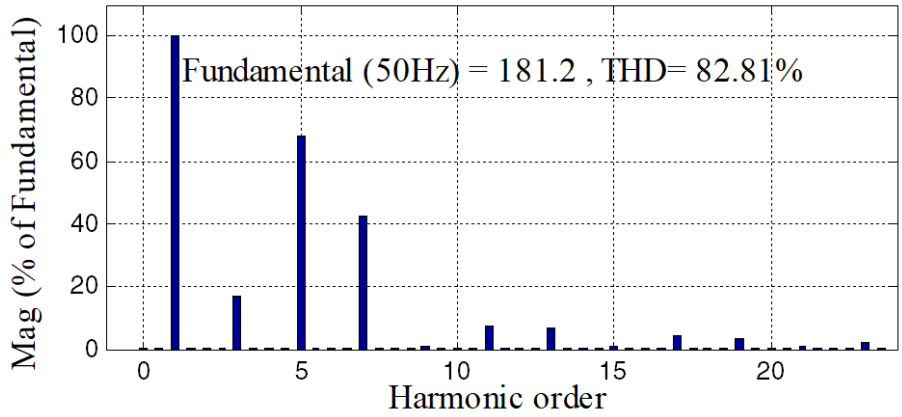


Figure 6.30 Transient response of CHB-MLI based SAPF with proposed control algorithm with load decrement under distorted source voltage and unbalanced R-C loading

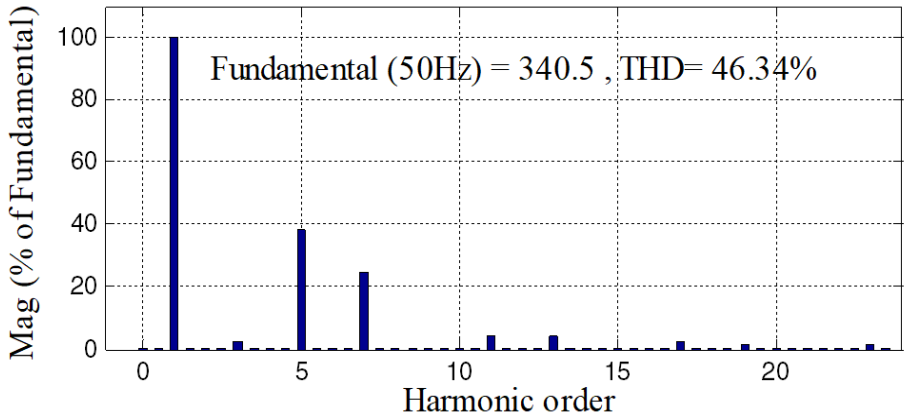
Figure 6.31 depicts unbalanced source current with magnitude and their THDs. The THD of source voltage is reduced from 42.94% to 3.21% in phase 'A', 82.81% to 3.04%, and 46.34% to 3.08% in phase 'C', respectively. Figure 6.31 shows FFT spectrum of source current for phase 'A', 'B' and 'C' before compensation.



(a)



(b)



(c)

Figure 6.31 THD profile of I_S before compensation (a)THD profile of Phase 'A' (b) THD profile of Phase 'B' and (c) THD profile of Phase 'C'

FFT spectrum of source current for phase ‘A’, ‘B’ and ‘C’ before compensation was non-sinusoidal in nature whereas source current THD for phase ‘A’, ‘B’ and ‘C’ becomes below 5% after successful operation of SAPF, as shown in Figure 6.32. FFT analysis also shows source current is perfectly balanced after connecting SAPF unit to grid.

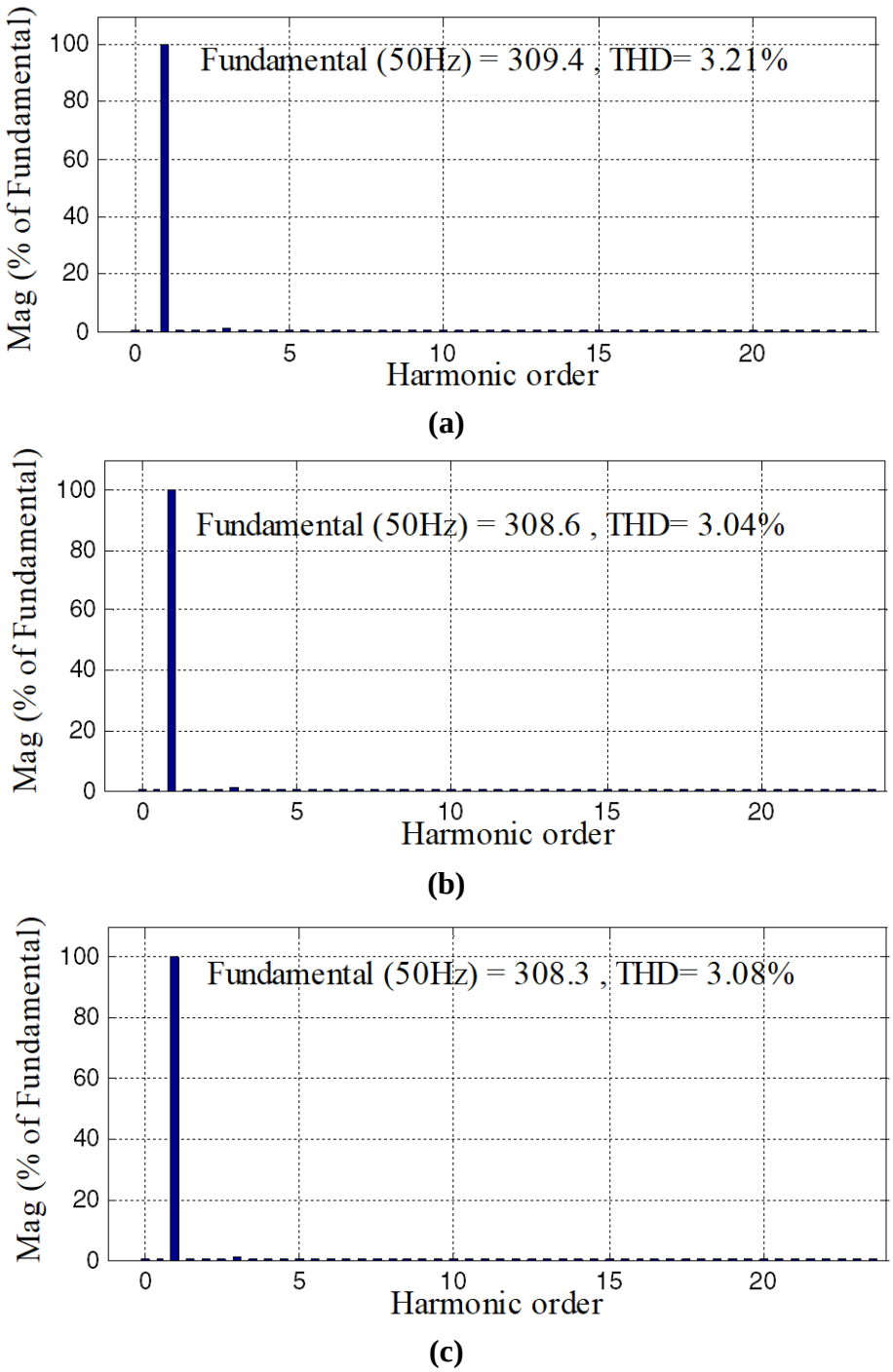


Figure 6.32 THD profile of I_S after compensation (a)THD profile of Phase ‘A’, (b) THD profile of Phase ‘B’, and (c) THD profile of Phase ‘C’

The effectiveness of the proposed control algorithm is tested with distorted source voltage and with balanced/ unbalanced current-source and voltage-source type of non-linear loading condition. Controller is able to provide good compensation in different possible source voltage and loading conditions. Advanced PLL block is able to provide exact phase angle information even during distorted source voltage conditions.

6.5 LABORATORY PROTOTYPE DEVELOPMENT OF MODIFIED SRF THEORY WITH ADVANCED PLL

This section first explores advanced PLL performance under different line conditions and further control theory composed of advanced PLL is developed for MLI based SAPF application. Proposed PLL is implemented in MATLAB/ Simulink system and it is finally integrated to dSPACE 1104 controller. The prototype of five-level single-phase CHB-MLI based SAPF with modified control algorithm is implemented in laboratory as shown in Chapter 3. Advanced PLL based control algorithm is implemented using MATLAB/ Simulink and dSPACE 1104 real-time controller. Non-linear load is designed with diode-bridge rectifier with R-L load and later it is tested with R-C load as depicted in Chapter 3. The parameters are chosen for experimental set-up is shown in Appendix D. The dSPACE 1104 real-time controller generates the required gate pulses for MLI using PS-PWM technique.

Firstly, PLL performance is checked with different possible source voltage conditions which show effectiveness of the proposed PLL and accuracy of phase angle extraction in presence of distorted source voltage conditions. Further, its real-time performance is compared with other recently proposed PLLs. Distorted voltage source having 15-21% THD is considered for experimentation. Injection of dc component to source voltage is also considered in order to check the effectiveness of the advanced PLL using dSPACE 1104 controller. Steady-state and transient performance of the advanced PLL is tested with highly distorted source voltage condition which is depicted on Figure 6.33 (a) - (d). Figure 6.33 (a) - (c) shows steady state performance of the advanced PLL with 15.8%, 17% and 21.2% of THD in the line voltage, respectively. Around 7% of dc component is injected into source voltage and PLL performance is checked in Figure 6.33 (d). Generated unit templates from advanced PLL is compared with existing PLLs in

presence of dc and harmonic content in source voltage, as seen from Figure 6.33 (a), (b), (c) and (d).

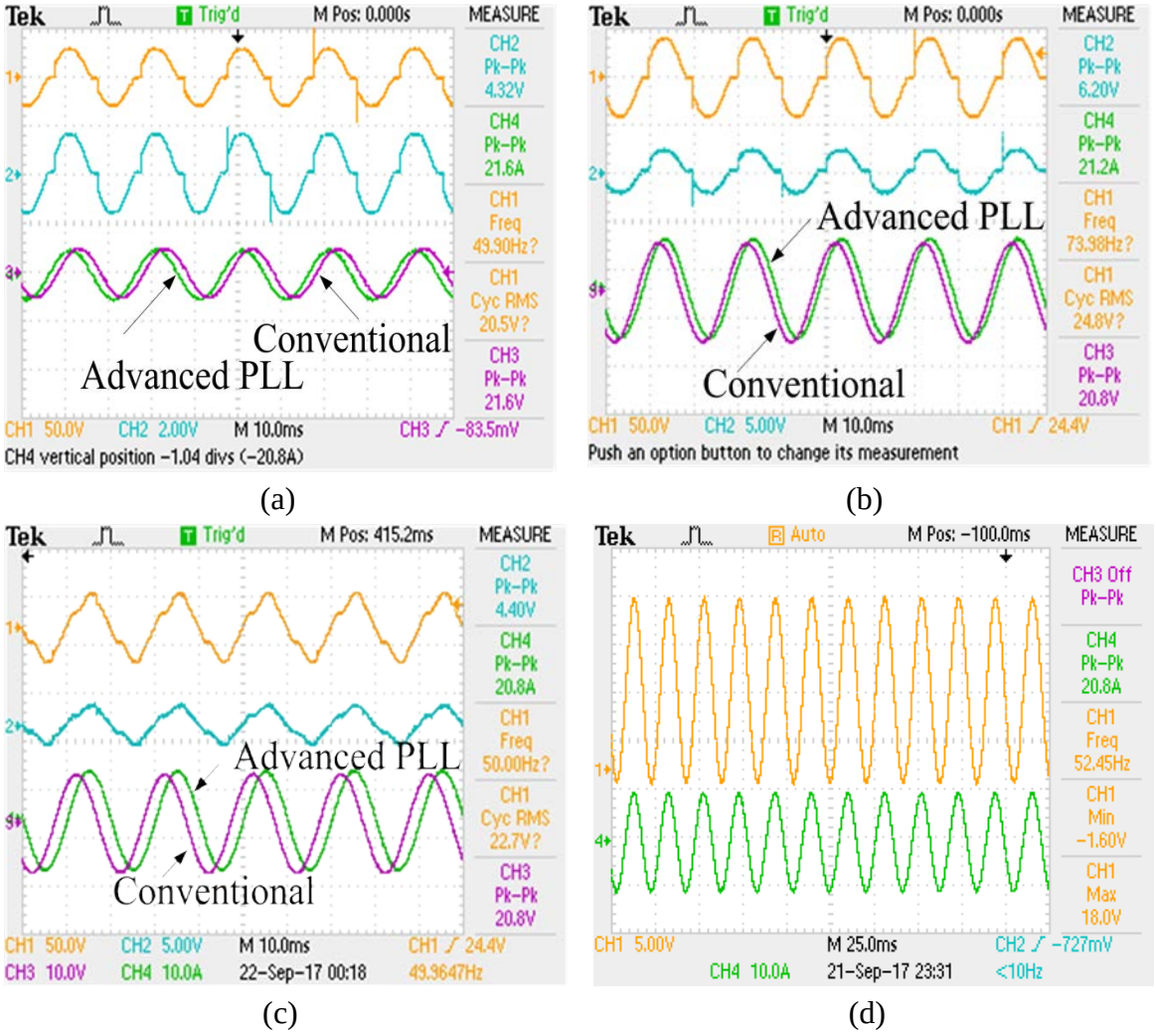


Figure 6.33 Steady-state performance of advanced PLL with respect to conventional PLL in distorted source voltage condition with (a) 15.8% THD, (b) 17% THD, (c) 21.2% THD, and (d) dc component

Figure 6.33 show steady-state performance of the advanced PLL distorted source voltage condition. THDs of source current are measured with Fluke 43B power quality analyzer. Figure 6.33 (a)-(d) shows harmonic content present in source voltage. Figure 6.34 depicts that source voltage contains 15.8%, 17% and 21.2% of THD in the line voltage, and 7.4% dc component, respectively. It can be concluded from Figure 6.33 and 6.34 that advanced PLL shows a very good steady-state response in distorted source voltage condition. As a result, phase angle tracking and frequency estimation is quite perfect in presence of harmonic component in source voltage.

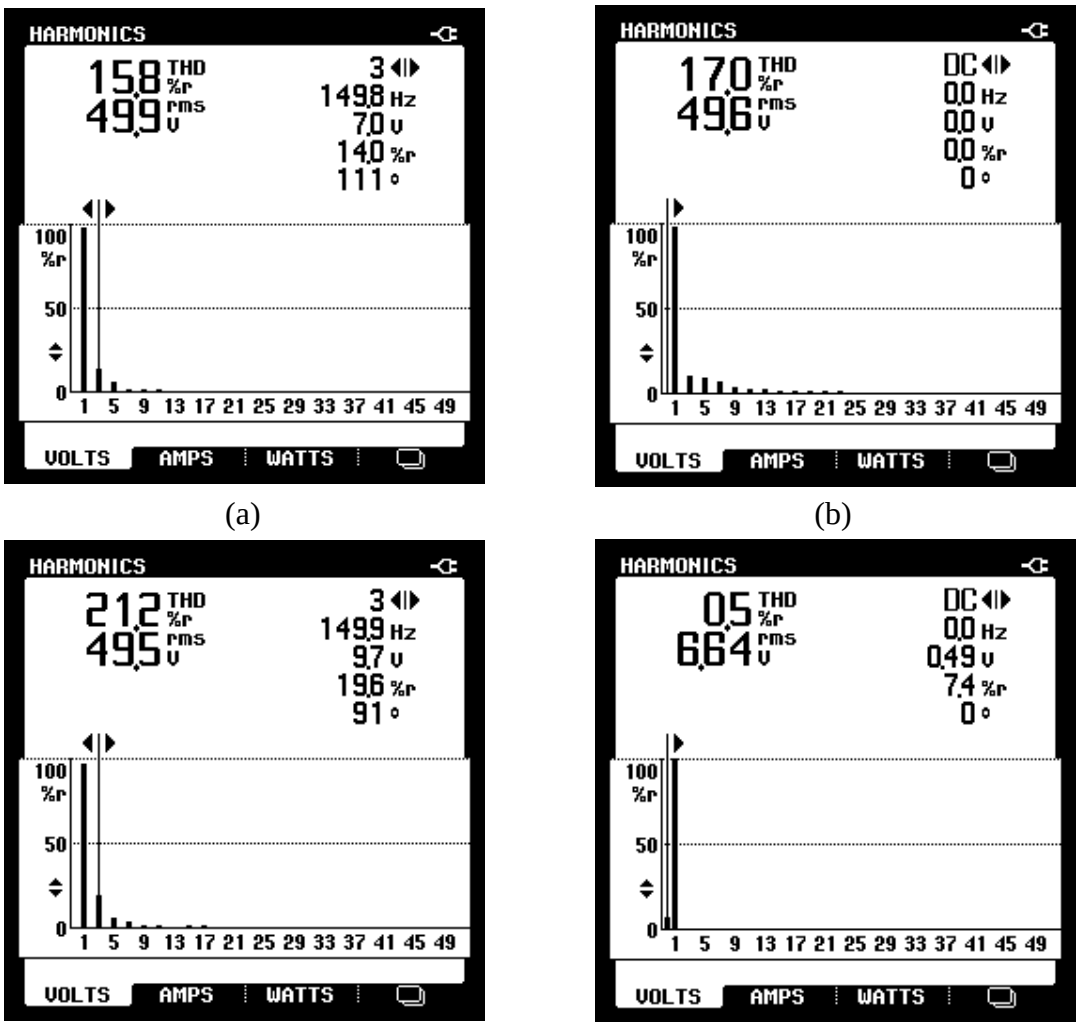


Figure 6.34 Source voltage with THD profile of (a) 15.8%, (b) 17%, (c) 21.2%, and (d) 0.5% dc

Transient performance of the advanced PLL is also depicted with change in magnitude and frequency. Performance of this PLL is tested with source voltage having dc component and the effect is shown in Figure 6.35 (a) - (d) to prove dc component rejection capability. Figure 6.35 (a) depicts unit vector generation capability of the advanced PLL in comparison to conventional PLL. Figure 6.35 (b) shows performance of the advanced PLL with variation of supply voltage. Response is compared with E-PLL performance. Figure 6.35 (b) shows performance of the advanced PLL with variation of supply voltage as well as line frequency. Response of advanced PLL is compared with response of FR-PLL and it has been found that the advanced PLL is having better transient handling capability than FR-PLL. Step change of frequency variation has been applied to this supply with change is supply voltage and Figure 6.35 (d) shows that the

transient performance of the advanced PLL is better as compared to DSOGI-PLL when frequency and magnitude is varied.

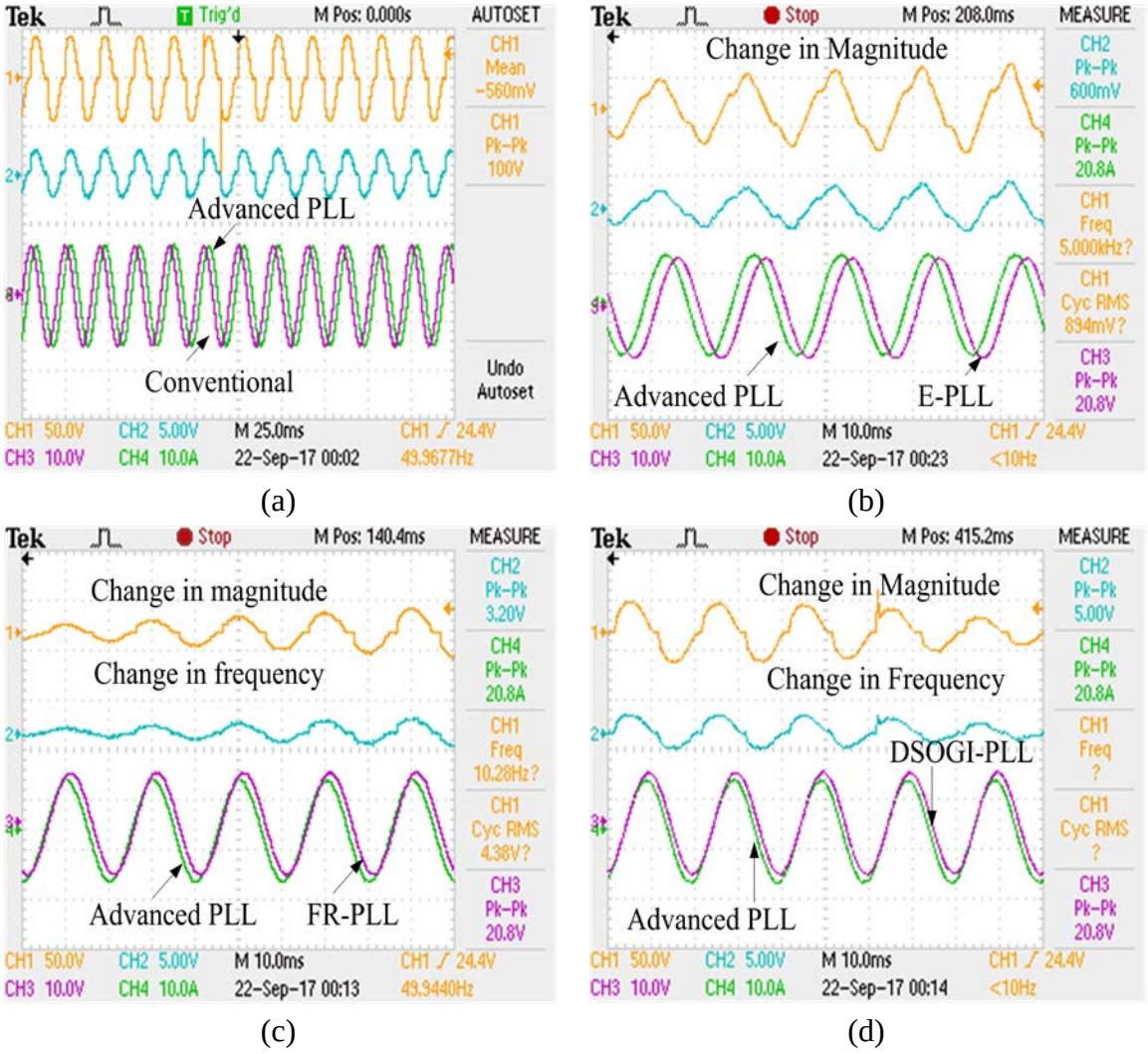


Figure 6.35 Performance of PLL in steady-state and transient conditions (a) steady-state performance with dc injected source voltage, (b) transient behavior with change in amplitude in presence, (c) transient behavior with increment in amplitude and frequency, and (d) transient behavior with decrement in amplitude

A summarized comparative analysis among advanced PLL, E-PLL, DSOGI-PLL, FR-PLL is also conducted and presented in Table 6.2. Steady-state and transient analysis of proposed PLL has been checked in real-time scenario and compared with other PLLs. Results are shown on Table 6.2 with different line voltage condition including change in voltage magnitude and frequency. It can be concluded from above analysis that the advanced PLL is having better dynamic stability with change in frequency and magnitude of input voltage during the presence of dc or highly harmonic component.

Table 6.2 Comparative analysis of PLLs based on performance

Parameter under Consideration	Advanced PLL	E-PLL [190]	DSOGI-PLL [186]	FR-PLL [187, 188]
DC offset Estimation Capability	Yes	No	Yes	Yes
Peak overshoot of frequency response with 1% of fundamental frequency change (Hz)	0.02	0.03	0.04	0.03
Parameter Selection	Four	Three	Four	Four
Settling time in case of input voltage with distortion of 10%	0.06 sec	0.12 sec	0.1 sec	0.06 sec
Settling time in case of input voltage with dc component of 10%	0.08 sec	-	0.12 sec	0.1 sec

A detailed experimental analysis on single-phase CHB-MLI based SAPF has been performed using this laboratory prototype and results have been presented for the validation of the performance of control algorithm. Modified single-phase SRF theory based control technique used for reactive power compensation and harmonic current suppression which is shown in Figure 6.36. SAPF will provide only reactive and harmonics component of supply current in phase opposition. Normally, MLI based SAPF produces switching losses in real time operation along with some leakage losses. Therefore, SAPF needs to supply these additional components. Modified control system is composed of four sections i.e. PI compensator based DC voltage controller, current reference generation, advanced PLL and PS-PWM technique. Advanced PLL can track frequency and phase with high accuracy from polluted signal. Operation of the projected PLL is already described in the previous sub-section. The advanced PLL solves synchronization issue in highly distorted supply voltage condition. DC voltage control is the first and foremost control aspect while considering CHB-MLI based SAPF. Two DC capacitors are used for five-level CHB-MLI which supplies energy during transient condition. This modified control theory uses only one PI controller for controlling two DC-link voltages in case of five-level converter because tuning of more than one PI compensator increases the complexity of the control circuit. This principle can be extended successfully if number of levels will be in higher side also. Precise DC voltage control is required so that one PI controller can be sufficient enough to take care of all DC-link voltages. SRF theory is generally one of most popular techniques available in literature for SAPF applications. This theory can be successfully applied in case of MLI

based SAPF also. In this theory, three-phase load currents are being sensed and it is converted from 'abc' frame to synchronously rotating 'd-q' frame. This theorem is modified for its use in for single-phase system along with advanced PLL in this chapter. Modifications have been made for its suitable use in case of single-phase system. Hardware validation mainly focuses on the performance enhancement of MLI based SAPF due to use of advanced PLL.

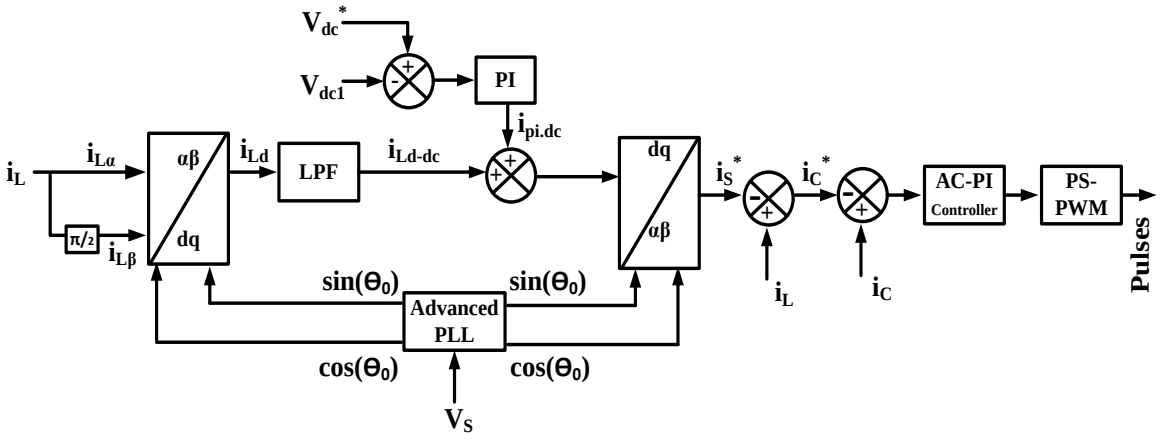


Figure 6.36 Modified control theory used for CHB-MLI based SAPF

Fictitious single-phase load currents are represented by $i_{L\alpha}$ and $i_{L\beta}$, where $i_{L\beta}$ is delayed by 90 degrees from $i_{L\alpha}$. These components are transformed to 'd-q' plane components where i_{Ld} can be represented as $i_{Ld} = i_{L\alpha}\sin\theta_0 + i_{L\beta}\cos\theta_0$. DC component of d-axis load current is obtained by using a low-pass filter. This portion represents peak magnitude of fundamental component of $i_{L\alpha}$. Output signal of dc-bus controller is depicted the switching loss related component, which is denoted by $i_{pi.dc}$. Source current reference is denoted by $i_s^* = (i_{Ld-dc} + i_{pi.dc})\cos\theta_0$ and reference compensating current can be generated by $i_C^* = i_L - i_s^*$. Reference current generated by comparing reference compensating current signal with sensed compensating current signal and error is passed through an AC-PI controller. Consequently, this reference signal is compared with phase-shifted triangular carrier waveform of 1 KHz for generation of gate pulses.

6.5.1 Uncontrolled Converter with R-L Loading

The experimental waveforms of the source voltage (V_S), source current (I_S), compensating current (I_C), load current (I_L), inverter output voltage (V_C) and DC-link

voltage (V_{dc}) of SAPF system is shown in Figure 6.37 (a) - (d) with diode-bridge rectifier and resistive-inductive (R-L) loading condition. Figure 6.37 (a) depicts sinusoidal source voltage waveform with non-sinusoidal current due to the use of rectifier fed R-L load whereas Figure 6.37 (b) shows sinusoidal source current along with sinusoidal source voltage after the operation of SAPF unit. Steady-state V_S and I_S waveform also confirms unity power factor. DC-link voltage is stabilized at its reference value during steady-state condition. Figure 6.37 (c) shows V_S, I_S, I_C, and V_{dc} in steady state operation of MLI based SAPF unit. Five-level voltage is generated by inverter unit which is seen from Figure 6.37 (d). Steady-state operation confirms effectiveness of the proposed control algorithm in non-linear loading condition.

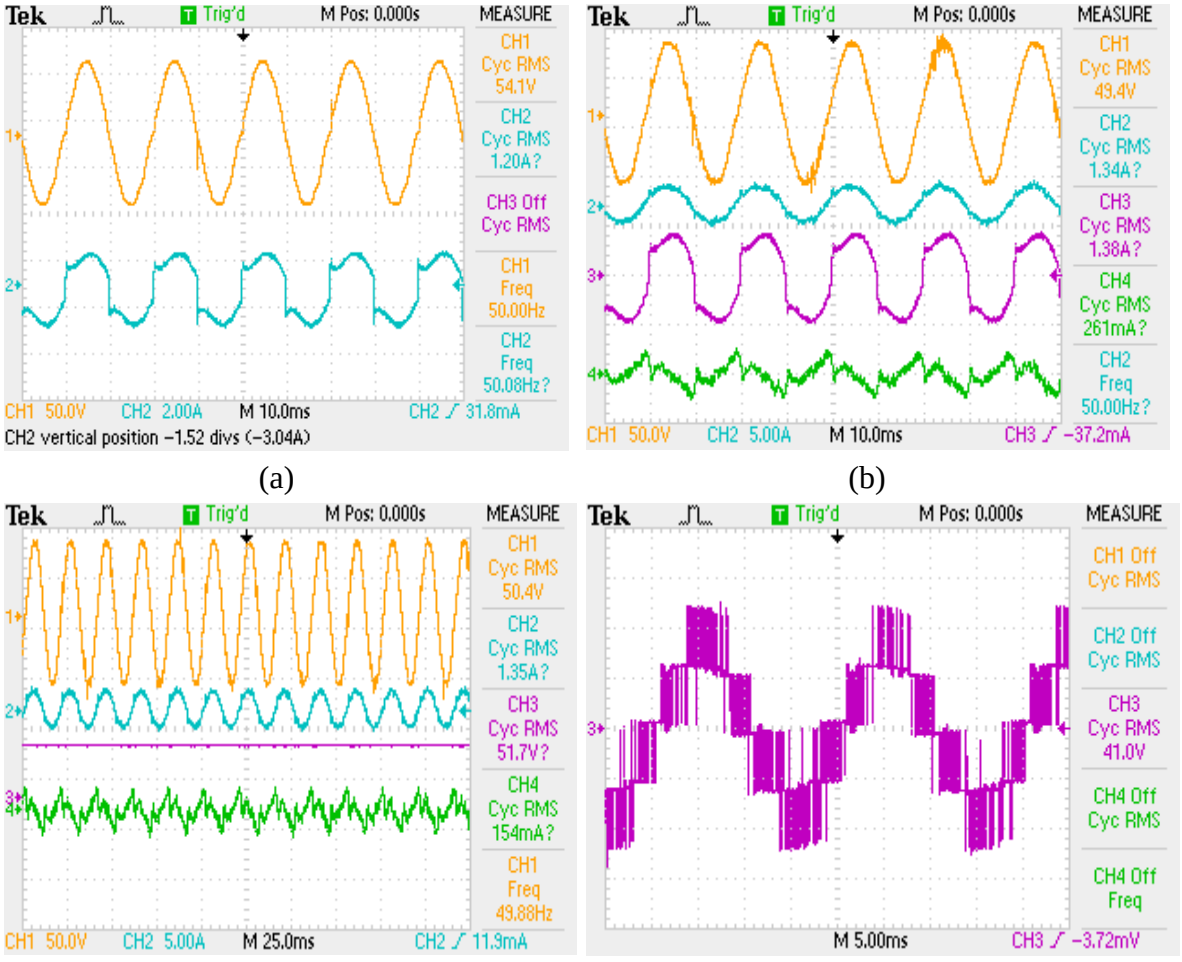
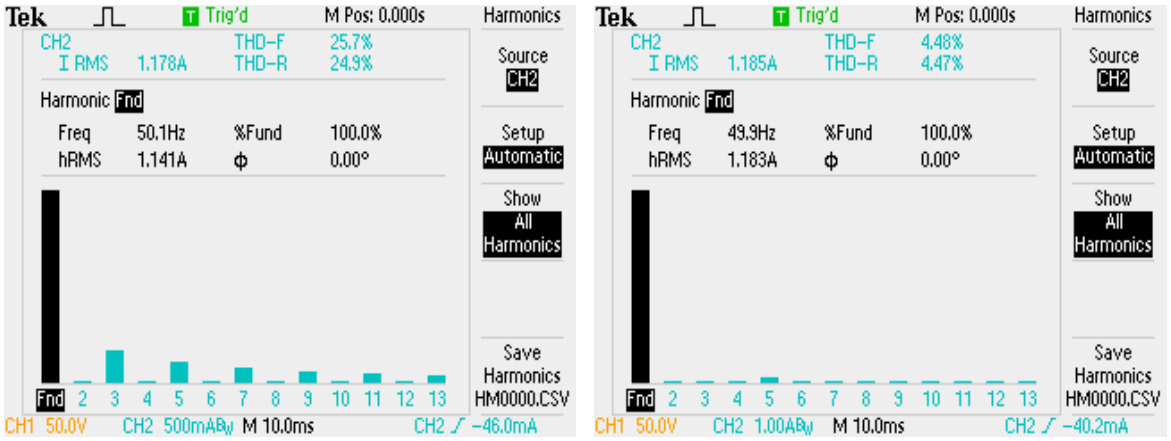


Figure 6.37 Steady-state performance of CHB-MLI based SAPF (a) V_S with non-linear current before compensation, (b) V_S and I_S after compensation with MLI output voltage, (c) V_S, I_S, V_{dc} and I_C waveform in steady state condition, and (d) V_S, I_S, I_L and I_C waveform in steady state condition

Source current is in phase with V_S and it almost maintains its sinusoidal shape during its operation which can be depicted from these figures. Source current THD is 25.7% due to non-linear loading which is shown in Figure 6.38 (a) whereas source current THD is reduced to 4.48% after the operation of SAPF unit which can depicted from Figure 6.38 (b). This THD is well within IEEE-519 permissible limit. Active power, reactive power, power factor are calculated using Fluke 43B power quality analyzer. Power factor of the utility is improved from 0.85 to 0.99. Maximum amount of reactive power has been compensated as reactive power demand comes down from 0.90 kVAR to 0.09 kVAR.



(a) (b)

Figure 6.38 THD of I_S (a) before compensation, and (b) after compensation

Effectiveness of the advanced controller is also tested during transient conditions with increment in loading and decrement of loading. Figure 6.39 (a) and 6.39 (b) show source current and load current behavior. Load is decreased and its associated voltage and current waveforms are shown in Figure 6.39 (a). DC-link voltage regulation is also tested and it is seen that, DC-link voltage is stabilized successfully with the change in loading condition. DC-link voltage behavior due to increment of loading is shown in Figure 6.39 (b).

Again load is increased and its associated voltage and current waveforms are shown in Figure 6.39 (c). The magnitude of load current is varied from 1A to 2 A rms. DC-link voltage regulation is also tested and it is seen that, DC-link voltage is stabilized successfully with the change in loading condition. Waveforms depicted in Figure 6.39 prove the stability of the system during load changing condition. DC-link voltage behavior is shown in Figure 6.39 (d) due to decrement of loading.

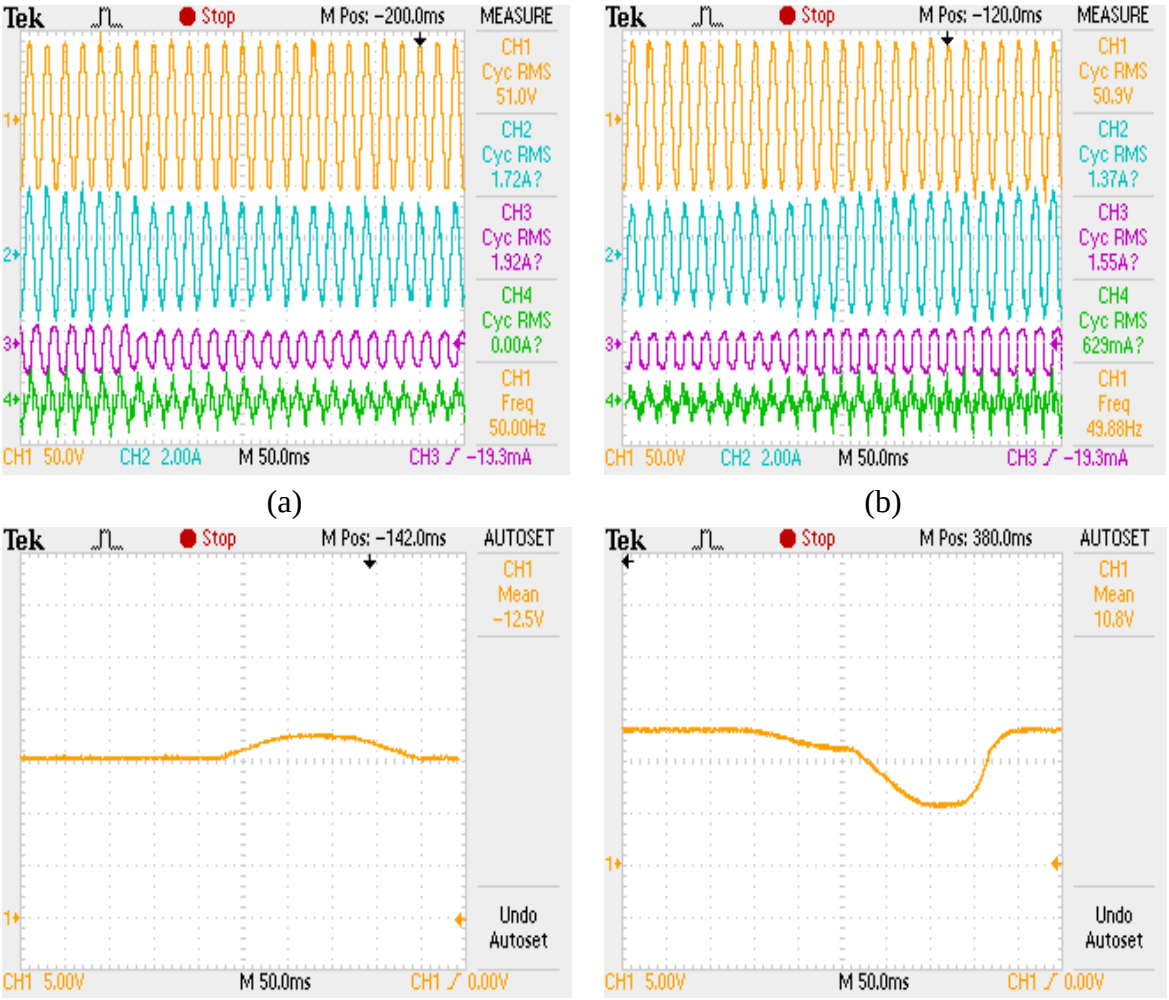


Figure 6.39 Transient behavior of CHB-MLI based SAPF (a) V_S, I_S, I_L and I_C waveform with load perturbation, (b) V_S, I_S, I_L and I_C waveform with step change of load, (c) DC-link voltage during decrement of loading, and (d) DC-link voltage during increment of loading

These voltage waveforms confirm better voltage regulation of this CHB-MLI based SAPF module during load changing behavior. So, this control theory possess better voltage regulation in terms of settling time and peak overshoot/ undershoot during the presence of highly non-linear loading.

Performance of the advanced control has been also verified under distorted supply voltage conditions as depicted on Figure 6.40 (a) - (d). Performance of the SAPF proves the effectiveness of the advanced controller in distorted source voltage condition. Distorted source voltage is depicted in Figure 6.40 (a) with non-linear I_S waveform. Steady-state performance of the advanced controller under this distorted V_S condition is

shown in Figure 6.40 (b). Source current becomes sinusoidal even if V_S is distorted. Five-level voltage waveform is generated at inverter output terminal which is shown in Figure 6.40 (c). THD of distorted source voltage is shown in Figure 6.40 (d) which is 16.6%. Steady-state detailed analysis of MLI based SAPF proves efficacy of the proposed control algorithm in distorted source voltage condition where advanced PLL is able to filter out the negative effects of distorted source voltage.

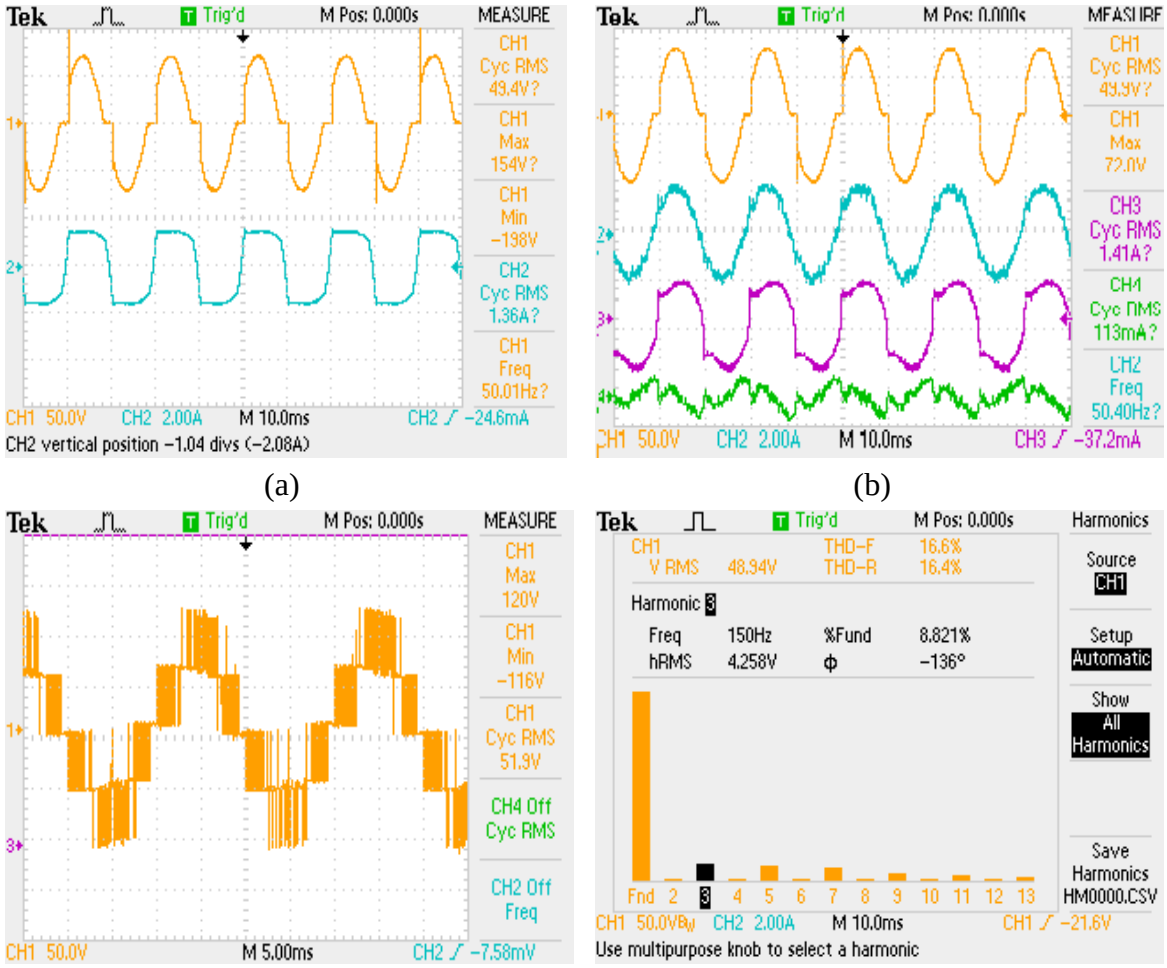
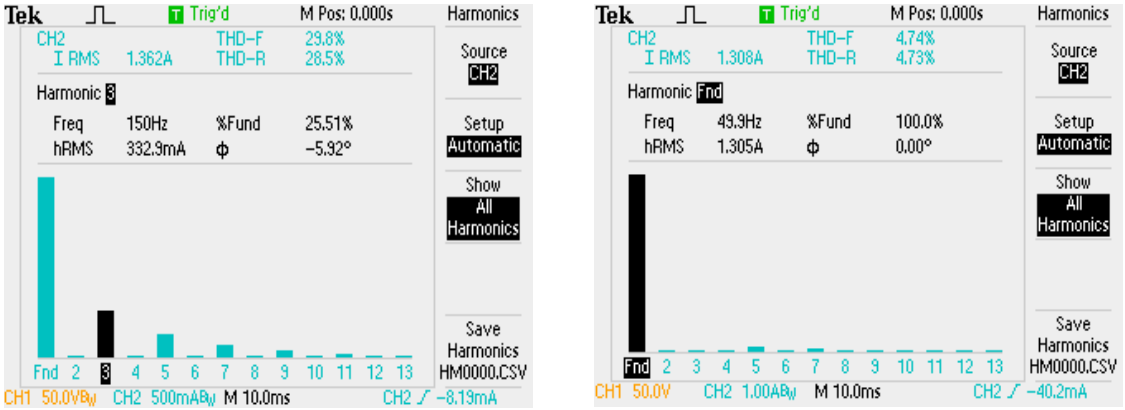


Figure 6.40 Performance of MLI based SAPF with distorted supply (a) distorted supply with non-linear source current, (b) V_S, I_S, I_L and I_C waveform in steady state condition, (c) five-level inverter output (CH3: 50V/div.), and (d) distorted source voltage THD

Source current THD before compensation is 29.8% as shown in Figure 6.41 (a). Source current THD becomes 4.74% after successful operation of SAPF unit under these circumstances as shown in Figure 6.41 (b). Therefore, from above analysis it can be concluded that the advanced controller is producing superior performance than

conventional control technique in case of filtering application in normal/ distorted V_S condition.

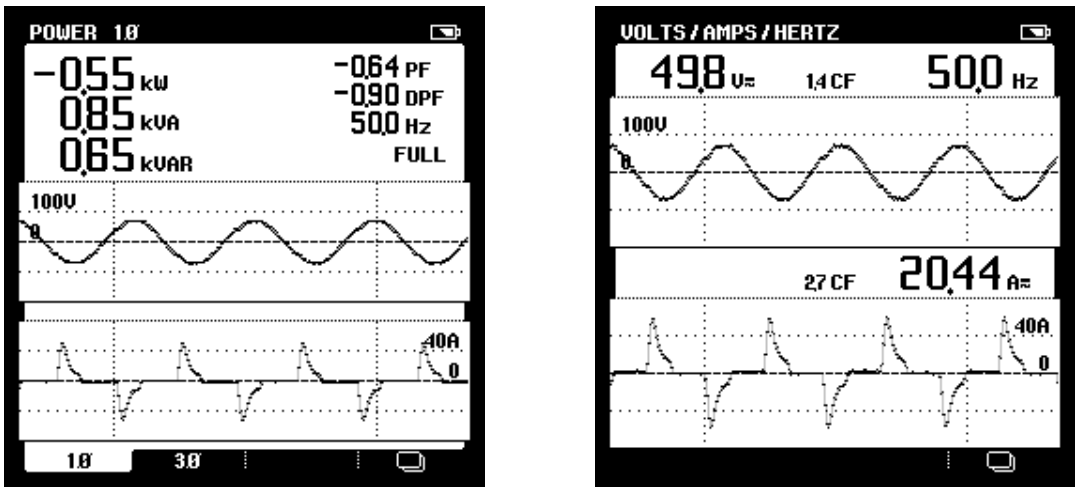


(a) (b)

Figure 6.41 THD of I_S (a) before compensation, and (b) after compensation

6.5.2 Uncontrolled Converter with R-C Loading

This control theory is also tested with diode bridge rectifier and R-C loading. Power factor was 0.64 due to the use of non-linear loading which is shown in Figure 6.42 (a). Figure 6.42 (b) depicts sinusoidal V_S waveform with non-sinusoidal I_S due to the use of rectifier fed R-C load.

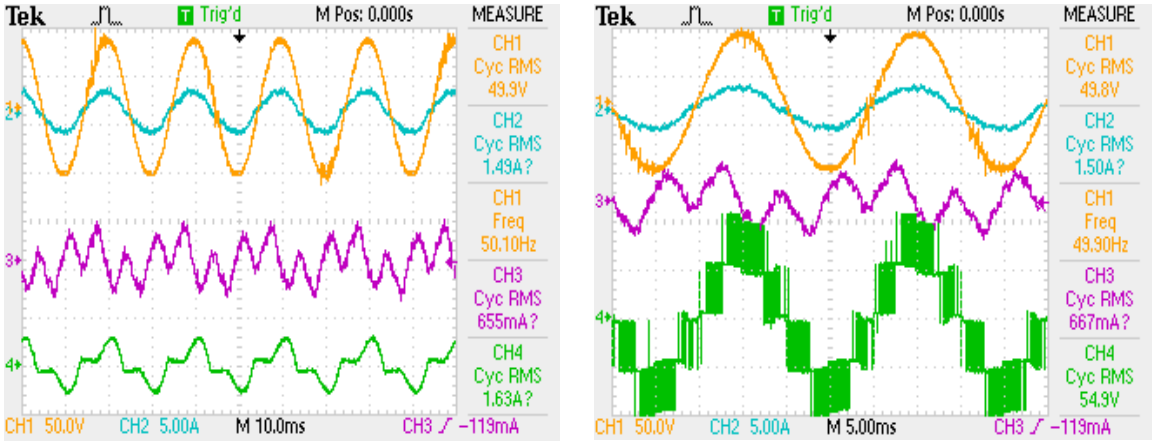


(a) (b)

Figure 6.42 (a) Source votlage and non-linear current waveform showing reactive power and power factor and (b) V_S and I_S waveform

The experimental waveforms of the I_S, I_C, I_L, V_C and V_{DC} of MLI based SAPF system with proposed control algorithm is shown in Figure 6.43 (a) - (b) with diode-bridge rectifier and R-C loading condition. Sinusoidal I_S is shown in Figure 6.43 (a)

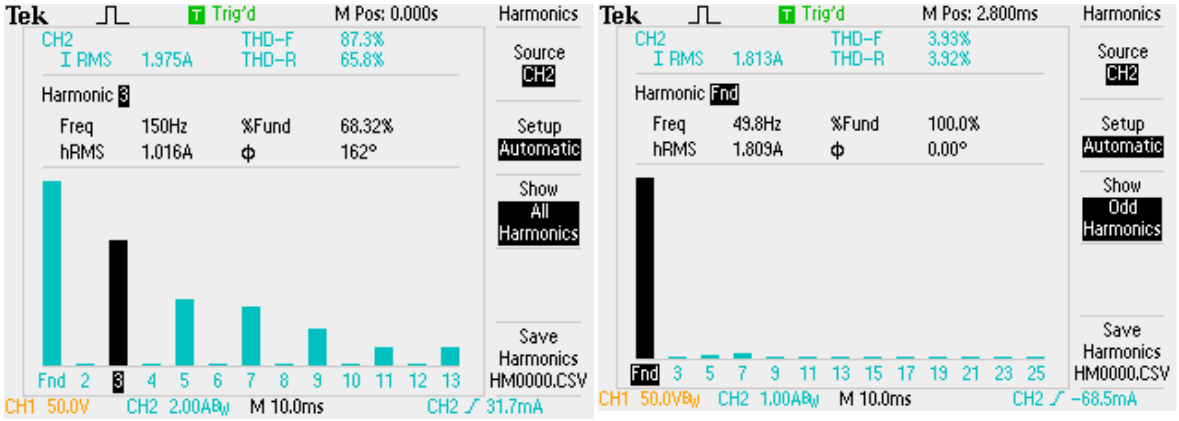
along with sinusoidal V_S after the operation of SAPF unit with near about unity power factor. Five-level voltage is generated by inverter unit which is seen from Figure 6.43 (b). Steady-state SAPF performance (V_S, I_S, I_C, I_L) is shown in Figure 6.43 (a) - (b).



(a) (b)

Figure 6.43 Performance of CHB-MLI based SAPF with R-C loading and normal supply (a) V_S, I_S, I_L and I_C waveform in steady state condition, and (b) MLI voltage output with V_S and I_S

Source current THD is 87.3% due to non-linear loading which is shown in Figure 6.44 (a) whereas source current THD reduced to 3.93% after the operation of SAPF unit which can depicted from Figure 6.44 (b). This THD of source current is well within permissible IEEE-519 limit.

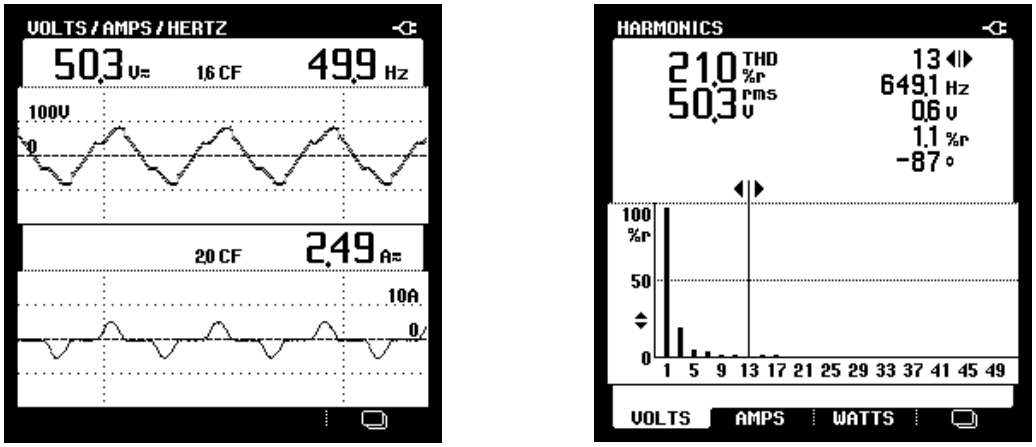


(a) (b)

Figure 6.44 THD profile of I_S (a) before compensation, and (b) after compensation

The effectiveness of the control algorithm is finally tested with R-C loading and distorted V_S. Distorted V_S is shown in Figure 6.45 (a) with non-linear current waveform and non-ideal voltage THD is shown in Figure 6.45 (b) which is 21%. Highly distorted

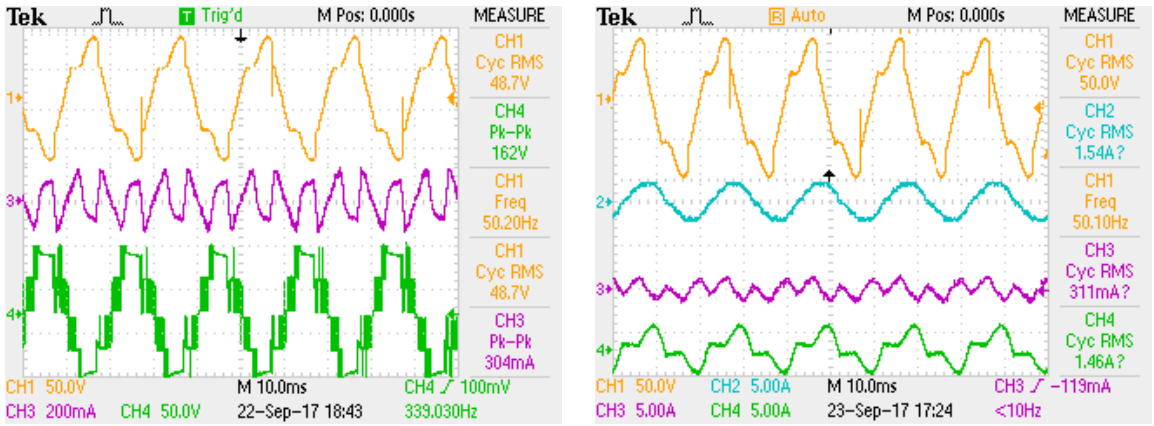
source is considered in order to prove the effectiveness of the proposed controller with R-C loading condition.



(a) (b)

Figure 6.45 (a) V_S and non-linear I_S waveform, and (b) THD of I_S before compensation

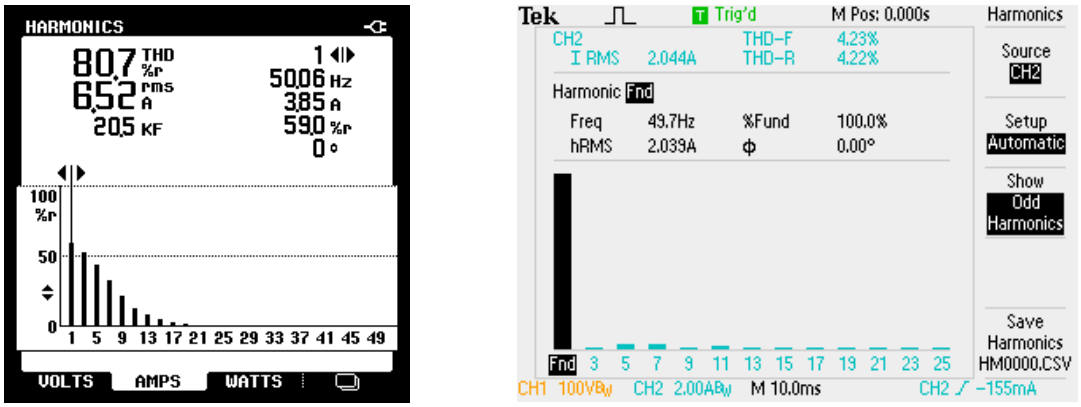
Steady-state performance of the proposed controller under this distorted supply voltage condition is shown in Figure 6.46 (a) and (b). Five-level voltage is shown in Figure 6.46 (a) whereas non-sinusoidal load current along with sinusoidal source current is shown in Figure 6.46 (b). Source current becomes sinusoidal even if V_S is distorted. Compensating current, V_C and I_L are also shown for the sake of explanation.



(a) (b)

Figure 6.46 Performance of CHB-MLI based SAPF with R-C loading and distorted supply (a) V_S and I_C waveform with MLI output and (b) V_S, I_S, I_L and I_C waveform in steady state condition

Source current THD of load current before compensation was 80.7% which is shown in Figure 6.47 (a). Source current THD becomes 4.23% after successful operation of SPAF unit under these circumstances as shown in Figure 6.47 (b).



(a) (b)

Figure 6.47 THD of I_S (a) before compensation, and (b) after compensation

Therefore, from above analysis it can be concluded that the proposed controller is producing better performance than conventional control technique in case of filtering application with normal/ distorted source voltage conditions. Hardware implementation of advanced PLL and PLL based control algorithm is rigorously tested in different non-linear loading conditions as well as under different supply conditions. PLL effectiveness can be depicted from the above calculative analysis as well as its hardware result validation. Finally, these results are compared with recently published work. The advanced PLL is effectively used in case of MLI based filtering applications with different loading condition. This shows the efficacy of the advanced PLL and PLL based modified control algorithm.

6.6 CONCLUSION

An improved synchronous reference frame theory based control algorithm is proposed in this chapter for solving current related power quality problems. This proposed control is a complete solution in case of balanced and/or unbalanced loading condition in existing distribution system. This control algorithm is equally effective in case of distorted and/or unbalanced supply voltage condition due to the use of advanced PLL. Complete mathematical modeling and stability analysis of the advanced PLL is proposed in this chapter which is capable of exact phase angle, amplitude and fundamental component measurement along with dc offset removal from normal / polluted source voltage. A novel effective methodology based on Eigen value analysis is proposed for parameter design of PLL constants. Theoretical analysis, simulations and hardware prototype results prove that the advanced PLL is effective and gives better

performance than recently published work in both steady-state and transient conditions. An experimental study of five-level CHB-MLI based SAPF with advanced PLL is also carried out to prove the effectiveness of the advanced PLL based controller in case of polluted supply and under different non-linear loading conditions. Transfer function based approach has been performed for closed-loop stability analysis of modified SAPF control theory. Simulation and experimental validation prove that the advanced PLL based SAPF control algorithm is well capable of maintaining sinusoidal source current even in distorted supply voltage conditions. Therefore, proposed system provides a complete solution to PQ problems in medium- to high-voltage applications.

CHAPTER 7

ACTIVE AND REACTIVE POWER MANAGEMENT OF CHB-MLI BASED GRID-TIED PHOTOVOLTAIC

List of Publications

1. **S. Ray**, N. Gupta, R. A. Gupta, "Active and Reactive Power Management of Photovoltaic Fed CHB Inverter Based Active Filter with Improved Control under Normal/Distorted Supply," in Proc. *of 12th IEEE International Conference on Industrial Electronics and Applications (ICIEA)*, June 2017, Siem Reap, Cambodia, pp. 572-577.
2. **S. Ray**, N. Gupta, R. A. Gupta, "Advanced PWM for Balancing DC-link Voltages in Seven-Level CHB Inverter based Active Filter," in Proc. *of 2nd IEEE International Conference on Recent Development in Control, Automation and Power Engineering, (RDCAPE)*, Oct. 2017, Delhi, pp. 1-6.

CHAPTER 7

ACTIVE AND REACTIVE POWER MANAGEMENT OF CHB-MLI BASED GRID-TIED PHOTOVOLTAIC

[This chapter shows application of five-level CHB-MLI based SAPF for active and reactive power management with grid-tied photovoltaic. Therefore, this chapter first presents modeling of two-stage CHB-MLI based SAPF for active and reactive power management in grid-tied PV application. A boost converter is used in between PV and CHB-MLI for scaling up voltage level. Control algorithm of this two-stage conversion system is composed of boost converter control and CHB-MLI control. Perturb and Observe (P and O) MPPT is used for ensuring maximum power point tracking during variable irradiance. Self-charging algorithm is used for balancing dc-link voltages of five-level CHB-MLI. PS-PWM technique is used for generating MLI gate pulses. Advanced PLL which is projected in previous chapter is used in control algorithm in order to ensure its operation under non-ideal source voltage conditions.]

7.1 INTRODUCTION

Grid interconnection of different renewable energy sources is gaining its importance around the globe because of its cost-effective nature [192-201]. At the same time, distributed generation (DG), combination of conventional and renewable energy sources, also provides a better platform for future power generation scenario. DGs are capable of supplying up to 10 kW load and located near load centers [202-212]. Among all these available energy resources, photovoltaic (PV) is having better potential in current scenario. By analyzing the importance of grid-tied solar energy, utmost quantity of researches is going on in the course of active and reactive power control of grid-side converter, system efficiency improvement, choice of different converters and optimal use of passive elements while integrating PV to grid.

Cost and system effectiveness are major concerns among researchers while connecting PV to existing grid. But, at the same instant of time, use of power electronic converters (PECs) in distribution sector produce harmonics, create extra demand for reactive power in distribution grid hence create different power quality (PQ) problems. These PQ problems can be solved by implementing passive filters (PF), active power filters (APFs), unified power quality conditioner (UPQC) etc. in existing line. Among all

these available solutions, shunt APF (SAPF) is the most useful solutions available for mitigating above mentioned PQ problems in this era of power electronics. Line-frequency transformer is needed while connecting inverter module to PCC of medium-voltage grid. Use of transformer reduces system efficiency and they are bulky in size. In this context, multilevel inverter based filtering approach can provide transformer-less interconnection of converters, gives cost-worthy solution and provides better power quality. Multilevel inverters are becoming popular day by day because of its unique advantages over two-level inverter such as lower switching stress during turn-on and turn-off of semiconductor devices; need to bear less reverse voltage and current rating, lower rating filter requirement etc. Multilevel inverters can be categorized into three basic topologies i.e. DC-MLI, FC-MLI and CHB-MLI. Among these three, CHB-MLI is having advantages over other two converter topologies because of its modular structure and requirement of lesser amount of switching devices. Modules can be replaced easily during maintenance and even modules can be bypassed with proper control algorithm in faulty condition.

Therefore, in this chapter, single-phase CHB-MLI based transformer-less grid-tied PV system is proposed with modified control strategy so that system can supply active as well as reactive power in day time and can act as SAPF during night time. The proposed control algorithm is composed of self-charging algorithm, which is responsible for DC-link voltage regulation and advanced PLL, which can extract exact phase angle information even in distorted source voltage conditions. This proposed structure, as shown in Figure 7.1, consists of PV array, boost converter and five-level CHB inverter. PV array with boost converter is used as DC voltage source of each H-bridge of CHB, where P and O MPPT algorithm decides the switching pattern of boost converter for improving efficiency of the proposed system. Advanced PLL which is projected in previous chapter is used in control algorithm in order to ensure its operation under non-ideal source voltage conditions. A detailed mathematical modeling of the proposed system is presented and the total system in lower scale is simulated in MATLAB/Simulink. This system with modified control algorithm is rigorously tested in different non-linear loading conditions as well as with different irradiations. Transient and steady-state behavior of the proposed system decides effectiveness of the proposed scheme during night-time and in different weather conditions during day-time.

7.2 SYSTEM DESCRIPTION

Figure 7.1 depicts proposed grid-tied system which consists of PV arrays, boost converters, DC balancing capacitor, single-phase five-level CHB inverter and grid interfacing inductor. This proposed system is tested with $400V_{p-p}$ AC voltage grid. PV arrays are capable of supplying 2 kW of peak power. However, this proposed topology can be extended for medium-voltage and high-power distribution system. Boost converter 1 and 2 consist of self commutating switch S1 and S2, respectively which are switched by P and O MPPT technique. C_{dc1} and C_{dc2} are dc voltage balancing capacitors before connecting boost converter output to H-bridges. Five-level inverter is used for this study.

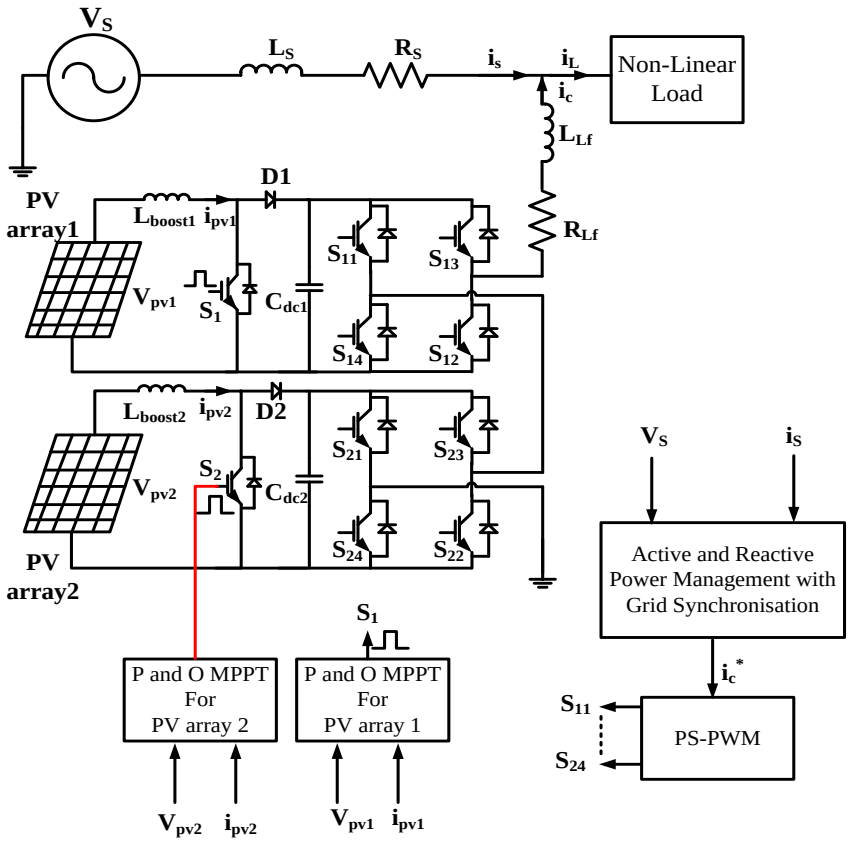


Figure 7.1 Proposed grid-tied system with power quality improvement phenomenon

Therefore, two numbers of H-bridges are used for generation of five-level voltage output at the inverter end. S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24} are switches of two H-bridges which are switched with the help of phase shifted PWM techniques. One grid interfacing inductor is used before connecting this module to PCC of the grid. This system can work with linear as well as highly non-linear loads. Modified control

algorithm takes care of proper reactive power management of inverter module during the operation of SAPF mode and active power transfer between PV and grid as well as reactive power minimization during day time. P and O MPPT is applied to boost converter switches for improving efficiency in different weather conditions.

7.3 MODELING OF PROPOSED SYSTEM

The grid-tied PV system modeling is given in this section for different converters and required passive elements.

7.3.1 Modeling of PV Array

The proposed system is designed for 2 kW peak power capacity at PCC of grid. Active power demand of the proposed system can be calculated by using Equation 7.1 [192].

$$P_{max,m} = V_{mpp,m} \text{ x } I_{mpp,m} \tag{7.1}$$

In most of the condition, maximum voltage at maximum power point ($V_{mpp,m}$) is 85% of open-circuit voltage (V_{OC}) and maximum current at maximum power point ($I_{mpp,m}$) is 85% of short-circuit current (I_{SC}).

7.3.2 Modeling of DC-DC Boost Converter

The ripple content in inductor current (i_1) of boost converter is designed as per Equation 7. 2 [192].

$$i_1 = \frac{V_d D(1-D)}{2.\Delta i_1.f_{SW}} \tag{7.2}$$

where, boost converter operates with duty cycle D. DC- link voltage at capacitor C_{dc1} and C_{dc2} is considered as V_d. Permissible change in current ripple (Δi_1) is considered as 3% of i_1, where i_1 is calculated by Equation 7.3 [192].

$$i_1 = P/V_i \tag{7.3}$$

where, V_i is the input voltage applied to boost converter.

7.3.3 DC Bus Voltage Selection

Adequate reactive power compensation can only be done when DC-link voltage ($V_{dc\text{-}link}$) is greater than grid voltage which can be calculated as per Equation 7.4 [192].

$$V_{dc-link} = \frac{2\sqrt{2}\, V_L}{\sqrt{3}m} \tag{7.4}$$

where, m denotes modulation index of inverter module.

7.3.4 DC-link capacitor selection

DC-link needs to sustain disturbances during load perturbation. It is the main criteria while selecting DC bus capacitor. It can be found out from Equation 7.5 [192].

$$C_{dc} = \frac{I_d}{2.\omega.V_{dc.ripple}} \tag{7.5}$$

where, I_d can be found from Equation 7.6 and $V_{dc.ripple}$ is considered as 3% of V_{dc}.

$$I_d = P_{dc}/V_{dc-link} \tag{7.6}$$

7.3.5 Inductor Selection

One interfacing inductor (L_{Lf}) is required before connecting total unit to PCC of grid. L_{Lf} can be calculated as per Equation 7.7 [192].

$$L_{Lf} = \frac{\sqrt{3}.m.V_{dc}}{12.h.f_s.\Delta I_{d.ripple}} \tag{7.7}$$

where, h denotes overloading factor and $\Delta I_{d.ripple}$ is considered 10% of I_d.

7.4 CONTROL STRATEGY

A modified control strategy for active and reactive power management of inverter during day time is proposed in this chapter. The same control technique also ensures reactive power compensation with harmonic current cancellation during night time. This proposed control is also able to operate perfectly under distorted source voltage conditions with the help of advanced PLL as mentioned in the previous chapter. This PLL is able to extract exact phase angle information even with harmonic component present in the grid voltage. Self-charging algorithm confirms stable operation of DC-link voltages during steady-state and transient conditions. At the same instant of time, P and O MPPT ensures the boost converter operation at maximum power point in all weather conditions whereas five-level CHB is switched using phase-shifted PWM technique (PS-PWM). The proposed control mechanism is depicted in Figure 7.2.

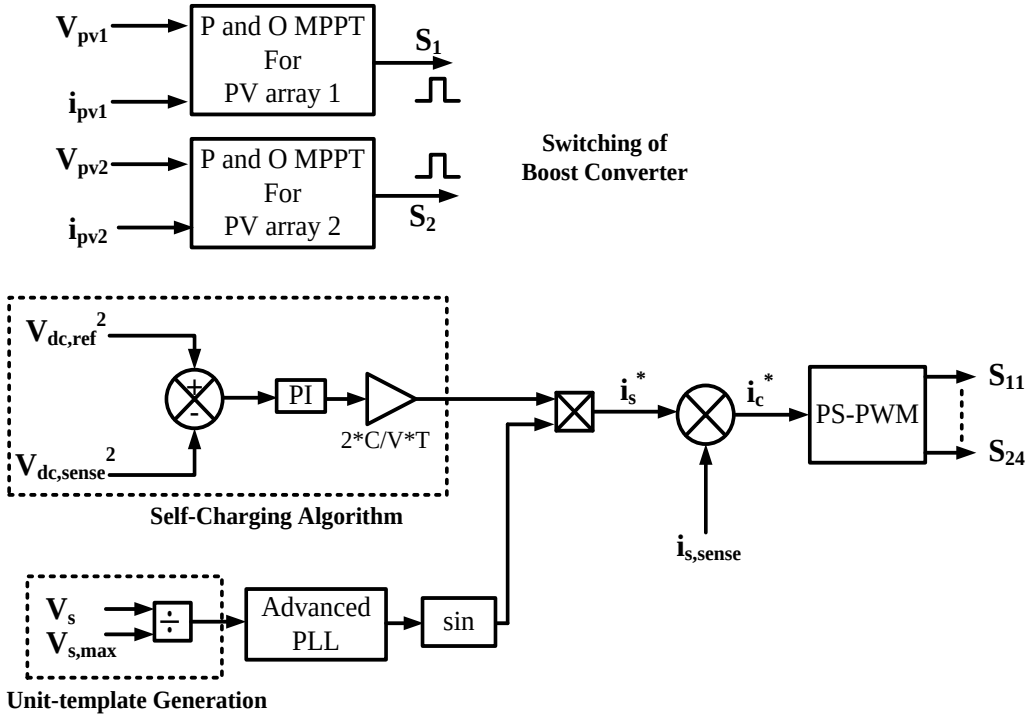


Figure 7.2 Proposed control theory for active and reactive power management

Control mechanism of PV fed CHB-MLI based SAPF is mainly divided into two portions i.e. control of DC-DC boost converter and control of multilevel inverter unit.

7.4.1 P and O MPPT Control

The photovoltaic system has some major disadvantages, the conversion and generation of power is not efficient and power changes with varying insolation as well as with temperature. Power-voltage and current-voltage relationship of solar PV is non-linear in nature. A unique point is present in power-voltage curve or in current-voltage curve called maximum power point (MPP), at which point that module operates with maximum efficiency at particular weather condition. The exact value of maximum power point is not fixed, but can be found by using search type algorithms. Mainly incremental conductance (IC) and perturb and observe (P and O) MPPT algorithms are used for deciding maximum power point in any weather condition. Among these available options, P and O MPPT algorithm is simpler for implementation purpose and having better performance characteristics [199]. Figure 7.3 shows flow-diagram of P and O MPPT algorithm. This algorithm is based on the calculation of output power of PV module and power is calculated by current and voltage.

This P and O MPPT algorithm takes voltage and current of PV strings as input quantities and these inputs are multiplied at each instant. Therefore, it calculates the value of power at k^{th} instant. The next sample is also taken as input parameters and these samples will calculate power for next instant i.e. for $(k+1)^{th}$ instant. Difference between voltages and power in k^{th} instant and $(k+1)^{th}$ instant is calculated in the next step. If the magnitude of difference in the power is increasing in nature, then the difference between voltage at k^{th} instant and $(k+1)^{th}$ instant is also measured. If this quantity also becomes negative, the perturbation in duty ratio (" D) will continue to rise in the same direction in the next cycle, otherwise reversed [211].

The detailed calculation mechanism of duty ratio for switches S1 and S2 depends on the following four conditions.

Condition 1:

If $\Delta P_{PV}>0$ and $\Delta V_{PV}<0$, then perturbation in duty ratio (ΔD) will increase.

Condition 2:

If $\Delta P_{PV}>0$ and $\Delta V_{PV}>0$, then perturbation in duty ratio (ΔD) will decrease.

Condition 3:

If $\Delta P_{PV}<0$ and $\Delta V_{PV}<0$, then perturbation in duty ratio (ΔD) will decrease.

Condition 4:

If $\Delta P_{PV}<0$ and $\Delta V_{PV}>0$, then perturbation in duty ratio (ΔD) will increase.

This procedure is applied for selection of duty cycles for switches S1 and S2, separately. Voltage and current quantities required for MPP is sensed separately in order to ensure MPPT operation for both the boost converters. At MPP, in order to reduce voltage oscillation during weather changing condition, the perturbation step size should be minimized. Therefore, " D is an important deciding factor while calculating duty ratio for MPP condition. If " D is small enough, then the duty cycle variation will be near about perfect. This will indirectly impact the system performance. These corrected duty ratio as per P and O MPPT have been applied to the boost converter switches S1 and S2 which will ensure operation of boost converter in all weather conditions.

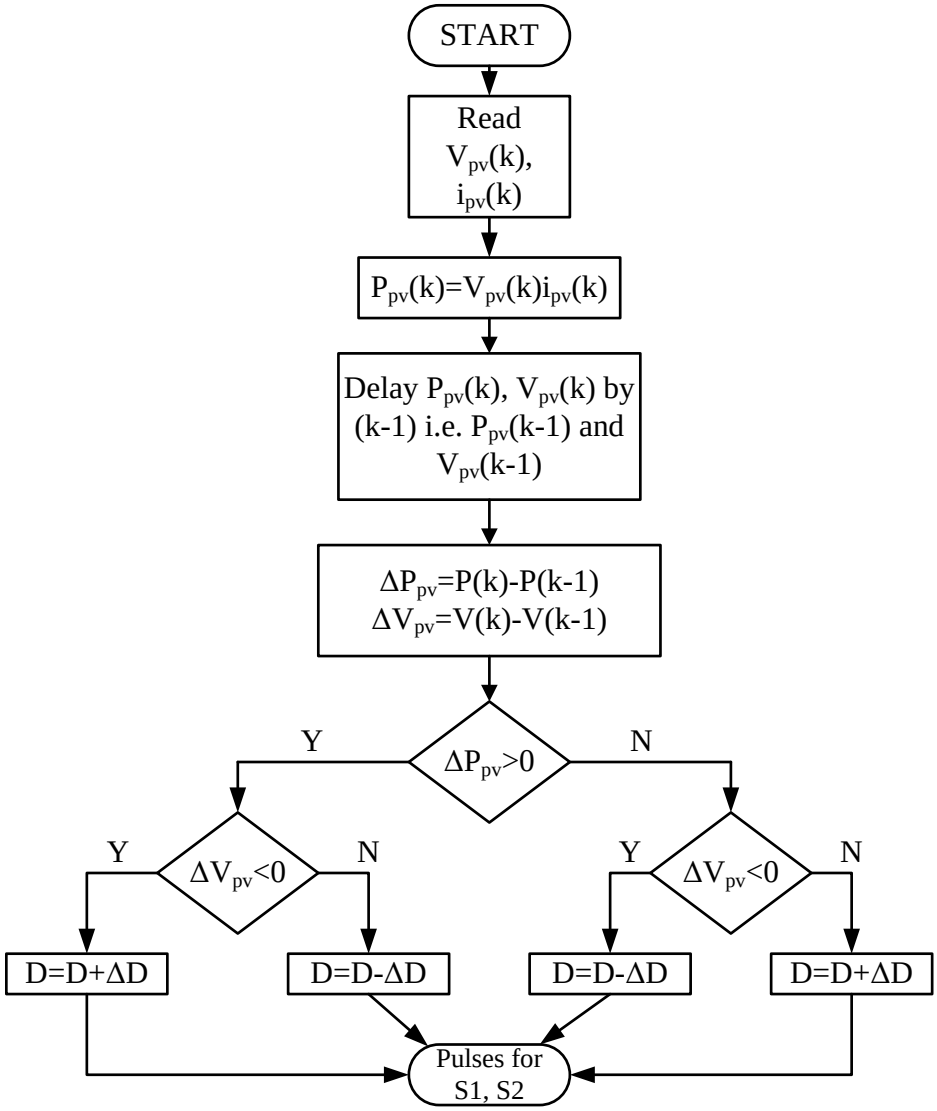


Figure 7.3 P and O MPPT applied to DC/DC boost converter [211]

7.4.2 DC-link Voltage Control

Control strategy of inverter can be divided into three sections. Firstly, source current (I_s) and source voltage (V_s) and DC-link voltage ($V_{dc\text{-}link}$) signals are sensed by current and voltage sensors. Advanced PLL, as mentioned in the previous chapter, gives idea about phase angle with respect to V_s, which is shown in Figure 6.1 (b). Advanced PLL helps to find out phase angle in proper manner even if the source voltage is distorted. Secondly, I_S^* is compared with I_S in order to generate reference current. Finally current error is processed through PS-PWM technique for generation of gate pulses for IGBTs present in five-level CHB-MLI. P and O MPPT is used for boost converter operation

which is shown in the Figure 7.2 for the sake of the complete control strategy of the proposed system.

For successful operation of five-level CHB as a SAPF, DC-link voltages, V_{dc1} and V_{dc2} need to be maintained constant at same reference value in different loading conditions and during load perturbations. For five-level CHB inverter, two DC-links are used. Normally, two different PI controllers are used for balancing DC voltage for wide range of variations of irradiations during day-time and during its operation as SAPF. In this proposed control mechanism, only one PI controller is used for tracking any one of the DC-link voltages, as both voltages are symmetrical in nature. This results reduction in number of sensors and sensor related amplifier circuit components. This further reduces complexity of the circuit. Finally, self balancing algorithm [207] is used instead of normal DC voltage controller as its produces fine response in terms of voltage overshoot, response time during transient conditions.

Energy conversion principle is used in self-charging algorithm for charging and discharging of DC-link capacitors. At the starting of the SAPF system, an additional energy is required to regulate dc-link voltage from the utility for charging the capacitors. Throughout the charging procedure, capacitor voltage has little fluctuation nearer to the desired DC-link voltage. This phenomenon provides some amount of energy change in the dc-link. The amount of energy stored in the capacitor is denoted by:

$$\Delta E = C_{dc}/2 \,.\, [(V_{dc}^{*})^2 - (V_{dc})^2] \tag{7.8}$$

At the same time, the energy delivered by utility for the capacitor is represented by Equation 7.9.

$$E_{ac} = P.\, t_C = V_{RMS} I_{RMS} t_C \tag{7.9}$$

As capacitor takes one half-cycle to charge itself so, t_c can be considered as T/2, where T can be defined as per supply frequency 50 Hz. Again, V_{RMS} and I_{RMS} can be expressed in terms of peak magnitudes as described by Equation 7.10.

$$E_{ac} = V/\sqrt{2} \,.\, I_{dc}/\sqrt{2} \,.\, T/2 \tag{7.10}$$

As per energy conversion principle, by neglecting switching losses of CHB-MLI based VSI, change in energy is denoted by

$$\Delta E = E_{ac} \tag{7.11}$$

So, from Equation 7.9 and Equation 7.11, Equation 7.12 is formed.

$$C_{dc}/2\,.\,[(V_{dc}^{*})^2 - (V_{dc})^2] = (V.I_{dc}.T)/4 \tag{7.12}$$

So, I_{dc} can be defined as per Equation 7.13.

$$I_{dc} = (2C_{dc}/VT).[(V_{dc}^{*})^2 - (V_{dc})^2] \tag{7.13}$$

In self-charging algorithm, voltage error 'e' can be defined as per Equation 7.14. Voltage error is minimized through PI compensator.

$$e = [(V_{dc}^{*})^2 - (V_{dc})^2] \tag{7.14}$$

Self-charging algorithm is having a simple construction of DC voltage control in case of CHB-MLI based SAPF. This algorithm exhibits good transient response of DC-link voltages with respect to PI controller based approach. Above mentioned simple calculative effort is only needed for the generation of reference signal.

7.4.3 Phase Angle Control using Advanced PLL

Another important portion of this control algorithm is use of Advanced PLL logic, as mentioned in previous chapter and shown in Figure 6.1 (b). This Advanced PLL is used in this control mechanism for extracting fundamental component of source voltage and measurement of phase angle with better accuracy even when the source voltage is polluted. Figure 6.9 (a) shows Advanced PLL performance in distorted source voltage condition. Figure depicts that fundamental component is successfully extracted from polluted source voltage.

7.4.4 Gate Pulse Generation using PS-PWM

Modulation technique is an important part of any control scheme of inverter circuit. Proposed work has used PS-PWM technique for generating gate pulses of CHB-MLI. This modulation technique allows even amount of power distribution among H-bridge cells as this is very much important for voltage balancing. Four numbers of triangular signals are used as carrier wave. As four numbers of carriers are present, each carrier is phase shifted by 90 degree. If first triangular signal magnitude is lesser than sinusoidal reference signal magnitude, then upper switch of one leg and one H-Bridge is

on and else it will be on zero/off condition. The other switch of that particular leg will follow the reverse logic. Similarly, switching of the rest of the three legs will be decided by the same manner. PS-PWM technique working principle is depicted on Figure 6.6 (a) whereas pulses of switches S11, S14, S21 and S24 are shown in Figure 6.6 (b) for ready reference.

7.5 PERFORMANCE ASSESSMENT OF CHB-MLI BASED GRID-TIED PV SYSTEM USING MATLAB/ SIMULINK

Modeling of 2kW grid-tied PV system is done in MATLAB/Simulink environment. The proposed system is tested with solar irradiation of 500 W/m^2 during day time. Irradiation is considered as 0 during night time whereas temperature is fixed at 25^0C. P and O MPPT is implemented in MATLAB/Simulink for switching of boost converter in order to extract maximum power point. Self-balancing algorithm, Advanced PLL and PS-PWM is implemented for required gate pulse generation of inverter switches. This proposed topology is tested in varying irradiations.

This proposed system is tested under varying irradiations and under different loading conditions. Figure 7.4 depicts source voltage (V_S), source current (I_S), inverter output current (I_C), PCC voltage (V_C) and DC-link voltage (V_d) during day and night time with diode-bridge rectifier based R-L loading condition while Figure 7.5 depicts PV fed CHB-MLI based SAPF behavior in load changing condition. Figure 7.4 shows that MLI basedSAPF unit is connected to PCC at t=0.1 sec. instant during day time with an irradiance of 500 W/m^2. At t=0.4 sec. instant, irradiation becomes zero. At this instant, source current magnitude increases though load current magnitude is fixed. This result clearly clarifies that current is being supplied during day-time by the solar PV inverter unit while during night time; it is not feeding any kind of active power. It is worth noting that, source current is still sinusoidal during night time even though load current is non-linear in nature. It can be also depicted from the figure that DC-link voltages of two capacitors are stabilized at their reference value during the change in irradiation which confirms the effectiveness of self-charging algorithm based DC-link control. Five-level voltage is also generated at inverter output which confirms the proper operation of five-level CHB inverter.

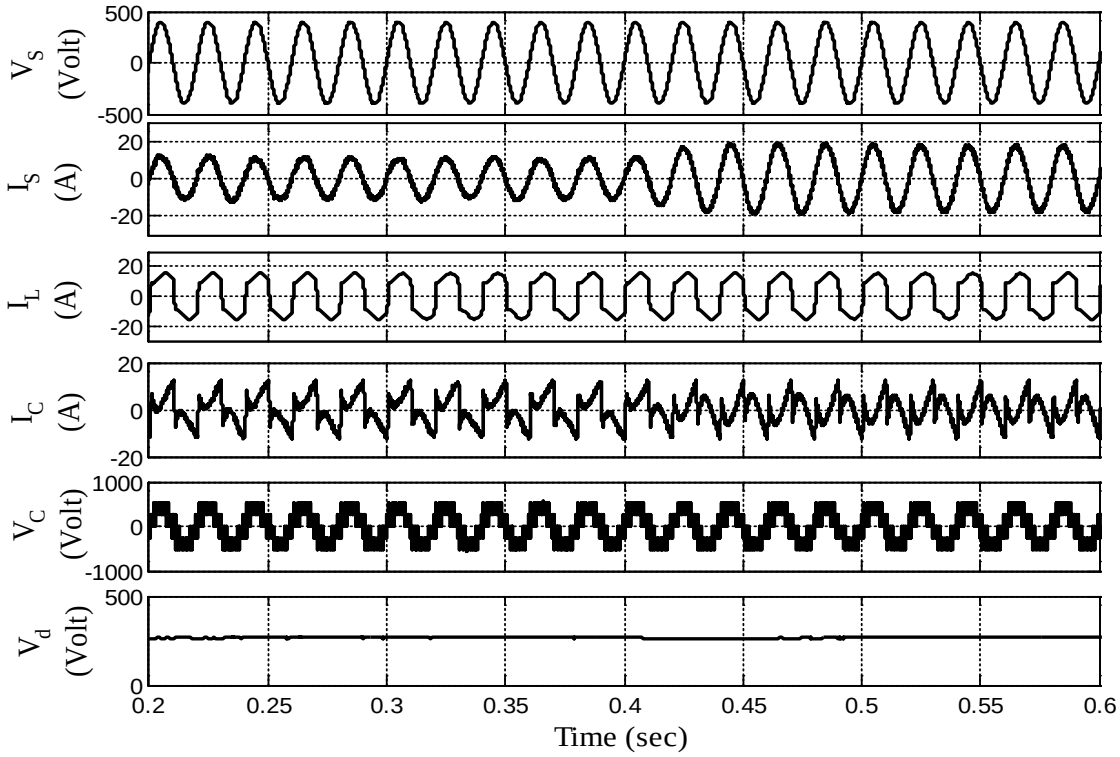


Figure 7.4 Performance of proposed grid-tied PV system with change in irradiance with diode bridge rectifier and R-L loading condition

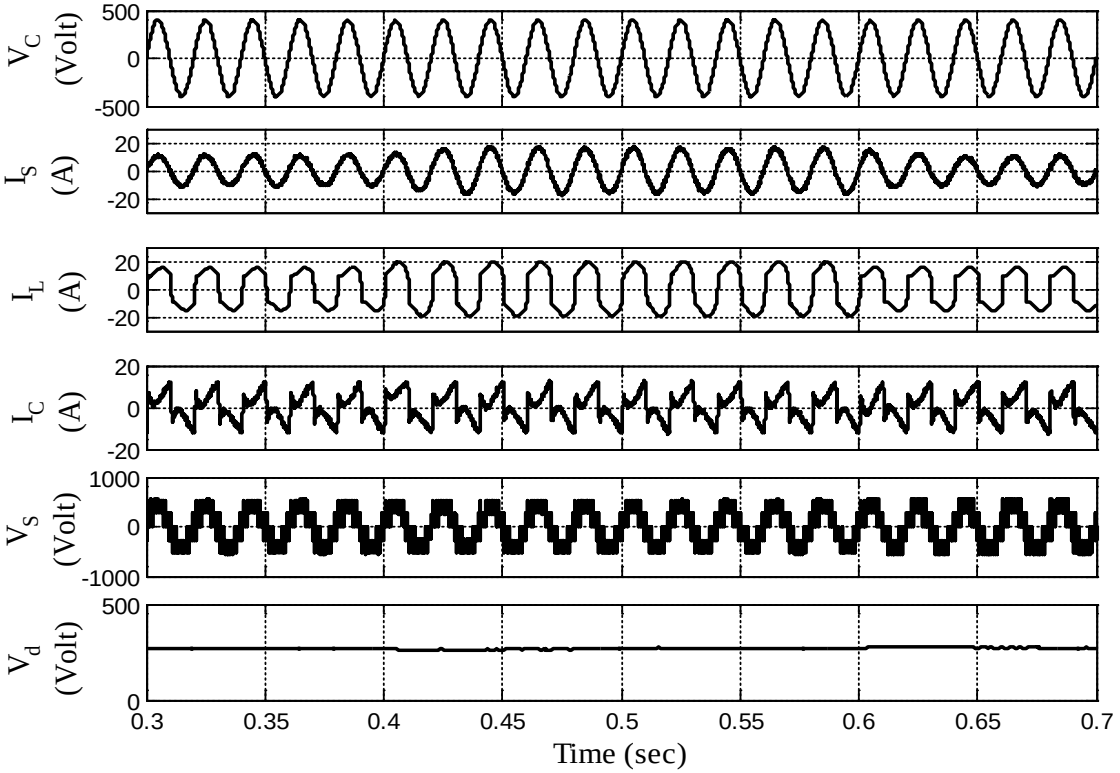


Figure 7.5 Performance of proposed grid-tied PV system with change in loading conditions with diode bridge rectifier and R-L loading condition

Effectiveness of this proposed control technique with PV fed SAPF is also tested with load changing conditions with R-L loading. Figure 7.5 shows load is increased first at an instant of 0.4 sec. It can be seen from the figure that DC-link voltage fluctuation from its reference value is very minimal and becomes stable very quickly to ensure its proper operation. Again, load is decreased at an instant of 0.6 sec. At the same instant, DC-link voltage becomes stable after a minimal fluctuation. Figure shows the effectiveness of the self-charging algorithm in varying load conditions as fluctuations in DC-link are very minimal and settling time is very less. Five-level inverter output is generated during steady-state and transient conditions. Figure shows satisfactory system performance in load changing conditions.

Figure 7.6 shows active and reactive power of grid during different irradiations. Figure shows that active power supplied from SAPF module to grid is zero from instant t=0 sec. to t=0.1 sec. At t=0.1 sec, active power is supplied by this module when irradiation is present. Active power supplied by this module becomes zero when irradiation becomes zero i.e. during night time. Figure also shows that continuous reactive power has been supplied by this PV fed SAPF module irrespective of irradiation. Therefore, it can be concluded from the figure that only reactive power is supplied during night time.

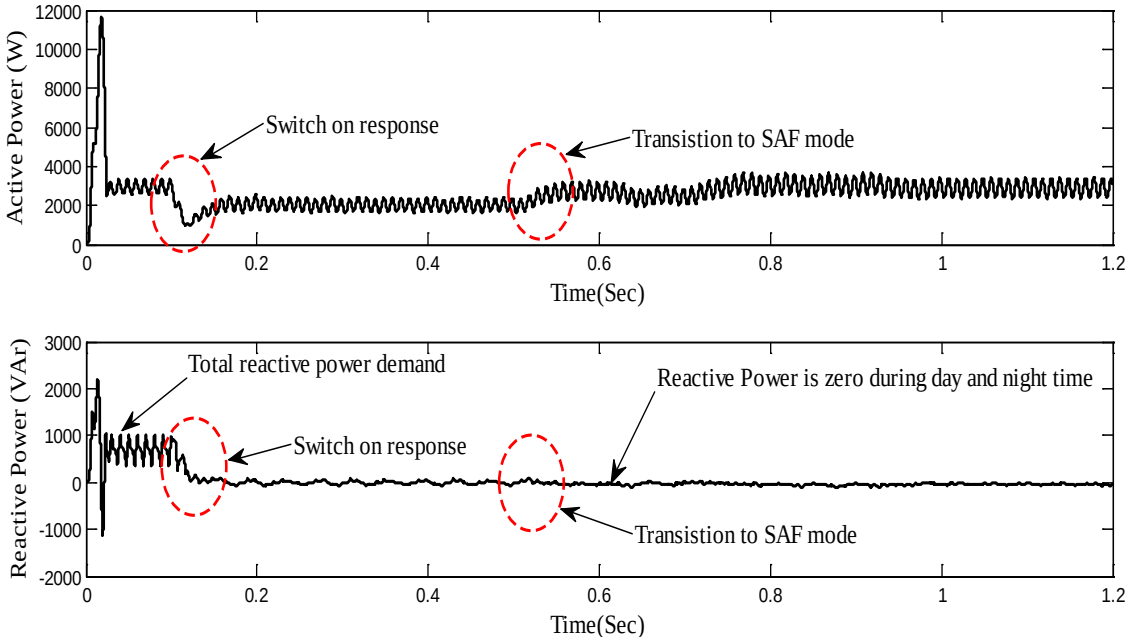


Fig. 7.6 Active and reactive power profile of grid during day and night time

The control algorithm effectiveness is not only tested with current type non-linear loading it is also tested with voltage type of non-linear loading. Figure 7.7 depicts V_S, I_S, I_C, V_C and V_d during day and night time with diode-bridge rectifier based R-C loading condition. Figure 7.7 shows that PV fed SAPF unit is connected to PCC at t=0.1 sec. instant during day time with an irradiance of 500 W/m^2. At t=0.3 sec. instant, irradiation becomes zero. At this instant, source current magnitude increases though load current magnitude is fixed. This result clearly clarifies that current is being supplied during day-time by the solar PV inverter unit while during night time; it is not feeding any kind of active power. It is worth noting that, source current is still sinusoidal during night time even though load current is non-linear in nature. It can be also depicted from the figure that DC-link voltages of two capacitors are stabilized at their reference value during the change in irradiation which confirms the effectiveness of self-charging algorithm based DC-link control. Five-level voltage is also generated at inverter output which confirms the proper operation of five-level CHB inverter.

Effectiveness of this proposed control technique with PV fed SAPF is also tested with load changing conditions where diode-bridge rectifier based R-C loading is used. Figure 7.8 shows that load is increased first at an instant of t=0.4 sec. It can be seen from the figure that DC-link voltage fluctuation from its reference value is very minimal and becomes stable very quickly to ensure its proper operation. Again, load is decreased at an instant of t=0.6 sec. At the same instant, DC-link voltage becomes stable after a minimal fluctuation. Figure shows the effectiveness of the self-charging algorithm in varying load conditions as fluctuations in DC-link are very minimal and settling time is very less. Five-level inverter output is generated during steady-state and transient conditions. Figure shows satisfactory system performance in load changing conditions when SAPF system feeds power from PV to grid. Inverter switching ensures proper operation of SAPF unit with PV as an active power source with 500 W/m^2 of irradiation. Figure 7.7 and 7.8 ensure the proper operation of PV-fed SAPF unit during varying irradiation condition and under load changing conditions when diode-bridge rectifier with R-C loading is used as non-linear load. Figure 7.7 and Figure 7.8 also show source current is sinusoidal in all possible conditions and maintains unity power factor even if non-linear load is present in the system.

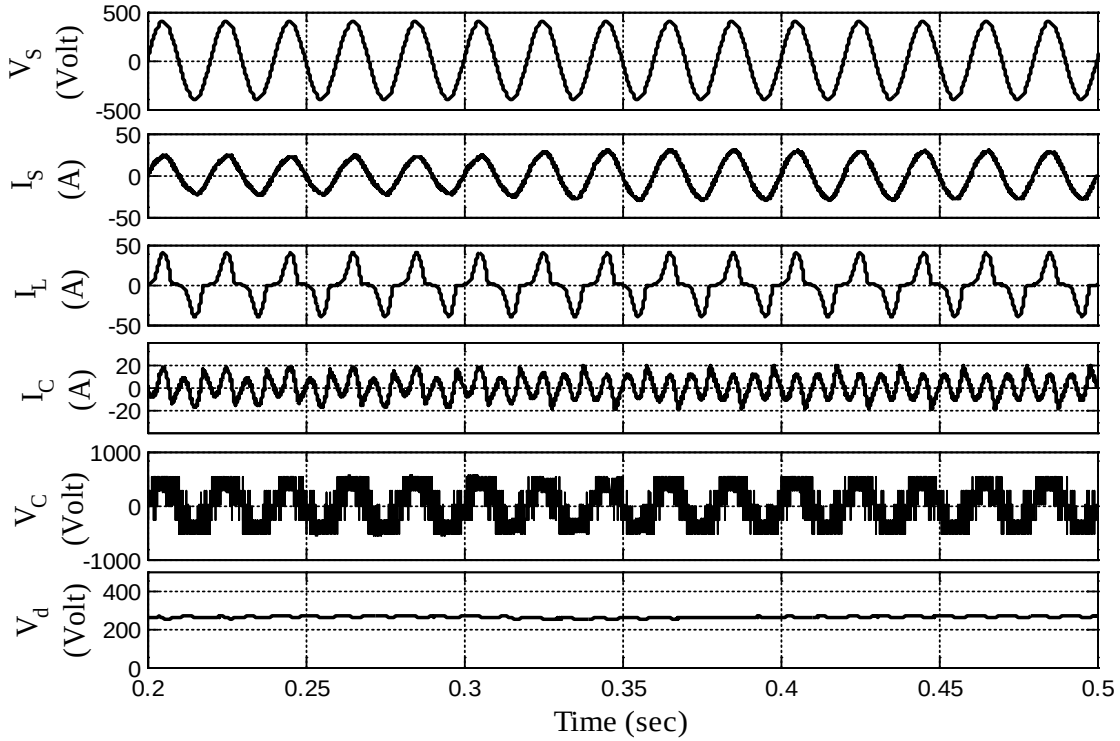


Figure 7.7 Performance of proposed grid-tied PV system with change in irradiance with diode bridge rectifier and R-C loading condition

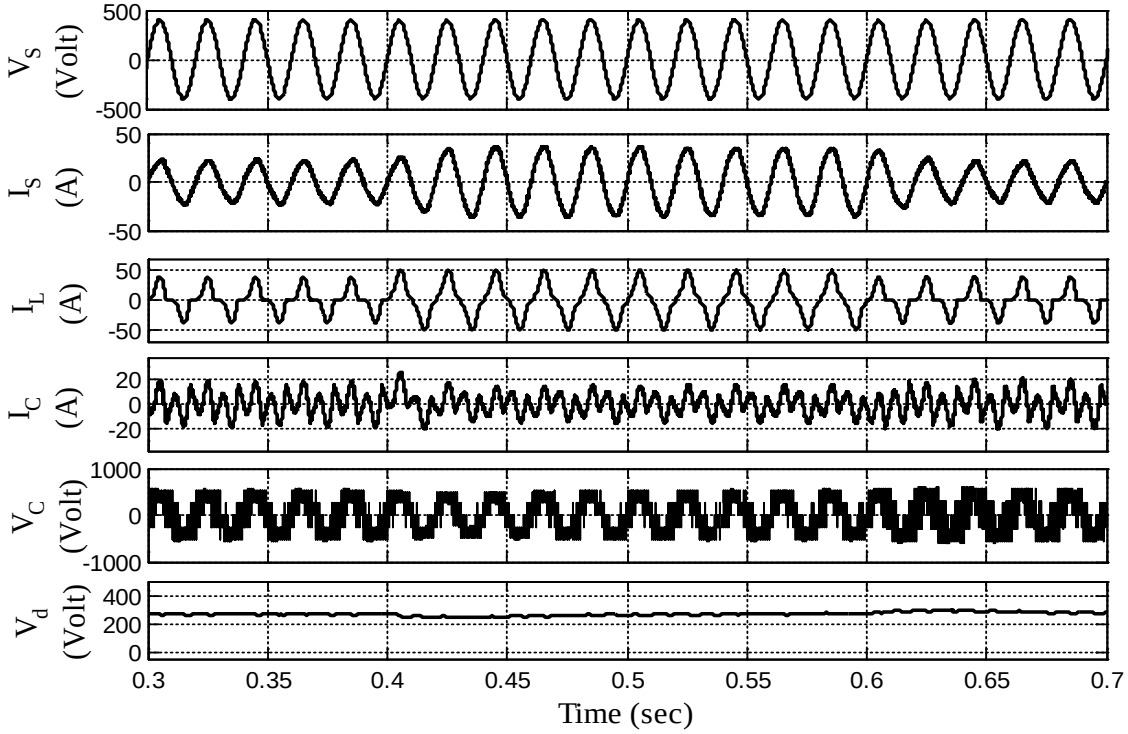


Figure 7.8 Performance of proposed grid-tied PV system with change in loading conditions with diode bridge rectifier and R-C loading condition

The proposed system is also checked with distorted source voltage conditions as grid voltage may be often distorted. PV-fed SAPF unit is switched on at the instant of t=0.1 sec. Figure 7.9 shows performance of proposed control technique with PV fed SAPF unit under diode-bridge based R-L loading arrangement with distorted source voltage condition. An irradiation of 500 W/m^2 is applied for checking system performance. Advanced PLL is able to find fundamental component from distorted source voltage and it extracts phase angle information even if source voltage is polluted with harmonic components. Figure also shows source current becomes sinusoidal after successful operation of this PV fed unit even if source voltage is having THD of 11.42%. Third and fifth harmonic contents are being introduced in to the sinusoidal source voltage. Irradiation becomes zero (during night) at the instant of t=0.4 sec. Figure shows that dc-link voltage maintains its reference value after a small fluctuation from its reference value. It can be seen from figure that source current magnitude increases during night time even if the load current is constant. This result clearly clarifies that during night time, only compensating current is fed to the grid through PCC in order to maintain sinusoidal source current wave shape with unity power factor.

Effectiveness of this proposed control technique with PV fed SAPF is also tested with load increment and decrement under distorted source voltage condition. Figure 7.10 shows that load is first applied at an instant of t=0.4 sec. It can be seen from the figure that DC-link voltage fluctuation from its reference value is very minimal and becomes stable very quickly to ensure its proper operation. Again, load is withdrawn at an instant of t=0.6 sec. At the same instant, DC-link voltage becomes stable after a minimal fluctuation. Figure shows the effectiveness of the self-charging algorithm in varying load conditions as fluctuations in DC-link are very minimal and settling time is very less. Five-level inverter output is generated during steady-state and transient conditions. Figure shows satisfactory system performance in load changing conditions during PV-fed CHB-MLI based SAPF.

From both the figure, it can be depicted that source current maintains its sinusoidal wave-shape during change in irradiance and change in loading. Its proper operation also confirms that source current is in phase with source voltage which confirms unity power factor operation in all possible conditions.

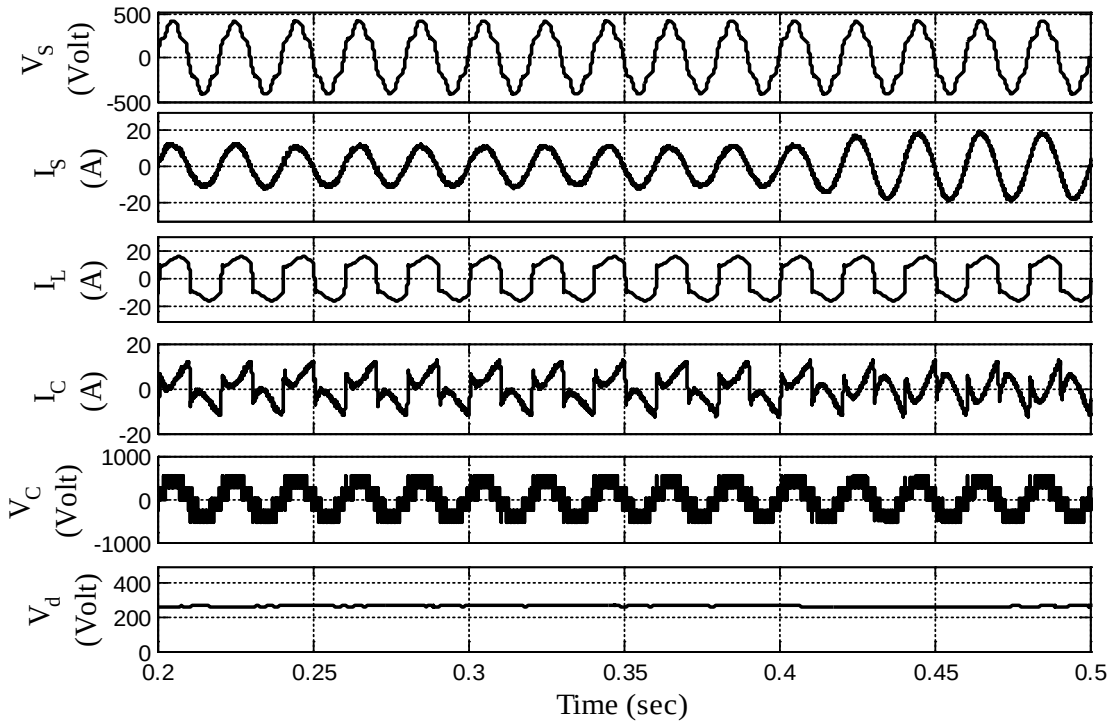


Figure 7.9 Performance of proposed grid-tied PV system with change in irradiance with diode bridge rectifier based R-L loading arrangement under distorted source voltage condition

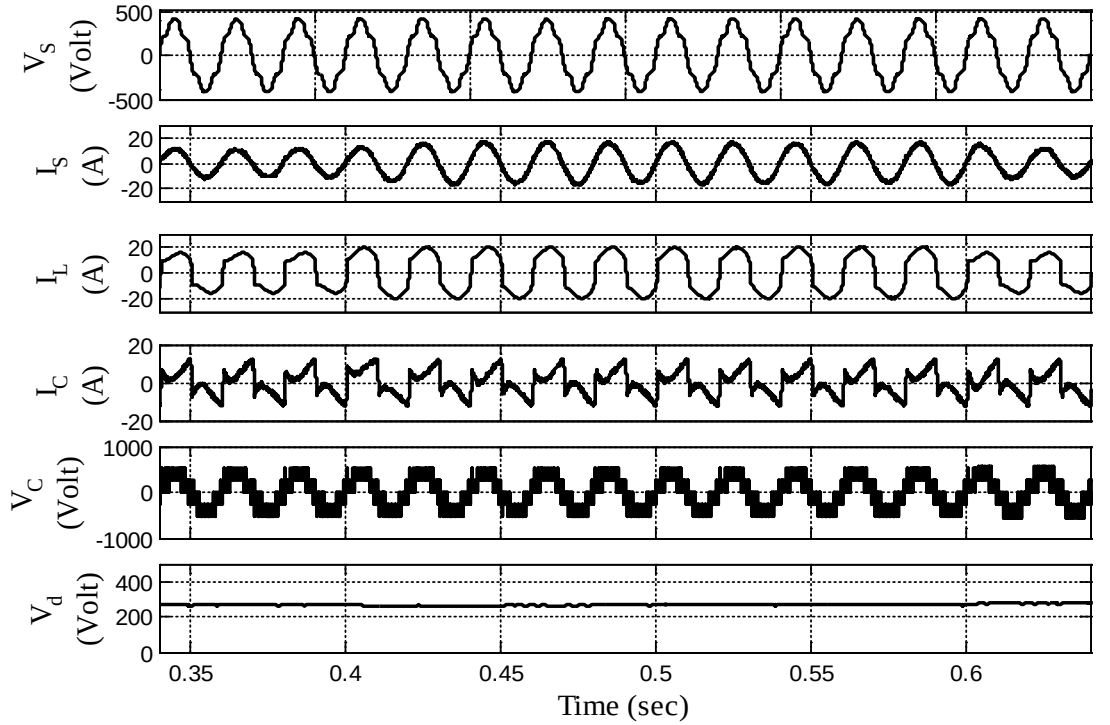


Figure 7.10 Performance of proposed grid-tied PV system with change in loading with diode bridge rectifier based R-L loading arrangement under distorted source voltage condition

The control algorithm effectiveness is also tested with voltage type of non-linear loading under distorted source voltage conditions. Figure 7.11 depicts V_S, I_S, I_C, V_C and V_d during day and night time with diode-bridge rectifier based R-C loading condition with source voltage THD of 11.42%. Third and fifth harmonic components are introduced in the source voltage in order to get distorted supply voltage. Figure 7.11 shows that PV fed SAPF unit is connected to PCC at t=0.1 sec. instant during day time with an irradiance of 500 W/m^2. At t=0.3 sec. instant, irradiation becomes zero. At this instant, source current magnitude increases though load current magnitude is fixed. This result clearly clarifies that current is being supplied during day-time by the solar PV inverter unit while during night time; it is not feeding any kind of active power. It is worth noting that, source current is still sinusoidal during night time even though load current is non-linear in nature. It can be also depicted from the figure that DC-link voltages of two capacitors are stabilized at their reference value during the change in irradiation which confirms the effectiveness of self-charging algorithm based DC-link control. Five-level voltage is also generated at inverter output which confirms the proper operation of five-level CHB inverter.

Effectiveness of this proposed control technique with PV fed SAPF is also tested with load increment and decrement under distorted source voltage condition. Figure 7.12 shows that load is first applied at an instant of t=0.4 sec. It can be seen from the figure that DC-link voltage fluctuation from its reference value is very minimal and becomes stable very quickly to ensure its proper operation. Again, load is withdrawn at an instant of t=0.6 sec. At the same instant, DC-link voltage becomes stable after a minimal fluctuation. Figure shows the effectiveness of the self-charging algorithm in varying load conditions as fluctuations in DC-link are very minimal and settling time is very less. Five-level inverter output is generated during steady-state and transient conditions. Advanced PLL also able to filter out the harmonic component present in the source voltage as well as it is able to track line frequency perfectly even if in source voltage condition. Figure shows satisfactory system performance in load changing conditions as source current maintains its sinusoidal wave shape during change in irradiance and change in loading. Its proper operation also confirms that source current is in phase with source voltage which confirms unity power factor operation in all possible conditions.

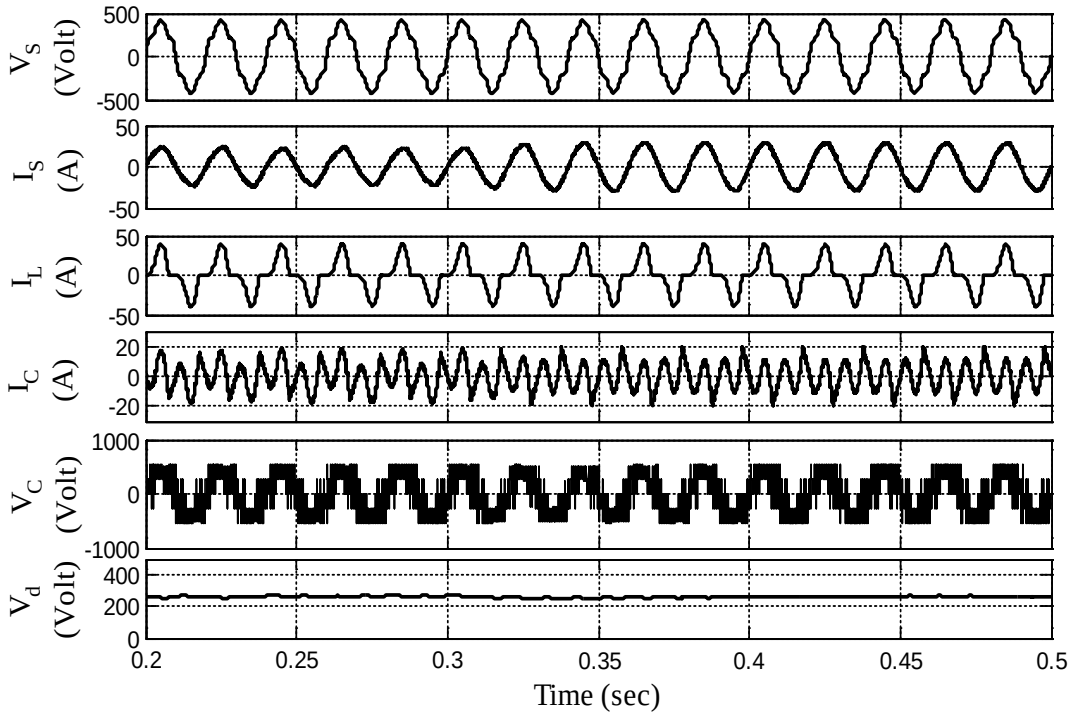


Figure 7.11 Performance of proposed grid-tied PV system with change in irradiance with diode bridge rectifier based R-C loading arrangement under distorted source voltage condition

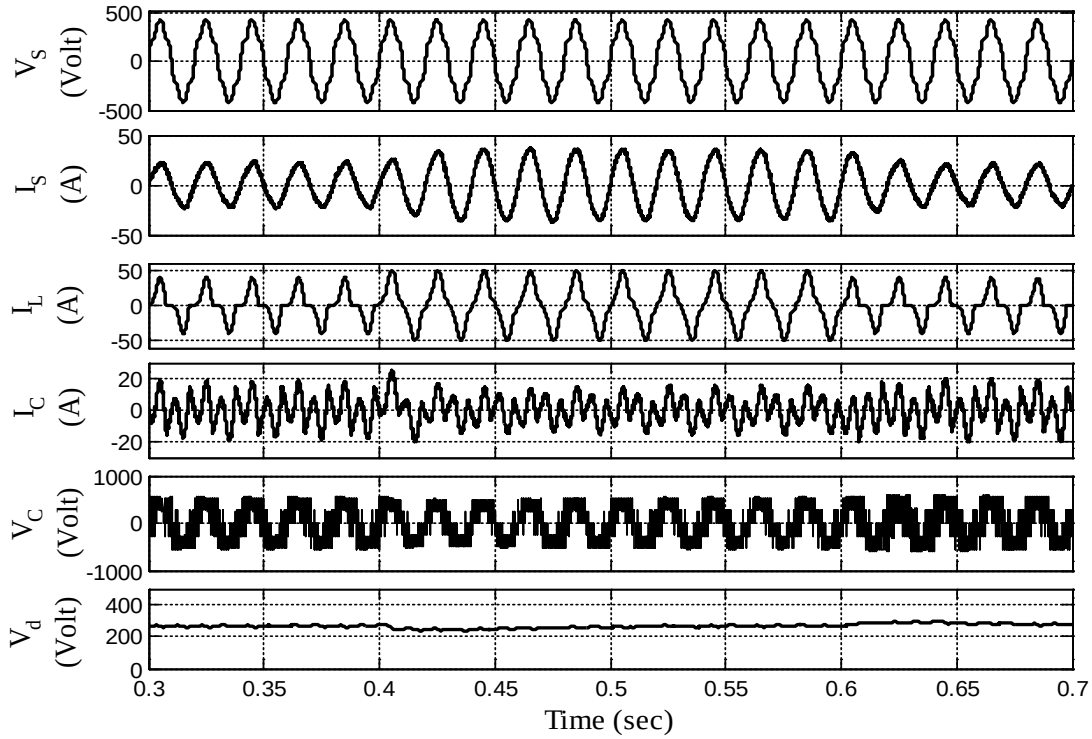


Figure 7.12 Performance of proposed grid-tied PV system with change in loading with diode bridge rectifier based R-C loading arrangement under distorted source voltage condition

Table 7.1 shows detailed comparative analysis of PV fed SAPF in different operating condition. It can be depicted from Table and figure that, this PV fed MLI based SAPF module is well capable to supply active power during day-time with power factor improvement and current harmonic minimization. This module is acting as SAPF only during night. Advanced PLL helps this unit operate smoothly under distorted source voltage conditions with R-L and R-C type of non-linear loading. Performance is also compared with conventional control technique applied to same system.

Table 7.1 Analysis of PV fed SAPF in different operating conditions

With R-L loading	Proposed Control	
	Day-time	Night-time
THD before compensation	32.37%	32.37%
THD after compensation	4.77%	4.23%
Power Factor before compensation	0.9	0.9
Power Factor after compensation	0.985	0.99
Active Power supplied	500 W	0 W
With R-C loading	Day-time	Night
THD before compensation	32.37%	32.37%
THD after compensation	4.77%	4.23%
Power Factor before compensation	0.87	0.87
Power Factor after compensation	0.985	0.99
Active Power supplied	500 W	0 W
With R-L loading	Day-time	Night-time
THD of source voltage	11.42%	11.42%
THD before compensation	32.37%	32.37%
THD after compensation	4.77%	4.23%
Power Factor before compensation	0.9	0.9
Power Factor after compensation	0.985	0.99
Active Power supplied	500 W	0 W
With R-C loading	Day-time	Night
THD of source voltage	11.42%	11.42%
THD before compensation	52%	52%
THD after compensation	4.89%	4.55%
PF before compensation	0.87	0.87
PF after compensation	0.993	0.992
Active Power supplied	500 W	0 W

7.6 CONCLUSION

This chapter presents a compact grid-tied PV fed SAPF module for medium voltage distribution system which can be realized for medium voltage and high power

level. PV fed CHB based structure provides modularity into the system and transformer-less interconnection with grid. Therefore, this structure provides higher efficiency. P and O MPPT ensures effective operation of boost converter in different weather conditions. Improved grid-side control technique comprises of self-charging algorithm which gives faster dynamic response and less peak overshoot during transient conditions. Modified control algorithm takes care of proper active and reactive power management during different irradiation whereas same system can act as SAPF unit during night time with this control technique. This control also takes care of smooth transition between SAPF mode and PV fed SAPF mode during day-time which increases operating range of control. Advanced PLL takes care of harmonic content rejection and it ensures proper operation of control algorithm under distorted supply conditions also which is a very important feature in DG systems comprising PV arrays. This complete set-up will provide a better solution in grid tied PV system which can be utilized as SAPF in night time also which makes the system more feasible in medium voltage distribution grid. This system can be practically a viable solution for large-scale grid-tied photovoltaic with better utilization factor.

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

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CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

Today, power electronics converter based systems are used in industrial sector as well as in commercial sectors. These power electronic converter based systems are highly energy and cost effective, compact in nature and are capable to provide improved performance. Proliferation of static power converters, adjustable-speed drives, utility interface with non-conventional energy sources etc. have become more and more popular due to technological advancements. However, usage of these converter based system introduce non-linear behavior into the existing distribution system due to converter switching action. Consequently, this phenomenon leads to various power quality problems like introduction of voltage harmonics and power factor degradation by injecting current harmonics. Converters and inverters are widely used in DC and AC industrial fixed or variable speed drives, switched mode power supply, HVDC transmission and grid interface with non-conventional energy resources. Engineers and researchers are facing a bigger challenge of alleviating harmonic distortions and reactive power flow at various buses. In fact, it is becoming extremely difficult for utilities to maintain power quality standards imposed by several national and international standards. Overheating of transformers, induction motors and malfunctioning of other electrical and relay equipments are other major disadvantages associated with it.

Passive filters are traditionally used for mitigating current related power quality problems. However, these passive compensation techniques are having disadvantages as enumerated in chapter 1. Among all other options available, SAPF promises as most suitable solution to counter these power quality related issues. Application of SAPF in medium-voltage and high-power distribution system is gaining its importance as large number of high power industrial drive system is used by industries. Normally, two-level inverters are used as a main component of SAPF unit but, in case of medium-voltage distribution system it is having limitations as high voltage and current stress of power

semiconductor devices, use of line-frequency transformer, space, size, electromagnetic interference etc. Therefore, MLIs are one of the best available solutions for industries in case of high power applications due to its distinct advantages over conventional inverters such as lower switching stress, lower dv/dt and di/dt ratings, high efficiency and low electromagnetic interference etc. Bulky and spacious line-frequency transformers are no longer necessary before connecting this unit to grid through point of common coupling. Total harmonic distortion in output voltage is also decreasing in nature with increment of number of levels at inverter output. If number of levels are high enough, voltage become almost sinusoidal in nature. However, the control theory complexity increases with higher number of levels. Among available conventional MLI topologies, cascaded H-bridge MLI is modular in structure and it requires least number of power electronic switches as compared to other two types. Therefore, this topology attracts researchers around globe in different applications like high power electric drives, static compensators, SAPF etc. As no active power source is required for SAPF applications, only separate DC-link capacitors are required with different H-bridge modules.

CHB-MLI based SAPF is proved as an effective and better choice to control non-linear current and for improving power quality by compensating current harmonics at the consumer end. Consequently, control theories applied to SAPF play major role for shaping source current in sinusoidal shape. Therefore, an investigation on different topologies and control techniques related to MLI based shunt active power filter is done primarily for choosing the best solution.

Current control plays a significant role for defining current shape and magnitude in case of shunt type active filtering applications. Normally, P or PI controllers are used as a significant part of current control loop for defining current shape but use of these controllers in current control loop cannot completely nullifies steady-state error. Therefore, conventional compensators are replaced by proportional-resonant (PR) compensator in order to acquire better steady-state and transient performance in sinusoidal current controllability. PR compensator based advanced current controller is used in current control loop to introduce infinite gain at selected frequency. Consequently, the behaviour of this PR compensator is similar to an integrator and its infinite gain ensures zero steady state error in terms of magnitude and frequency.

Modified control algorithm composed of PR compensator is applied to five-level CHB-MLI based SAPF in order to acquire better steady-state source current response. However, recognition of dc integrator having infinite gain is not possible due to limitation of analog system. Therefore, quasi-resonant compensator is applied in current control loop for practical application of SAPF. Stability of proposed closed-loop control composed of PR/ quasi PR compensator is rigorously checked with root-locus analysis and R-H criteria. Moreover, compensator constants are tuned with the help of bode-plot based technique. Detailed simulation is carried out, results are presented and performance is compared with conventional PI compensator results. A laboratory prototype model of CHB-MLI based SAPF has been developed for experimental analysis using dSPACE. Detailed hardware results also confirm the effectiveness of the proposed controller over conventional one.

However, use of PR compensator in current control loop causes reduction in stability margin of the system and it is also responsible to create undesired peaks during real-time applications. Therefore, PI-vector proportional-resonant (VPI) compensator based current controller is designed in order to maintain superior SAPF performance during its operation. This compensator is able to do selective harmonic elimination from current control loop. This projected compensator eliminates 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonic component. Therefore, sinusoidal source current of zero-steady state error is obtained in case of SAPF operations. Simulation is carried out in MATLAB/ Simulink platform for PI-VPI compensator based SAPF control. Bode-diagram shows that the closed-loop current control loop is able to mitigate selective harmonic components from current control loop and root-locus analysis shows closed-loop control system stability. Detailed experimental analysis show sinusoidal source current according to IEEE-519-1992 standard after successful operation of SAPF unit with different non-linear loading conditions.

Shunt APF with proper control algorithm mitigates current related power quality problems with non-linear loading not only in sinusoidal but also in distorted supply voltage condition. Supply may be often distorted with the presence of industrial sector loading. DC component may be also present in the existing system due to offset of DC/AC voltage sensors, characteristics mismatch among power electronic switches, dc

offset in analog to digital converters etc. It degrades the performance of phase locked loop (PLL) as well as performance of control algorithm. In view of this, advanced PLL based modified synchronous reference frame (SRF) control algorithm is used for active filtering applications. Advanced PLL is capable of exact measurement of phase angle, fundamental component extraction even from polluted signal including DC component. Load currents are being sensed and converted to synchronous reference frame. Park's and Inverse Park's transformation needs phase angle information for transferring 'abc' quantities to 'dq' quantities. Improved PLL extracts exact phase angle information in ideal and in distorted supply conditions. The projected PLL is an extension of enhanced PLL (E-PLL) where an additional loop is present for detecting dc component. Eigen value analysis is used as an effective tool to design of constant parameters for this PLL. In addition, a detailed mathematical modeling of advanced PLL is presented and its rigorous stability analysis has been tested using R-H criteria and bode diagram. Performance of advanced PLL is rigorously tested and compared with other recently proposed PLLs which are having dc rejection capability. Loss component of MLI based SAPF is obtained by comparing DC-link voltage to its reference value and PI controller is used to regulate DC-link voltage. Current control loop decides the shape of source current. Finally, PS-PWM technique is used for generation of gate pulses. The proposed model is developed and simulated in MATLAB/Simulink environment for steady-state and transient conditions under ideal mains and distorted source voltage conditions with current/ voltage type of non-linear loading. Simulated response of source voltage, source current, compensating current, load current and DC-link voltage have been presented for validation of the proposed work. Finally, five-level CHB-MLI based SAPF with advanced PLL based control algorithm is tested with different non-linear loading conditions in MATLAB/ Simulink platform. Transient as well as steady-state behavior of the proposed system shows its effectiveness under highly distorted grid condition. Exhaustive simulation and hardware results show the efficacy of the proposed control technique in active filtering application.

Cost and system effectiveness are major concerns among researchers while connecting large-scale PV to existing grid. Simultaneously, current related power quality issues are also present in distribution sector. In this context, CHB-MLI based filtering

approach can provide transformer-less interconnection of converters, gives cost-worthy solution and provides better power quality. Therefore, single-phase CHB-MLI based large-scale grid-tied PV system is proposed for active and reactive power management during day time and this unit can minimize reactive power at night time. This proposed system is implemented in MATLAB/ Simulink environment and are rigorously tested with different irradiations and under different non-linear loading conditions.

To summarize, in this thesis, consolidated efforts have been made to investigate the performance of five-level CHB-MLI based SAPF for current harmonics mitigation, reactive power minimization in case of medium-voltage and high-power three-phase three-wire distribution system. An advanced current controller composed of PR and quasi-PR compensator is designed in order to get zero steady-state error in source current. However, use of PR compensator in current control loop is having limitations during real-time applications. Therefore, PI-VPI compensator based current controller is designed in order to maintain zero steady-state error during SAPF performance. An advanced PLL having dc component and harmonic rejection facility is used for proper phase angle measurement in case of active filtering control mechanism. A prototype model of five-level CHB-MLI has been designed and developed in the laboratory. Real-time controller dSPACE 1104 is used for executing projected SAPF control algorithms. Detailed experimental results and comprehensive analysis show effectiveness of the proposed system with different non-linear loading arrangements. Finally, CHB-MLI based SAPF is used for active power injection as well as reactive power minimization for large-scale grid-tied PV applications. Detailed simulation results show effectiveness of the proposed scheme under varying irradiation conditions. Effectiveness of the proposed control algorithm is tested with MATLAB/Simulink environment. Detailed steady-state and transient performance analysis through simulative and experimental study prove the effectiveness of the proposed system.

8.2 FUTURE SCOPE

Research is a continuous process. An end of a research project is a beginning to a lot of other avenues for future work. A door to new research issues is opened upon the

end of a research work. Some of the important aspects as identified for future research works in this area are as:

(1) Determination of size and location of MLI based SAPF in the distribution network is a potential area for research.

(2) The present work can be extended with higher-level of multilevel inverter topologies. Harmonic distortion and efficiency calculation can be compared for different levels of CHB-MLIs so that optimum usage of CHB-MLI can be chosen for high-power applications.

(3) Practical implementation of multilevel inverters for medium-voltage and high-power applications is still an issue as large number of power electronic devices are needed for generating more number of levels and hence control becomes complex with higher number of voltage levels. Intensive research need to be done on developing new/ modified multilevel inverter topologies with reduced switches count. Moreover, suitable control theory needs to be developed for proper switching of these reduced switch count multilevel inverters.

(4) FPGA platform can be used for the implementation of control algorithm and performance comparison of FPGA and DSP may be a research area in terms of speed, memory requirement, etc.

(5) Artificial intelligence technique can be applied for optimal tuning of PI controller constants for minimizing settling time and peak overshoot/ undershoot of DC-link voltage during load changing conditions.

(6) The addition of CHB-MLI based SAPF functions can be applied for three-phase three-wire grid-tied PV system. Voltage and power balance issues among H-Bridge modules are also a potential area of research.

(7) D-Q reference frame theory can be used to generate the reference compensating current for APF while neuro-fuzzy can be used for capacitor DC-link regulation.

(8) Seven-level CHB-MLI based SAPF can be adopted for improving PQ in distribution network.

(9) LS-PWM and APOD-PWM can be adopted in investigate the performance of CHB-MLI based DSTATCOM.

(10) Performance of seven-level CHB-MLI based DSTATCOM can be also investigated for improving PQ in distribution network.

LIST OF PUBLICATIONS FROM RESEARCH WORK

List of Journals Accepted/ Published

1. **S. Ray**, N. Gupta, R. A. Gupta, "Mathematical and Experimental Investigation on Advanced PLL for Cascaded H-Bridge Multilevel Inverter in Active Filtering Application," *Electric Power Components and Systems*, Taylor and Francis. **(In Press)**
2. **S. Ray**, N. Gupta, R. A. Gupta, "Hardware Realization of Proportional-Resonant Regulator Based Advanced Current Control Strategy for Cascaded H-Bridge Inverter Based Shunt Active Power Filter," *International Transactions on Electrical Energy Systems*, Wiley, Sep. 2018.
   DOI: https://doi.org/10.1002/etep.2714
3. **S. Ray**, N. Gupta, R. A. Gupta, "A Comprehensive Review on Cascaded H-bridge Inverter-Based Large-Scale Grid-Connected Photovoltaic," *IETE Technical Review*, Taylor and Francis, vol. 34, no. 5, pp. 463-477, Sep. 2017.
   DOI: https://doi.org/10.1080/02564602.2016.1202792
4. **S. Ray**, N. Gupta, R. A. Gupta, "A Novel Non-linear Control for Three-Phase Five-Level Cascaded H-Bridge Inverter Based Shunt Active Power Filter," *International Journal of Emerging Electric Power Systems*, De Grutyer Press, vol. 19, no. 5, pp. 1-11, Oct. 2018.
   DOI: https://doi.org/10.1515/ijeeps-2018-0052
5. **S. Ray**, N. Gupta, R. A. Gupta, "Prototype Development and Experimental Investigation on Cascaded Five-level Inverter based Shunt Active Power Filter for Large-Scale Grid-tied Photovoltaic," *International Journal of Renewable Energy Research*, Gazi University Press, vol. 8, no. 3, pp. 1800-1811, Sep. 2018.
6. **S. Ray**, N. Gupta, R. A. Gupta, "Cascaded vector resonant controller based novel active filtering using multilevel inverter based shunt active power filter," *Journal of Electric Systems*. **(In Press)**
7. **S. Ray**, N. Gupta, R. A. Gupta, "Power Quality Improvement using Multilevel Inverter Based Active Filter for Medium-Voltage High-Power Distribution

System: A Comprehensive Review," *International Journal of Power Electronics*, Inderscience. **(In Press)**

List of International Conferences

1. **S. Ray**, N. Gupta, R. A. Gupta, "Comparative Analysis of Conventional and Modified Peak-detection Based Control Technique for Cascaded H-Bridge Multilevel Inverter based Shunt Active Power Filter," in Proc. *of IEEE International Conference on Innovations in Power and Advanced Computing Technologies (i-PACT2017)*, Apr. 2017, Vellore, pp. 1-6.
2. **S. Ray**, N. Gupta, R. A. Gupta, "Active and Reactive Power Management of Photovoltaic Fed CHB Inverter Based Active Filter with Improved Control under Normal/Distorted Supply," in Proc. *of 12th IEEE International Conference on Industrial Electronics and Applications (ICIEA)*, June 2017, Siem Reap, Cambodia, pp. 572-577.
3. **S. Ray**, N. Gupta, R. A. Gupta, "Advanced PWM for Balancing DC-link Voltages in Seven-Level CHB Inverter based Active Filter," in Proc. *of 2nd IEEE International Conference on Recent Development in Control, Automation and Power Engineering, (RDCAPE)*, Oct. 2017, Delhi, pp. 1-6.
4. **S. Ray**, N. Gupta, R. A. Gupta, "Improved Single Phase SRF Algorithm for CHB Inverter Based Shunt Active Power Filter under Non-ideal Supply Conditions," in *Proc. of 9th IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov. 2017, Bangalore, pp. 1-6.
5. **S. Ray**, N. Gupta, R. A. Gupta, "Modified Three-Layered Artificial Neural Network based Improved Control of Multilevel Inverters for Active Filtering," in Proc. *of 7th International Conference on Soft Computing and Problem Solving (SocPros 2017)*, Dec. 2017, Bhubaneswar.

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APPENDIX-A

Hardware Circuit and Set-Up Photograph

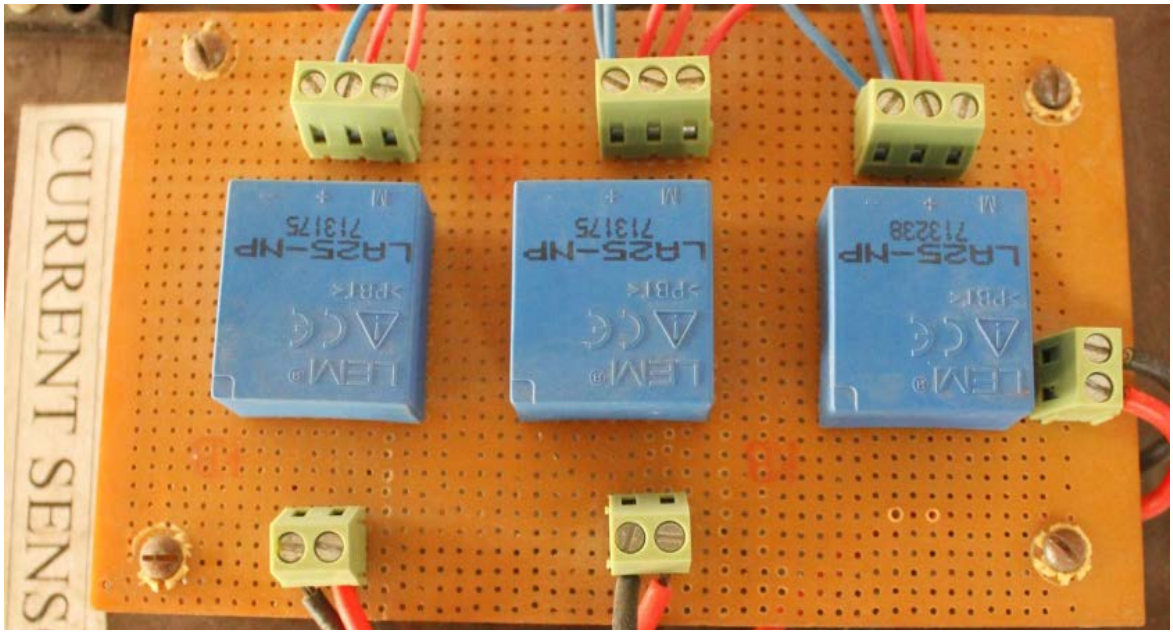

Figure A.1 Current sensors

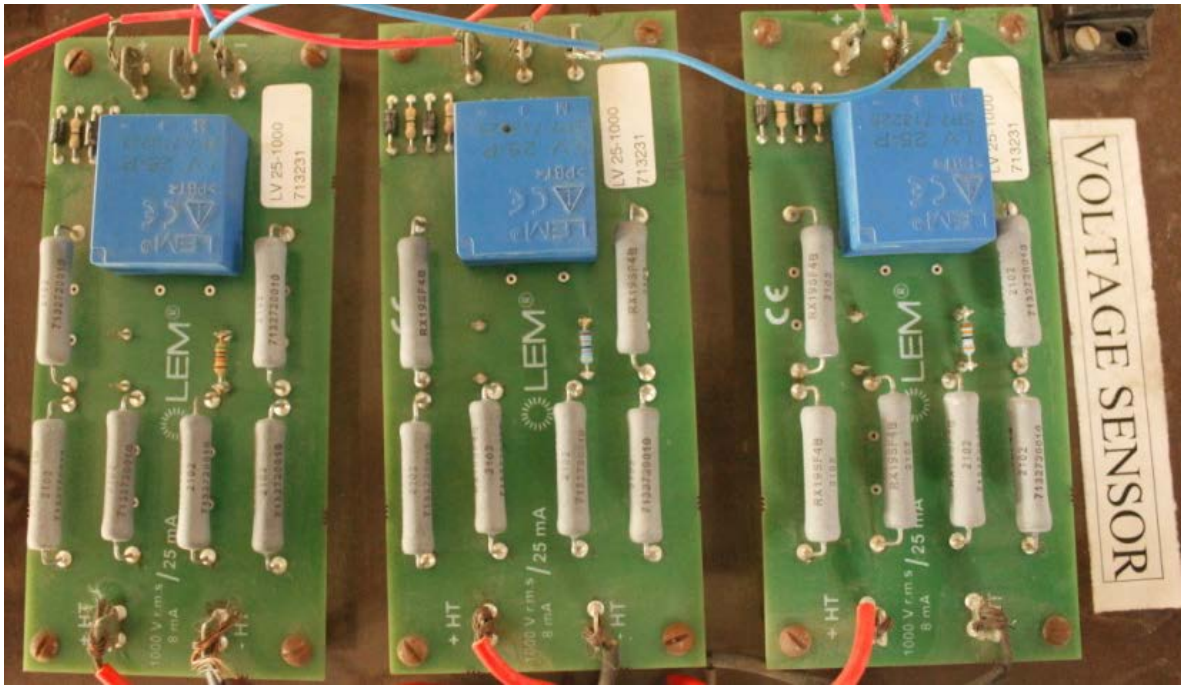

Figure A.2 Voltage sensors

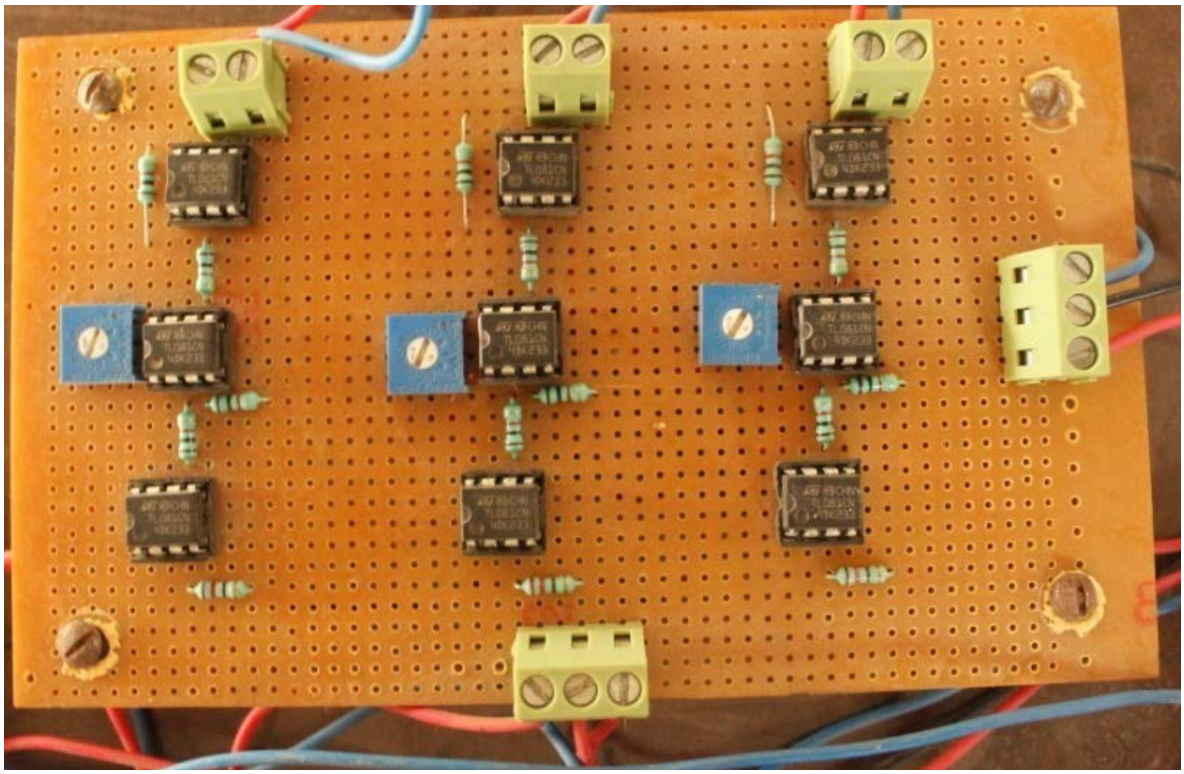

Figure A.3 Amplification and isolation circuit required for sensors

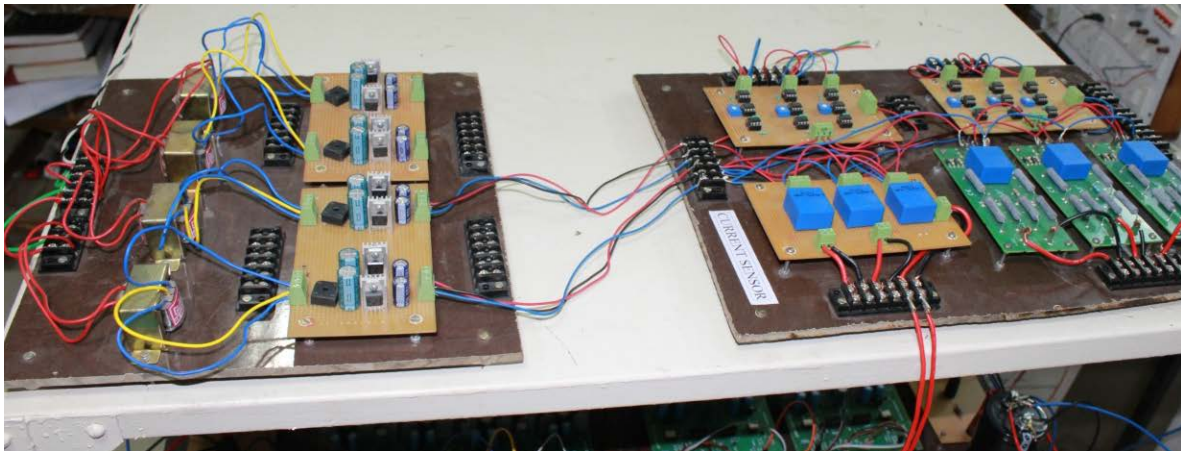

Figure A.4 Voltage and current sensor circuit with amplification and isolation

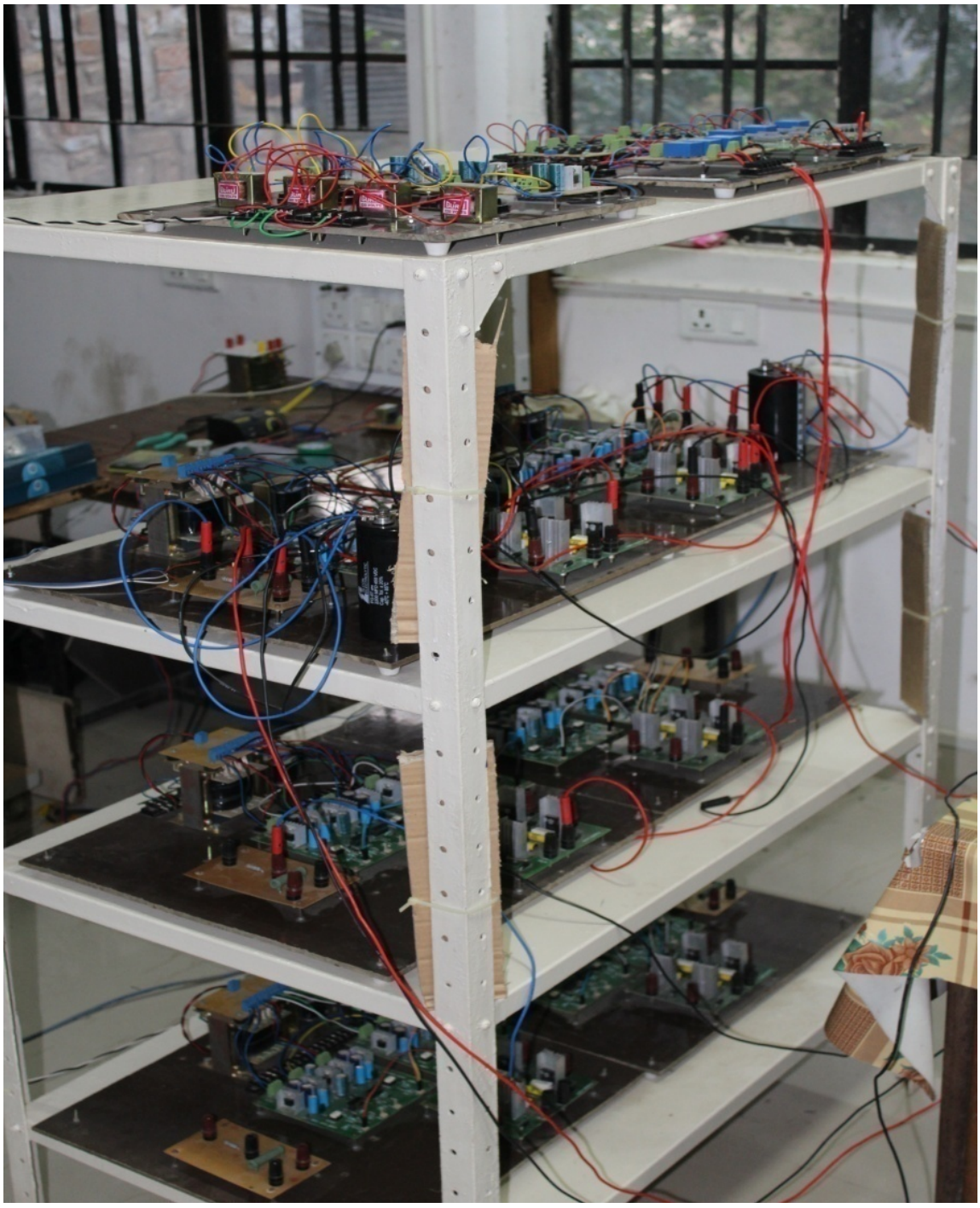

Figure A.5 Five-level CHB-MLI set-up

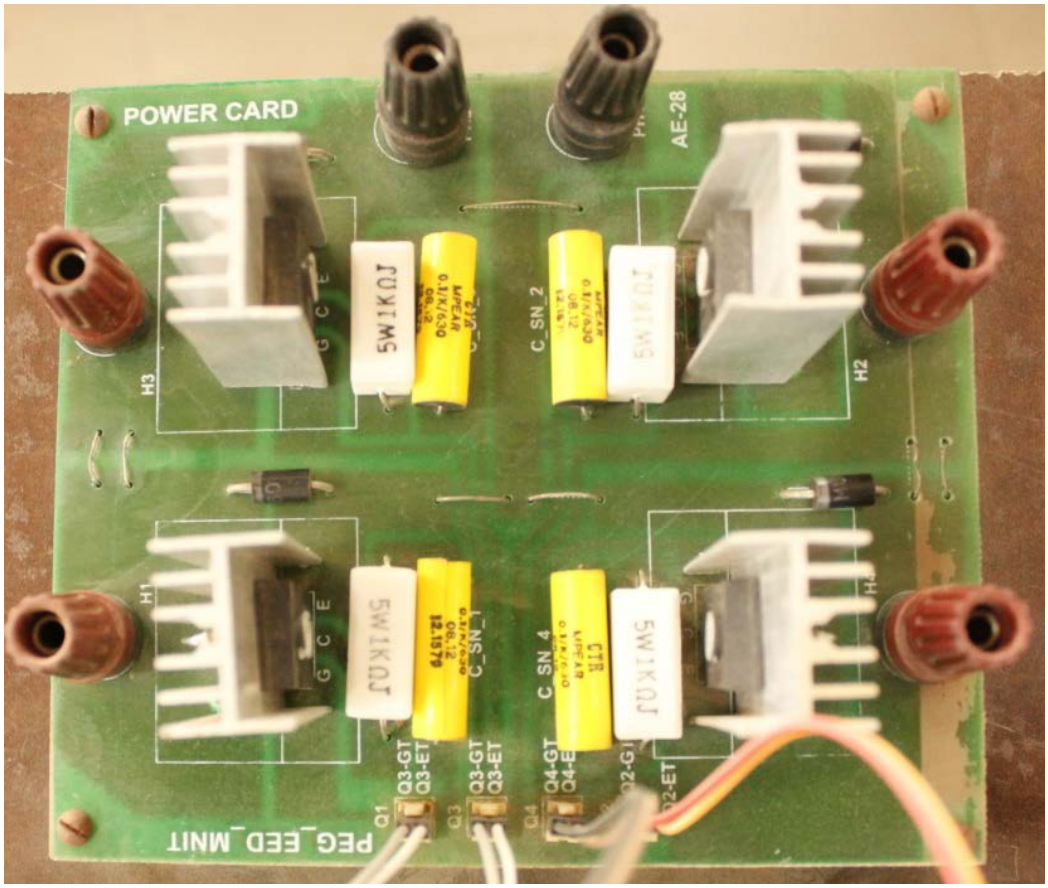

Figure A.6 H-bridge inverter

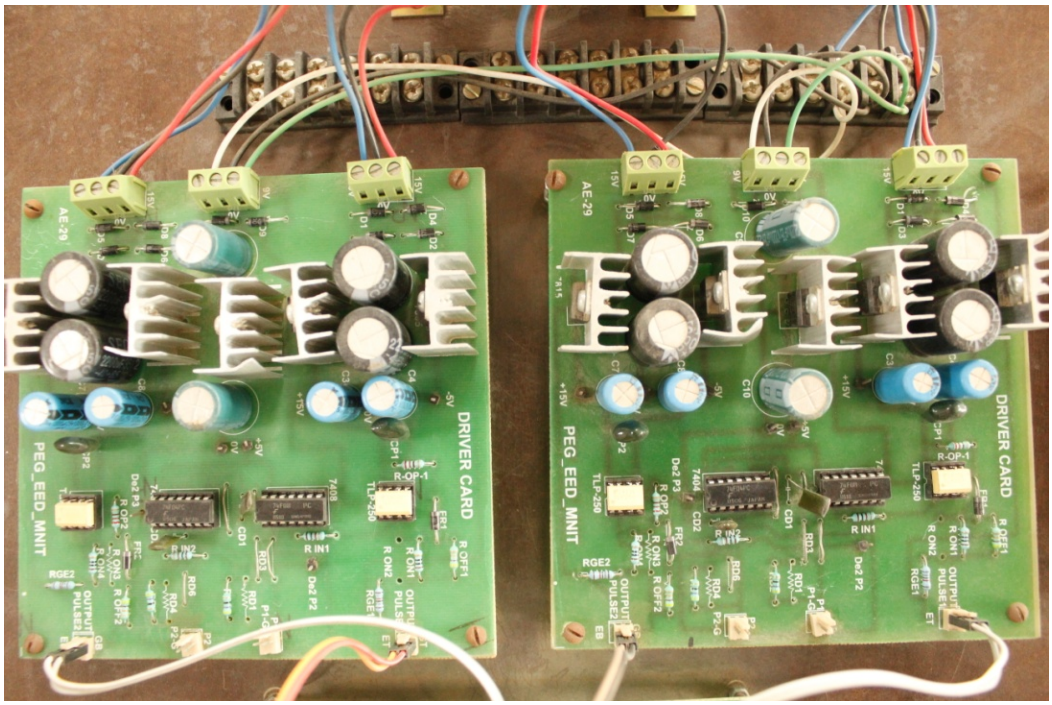

Figure A.7 Driver circuit for H-bridge inverter

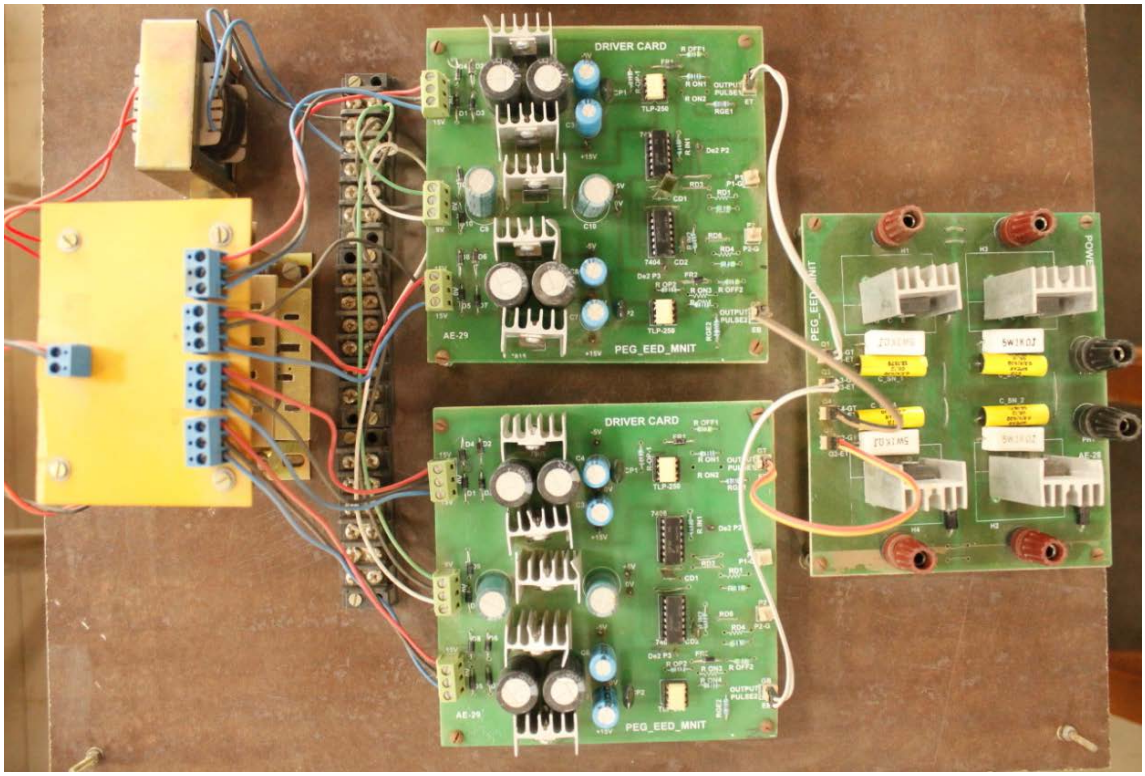

Figure A.8 H-Bridge Inverter with power and control circuit

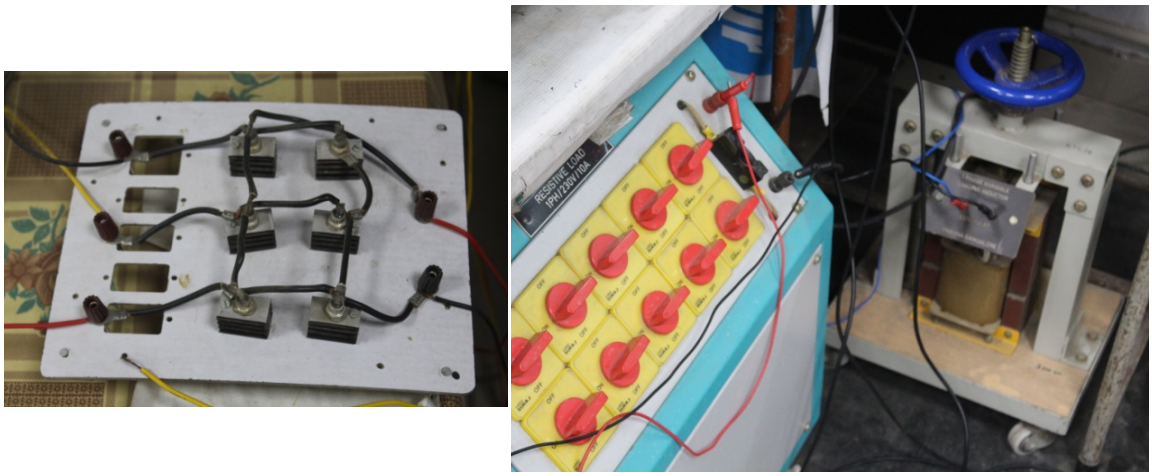

Figure A.9 Diode-bridge rectifier based R-L loading

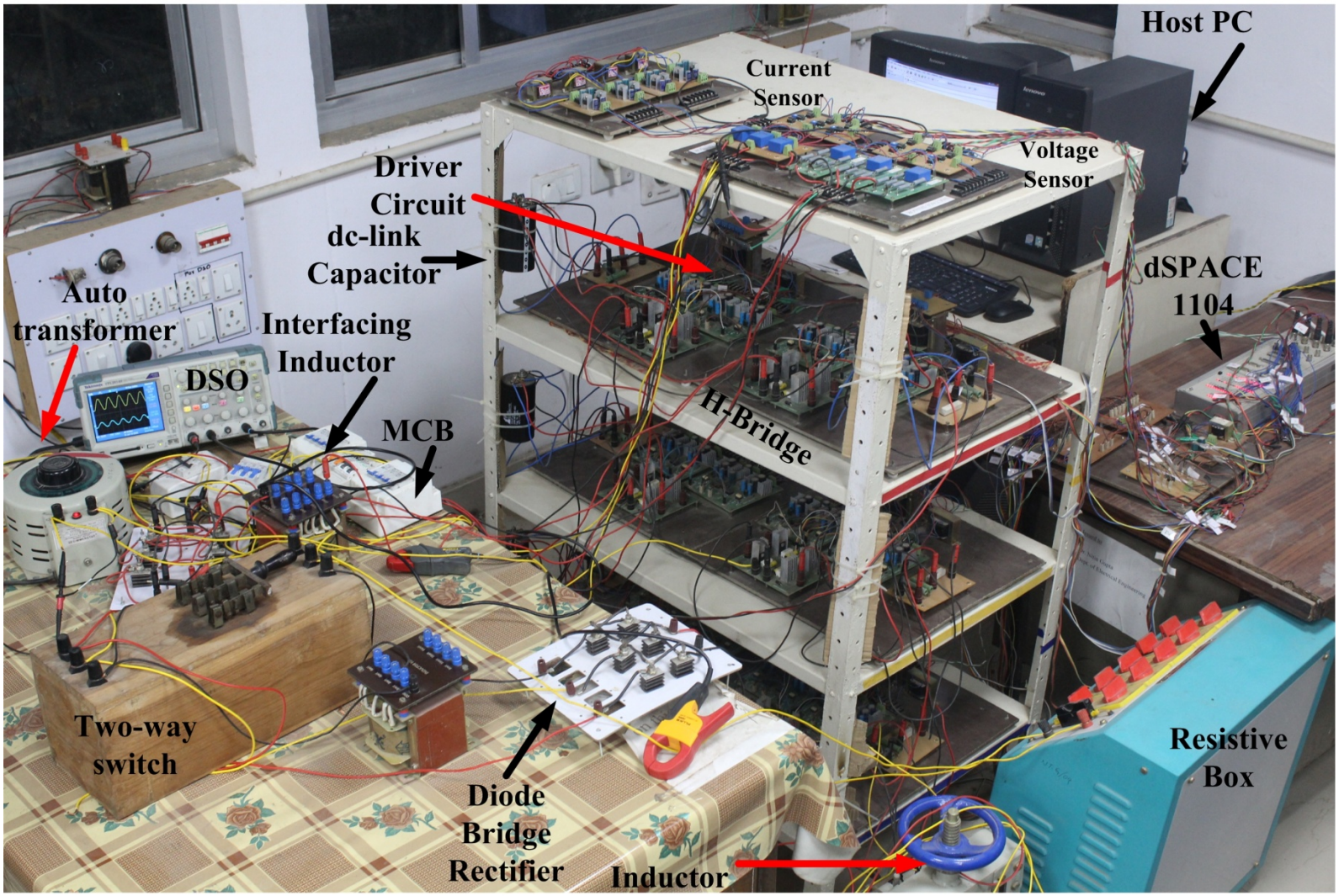

Figure A.10 Complete set-up of five-level CHB-MLI based SAPF for experimental analysis

APPENDIX-B

Table B.1 Design of Power Circuit Parameters [123, 124]

Parameters	Formula for five-level CHB-MLI based SAPF	Value in Simulation	Value in Hardware
DC-link reference voltage	$V_{d-ref} = \frac{2\sqrt{2}V_L}{\sqrt{3}m}$ where m=0.8	$= 6735.2$ V $V_{d\text{-}ref}$ is taken as 6800 V	=51.02V $V_{d\text{-}ref}$ is taken as 52 V
DC-link capacitor	$C_{dc} = \frac{K_L I_C V_L T}{2\left[V_{d-ref}{}^2 - V_d{}^2\right]}$ where K_L=1.2=overloading factor and T=0.02 sec	=5835 μF C_{dc} is taken as 6000 μF where I_C= 25 A	=2205.88 μF C_{dc} is taken as 2200 μF where I_C= 3 A
Interfacing Inductor	$L_{Lf} = \frac{\sqrt{3}m_a V_{d.ref}}{12K_L(m-1)f_{sw}\Delta I_{sw.p-p}}$	8.175 mH L_{Lf} is taken as 8 mH	3.16 mH L_{Lf} is taken as 3 mH

APPENDIX-C

Table C.1 Parameters Used for Simulation Study

Parameters	Value	Parameters	Value
$V_{d\text{-}ref}$	6800 V	φ	70°
L_{Lf}	8 mH	ω	314 rad./sec
$K_{PS\text{-}PWM}$	$5.33*10^{-4}$	V_S	11 kV
f_{SW}	2000 Hz	R_S	0.5 ohm
ω_G	12566	L_S	0.1 mH
R_{Lf}	0.5 ohm	V_d'	5321 V
C_{dc}	2200 μF		
R-L Loads for Simulation			
R_L	230 ohm	L	550 mH
R-C Loads for Simulation			
R_C	1000 ohm	C	150 μF

APPENDIX-D

Table D.1 Parameters Used for Experimental Study

Source Voltage	50 V
Source Inductor	0.1 mH
Interfacing Inductor	3 mH
DC-bus Capacitor	2200 μF
Resistance across DC-bus capacitor	10k/ 10 W
Multilevel Inverter	H-bridges having 4 number of IGBTs (IGBT- STGW30NC120HD)
Driver Circuit	TLP-250 is used as opto-isolator, Separate Dead-band circuit is used
Current and Voltage Sensor	LA 25-NP, and LV 25-1000, respectively
Switching frequency in PS-PWM	1 kHz
Non-linear Load	Resistive load box (230V, 10 A), Inductance (0-200 mH) Capacitor (220 μF)