DESIGN, DEVELOPMENT OF INVERTER TOPOLOGIES AND CONTROL TECHNIQUES TO ENHANCE THE OPERATION OF SHUNT APF FOR POWER QUALITY IMPROVEMENT

Ph.D. Thesis

VIJAYAKUMAR GALI

(2014REE9516)

DEPARTMENT OF ELECTRICAL ENGINEERING

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR

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Design, Development of Inverter Topologies and Control Techniques to Enhance the Operation of Shunt APF for Power Quality Improvement

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Vijayakumar Gali

(2014REE9516)

Under the Supervision of

Dr. Nitin Gupta **Prof. R. A. Gupta**

DEPARTMENT OF ELECTRICAL ENGINEERING

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR

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DECLARATION

I, **Vijayakumar Gali**, declare that this thesis titled, **"Design, Development of Inverter Topologies and Control Techniques to Enhance the Operation of Shunt APF for Power Quality Improvement"** and the work presented in it, are my own. I confirm that:

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Place: Jaipur

Date:

Vijayakumar Gali

(2014REE9516)

Department of Electrical Engineering
MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY
JAIPUR

CERTIFICATE

This is to certify that the thesis entitled **"Design, Development of Inverter Topologies and Control Techniques to Enhance the Operation of Shunt APF for Power Quality Improvement"** being submitted by **Vijayakumar Gali (ID No. 2014REE9516)** is a bonafide research work carried out under our supervision and guidance in fulfillment of the requirement for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Malaviya National Institute of Technology, Jaipur, India. The matter embodied in this thesis is original and has not been submitted to any other University or Institute for the award of any other degree.

Place: Jaipur

Date:

Dr. Nitin Gupta
Assistant Professor
Department of Electrical Engineering
MNIT Jaipur
Jaipur -302 017, India

Prof. R. A. Gupta
Professor
Department of Electrical Engineering
MNIT Jaipur
Jaipur -302 017, India

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(VIJAYAKUMAR GALI)

ABSTRACT

The rapid advancement in power electronics technology and high-speed digital signal processors has caused the widespread use of power electronics based equipment in various industrial and domestic applications. The power electronic devices are operated as switches for efficient control of power, hence such operation affects the power quality (PQ) of three-phase three-wire (3P3W) and three-phase four-wire (3P4W) including single-phase electrical power system network. Hence, harmonic mitigation and reactive power compensation have become prime importance for suppliers and end utilities.

The custom power devices (CPDs) or active power filters (APFs) are found to be a feasible solution to counter various PQ problems. Three types of APFs are available in the literature such as shunt-, series-APF and unified power quality conditioner (UPQC). The shunt APF is widely used as an active compensation approach to mitigate PQ problems like current harmonics by injecting compensating component of current at the point of common coupling (PCC) or point of interconnection (POI), reactive power compensation to ensure unity power factor, load balancing with neutral current compensation. Therefore the source current remains sinusoidal with total harmonic distortion (THD) level well within limits at the customer end. The shunt APF is a current source inverter (CSI) or voltage source inverter (VSI), connected parallel at PCC. The VSI based shunt APF topology is extensively used in the literature due to its advantages such as cheaper cost, lighter weight and flexible control compare to CSI based shunt APF topology.

Reference current generation techniques play a significant role in controlling the flow of compensating current and reactive power compensation. The performance of the shunt APF is highly depended on the accuracy of the generated reference current. However, these control techniques are significantly influenced by the supply voltage and grid conditions. The generated harmonics in the present power system are time-varying in nature because of continue changing of the load demand. To address these issues, several advanced control techniques are proposed by researchers in the literature. But, most of the control techniques are required complicated calculations which limits the real-time implementation. By acknowledging the aforementioned problems, design, develop and investigate a shunt APF

to mitigate current harmonics, reactive power to ensure unity power factor is a cost-effective solution. A field survey of various power quality events like voltage and current harmonics, reactive power requirement of load have been conducted as a first objective. This survey is helpful to understand the level of harmonic pollution produced by the various equipment in the present modern power system network and quality of power at the utility end. Moreover, it is obliging to design and implement control techniques to compensate various power quality problems in the present power system.

Design and development of single-phase shunt APF to mitigate current harmonics and reactive power to ensure unity power factor under sinusoidal and distorted supply voltage conditions with improved switching technique are considered to investigate a second objective. The control technique is divided into two parts, one is to extract the fundamental frequency component of supply voltage using Hilbert transform based adaptive tuned filter (ATF) followed by reference current generation using DC-link energy balance theorem. Second deals with an improved pulse width modulation (PWM) technique using a unipolar hysteresis current controller (UHCC) which reduces switching ripples and switching frequency for voltage source inverter (VSI) fed shunt APF. This control technique requires one current and two voltage sensors to detect the grid voltages and currents. MATLAB®/ Simulink software is used for implementing the single-phase shunt APF. The performance of the single-phase shunt APF using Hilbert transform based ATF with UHCC switching scheme in comparison with the single-band hysteresis current controller (SBHCC) is investigated under sinusoidal and distorted supply voltage conditions. The simulation results are validated by implementing a prototype model in the laboratory using dSPACE 1104 controller.

Shoot-through mode is one of the most perilous failure modes encountered in conventional inverter circuits of active power filters. In conventional VSI, when two power electronic devices of the same leg turn on abruptly, this causes to flow high short-circuit current in the circuit operation and damage the devices. This shoot-through phenomenon has noticeable drawbacks such as ringing effect, increase temperature in power devices, causes electromagnetic interference (EMI) and degrade the efficiency of the circuit. To address these issues of shoot-through problems, an interleaved inverter is presented as a shunt APF. The present power system is having inevitable sensible non-linear loads which

create harmonic pollution and decrease the compensation capability of shunt APF due to large variations in supply voltage distortions. Predictive tuned filter with symmetrical component theory is presented to extract fundamental component signal from distorted and/ unbalance voltages. The extracted fundamental signal is further proceeded through reference current generation. Conventional feedforward control techniques carry forward switching notches and distortions in the reference currents. To avoid this problem, a modified indirect current control technique is introduced with a tuned low pass filter (LPF) to separate the ac and dc components of the instantaneous power. Further, the dc component of power is used for reference source current. A controlled and uncontrolled rectifier with R-L load are modelled as a non-linear load for testing the effectiveness of the interleaved SAPF with modified control algorithm. The effectiveness of the interleaved inverter based SAPF with modified control algorithm has been thoroughly tested in MATLAB®/ Simulink platform and verified experimentally.

The DC-link capacitor voltage plays a significant role in the active power filters. It supplies harmonic component of currents, switching losses, reactive power under steady-state and real power under the transient condition of the load. During transient condition of the load, there is a large variation between reference and actual values of DC-link voltages. The DC-link voltage has to be maintained at its reference value for accurate compensation. The PI controllers are well-established controllers to stabilize the DC-link voltage because of its simplicity, reliability and ease of implementation with low-cost controllers. It requires precious mathematical modelling of system for obtaining the gain parameters. However, it has demerits like sluggish response during transient condition of the load and under distorted supply voltage conditions. Sliding mode controllers (SMCs) are acknowledged a remarkable response in the application of APF. The main advantage of the SMC is that, it is sensitive to parameter uncertainty and external disturbances. Therefore, the SMC is the most suitable for the closed-loop control of the converters. However, the conventional SMC has demerits like poor response under mismatched system uncertainties/ disturbances. Therefore, multitudinal sliding mode controller (MSMC) is developed to overcome the problems of conventional SMC. The MSMC uses multiple surfaces for mismatched system disturbances/ uncertainties. Moreover, it uses inertial delay control (IDC) to control the mismatched disturbances/ uncertainties. Various

simulation and experimental studies have been conducted to verify the compensation competence of MSMC in comparison to conventional SMC. The test is conducted under steady-state and transient condition of load with different supply voltage conditions.

The power system network has different types of linear and non-linear loads which continuously switches on and off. The PI controller gain parameters have to be tuned according to the non-linear system behaviour. This is a major challenge for the researchers to tune the gain parameters of PI controller for stabilizing the DC-link voltage. Various artificial intelligent techniques have been proposed by the researchers across the globe to tune the PI controller gain values. In which, swarm evolutionary theorems have become more popular to solve multi-objective function of the non-linear system. Particle swarm optimization (PSO) is found to be reliable solution for tuning the PI controller gain values. A swarm processed in the search space to discover optimal solutions. The particles in the search space try to reach its optimal solution by updating position on own best position obtained by each particle. Due to its simplicity, ease of implementation with low-cost controllers and well-balanced mechanism to reach out local and global best, it became more popular in various applications. However, it has disadvantages like exploring all local best position obtained by the all particles in the search space. This increase the complexity of the computation, reduce the speed of the processors, and increase the number of iterations. By considering the above issues of optimization problems, enhanced particle swarm optimization (EPSO) technique is introduced to solve multi-objective function by eliminating the local best opposition and improve the converge speed obtained by the particles in the search space. The performance pre-eminence of EPSO technique is tested in comparison with the conventional PI and PSO based control techniques. Various simulation and experimental studies have been conducted under different load and supply voltage conditions to show the performance improvement of the EPSO based modified control technique.

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LIST OF SYMBOLS

The symbols used in the text have been defined at appropriate places. However, for easy reference, the list of principle symbols are being given below.

v_s	RMS supply voltage
C_{dc}	DC-link capacitor voltage
L_{a1}, L_{b2}, L_{b1}, L_{b2}	Interfacing inductors
I^*_{sm}	PI controller output
K_p	Proportional constant
K_i	Integral constant
I_c	Peak value of Inverter current
V_s	Peak value of Supply voltage
r_{a1}	Interfacing inductor resistance
V_{dc}	DC-link capacitor voltage
μ	Switching state
i_c	Compensating current
x_1, x_2, x_3	Sliding mode Variables
y(t)	Sliding surface output function
U_{eq}	Sliding surface equivalent
$e_2(t)$, $e_3(t)$	System disturbances
$e_1(t)$	Lumped uncertainty
k	Sliding gain
S	Sliding surface
S_1	First Sliding surface
λ	Surface boundary
$V_{dc,ref}$	Reference DC-link voltage
S_1	First sliding surface
S^*_1	Modified first sliding surface
β	Sliding surface Constant value

$\hat{w}$	IDC output
S_2	Second Sliding surface
S_2^*	Modified second sliding surface
τ	Time constant
a, b	Control Constants
i_{Load}	Load current
I_{Lm}, I_h	Peak values of fundamental, harmonic component of load currents
φ_{Lm}, φ_h	Load current and harmonic current phase angles
$i_{Lmp}(t)$, $i_{Lmq}(t)$, $i_{Lh}(t)$	Active, reactive and harmonic components of load Currents
$P_{Load}(t)$	Load power
U_m	Maximum value of supply voltage
$P_{Real}(t)$	Real Power
$Q_{Reactive}(t)$	Reactive Power
$P_{Harmonic}$	Harmonic Power
i_s^*	Reference source current
v(t)	Unit template
$i_{s,actual}$	Actual source current

LIST OF ABBREVIATIONS

The abbreviations used in the text have been defined at appropriate places. However, for easy reference, the list of abbreviations are given below.

ABBREVIATION	EXPLANATION
AC	Alternating Current
AI	Artificial Intelligent
APF	Active Power Filter
ADC	Analog to Digital Converter
ASD	Adjustable Speed Drives
ATF	Adaptive Tuned Filter
BFO	Bacterial Forgiving Optimization
CSI	Current source Inverter
CPD	Custom Power Device
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EPSO	Enhanced Particle Swarm Optimization
FB IB-APF	Full Bridge Interleaved Buck Active Power Filter
FPGA	Field Programmable Gate Array
FLC	Fuzzy Logic Controller
FFT	Fast Fourier Transform
GTO	Gate turn off thyristor
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	International Electrical & Electronics Engineering
IGBT	Insulated Gate Bipolar Transistor
IRPT	Instantaneous reactive power theory
LPF	Low Pass Filter
MSRF	Modified Synchronous Reference Frame

MSMC	Multitudinal Sliding Mode Controller
NN	Neural Network
PLL	Phase Lock Loop
POI	Point of Interconnection
PQ	Power Quality
PSO	Particle Swarm Optimization
PWM	Pulse Width Modulation
RMS	Root Mean Square
RTDS	Real-Time Digital Simulator
RLS	Recursive Least Square
SGOI	Second-Order Generalized Integrator
SMC	Sliding Mode Controller
SPMS	Switched Mode Power Supplies
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
SVM	Space Vector Modulation
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
UPQC	Unified Power Quality Conditioner
UPS	Uninterruptable Power Supplies
VSI	Voltage Source
3P3W	Three-phase Three-wire
3P4W	Three-phase Four-wire

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "Mitigation of Power Quality Problems using Shunt Active Power Filters: A Comprehensive Review," in *Proc. of 12th IEEE Conference on Industrial Electronics and Applications (ICIEA 2017)*, Cambodia, pp. 1100-1105, June 18th-20th, 2017.

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Overview

Electrical energy has become the most easily accessible energy source across the world. The use of alternating current circuits in electrical power system have been a common practice since, very inception of the interconnected power system network. In such system, two types of loads are available i.e. linear and non-linear loads. The linear loads which are constant power, constant current and constant impedance loads. Therefore, the wave shapes of voltage and current are nearly sinusoidal. But, due to presence of inevitable non-linear loads in the power system network, the wave shape of voltage and/ or current waveforms are severely affected which further degrade power quality of the system. According to power quality definition, the wave shape of voltage and/or current should be maintained nearly sinusoidal with their magnitude and frequency within the statutory limits [1-3].

The PQ is generally used for assess and maintain the good quality of power at the level of generation, transmission, distribution, and at the utility end. Since, the pollution of electric power supply system is much severe at the utilization level due to rapid use of power electronic based converters in high-, and low-power applications. The high-power applications like adjustable speed drives (ASDs), high voltage direct current (HVDC) systems, large arc furnaces, electric traction system, etc. as wells as low-power applications like switched mode power supplies (SMPS), uninterruptible power supplies (UPS), residential electronic appliances, etc. are having the dominant share in consumption of electrical energy and injection of PQ issues into the system. The power electronic converters with advanced high-speed digital signal processors (DSP) offer enormous advantages such as flexible control, reduced cost and size, increase the robustness, etc. in the aforementioned applications [4]. Therefore, continue proliferation of power electronic devices create immense PQ problems like current harmonics, reactive power burden which leads to poor power factor, excessive neutral current, etc. in the electrical distribution

system as well as voltage sag, voltage swell, etc. in the electrical transmission system [5-10].

1.2 State of Art on Power Quality

The power quality problems are subjected to present in the entire power system network due to proliferation of non-linear loads. Hence, it affect the protection systems and results mal-operation of protective devices. This may also interrupt many operations and processes in the industries and other establishments, affect different measuring instruments and metering of the various quantities such as voltage, current, power, and energy. Moreover, these problems affect the monitoring systems of critical, emergency, and costly equipment, etc. [11]. Hence, the study of the PQ becoming more important subject for both suppliers and end users. Many International standards such as Institute of Electrical and Electronics Engineers (IEEE), International Electrotechnical Commission (IEC), etc. have been developed and enforced voltage and current distortions limits for different voltage levels so that the PQ of an electrical system can be maintained [7]. Several standards such as IEEE 519-1981,-1992, and -2014, IEC 61000, have been implemented permissible limits in the levels of deviations and distortions in various electrical quantities such as voltage, current, and power factor. Table 1 shows the maximum % harmonic distortions limits in 120V through 69 kV system [12-15].

Table 1.1

IEEE Standard 519-2014: Maximum current distortion limits for systems rated 120V through 69 kV [14]

Maximum harmonic current distortion (in per cent of I_L)						
Individual harmonic order (odd harmonics)[a, b]						
I_{sc}/I_L	3<h<11	11<h<17	17<h<23	23<h<35	35<h<50	TDD
<20[c]	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

[a]Even harmonics are limited to 25% of the odd harmonic limits above.

[b]Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed

[c]All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/IL

Where,
I_{sc}=maximum short-circuit current at PCC.

I_L = maximum demand load current (fundamental frequency component) at the PCC under normal load operating conditions.

There are several mitigation techniques have been introduced by many researchers across the globe to solve the PQ problems and maintain the voltage and currents in its permissible limits as per standards. Over the years, aforementioned problems have been resolved by a passive approach, which is a combination of L-C components. It is a tuned filter having distinct advantages like current/voltage harmonic elimination, reactive power compensation, etc. [16]. However, these approaches are having some demerits as enumerated in [13]. Various custom power devices or active power filters such as shunt APF, series APF and unified power quality conditioner have been developed to solve various voltage and/ or current related PQ problems in the distribution and transmission systems with advantages over conventional passive filtering methods [17-18]. These APFs are built with power electronic devices with inductor/ capacitor on its DC side. The converter switches are controlled to supply compensating currents to the grid for mitigating the harmonic currents and reactive power burden simultaneously. Due to advantages of APFs, there is tremendous interest created among the researchers to solve PQ problems in the present power system.

1.3 Literature Survey

The mitigation of power quality issues has become a major concern for the power and electrical engineers due to intensive use of power electronic based converters in small-, medium-, and high-power applications [19-20]. Conservatively, passive filters have been used to mitigate the current harmonics, reactive power burden to improve the power factor of the system. These filters offer either low impedance path or high impedance path to divert or block the harmonic currents flowing into the system. Also, it is tuned to a particular frequency component or multiple frequency harmonic component of signals to accomplish this goal [21]. However, passive filters have limitations as, the addition of passive elements create resonance with the system impedance, increase the cost and size with increase the compensation level. To overcome the drawbacks of conventional passive

filtering, researchers across the globe came with a new type of approaches, i.e. active filtering methods [22].

In concern to these problems of conventional passive filtering methods, the concept of custom power devices or active power filtering came into existence. Mainly, three types of active filters are available in the literature such as shunt-, series-APF and UPQC. The voltage related problems mainly occurred in the transmission system such as voltage sag, voltage swell, voltage flickers will be solved by series APFs. Whereas, the current related problems mainly occurred in the distribution system such as current harmonics, reactive power compensation, etc. have been solved by shunt APFs. The UPQCs have been designed to solve both voltage and current related PQ problems. The shunt APF is the most commonly used topology over the series APF and UPQC, because of many industrial and domestic applications require current harmonic compensation [23-29].

The basic idea of shunt active filtering is proposed by Sasaki and Machida in 1971 [30]. The shunt active power filter injects the reactive, unbalanced and harmonic component of load currents into the grid with the same magnitude and opposite phases. Gyugyi et al. [31] have presented the structure of shunt-, and series-APF in 1976, where PWM inverter is implemented by using transistors. This has lack of control techniques, hence practical implementation became complicated.

Advancement of power semiconductor device technology in terms of switching speed and power handling capability, the shunt active power filters with PWM inverters become more reliable in practical implementation [32]. This tremendous achievement in the power handling capability and switching speed of gate turn off thyristor (GTO), insulated gate bipolar transistor (IGBT) and metal oxide semiconductor field effect transistor (MOSFET) in combination with microcomputers and DSPs have achieved flexible control of APFs [33].

However, the practical power system problems have not been solved because of their lack of control techniques, higher initial cost, and significant losses in the system. Continue advancement in microelectronics and power semiconductor technology, the researchers are motivated to study and make improvements in the control strategies, topologies for shunt active power filters [34]. Hence, shunt APF for compensating the current harmonics and reactive power burden has been presented in this thesis work.

1.3.1 Shunt APF Configurations

Various types of shunt APF topologies are available in the literature. Again this subcategorized into three types based on circuit configuration, power source and inverter circuitry [35-36].

Bilgin et al. [37] have presented the current source inverter based shunt APF. The inductor is used for forming a DC-link at the DC side of shunt APF. This type of topology is having boost characteristics, longer life of storage, high capability of fault protection and control over source current. However, it has some disadvantage such as higher conduction losses due to higher inductance employed as energy storage device, size of inductor and increases the complexity of control technique [38].

Singh et al. [39] have presented voltage source inverter based topology, the capacitor is being used to form the DC-link. It is having a very compact size, lower cost and higher efficiency. Mostly, the electrical power system loads are three-phase and single-phase. These loads are connected through single-phase, three-phase three-wire and three-phase four-wire (3P4W) source [40-41]. The shunt APF can be divided on the basis of supply system configurations to mitigate various PQ problems. The harmonic current and reactive power burden are same in 3P3W and single-phase system. Besides, neutral and unbalanced currents are being raised in the 3P4W system [42].

Most of the loads in the electrical distribution are single-phase, hence these type of single-phase loads produce more PQ problems and inject into the system. Torry et al. [43] have presented to single-phase shunt APF for mitigating the generated harmonic currents by multiple non-linear loads and investigated harmonic spectral analysis of different nonlinear loads. Rahmani et al. [44] have demonstrated the simulation and experimental performance of single-phase shunt hybrid APF system. A 1 KVA laboratory prototype is implemented to validate the simulation results. Song et al. [45] are implemented simple model predictive power control theory based control technique with optimized constant switching frequency technique for single-phase shunt APF using TMS320F2812 DSP controller. A substantial simulation and experimental results are performed to mitigate various current harmonic which ensure the unity power factor operation of the system. Biricik et al. [46] have developed the single-phase shunt APF system in RT-LAB real-time

platform. This type of system reduces the complexity and improves the efficiency however the actual grid interface problems and real-time environmental effects may not considered while testing the system.

Mishra et al. [47] have demonstrated 3P3W shunt APF topology to mitigate harmonic currents and reactive power drawn by the nonlinear loads. Thus, making the supply current sinusoidal with a unity power factor (UPF) operation. A. Chaoui et al. [48] have developed three-phase shunt APF system with simple control algorithm to mitigate current harmonics and reactive power. The shunt APF experimental prototype was developed in laboratory by using DS1104 of dSPACE controller. Garanayak et al. [49] have presented recursive least square (RLS) technique for 3P3W shunt APF system to detect the amplitude and phase angle of the fundamental and harmonics, respectively. The simulation performance displayed good results in terms of tracking time and accuracy by eliminating the harmonics and reactive power of the non-linear load. Singh et al. [50] have designed 3P3W shunt APF system with ripple filter. The passive ripple filter is connected at PCC parallel to the loads to suppress high frequency switching noise at PCC voltages caused due to switching of VSC. An extensive simulation studies have been carried out to test the system under various supply and load conditions. The simulation results have been validated by experimental verifications. This type of topology used by many authors to demonstrate the compensation competence of various control techniques to mitigate various customer generated harmonics in the system [51-52].

In the 3P4W system, reduction of neutral current is a major concern for the researchers. The neutral current is $\sqrt{3}$ times of the phase current [53]. Gruzs [54] has presented different topological and control strategies for three-phase shunt APF system to mitigate PQ problems. There is a two-capacitor spilt type model (2C), four leg inverter topology and three full bridge topology (3HB). In 2C type model, the two capacitors equally spilt and fourth wire for the neutral is connected through mid-point of the two capacitors. The neutral current has been compensated through this manner of connection [55]. However, it has limitations that the balancing of the DC-link capacitor values for effective neutral current compensation is a major challenge and difficult in the practical implementation. Moreover, it requires additional control loop to maintain both capacitors at required voltage levels [56-57]. To overcome the problems of 2C type topology, an additional inverter leg is

introduced to make four leg inverter topology for compensating the neutral current [58-59]. It has been proven with better results compared to 2C type topology. However, it has disadvantages such as requirement of additional inverter leg which increases the cost and complexity of control algorithm. The 3HB topology consists of three single-phase inverter legs which are having a common DC-link capacitor and connected through three independent transformers at the point of common coupling (PCC). Hence, each phase of the 3P4W system is controlled independently in conjunction with other phases, therefore the controllability of the system is improved [60-61].

Latran et al. [62] have presented a thorough review of different advanced topological aspects of shunt APF. The multi-level topologies are used in medium and high power applications. These are efficient in compensation capability with reduce dv/dt losses in the switching devices [63-65]. There are different multi-level topologies mentioned in the literature such as diode clamped, flying capacitor and H-bridge and modular multi-level topologies [66]. However, the complexity of the power circuit and control algorithm increases.

The most aforementioned shunt APF topologies are VSI based topologies which are facing serious problems such as shoot-through effect, electromagnetic interference (EMI), temperature rise in the switches due to ringing effect [67]. To overcome the problems of conventional inverter topologies, the researchers have come with new inverter topologies to overcome the problems of conventional topologies [68-69].

Grandi et al. [70] have investigated the effect of dead-time in the operation of VSI. The dead-time affects the output variables of the three-phase inverters by creating ripples in the output current. Many researchers across the globe have implemented various PWM dead-time elimination techniques to overcome the shoot-through effects. Chen et al. [71] have suggested a dead-time elimination method. A substantial simulation and experimental work have been presented to prove the dead-time elimination technique. Goluszek [72] invented interleaved buck inverter to replace the conventional VSI topology with the advantage of eliminating the shoot-through problems by changing circuit configuration. Hong et al. [73] have developed a prototype of interleaved dual buck full bridge three-level inverter for grid connected system. Yao et al. [74] have developed dual-buck full bridge inverter with reduced number of sensors. Panda et al. [75] have presented simulation and

OPAL-RT lab analysis of 3P4W full bridge interleaved buck active power filter (FB IB-APF) which eliminates the shoot-through phenomenon. This topology needs more number of switches which increases the cost, complexity of circuit and control algorithm. Even though the shoot-through problem were eliminated with this topology, but the size of DC-link capacitor and interfacing inductor were increased. Moreover, practical grid voltage conditions have not been considered while developing the prototype model using OPAL-RT environment [76].

1.3.2 Reference Current Extraction Techniques

Reference current extraction techniques play a significant role in the active power filters for accurate compensation of PQ problems. The literature enriched with various reference current generation techniques. The reference current extraction techniques are mainly categorized into two types, i.e. frequency-, and time-domain techniques [77-78]. The frequency-domain control techniques have been used in both single-phase and three-phase systems such as fast Fourier transform (FFT) analysis, Kalman filter, wavelet transform based techniques, etc. [79]. The FFT is used in shunt APF to extract the harmonic components from the polluted harmonic signal. The main drawback of this type of technique is that it requires huge computations which increase the complexity of control technique [80]. The Kalman filter requires a state variable model and recursive estimator to estimate the parameters and measure the equations related to the discrete state variables. It is used for real-time applications because it can calculate the time-varying harmonic content [81]. The wavelet transform converts voltage/ current signals into frequency domain from time-domain for calculating the active and reactive powers in terms of frequency domain [82]. Even though, these frequency-domain techniques are having distinct advantages, implementation in real-time system is more complex by increasing the burden of calculation on DSPs.

The time-domain control techniques are becoming more popular because of their simple structure and ease of implementation in the real-time controllers. The more number of researchers across the globe have worked on these time-domain techniques because of their robustness, ease of implementation, etc. These time-domain techniques have designed for both 3-phase and single-phase systems [83-84].

Akagi et al. [85] have presented *p-q* theory which is also called as instantaneous reactive power theory (IRPT). This IRPT works by converting the three-phase voltage/ current signals into two-phase voltage/ current signals by using Clarke's transformation. The active and reactive powers are calculating without any time delay in this control technique [86-87]. The supply voltages are assumed to be ideal in this theory. But, practically the supply voltages also get distorted and/ or unbalanced due to continue use of non-linear loads. Hence, the assumption of being ideal supply voltage make false calculation of reference current generation. Hence, it affect the accuracy and performance of control algorithm under distorted and/ or unbalanced supply voltage conditions.

Mishra et al. [88] have demonstrated IRPT for 3P4W electrical system. A general instantaneous vector expression for filter current in terms of active and reactive powers has been derived. The effect of supply voltage unbalance nature is clearly analyzed and the balanced fictitious set of voltages are assumed for the reference current generation. The system has tested under balanced and unbalanced supply voltage conditions. The substantial simulations studies have presented to evaluate the performance of the aforementioned control algorithm.

Singh et al. [89] have demonstrated a comparative experimental investigation on the direct and indirect current control techniques. Indirect current control technique offers better performance, requires less number of sensors, removes the notches occurs due to switching action of VSI and ripples from the compensated source current. The hardware is implemented using TMS320C31digital signal processors [90-91].

Zaveri et al. [92] have presented a simulation study of synchronous reference frame (SRF) theory. According to this theory, the fundamental components and dc components are extracted by transforming the voltage and current signals into synchronously rotating frame. The DC-voltage control loop is used for maintaining the DC-link voltage. Jayaprakash et al. [93] had implemented SRF theory by using dSPACE1104 controller. Immense experimental investigations have been conducted to test the performance of the control algorithm under available and distorted supply voltage case. C. H. da Silva et al. [94] proposes a novel phase lock loop (PLL) control strategy to synthesize unit vector modified synchronous reference frame theory (MSRF). The unit vector is used for vector rotation or inverse rotation in vector-controlled three-phase grid-connected converting

equipment. The developed MSRF-PLL is fast in transient response compared to standard PLL technique [95-96]. The performance is robust against disturbances on the grid voltages with harmonic compensation.

Karuppanan et al. [97] have implemented unit current vector control technique. The source currents are sensed for calculating the unit sine vector templates. It achieves unity power factor operation by maintaining the supply voltages and currents are in phase. This requires less number of sensors, ease of implementation and reduces the complexity burden on the processors. The author presented simulation performance of 3P3W shunt APF with the sine unit vector control algorithm. This control algorithm actively compensates the current harmonics and reactive power along with the improvement in power factor for sinusoidal supply voltages. The practical implementation of the control technique is not addressed.

Singh et al. [98] have presented a comprehensive review of shunt APF configurations, control strategies, selection of components, other related economic and technical considerations, and their selection for specific applications. This review gives clear perspective on various aspects of the shunt APF to the researchers and engineers working in this field.

The generated reference currents significantly affected by the supply voltage and/or grid condition. The practical power system has polluted with various combinations of linear and/or non-linear loads [99]. Hence, these loads highly disturb the grid and/or supply mains. The extraction of the fundamental frequency component of supply voltage from distorted and/ or unbalanced supply mains is a big challenge for the researchers. Researchers are working with PLL based control techniques to generate unit template in synchronism with the input signal. It should act fast by detecting phase angle and amplitude in a faster rate. Patjoshi et al. [100] have presented a simulation study of PLL based shunt APF under distorted supply voltage. da Silva et al. [101] have recommended single-phase and three-phase PLL based modified p-q theory. The PLL gain values are being tuned by second-order generalized integrator (SGOI). The SGOI is frequency dependent, hence it makes frequency non-adaptive in contemplation to the PLL resonance frequency. However, apart from distinct advantages of PLL, it is also suffering from some

disadvantages such as tuning of PLL gain parameters under distorted grid supply voltage conditions and transient condition of non-linear conditions [102-104].

Song et al. [105] have developed a self-tuning filter (STF) to extract a selected frequency component from the distorted supply voltage. Later, many researchers have applied this technique to the different topology of single-phase and three-phase APF. Abdusalam et al. [106] applied STF-based control with the *p-q* theory for extracting the voltage and current signals, without the use of any low-pass or high-pass filters. Biricik et al. [107] have used the STF algorithm to extract the harmonic components of distorted supply voltage and unbalanced load currents. This method eliminates the additional low pass or high pass filters hence, no delay problems. Gupta et al. [108] have applied this technique for extraction of the fundamental component of voltage signal from the distorted supply voltage which further processed for the reference current generation using DC-link energy balance theorem. Also, a laboratory prototype has developed using TMS320F28335 DSP and tested compensation capabilities of the control technique under sinusoidal and distorted supply voltage conditions. Singh et al. [109] have implemented notch filter based fundamental frequency component extraction technique to mitigate current related PQ problems using shunt APF under distorted supply voltage conditions. This notch filter is designed to retain its property of fundamental frequency component extraction without any extra calculation to work even under variation of grid frequency. Patel et al. [110] have been implemented nonlinear adaptive Volterra filter for calculating weights of the load fundamental frequency components. These weights are used for the reference current generation such that the source currents become sinusoidal close to unity power factor. Sreeraj et al. [111] have been implemented one cycle based control algorithm for extracting the fundamental frequency component of voltage signal and grid synchronization without phase delay. The one cycle control algorithm makes them robust with absence of PLL and also ensures that they can be realized by employing simple analog circuits. A rigorous simulation and experimental studies have carried out to test the compensation competence of one cycle based control algorithm.

The reference current generation and accuracy of compensation depend on the DC-link voltage stabilization. The control technique contains two control loops i.e. current control loop and voltage control loop in the closed loop operation of shunt APF. PI controllers are

well-established controllers used in voltage control loop to stabilize the DC-link voltage. This became very popular because of its simplicity, reliability and easy to implement with low-cost controllers [112]. However, it has demerits like sluggish response in the transient condition of the load and distorted supply voltage condition. Mahanty et al. [113] have designed sliding mode controller (SMC) for single-phase shunt APF to voltage control loop. This gives an impressive response in the application of APF by controlling the DC-link voltage. Ghamri et al. [114] have presented substantial simulation results of SMC based control algorithm for three-phase shunt APF. The prototype model was developed in LGEB laboratory to validate the simulation results. However, the conventional SMC has demerits like poor response under mismatched system uncertainties/ disturbances during distorted supply voltage and dynamic load change conditions [115-117]].

1.3.3 Artificial Intelligent Based Control Algorithms

Artificial Intelligence (AI) techniques are used increasingly as alternatives to more classical techniques to model different systems. Many researchers across the globe have proposed various AI techniques to design and model the system. AI can massively use in military, antiterrorism, automobile industry, internet search engines, robotics etc. [118]. The DC-link capacitor voltage plays a significant role in the compensation performance of the active power filters. It supplies harmonic component of currents, switching losses, reactive power under steady-state and real power difference under the transient condition of the load. There is a large variation in reference and actual DC-link voltage during the transient condition of the load. The DC-link voltage has to be maintained at reference value under different load and supply voltage conditions [119-120].

In 1942, Ziegler and Nichols were employed in the Tylor Instruments, developed a mathematical model for tuning of proportional-integral (PI) controller gain values [121]. Mikkili et al. [122] have demonstrated PI-based 3P4W shunt active power filters. The system was implemented in a real-time digital simulator (RTDS) hardware platform. These PI controllers have been used in the industry because of its simple structure, low cost, and less design complexity. The proportional gain value (k_p) helps to improve the system performance by reducing steady-state error and forced oscillations whereas integral gain value (k_i) enhance the overall system stability. Chaoui et al. [123] have presented PI controller based three-phase shunt APF system. A precise mathematical calculations have

been demonstrated for accurate tuning of PI controller gain values. The system has been modelled in MATLAB/ Simulink software and verified by developing a hardware prototype model in the laboratory using xPC Target system.

The non-linear loads in power system network are subjected to vary their demand frequently hence the amount of harmonic compensation changes accordingly. Therefore, the DC-link voltage changes from its reference value. This serious undesirable oscillations (overshoot and undershoot) are lead to the dielectric breakdown of the DC-link capacitor under the transient condition of the load. In other hand, the DC-link capacitor has to supply instant, real power to meet the load requirement which leads to a sharp decrement in DC-link capacitor voltage when load increased and vice versa [124-125]. It is important for the controller to adopt the changes in the system to maintain the reference value. Therefore, tuning of PI controller gain values has become a very important subject for efficient operation of shunt APF.

The AI techniques such as neural network (NN), fuzzy logic controllers (FLC), bacterial forgiving optimization (BFO), etc. have been using in the area of APF for optimal design of control parameters. It have gained much significance to tune optimal PI controller gain values. There are many researchers contributed different AI techniques across the globe for stabilizing the DC-link capacitor voltage of shunt APF.

Jain et al. [126] have found a fuzzy logic controller (FLC) to be an impressive tool because of its high robustness, insensitive to parameters changes, treating of non-linearity, etc. in APF applications. Panda et al. [127] have implemented the fuzzy logic-based control algorithm for tuning of PI controller gain values in shunt APF applications. The fuzzy logic controller has been tested under different supply voltage and load conditions to see the robustness of the control algorithm. The dynamic performance of shunt APF is improved by using fuzzy logic PI controller tuning. A comparative study has been conducted between conventional PI tuning and fuzzy logic PI tuning which were enumerated in [128-129]. The performance of shunt APF has shown an excellent compensation performance during load changing conditions which emphasizes the superiority of fuzzy logic controller. However, the fuzzy logic controller is suffering from disadvantages such as more number of rules are involving for finding the optimum values, huge computational time for fuzzification and defuzzification, etc. [130].

Passino [131] has motivated BFO algorithm to detect the foraging behaviour of bacteria that observes the chemical gradients in the environment and move towards or away from the specific signal. The behaviour of the bacteria proceeded into four sections, namely chemotaxis, swarming, reproduction, elimination and dispersal [132].

Mishra et al. [133] have implemented BFO algorithm in the shunt active power filter applications. In present power system scenario, the non-linear loads are injecting time-varying harmonics into the system. Therefore, the PI controller gain parameters have to be tuned according to load perturbations for stabilizing the DC-link voltage at its reference value. A fair comparison study between conventional PI tuning and BFO method also conducted. The simulation results have found that the stabilization of DC-link voltage by using BFO based tuning is better than the conventional PI controller tuning method under load perturbations as well as in system parameter variations [134-135].

Particle swarm optimization technique has been introduced by Eberhart and Kennedy [136] for understanding the swarming behaviour of the bird and fish flock. The PSO has advantages like solving multi-objective function, non-linearity and non-differentiability with the multi-diametrical problem. A swarm processed in the search space to discover optimal solutions. The particles in the search space try to reach its optimal solution by updating position on own best position obtained by each particle. Due to its simplicity, ease of implementation with low-cost controllers and a well-balanced mechanism to reach out local and global best, it became more popular in various applications [137-139].

Patnaik et al. [140] have developed PSO algorithm for the shunt APF applications to improve the tuning of PI controller. The proposed system developed for the 3P4W electrical distribution system to mitigate current harmonics, reactive power and neutral current compensation. Simulation studies are carried out to test the compensation competence of PSO based control algorithm with different supply and load conditions. The simulation results have verified by implementing a prototype model using Opal-RT lab software.

1.3.4 PWM Signal Generation Techniques

The PWM techniques are used for switching the solid-state devices of PWM converter which control the flow of the compensating current in the APFs. This PWM techniques are

employed in a wide diversity of applications, ranging from measurement and communications to power control and conversion [141].

The PWM techniques have been used for controlling the flow of compensation current by switching ON and OFF the solid state devices of the shunt APF. The aforementioned control techniques mentioned in section 1.3.2, generate reference current for harmonic compensation. The generated reference current is compared with the actual current which produce an error output. This error will further processed through suitable PWM control technique to generated switching signal for shunt APF switches. A wide variety of switching signal generation techniques are available in the literature. Mainly, the switching generation techniques are categorized into two types, open loop and closed loop methods. The open loop controllers or feed-forward controllers, are sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), etc. The closed-loop methods or feed-back controllers, are hysteresis current controller, sliding mode, deadbeat, etc. [142-143].

Feed-forward Controller

In SPWM controller, the sinusoidal signal is compared with the carrier triangular signal to generate the switching pulses. The multi-carrier based SPWM is used in the multi-level inverter based shunt APF to improve the compensation performance [144-145].

Ukande et al. [146] have implemented SPWM technique for single-phase shunt APF to improve the total harmonic distortion (THD) levels by controlling the inverter switches. The SPWM technique generates unique train of pulses, hence minimizes the switching losses. The switching pulses are generated by comparing the carrier signal with the triangular waves. Saeedifard et al. [147] presented space vector modulation (SVM) based STATCOM. This SVM offers great advantages such as higher magnitude on AC side of the inverter, hence lower level of DC-link voltage, higher degree selection of switching pattern will reduce the THD, balancing the DC-link voltages without additional control loop in multilevel inverter based shunt APF compared to SPWM.

Feedback Controller

In closed-loop controller, hysteresis controller is one of the prominent and widely used current control techniques among all other feedback controllers. The hysteresis controller

generates the switching signals by comparing the current error signal with the fixed hysteresis band. This controller is simple, robust, easy to implement, fast dynamic response and inherent peak-current limiting capability. However, this has some disadvantages such as variable modulation frequency which results higher switching frequency [148-151]. Many researchers have contributed their work to improve the performance of the conventional hysteresis current controller by attaining the fixed hysteresis modulation frequency.

Lohia et al. [152] have developed minimally switched control algorithm with hysteresis current controller for 3P4W shunt APF applications. The control technique has been formulated for reducing the switching frequency hence, reduces the switching losses. Both simulation and experimental study have carried out to verify the average minimal switching frequency technique. The experimental set up is implemented using low cost high-speed DSP TMS320F2812 controller which reduces the system cost and improves the system efficiency.

Dahono [153] has investigated a comparative study of different hysteresis current control techniques for single-phase full bridge inverters. The author has developed new hysteresis current controller to attain both advantages of unipolar and conventional hysteresis current controller. The new hysteresis controller has ensured to have equal switching among all the switching devices. Hence, the switching device can be fully utilized and improved the output wave shape of the inverter.

Sliding mode switching scheme is used for obtaining robust system performance against the parameter variations and the load perturbances. The sliding mode controller works on the building of the control law based on the state space of the system control surface and keep monitor to stay within the system surface irrespective of the variations. Jung et al. [154] have developed sliding mode switching scheme for closed-loop control of PWM inverter applications. These have inherent switching characteristics and robustness, hence PWM pattern can be obtained by sliding mode theory. This achieves higher switching frequency in the range of 10-100 kHz range, improves the performance of the converter.

Han et al. [155] have presented a deadbeat control algorithm implies an estimation of the line voltage instantaneous value which can also be used for the current reference generation. However, the inherent delay is a serious drawback of this technique. Due to the

requirement of high speed of response, it becomes the main limitation in active filter applications.

1.4 Identified Research Area and Contribution

The present electrical power system is subject to a wide variety of power quality problems due to continue proliferation of power electronic based nonlinear loads. The poor power quality can interrupt production process, affect sensitive equipment and cause downtime, scrap, and capacity losses. The current harmonics produced by the non-linear loads further lead to distortions in the voltage waveforms. Hence, maintaining the PQ at the utility end is the major challenge for the researchers and power engineers. As a repercussion, electrical utility and consumers are more concerned about power quality. Custom power devices or active power filters found to be viable solutions in the present power system network. The shunt APF is widely used as an active compensation approach to mitigate power quality problems like current harmonics by injecting compensating component of current at PCC, reactive power compensation to ensure unit power factor, load balancing with neutral current compensation so that the source current remain sinusoidal with THD well within limits.

A rigorous literature survey has been conducted in the field of active power filters. Many researchers and power engineers across the globe have put great efforts to improve the performance of shunt APF. There are number of topological and control techniques of shunt APF have been proposed to mitigate various PQ problems in the distribution system.

Conventionally, VSI has been used as shunt APF in many of the literature to solve these PQ problems. However, VSI is facing hazardous issues like shoot-through phenomenon, ringing effect which leads to a temperature rise in the power switches, EMI, etc. Therefore, it is required to introduce a new/ modified inverter topology for shunt APF applications to overcome the problems of shoot-through. An interleaved inverter is presented in this thesis to overcome the problems encountered with conventional VSI based shunt APF. The interleaved inverter based shunt APF is designed and developed for the compensation of current harmonics, load reactive power burden to improve the power factor, load unbalance. The rapid use of non-linear loads, will not only distort current waveform but also distort the voltage waveform. Therefore, it is to design a simple control technique to

compensate PQ problems under distorted supply voltage conditions both in single-phase and three-phase systems. The DC-link voltage plays an important role in the compensation of harmonics. A Multitudinal sliding mode controller is presented to provide a strategic approach for maintaining the stability under sudden change of load or external disturbances. The PI controller is used for controlling the outer DC-link voltage loop which requires a definite mathematical model of the system to determine controller gain values. However, due to the non-linearity of the system, precise mathematical modelling is not possible. Therefore, it is to design a simple and effective approach for tune the PI controller gain values under load perturbation conditions. An enhanced particle swarm optimization (EPSO) based interleaved shunt APF is depicted in this thesis to improve the dynamic performance of the system.

Author's contributions of the work are presented as follows:

1. Survey of PQ problems like harmonics, power factor, reactive power requirement, etc. in field to understand the level of harmonic pollution in the present distribution network.
2. Design, development and performance investigation of single-phase VSI based shunt APF under sinusoidal and distorted supply voltage conditions.
    - The implementation of Hilbert transforms based adaptive tuned filter for extraction of the fundamental frequency signal from the distorted supply voltage.
    - Unipolar hysteresis current controller is implemented to generate switching pulses for MOSFET switches of VSI based shunt APF.
    - A substantial simulation and experimental studies have been carried out to validate the suggested control technique under sinusoidal as well as under distorted supply voltage condition with the non-linear load. Various PQ events like THD, power factor, reactive power demand are observed before and after compensation.
3. Design and development of three-phase interleaved inverter based shunt APF
    - A three-phase interleaved shunt APF is designed and developed to overcome the problems of shoot-through phenomena along with PQ problems.

- Detailed simulation and experimental results have been carried out to evaluate the performance of the interleaved inverter based shunt APF with different supply voltage and/ or load conditions.

4. Design and implementation of multitudinal sliding mode controller for DC-link voltage regulation
    - A multitudinal sliding mode controller (MSMC) is suggested for DC-link voltage regulation with reduced steady-state error under mismatched uncertainties of load parameters.
    - A comparative study of PI, the conventional sliding mode controller and multitudinal sliding mode controller have been conducted to test the performance of the controller under different load conditions.
    - A considerable simulation and hardware results have been observed for different load conditions.
5. Implementation of enhanced particle swarm optimization for three-phase interleaved shunt APF
    - An enhanced particle optimization scheme have been designed and implemented to tune the PI controller gain values for the three-phase three-wire electrical system.
    - Extensive simulation and experimental studies have been conducted to test the performance of the presented controller algorithm under different load conditions in comparison with conventional PSO and PI controller.

1.5 Organization of Thesis

The whole work of the thesis is organized into seven chapters and each chapter briefly explained as follows:-

Chapter 1 depicts the concept of power quality, various PQ event in electrical distribution and transmission system, classical solutions and a comprehensive review on PQ which includes topological aspects, control techniques, artificial intelligence techniques and advanced PWM signal generation techniques.

A field survey is conducted and enumerated in **Chapter 2** to understand the various PQ in the modern power system network. The harmonic survey is carried out on lab premises which includes various lab equipment, rectifier load, various computer loads and lighting loads in the lab.

Chapter 3 presents the Hilbert transform based adaptive tuned filter for shunt APF. The control technique is divided into two parts: first associated with selected frequency signal extraction by using Hilbert transform based ATF from distorted supply voltage followed by reference current signal generation using DC-link energy balance method. Second deals with unipolar hysteresis current control technique which reduces switching ripple and switching frequency for VSI used as a shunt APF. A detailed simulation and experimental studies have been carried out to evaluate the performance of the presented control technique under sinusoidal as well as distorted supply voltage conditions.

Chapter 4 depicts the three-phase interleaved inverter based shunt APF to mitigate the current harmonics, the reactive power to improve the power factor and load unbalancing without shoot-through problems. Detailed simulation and experimental results are presented with different supply voltage and/ or load conditions.

Chapter 5 deals with the multitudinal sliding mode controller to stabilize the DC-link voltage with reduced steady-state error. The MSMC uses multiple surfaces for mismatched system disturbances/ uncertainties. Moreover, it uses to control the mismatched disturbances/uncertainties using inertial delay control (IDC). Hence, the DC-link voltage tracking capability is improved. Supportive simulation and hardware results have been presented in this chapter and compared with the PI and conventional SMC.

Chapter 6 presents the enhanced particle swarm optimization techniques to tune the PI controller gain values under uncertain conditions of load. This EPSO based control algorithm reduces the convergence time by eliminating the premature particle's best position and comprehends the computational complexity. Rigorous simulation studies have been conducted to validate the feasibility and effectiveness of the EPSO based control algorithm in comparison with conventional PI and PSO based control algorithms under the steady-state and transient condition of the load. The simulation results have been validated by implementing a prototype in the laboratory using a dSPACE1104 controller.

Chapter 7 depicts the general conclusions and important aspects of the work from the thesis. Further, this chapter presents some future directions for the research in the area of active power filters.

CHAPTER 2

HARMONIC SURVEY

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "Application of Shunt Active Power Filters in Medical Diagnosis and Critical Lab Equipment," in *Proc. of IEEE International Conference on Power and Embedded Drive Control (ICPEDC- 2017)*, SSN College of Engineering, Chennai, pp. 290-295, March, 2017.

CHAPTER 2

HARMONIC SURVEY

2.1 Introduction

The proliferation of power-electronic based equipment, nonlinear and unbalanced loads, has aggravated the power quality problems in the power distribution network. The quality of available AC mains has a direct impact on economics of any country. Therefore, the power quality has become a substantial subject both for end utilities as well as power suppliers in concern with the electric market. The power system network contains various industrial and commercial non-linear loads which are the main reason for the PQ issues. The power quality survey will help to identify various issues to initiate remedial action and develop standards for future survey which could define PQ trends. This PQ survey also help the electronic equipment designers to extrapolate the electrical parameter as per present trends and design future products which can withstand adverse situations.

2.2 Power Quality Survey

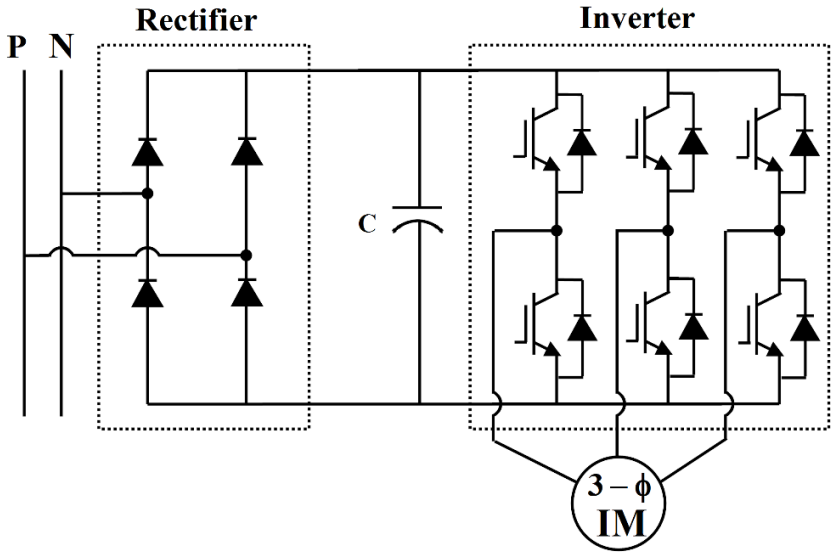
A PQ survey has been initiated to understand the existing level of harmonic pollution created by various equipment connected in the electrical power system. The harmonic survey has been conducted on various equipment such as computer loads, sensitive lab equipment, fluorescent lamps, etc.

2.2.1 Survey on Critical Lab Equipment

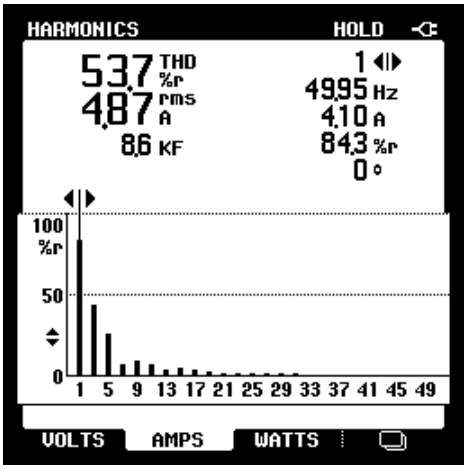
A survey has been conducted on various laboratory equipment in MNIT Jaipur to observe the various PQ events like current harmonics, reactive power burden, power factor, etc. The electrical engineering lab equipment such as rectifier load, induction motor drive system lab. The chemical engineering laboratory has contained dip-coater, magnetic stirrer, spin coating unit, refractive index analyzer, ultrasonicator and syringe pump. The harmonic study has been carried out to understand the harmonic injection level of these individual loads.

2.2.1.1 Variable Frequency Drive in the Laboratory

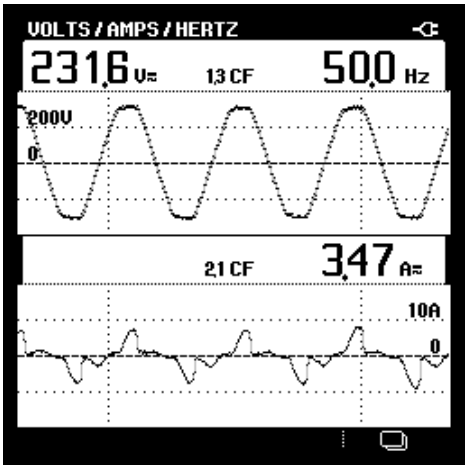
The variable frequency drives (VFD) consist of induction motor with power electronic converter system as shown in Figure 2.1 (a).



(a)



(b)



(c)

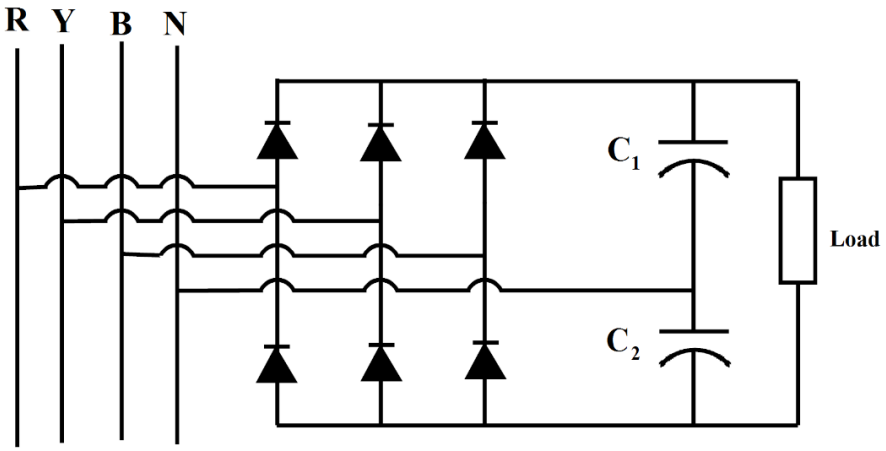
Figure 2.1 (a) Schematic diagram of variable frequency drive, (b) FFT spectrum of load current, and (c) Supply voltage and load current waveshape

These types of drives are commonly used in various industries for processing purposes. A harmonic survey has been conducted to investigate the harmonic power injected by variable frequency drive in the laboratory. The harmonic spectral analysis waveform and, line side of supply voltage and distorted currents are shown in Figure 2.1 (b) and (c),

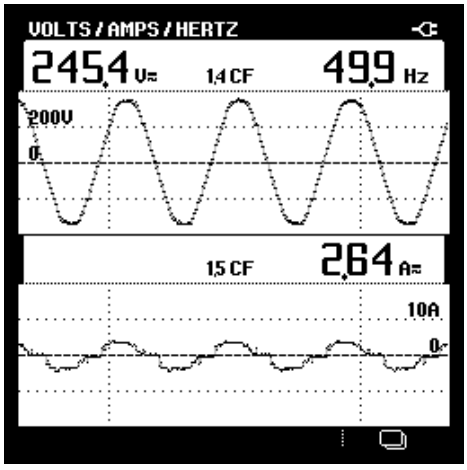
respectively. This particular VFD used a PWM switching scheme to control the speed of drive by varying the voltage and frequency of inverter output. The PWM output of the VFD is a noisy voltage waveform which contents lower order harmonics into the system. The single phase power analyzer captured this phenomenon for the voltage and current waveforms with the harmonic inject levels into the system.

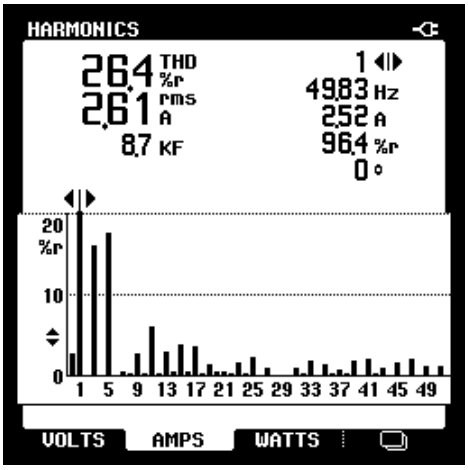
2.2.1.2 Rectifier Load

Figure 2.2 (a) shows the schematic diagram of single-phase rectifier with capacitor filter. The basic work of rectifier is to convert alternating current (AC) into direct current (DC).



(a)





(b) (c)

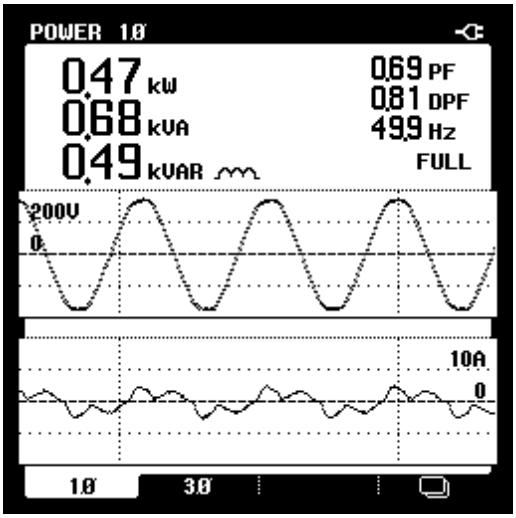
Figure 2.2 (a) Schematic diagram of three-phase rectifier, (b) Phase 'A' supply voltage and source current waveforms, and (c) Harmonic spectrum of phase-a source current

The rectifiers are commonly used in many appliances from small to high power equipment like mobile battery chargers, HVDC transmission system, electric traction system, telecommunication system, etc. The rectifiers are being implemented by using power diodes where its operation has inherent nonlinear characteristics. Due to its nonlinear nature, it injects large amount of harmonic contents into the power system network. The presence of harmonics in the electrical power absorbed leads on the electrical power loss and, in addition, the harmonics of an odd multiple of three causes additional load to the neutral conductor of the three-phase low-voltage system. The survey was conducted on the rectifier load in the power electronics laboratory in the electrical engineering department in the MNIT Jaipur. The input side of the rectifier is connected to three-phase AC supply, the generated DC output voltage rating of this rectifier is 220 V and 10 A. Figure 2.2 (b) shows the phase 'A' supply voltage waveform and source current. The harmonic spectrum of source current is shown in Figure 2.2 (c). The total harmonic distortion is recorded as 26.4% which shows the significant amount of pollution is injecting by this rectifier load.

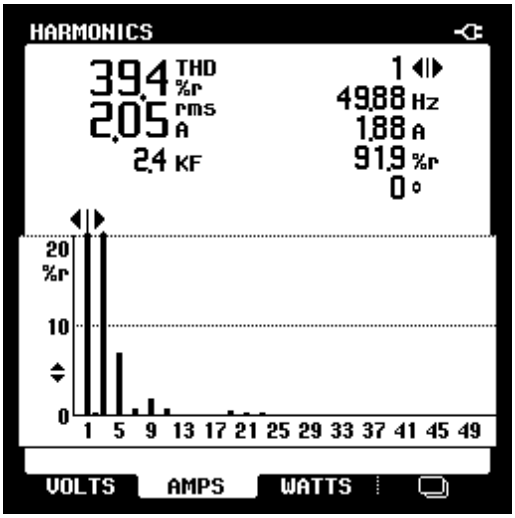
2.2.1.3 Dip-Coater

The dip-coater is designed to deposit a layer of materials in a controlled and repeatable manner. It has been designed to minimize the operator's effort. The variables like speed, duration, etc. are maintained accurately by computer control. The dip-coating process includes five stages: immersion, start-up, deposition, evaporation and drainage. The coating thickness depends on various parameters like the viscosity of the coating solution, immersion time, withdrawal speed, evaporation rate etc. Adjustable stroke length and accurate speed control are the exceptional features of this model along with its capability of achieving a uniform coating. A microprocessor-based system along with user-friendly software takes care of accurate control throughout the process. The dip-coater produces harmonic currents into the system due to the servo speed control unit in the machine. Figure 2.3 (a) shows the dip-coater machine in the laboratory. Supply voltage and load current along with active, reactive, apparent power and lagging power factor measurement is shown in Figure 2.3 (b). The harmonic spectrum has recorded as 39.4% as shown in Figure 2.3 (c). It is observed from the Figure 2.3 (c) that the equipment is injecting dominant odd harmonic contents into the system.

(a)



(b)



(c)

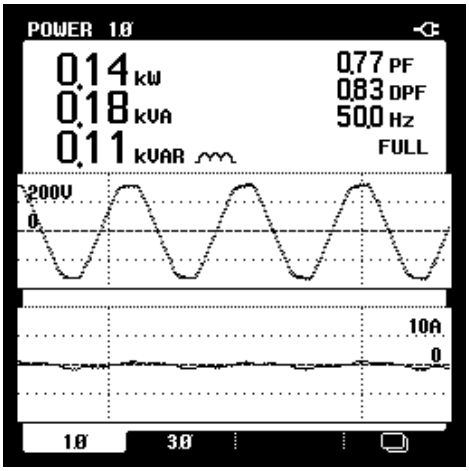
Figure 2.3 (a) Dip-coater, (b) Supply voltage and current waveform, and (c) Harmonic spectral of load current

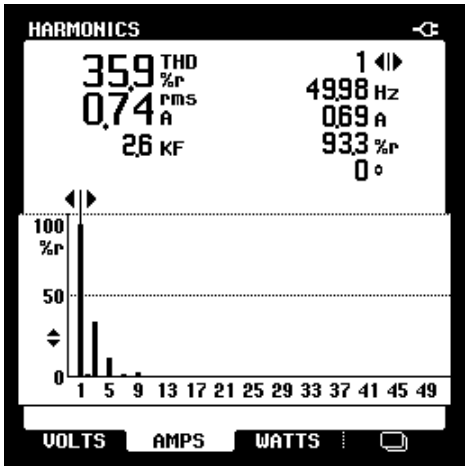
2.2.1.4 Magnetic Stirrer

The laboratory magnetic stirrer is shown in Figure 2.4 (a), which is used for mixing the solutions. A micromotor drives the magnet to generate rotating magnetic field to stir the stirring bar in the vessel, making a solution conduct completely mixed reaction, stirring speed is adjustable, widely applies to solvent stirring in different viscosity. The supply voltage and current waveforms along with power measurements are shown in Figure 2.4 (b). It is observed from Figure 2.4 (b) that due to the magnet and micro motor control

electronic devices used in the machine, it has drawn reactive power which leads to a lagging power factor of 0.77. The FFT spectrum of load current is shown in Figure 2.4 (c).

(a)





(b) (c)

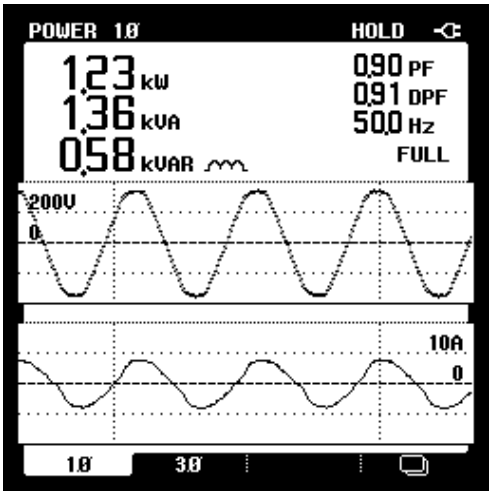
Figure 2.4 (a) Magnetic stirrer, (b) Phase voltage and current waveforms, and (c) FFT analysis of load current waveform

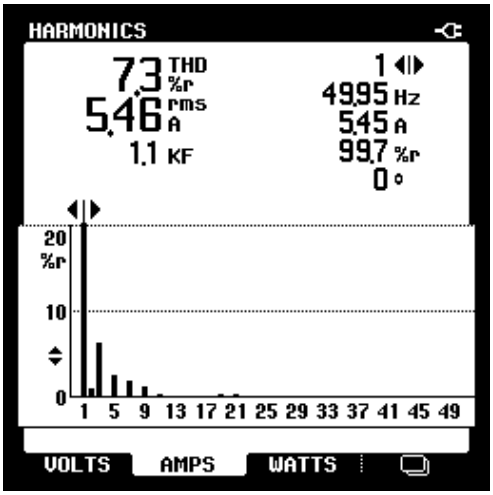
2.2.1.5 Spin Coating Unit

Spin coater is a dedicated tabletop system to spin coat small substrates in research laboratories with well-controlled spin process parameters. The spin coating machine is shown in Figure 2.5 (a) which has the high speed, and duration range allows the user to achieve the desired thickness or thinness of the film. The spin head actuator is a precision DC servo motor, which requires less maintenance, with accurate speed and acceleration control. A vacuum chuck powered by oil-less vacuum pump holds the substrate at the

spinning head. The combined supply voltage and load current waveforms are shown in Figure 2.5 (b) with injected harmonic spectrum is shown in Figure 2.5 (c). It is observed that it is injecting small significant amount of harmonics with violate the IEEE-519 standard.

(a)



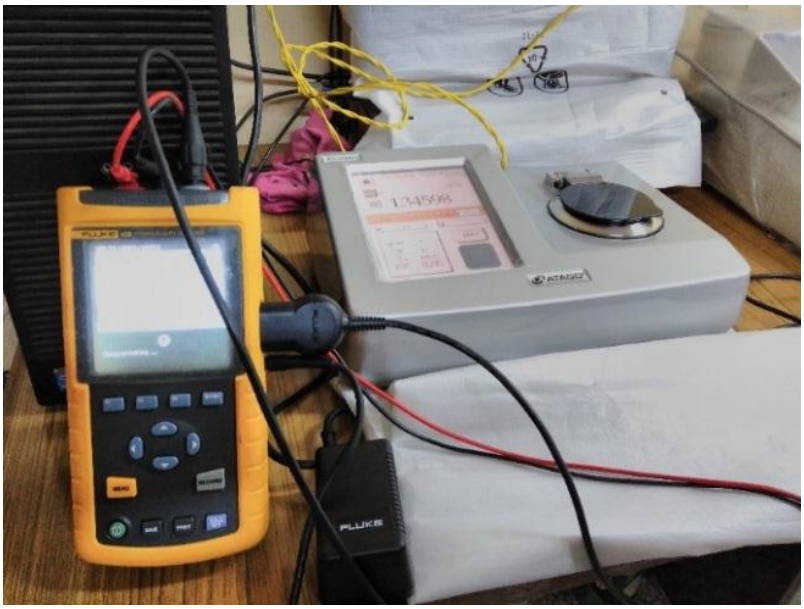


(b) (c)

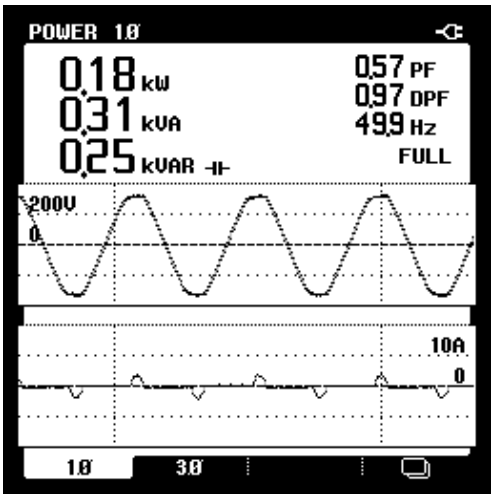
Figure 2.5 (a) Spin coating unit, (b) Phase voltage and current drawn by the spin coating unit, and (c) Harmonic spectrum of load current

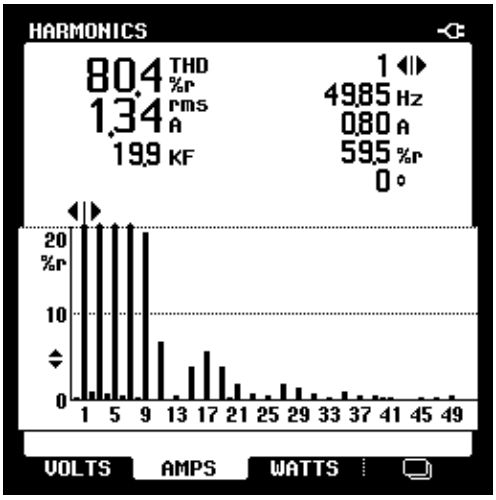
2.2.1.6 Refractive Index Analyzer

The refractive index analyzer is used in the laboratory for measurement of refractive index of various composite materials. The automatic refractive analyzer is shown in Figure 2.6 (a).



(a)





(b) (c)

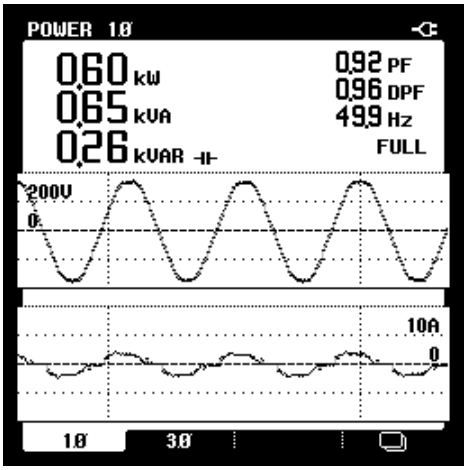
Figure 2.6 (a) Refractive index analyzer, (b) Supply voltage and load current waveforms, and (c) FFT spectral diagram

It contains an LED lighting system which is focused on prism surface via lens system. This automatic machine also contains microprocessor-controlled electronic devices. Hence, it injects the current harmonics and draw reactive power from the electrical system. The voltage and distorted current waveforms are shown in Figure 2.6 (b) with lagging power power factor of 0.57. The refractive index analyzer is injecting more triple harmonic contents into the system which are recorded as 80.4% as shown in Figure 2.6 (c). It is shown that there is huge harmonic pollution is created by refractive index analyzer.

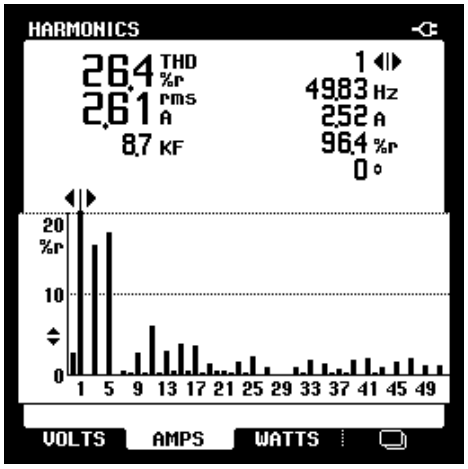
2.2.1.7 Ultrasonicator

An ultrasonicator system as shown in Figure 2.7 (a) is comprised of 3 major components: generator, converter and horn (also known as a probe).

(a)



(b)



(c)

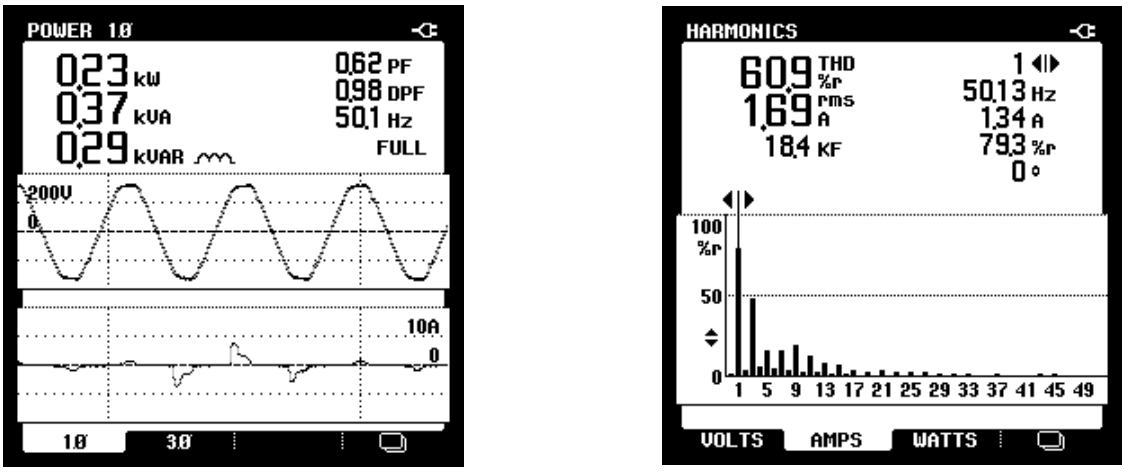
Figure 2.7 (a) Ultrasonicator instrument, (b) Supply voltage and load current waveforms, and (c) Harmonic spectrum of load current

The ultrasonic electronic generator transforms AC line power to high-frequency electrical energy. The generator features a keypad or buttons which allow the user to control the sonication parameters. The generator provides high voltage pulses of energy at a frequency of 20 kHz that drives a piezoelectric converter. The converter is a cylindrical

device which is connected to the generator by a high voltage cable. The converter transforms electrical energy to mechanical vibration due to the characteristics of the internal piezoelectric crystals. The supply voltage and load current behavior is shown in Figure 2.7 (b) which shows that the ultrasonicator pollute the system by injecting the more odd harmonic components which deviates the source current profile. The harmonic spectrum of load current is shown in Figure 2.7 (c) which has 5th dominant harmonic component compared to 3rd harmonic component.

2.2.1.8 Syringe Pump

A syringe pump is a small, positive-displacement pump used for gradually transfer precise volumes of fluid. The chemyx fusion series syringe pumps are all driven via a stepper motor. A lead screw, threaded through a pusher block, precisely turns the pump's stepper motor. This causes the pusher block to move.



(a) (b)

Figure 2.8 (a) Syringe pump load profile, and (c) Frequency spectrum of load current

The fluid ejects at an accurate and precise rate during infusion mode, when the pusher block pushes against the plunger of a secured syringe. When the stepper motor turns in the opposite direction, the pusher block moves such that the syringe plunger is pulled, thus drawing fluid into the syringe. The supply voltage and distorted currents with power measurements are shown in Figure 2.8 (a). The FFT analysis of load current of syringe pump is shown in Figure 2.8 (b). It concluded from the Figure 2.8 (a) and (b) that the syringe pump had injected more dominant odd harmonics into the system.

2.2.2 Survey on Residential and Commercial Loads

The power electronic equipment is playing a significant role in the home appliances like LED lighting systems, computer loads, etc. The sophisticated life style increases the use of these type of electronic equipment in various commercial and residential buildings. It is necessary to analyse the behaviour of the injected harmonic currents in the system. Further, these studies help to maintain the power quality of the distribution system. The harmonic pattern of the various appliances of home and laboratory have been conducted in the following sections.

2.2.2.1 Lighting System

The energy-efficient lighting system technology is increasing day by day due to rapid advancement in the power electronic technology. The PQ is a significant consideration at the utility end, but with the advent of LEDs, Compact Fluorescent Lighting (CFL), High-Intensity Discharge (HID) lighting and others, the obligation to an efficient power distribution system is essential than ever. Many new lighting technologies certainly efficient and adversely affect power systems by injecting the harmonics. This poor PQ may limit the number of devices that can be placed on the distribution network. Poor PQ management inevitably leads to an increase in operational costs and places an unnecessary strain on already dwindling resources. Therefore, lighting systems should be driven by efficient and sustainable power sources that will not unnecessarily burden the power grid while still providing the perfect electrical environment for advanced lighting systems.

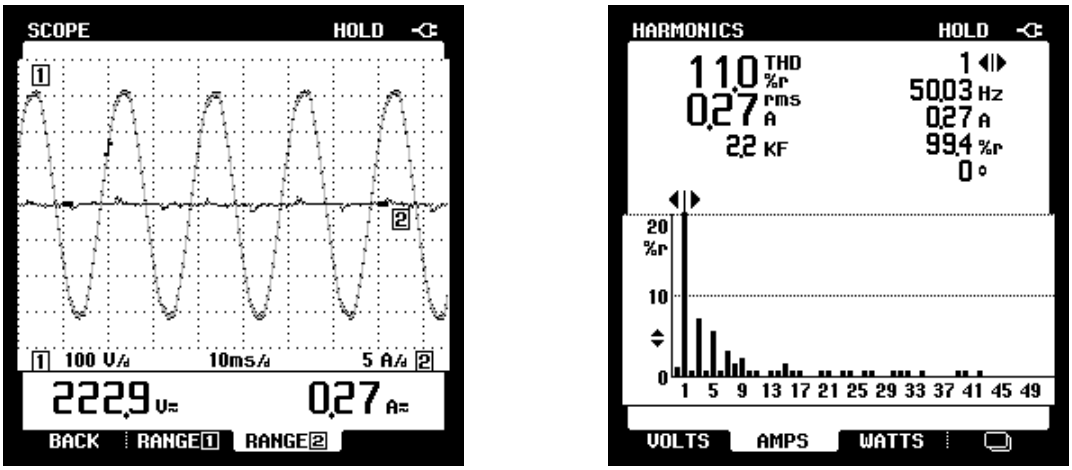


Figure 2.9 Harmonic analysis of LED lighting system

There are economic impacts on utilities, their customers and suppliers of load equipment. The harmonic survey has been conducted on various lighting equipment such as LED lighting system, fluorescent lamp and CFL are shown in Figure 2.9 to 2.11, respectively. This lighting system uses electronic ballasts which are capacitive nature to regulate the voltage levels. Hence, it injects a significant amount of harmonics into the system.

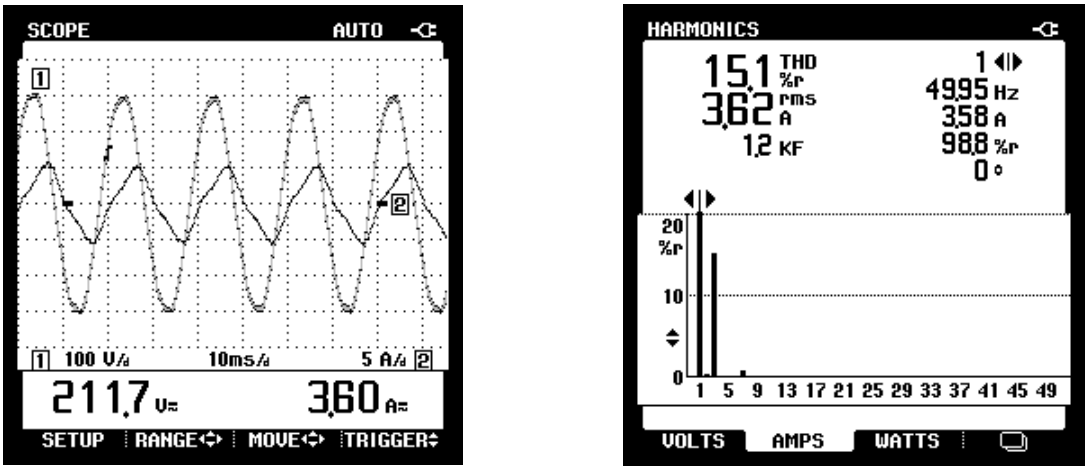


Figure 2.10 Harmonic analysis of Fluorescent lamp

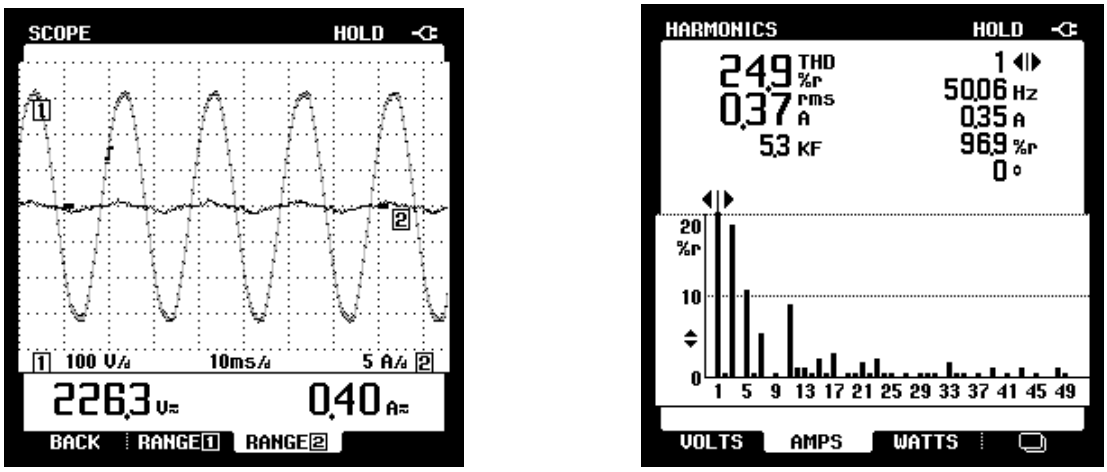
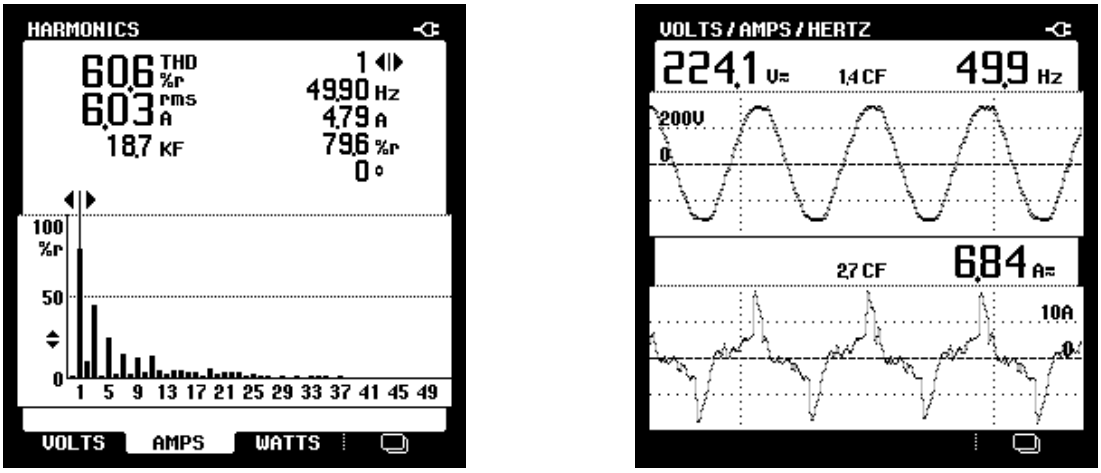


Figure 2.11 Harmonic analysis of CFL

2.2.2.2 Computer Load

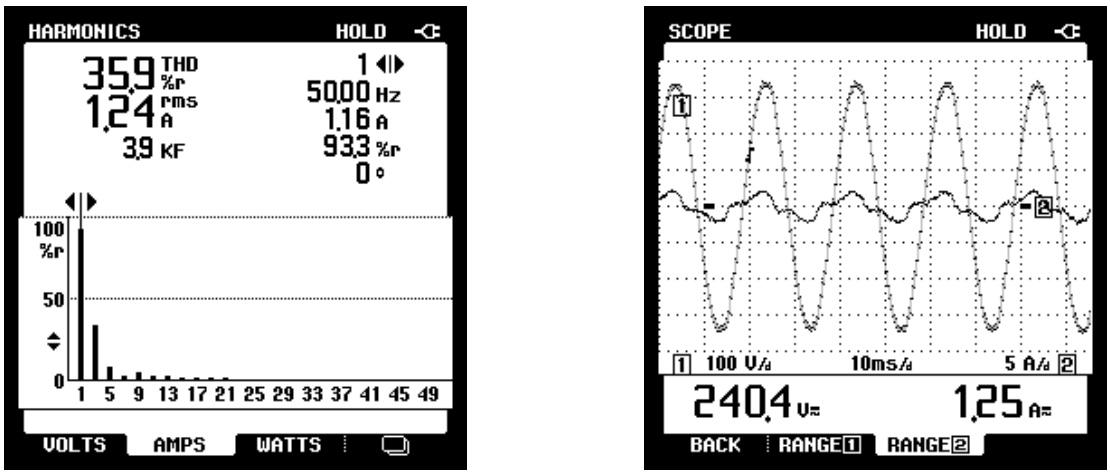
The computer loads are becoming more prominent user in all industries, commercial, educational and residential purposes. These computers are having switched mode power supplies (SMPS) which distort the waveform of supply current by injecting harmonic currents into the system. The harmonic survey has been conducted in the computer load.

The load current harmonic spectrum graph of computer system is shown in Figure 2.12 (a), where the supply voltage waveshape and the distorted load current is shown in Figure 2.12 (b). It is observed from these figures that significant amount of odd harmonics including dominant triple harmonic components are present in the load currents. The laptops are the most commonly used nonlinear loads in commercial and residential applications in the present scenario. These laptops tend to have high current distortion levels due use of high-speed processors which consists of numerous transistors, battery charger and LED display. The harmonic spectrum of the load current, the supply voltage and the distorted load current profiles are shown in Figure 2.13 (a) and (b), respectively. It is observed that the injection of harmonic is severe.



(a) (b)

Figure 2.12 Harmonic analysis of computer load (a) FFT spectrum, and (b) Supply voltage and load current



(a) (b)

Figure 2.13 Harmonic analysis of laptop (a) FFT spectrum, and (b) Supply voltage and load current

Table 2.1

Harmonic profile of residential loads

S. No	Equipment	Current (A)	%THD	Power factor	Reactive power drawn (kVAR)
1.	Dip-Coater	2.05	39.4	0.69	0.49
2.	Magnetic Stirrer	0.74	35.9	0.77	0.11
3.	Spin Coating Unit	5.46	7.3	0.90	0.58
4.	Refractive Index Analyzer	1.34	80.4	0.57	0.25
5.	Ultrasonicator	2.61	26.4	0.92	0.26
6.	Syringe Pump	1.69	60.9	0.62	0.29
7.	Wet Grinder	0.80	9.0	0.74	0.13
8.	LED light	0.27	11.0	0.9	0.02
9.	Fluorescent Lamp	3.62	15.1	0.95	0.07
10.	Compact fluorescent lamp (CFL)	0.37	24.9	0.87	0.43
11.	Computer load	6.03	60.6	0.70	1.09
12	Laptop	1.25	35.9	0.9	0.11

2.3 Conclusion

A harmonic survey has been conducted on various lab and home appliances. The voltage and current distortions levels also presented to effectively analyze the behaviour of harmonics in the power system network. A detailed harmonic survey has been tabulated in table 2.1. It is clear from the survey that the proliferation of harmonics is having an observable impact on the other linear loads which are connected at the POI. The harmonic voltage and current mitigation techniques are broadly discussed in the following sections.

CHAPTER 3

HILBERT TRANSFORM BASED ADAPTIVE TUNED FILTER FOR SHUNT APF

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Single-Phase Shunt APF to Mitigate Current Harmonics and Switching Frequency Problems under Distorted Supply Voltage," *IETE Journal of Research*, Taylor & Francis Publications, Nov. 2018.
   DOI: https://doi.org/10.1080/03772063.2018.1542351

CHAPTER 3

HILBERT TRANSFORM BASED ADAPTIVE TUNED FILTER FOR SHUNT APF

3.1 Introduction

The reference current generation techniques play a significant role in the harmonic compensation performed by shunt APF. The modern power system network is polluted significantly due to interconnection of various non-linear loads. The literature is enriched with various control techniques which classified into two categories, time-domain and frequency domain. The frequency-domain techniques depend on the FFT process which is accurate in calculating the individual and multiple harmonic components. However, these frequency-domain techniques have disadvantages like sluggish response, complex calculations, etc. [62]. In contrary, the time-domain techniques are fast and simple to implement in real-time applications. There are many time-domain control techniques like IRPT, synchronous reference frame theory, Fryze power theory, etc. These control techniques give immense results under the balanced supply and load conditions [87-88]. However, the practical power system network has been connected with various types of linear and non-linear loads which distort the source current as well as supply voltage. Hence, conventional reference current generation techniques give adequate results under these supply and load conditions [108].

To address these issues, the researchers have introduced PLL based control techniques. This PLL block is used to extract the unit template from the distorted voltage signal in synchronism with the grid [100]. However, the tuning of the PLL gain parameters is a big challenge. Various PLL-less systems are recommended in the literature to overcome the drawbacks of PLL [102-104]. Song et al. [105] have developed STF to extract a selected frequency component from the distorted supply voltage. Later, many researchers have applied this technique in different topology of single-phase and three-phase APF. This technique requires more number of sensors to detect grid voltage conditions accurately which increases the cost. Hence, the detection of grid voltage conditions, sensor

requirement, gain selection and transient response of tuned filter are the main challenges for designing the control technique [104].

To overcome the aforementioned challenges, a Hilbert transform based ATF is implemented for extracting the fundamental component of voltage signal from the distorted signal without phase delay in this chapter. Further, the reference current generation is estimated by using DC-link energy balance theorem to control the shunt active power filter under the sinusoidal and distorted supply voltage conditions.

Various PWM techniques are proposed for switching pulse generation of VSI such as hysteresis current controller sinusoidal PWM, triangular current controller, SVM and hysteresis current controller. Single band hysteresis current controller attracts researchers due to its simple structure and easy execution. However, SBHCC has disadvantages like higher switching losses due to higher switching frequency at lower modulation index [142]. These SBHCC problems are overcome by unipolar hysteresis current controller switching scheme. Detailed simulation and experimental study have been carried out to test the performance of the modified control scheme.

3.2 Principle of Single-Phase Shunt APF

3.2.1 Basic Compensation Principle

The basic principle of active compensation by using active power filters was proposed during 1970s. However, the actual design of active power line conditioner was proposed by Gyugyi and Strycula in 1976 [31]. The shunt APF is a voltage source inverter and connected in parallel to the grid at PCC through interfacing inductors. An energy storage DC-link capacitor is presented at the DC side of VSI. It operates as a current source injecting the harmonic components generated by the load but phase shifted by 180º. As a result, components of harmonic currents in the load current are cancelled by the effect of the shunt APF and the source current retains to sinusoidal and in phase with the respective voltage.

3.2.2 Characteristics of harmonics

The electrical power system has been polluted due to massive use of non-linear loads. The system voltage and currents are affected and contain different levels of harmonics. The electronic loads generate positive and negative sequence as well as zero sequence

harmonic currents. The Fourier series represents an effective way to study and analyze the harmonic distortion [108].

The Fourier series analysis as follows:

$$\begin{aligned} f(t) &= r_0 + \sum_{n=1}^{\infty} [r_n \cos(n\omega t) + b_h \sin(n\omega t)] \\ &= r_0 + \sum_{n=1}^{\infty} [d_n \sin(n\omega t) + \phi] \end{aligned} \tag{3.1}$$

Where,

$f(t)$- periodic function of frequency f; $2\pi f$ - angular frequency period; T = $2\pi/\omega$- time period; d_n - n^{th} harmonic of amplitude; ϕ - phase;

$$r_0 = \frac{1}{\mathrm{T}} \int_0^T f(\mathrm{t})\, \mathrm{dt} = \frac{1}{2\pi} \int_0^{2\pi} f(t) dx, where\ x = \omega t \tag{3.2}$$

$$r_h = \frac{2}{T} \int_0^T f(t) \cos(n\omega t) dt = \frac{1}{\pi} \int_0^{2\pi} f(t) \cos(nx) dx \tag{3.3}$$

$$b_h = \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt = \frac{1}{\pi} \int_0^T f(t) \sin(nx) dx \tag{3.4}$$

$$d_h = \sqrt{r_h^2 + b_h^2} \ \text{ and } \phi = \tan^{-1}\left(\frac{r_h}{b_h}\right) \tag{3.5}$$

The distorted periodic current or voltage waveform expanded by Fourier series as follows:

$$I(t) = \sum_{n=1}^{\infty} I_n \cos(n\omega t + \varphi_h) \tag{3.6}$$

$$V(t) = \sum_{n=1}^{\infty} V_n \cos(n\omega t + \theta_n) \tag{3.7}$$

Where,

I_n –n^{th} harmonic peak current, φ_n is the n^{th} harmonic current

V_n –n^{th} harmonic peak voltage, θ_n is the n^{th} harmonic voltage

ω-angular frequency $\omega = 2\pi f$, f is the fundamental frequency

3.3 Design and Analysis of Control Algorithm

In this section, design and analysis of Hilbert transform based ATF is presented for extraction of fundamental component of voltage signal from the distorted voltage signal.

3.3.1 Hilbert Transform based Adaptive Tuned Filter

The Hilbert transform based ATF effectively works to extract fundamental component from the distorted supply voltage to generate a unit template with grid synchronizing without phase delay. In this method, first, single-phase distorted supply voltage is converted into two signals with 90° phase difference by Hilbert transform function. The distorted supply voltage signal has a fundamental component and a harmonic component of supply voltage signals. Secondly, these Hilbert transform output signals will be processed in the ATF for extracting the tuned frequency (ω_f) signal from a group of frequencies. The Hilbert transform is a linear filter which shifts the phases of all frequency components of the input signals by -90^0. The definition of the Hilbert transfer function is as follows:

$$H\{x(t)\} = \frac{-1}{\pi} P \int_{-\infty}^{\infty} \frac{x(\lambda)}{\lambda - t} d\lambda = \frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{x(\lambda)}{t - \lambda} d\lambda \tag{3.8}$$

Where, $H\{x(t)\}$ is the Hilbert transform and P is the Cauchy principal value of integral. Eq. (3.8) can be used for getting quadrature signal of input signal. The input signal is as follows:

$$v_s = v_\alpha = x(t) = V_m \sin(\omega t) \tag{3.9}$$

Where, v_s is the RMS value of the supply voltage and V_m is the peak value of supply voltage. By applying the Hilbert transformation in Eq. (3.9):

$$H\{V_m \sin\omega t\} = \frac{-1}{\pi} V_m P \int_{-\infty}^{\infty} \frac{\sin\omega\lambda}{\lambda - t} d\lambda \tag{3.10}$$

Let $\lambda - t = z$,

$$H\{V_m \sin\omega t\} = \frac{-1}{\pi} V_m P \int_{-\infty}^{\infty} \frac{\sin\omega(z+t)}{z} dz \tag{3.11}$$

$$= \frac{-1}{\pi} V_m P \int_{-\infty}^{\infty} \frac{\sin\omega z.\cos\omega t + \sin\omega t.\cos\omega z}{z} dz \tag{3.12}$$

$$= -\frac{1}{\pi} V_m P \int_{-\infty}^{\infty} \frac{\sin\omega z.\cos\omega t}{z} dz - \frac{1}{\pi} V_m P \int_{-\infty}^{\infty} \frac{\sin\omega t.\cos\omega z}{z} dz$$

$$= -\frac{1}{\pi} V_m \cos\omega t . P\int_{-\infty}^{\infty} \frac{\sin\omega z}{z} dz - \frac{1}{\pi} V_m \sin\omega t . P\int_{-\infty}^{\infty} \frac{\cos\omega z}{z} dz$$

$$= -V_m \cos\omega t \qquad (3.13)$$

Since, $\frac{\cos\omega z}{z}$ is an odd function hence, its value will become zero and the convergent integration of $P\int_{-\infty}^{\infty} \frac{\sin\omega z}{z} dz$ is π.

It is observed from Eq. (3.13) that, the output signal of the Hilbert transform function is in quadrature and lagging with the input signal. These two signals further process in ATF for extracting selected frequency component.

3.3.1.1 Selected Frequency Extraction using ATF

The selected fundamental frequency extraction from distorted supply voltage is achieved by Hilbert transform based ATF. This approach is to extract the fundamental component of voltage from distorted supply voltage with better tuning and synchronization. The distorted supply voltage has different frequency components. The transformation of selected frequency extraction filter is as follows:

$$TF(s) = \frac{V_p(s)}{U_k(s)} = \frac{s + j\omega}{s^2 + \omega^2} \qquad (3.14)$$

Where $V_p(s)$ and $U_k(s)$ are the input and output of the ATF respectively. The impulse response of above transfer function can be written by using inverse Laplace transform is:

$$h(t) = \cos\omega t + j\sin\omega t = e^{j\omega t} \qquad (3.15)$$

It is clear from Eq. (3.15) that the adaptive tuned filter is a function of complex coefficient, which is the combination of sine and cosine. These two signals are taken from Eq. (3.9) and Eq. (3.13) as input of ATF. The mathematical derivation of the modified ATF is based on stationary and synchronously rotating reference frame concept. Introducing the gain factor (k) in ATF transfer function (TF) to get a fine cut-off frequency ω_f. The ATF passes the required frequency ω_f signal and stops the unwanted signals with a minimum phase delay. The Eq. (3.14) can be written by introducing gain factor k as follows:

$$TF(s) = k\frac{(s+k)+j\omega_f}{(s+k)^2+\omega_f^2} \tag{3.16}$$

Let, v_α, v_β and $\bar{v}_\alpha$, $\bar{v}_\beta$ are the input and output of ATF, respectively. The transfer function can be written as follows:

$$TF^k(s) = \frac{\overline{v_\alpha}(s)+j\overline{v_\beta}(s)}{v_\alpha(s)+jv_\beta(s)} \tag{3.17}$$

Equating Eq. (3.16) and Eq. (3.17) to obtain selected frequency components,

$$k\frac{(s+k)+j\omega_f}{(s+k)^2+\omega_f^2} = \frac{\bar{v}_\alpha(s)+j\bar{v}_\beta(s)}{v_\alpha(s)+jv_\beta(s)}$$

$$(k[(s+k)+j\omega_f)]*[v_\alpha(s)+jv_\beta(s)]) = ([(s+k)^2+\omega_f^2]*[\bar{v}_\alpha(s)+j\bar{v}_\beta(s)])$$

$$\left.\begin{aligned} &k(s+k)v_\alpha(s)+jk(s+k)v_\beta(s)+jk\omega_f v_\alpha(s)-\omega_f k v_\beta(s) \\ &=(s+k)^2\bar{v}_\alpha(s)+j(s+k)^2\bar{v}_\beta(s)+\omega_f^2\bar{v}_\alpha(s)+j\omega_f^2\bar{v}_\beta(s) \end{aligned}\right\}$$

$$\left.\begin{aligned} &k.(s+k).v_\alpha(s)-\omega_f.k.v_\beta(s)-(s+k)^2.\bar{v}_\alpha(s)-\bar{v}_\alpha(s).\omega_f^2 \\ &=j*[\bar{v}_\beta(s).(s+k)^2+.\omega_f^2.\bar{v}_\beta - k.v_\beta(s).(s+k)+k.\omega_f.v_\alpha(s)] \end{aligned}\right\} \tag{3.18}$$

By separating the real and imaginary parts from above Eq. (3.18), it simplifies as follows:

$$[(s+k)^2+\omega_f^2]\bar{v}_\alpha(s) = k(s+k).v_\alpha(s)-k.\omega_f.v_\beta(s)$$

$$\bar{v}_\beta(s)[(s+k)^2+\omega_f^2] = k.v_\beta(s).(s+k)+k.\omega_f.v_\alpha(s)$$

$$\bar{v}_\alpha(s) = \frac{k.(s+k)}{(s+k)^2+\omega_f^2}.v_\alpha(s)-\frac{k.\omega_f}{(s+k)^2+\omega_f^2}.v_\beta(s) \tag{3.19}$$

$$\bar{v}_\beta(s) = \frac{k.(s+k)}{(s+k)^2+\omega_f^2}.v_\beta(s)+\frac{k.\omega_f}{(s+k)^2+\omega_f^2}.v_\alpha(s) \tag{3.20}$$

By further simplifying above Eq. (3.19) and Eq. (3.20) can be expressed as follows:

$$\bar{v}_\alpha(s) = \frac{k}{s}[v_\alpha(s)-\bar{v}_\alpha(s)]-\frac{\omega_f}{s}.\bar{v}_\beta(s) \tag{3.21}$$

$$\bar{v}_\beta(s) = \frac{k}{s}[v_\beta(s)-\bar{v}_\beta(s)]-\frac{\omega_f}{s}.\bar{v}_\alpha(s) \tag{3.22}$$

The above Eq. (3.21) and Eq. (3.22) are the tuned frequency voltage components with grid frequency. The block diagram of the Hilbert transform based ATF has shown in Figure 3.1 This method can work effectively over conventional LPF by maintaining zero phase delay.

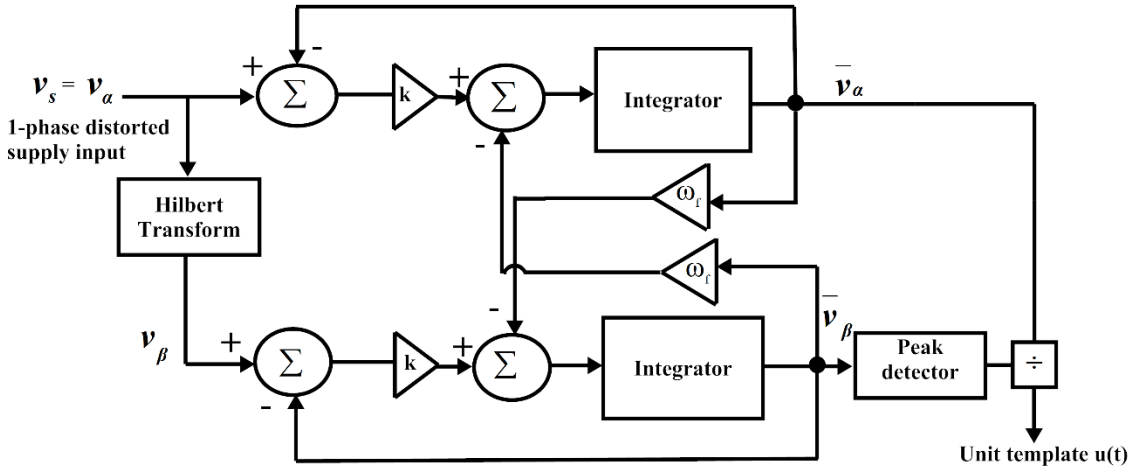


Figure 3.1 Block diagram of Hilbert transform based ATF for fundamental signal extraction

3.3.1.2 Bode Diagram and Stability Criteria

The stability analysis of the Hilbert transform based ATF control technique can be analyzed by using bode-diagram. The bode-diagram is plotted as per Eq. (3.16) for different gain parameters of controller transfer function.

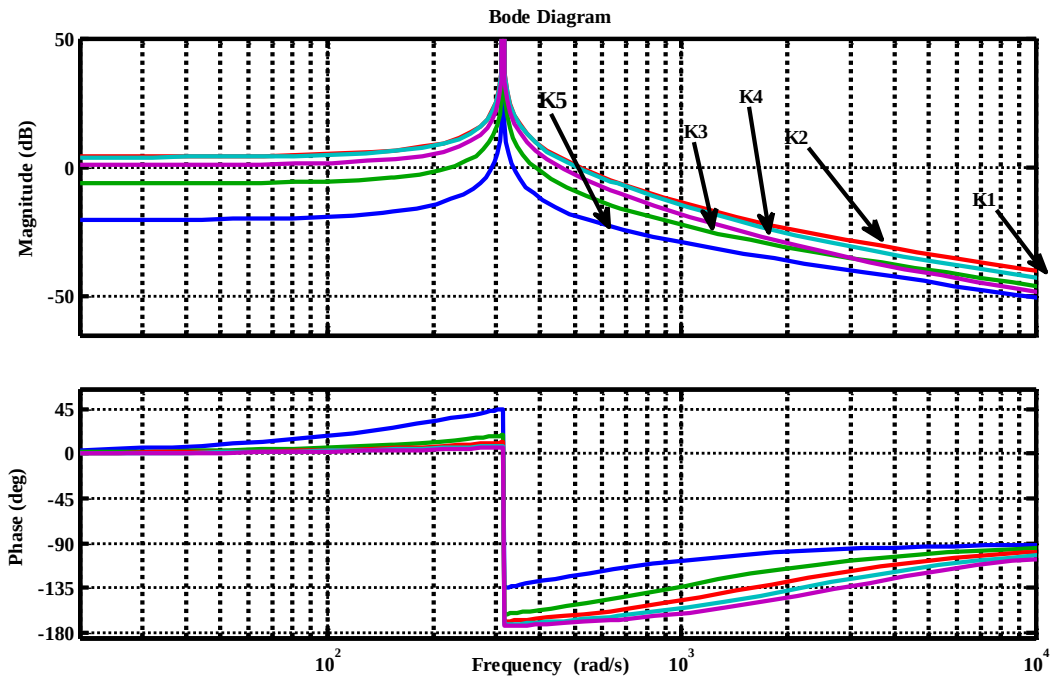


Figure 3.2 Bode plot of Hilbert transform based ATF for different values of gain k

According to bode plot as shown in Figure 3.2, increase in the phase margin, improves the response of the system with less overshoot and ringing. The %overshoot and %undershoot for different gain values are tabulated in Table 3.1. Therefore, phase margin is chosen 68º for the optimum gain of 30 (k_4) from Table 3.1 which gives better response and minimum distortions in the extracted fundamental supply voltage component.

Table 3.1

Effect of gain parameters on performance

The gain values	%Overshoot	%Undershoot
k_1=100	14.6	6.8
k_2=70	12.3	5.2
k_3=50	10.5	2.3
k_4=30	3.7	4.1
k_5=20	8.9	10.5

3.3.2 Reference Current Generation Technique

The reference current generation techniques play a substantial role in the harmonic compensation performance using shunt APF.

3.3.2.1 Characteristics of Harmonic Compensation

The instantaneous load current can be calculated as follows:

$$\begin{aligned} i_{Load}(t) &= I_{Lm}\sin(\omega t)*\cos(\varphi_{Lm}) + I_{Lm}\cos(\omega t)*\sin(\varphi_{Lm}) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_h) \\ &= i_{Lmp}(t) + i_{Lmq}(t) + i_{Ln}(t) \end{aligned} \tag{3.23}$$

Where, I_{Lm}, I_n and φ_{Lm}, φ_n are the peak values of fundamental, harmonic component of load current, and phase angles, respectively. The load current as shown in Eq. (3.23) has three major components, active $i_{Lmp}(t)$, reactive $i_{Lmq}(t)$ and harmonic $i_{Ln}(t)$ components of load currents respectively. The DC-link energy balance theorem has to detect the harmonics present in the system and generate required error signal for hysteresis current controller to control the flow of compensation through VSI based shunt APF [13]. The harmonic component of current (i_c) which has to inject by shunt APF is as follows:

$$i_c(t) = -[i_{Lmq}(t) + i_{Ln}(t)] \tag{3.24}$$

The load power can be calculated as follows:

$$P_{Load}(t) = v_s(t) * i_{Load}(t) \tag{3.25}$$

$$= \underbrace{V_m \sin(\omega t)}_{v_S} * \underbrace{\left\{ \begin{array}{l} I_{Lm}\sin(\omega t) * \cos(\varphi_{Lm}) + I_{Lm}\cos(\omega t) * \sin(\varphi_{Lm}) \\ + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_h) \end{array} \right\}}_{i_{Load}} \tag{3.26}$$

$$\begin{aligned} &= V_m \sin(\omega t) * I_{Lm}\sin(\omega t) * \cos(\varphi_{Lm}) + V_m \sin(\omega t) * I_{Lm}\cos(\omega t) * \sin(\varphi_{Lm}) \\ &\quad + V_m \sin(\omega t) * \sum_{n=2}^{\infty} I_n \sin(h\omega t + \varphi_h) \end{aligned} \tag{3.27}$$

$$\begin{aligned} &= V_m I_{Lm} \sin^2(\omega t) * \cos(\varphi_{Lm}) + V_m I_{Lm} \sin(\omega t) * \cos(\omega t) * \sin(\varphi_{Lm}) \\ &\quad + V_m \sin(\omega t) * \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_h) \end{aligned} \tag{3.28}$$

$$\begin{aligned} &= \underbrace{V_m I_{Lm} \sin^2(\omega t) * \cos(\varphi_{Lm})}_{P_{Real}} + \underbrace{V_m I_{Lm} * \sin(\omega t) * \cos(\omega t) * \sin(\varphi_{Lm})}_{Q_{Real}} \\ &\quad + \underbrace{V_m \sin(\omega t) * \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_h)}_{P_{Harmonic}} \end{aligned} \tag{3.29}$$

$$P_{Load}(t) = P_{Real}(t) + Q_{Reactive}(t) + P_{Harmonic}(t) \tag{3.30}$$

Where, $P_{Real}(t)$ is the real power, $Q_{Reactive}(t)$ and $P_{Harmonic}(t)$ are the reactive and harmonic component power of load, respectively. The shunt APF supplies sufficient amount of the reactive and harmonic component of power for improving the power quality of the system.

3.3.2.2 DC-link Energy Balance Theorem

The PI controller is a well-established controller to stabilize the DC-link voltage. It is a simple controller, easy to implement and does not require any complex calculations. The error is generated by calculating the difference of both reference DC-link voltage and sensed DC-link voltage is fed through the PI controller which produces I_{sm}^{*}. The gain parameters K_p (proportional constant) and K_i (damping factor) are to be calculated by the voltage control loop. The following equation is used for calculating the gain parameters.

$$1+\left[K_p+\frac{K_i}{s}\right]\frac{3[V_s-L_cI_{co}s-2I_{co}R_c]}{C_{dc}V_{dco}s}=0 \tag{3.31}$$

From the above Eq. (3.31), the optimum value of K_p and K_i are chosen which are tabulated in Appendix-B1. In DC-link energy balance method, unit template is generating from sinusoidal supply voltage hence, the control technique is also known as unity power factor (UPF) control technique. The PI controller output is referred as the peak value of reference source current (I_m^*). This I_m^* is computed by comparing the actual DC-link voltage (V_{dc}) and reference DC-link voltage ($V_{dc,\ ref}$) and processed by PI controller. The reference source current is computed by multiplying the reference peak value of source current with unit vector template u (t) which is extracted from the supply voltage. The reference source current can be computed by Eq. (3.32).

$$i_s^* = u(t).I_{sm}^* \tag{3.32}$$

Where, $u(t)=1*\sin\omega t$ is the unit vector template.

The capability of shunt APF depends on the certainty of the generated template. In the modified method, the template is generated using Hilbert transform based ATF. The switching pulses generate for VSI is based on the hysteresis band current controller, which depends on current error as follows:

$$\text{error} = i_{s,actual} - i_s^* \tag{3.33}$$

Where, the $i_{s,actual}$ is the actual source current.

The control law for switching of shunt APF as follows:

$$u=\begin{cases}+1, & \text{for error} > 0\\ -1, & \text{for error} < 0\end{cases} \tag{3.34}$$

The exact implementation of this control theory causes higher switching frequency and limit the VSI power devices. An UHCC switching scheme is presented in this thesis work in order to overcome the drawback of control law of Eq. (3.34). The conventional SBHCC and UHCC switching schemes are elaborated in the following sections. A complete block diagram of Hilbert transform based ATF along with UHCC switching is shown in Figure 3.3.

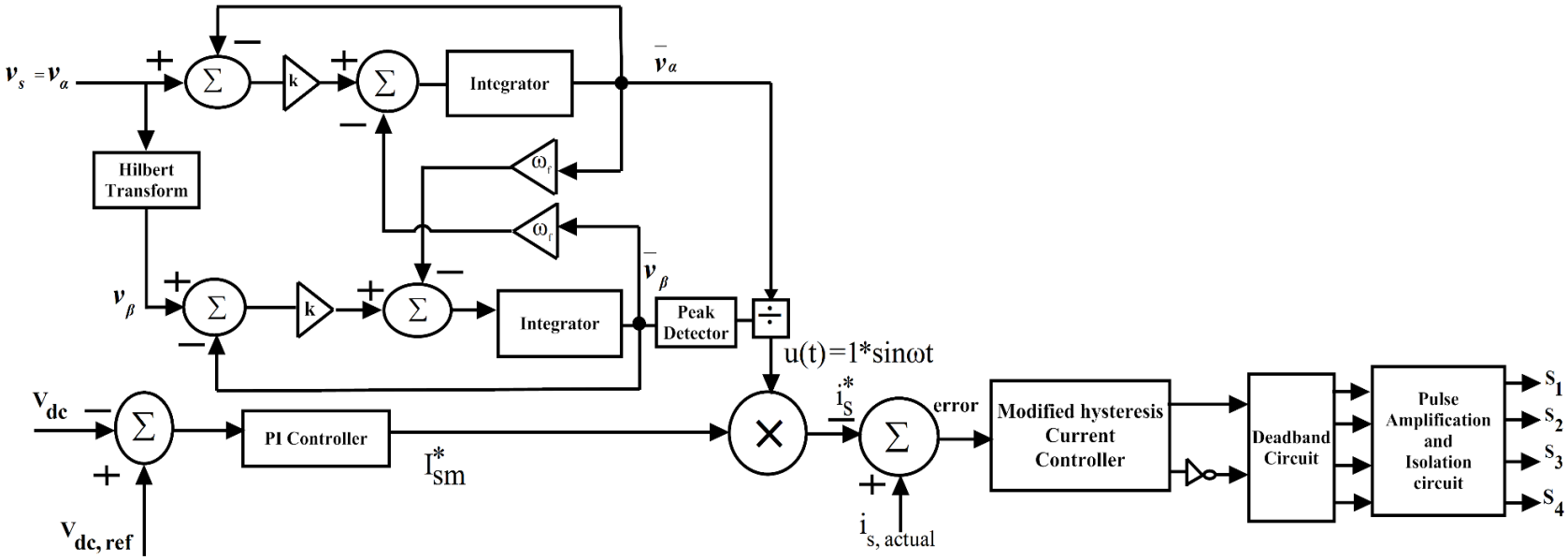


Figure 3.3 Hilbert transform ATF based DC-link energy balance theorem

3.4 Hysteresis Current Controller

Among the various PWM techniques mentioned in the literature, hysteresis current controller is often simple and easy to implement. The hysteresis band current controller works by comparison of current error with fixed hysteresis band which produce switching signals. Single band hysteresis current controller and unipolar hysteresis current controller are implemented in this thesis work.

3.4.1 Single-band Hysteresis Current Controller

The single-band hysteresis current-controller is function of two levels for switching ON and OFF the switches of VSI. The combination of upper switches and lower switches of S_1, S_2, and S_3, S_4 are switching ON and OFF simultaneously. The switching action of S_1 for one complete cycle is obtained as in Eq. (3.35), where h is the hysteresis band.

$$S_1 = \begin{cases} \text{ON, when} & i_{s,actual} > i_s^* + h \\ \text{OFF, when} & i_{s,actual} < i_s^* - h \end{cases} \tag{3.35}$$

The single-band hysteresis controller and switching scheme of VSI power switches during the expansion of filter current error is shown in Figure 3.4 (a) and (b), respectively.

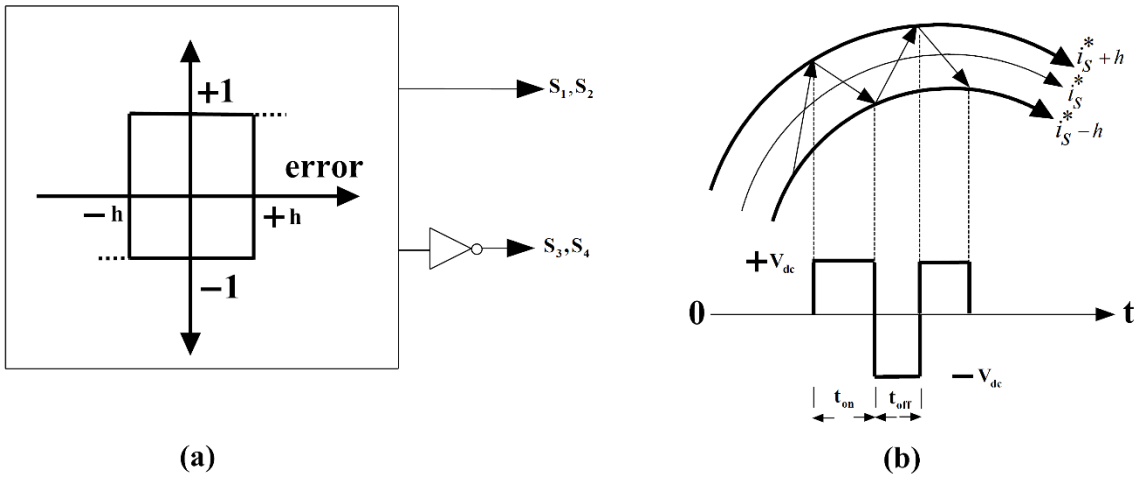


Figure 3.4 SBHCC switching pattern (a) Single-hysteresis band, and (b) Switching scheme

When S_1 and S_2 are ON (S_3 and S_4 are OFF), the inverter generates $+V_{dc}$. The power switches S_1 and S_2 remain ON until shunt APF current error reaches lower hysteresis band point $i_s^* - h$. The shunt APF current error modifies from +h to –h with adverse slope during

ON period. The ON period for S_1 switch can be calculated as per Eq. (3.36), where V_c is the output of the inverter.

$$T_{ON} = \frac{2hL_c}{V_{dc} - V_c} \tag{3.36}$$

Where, V_c is the inverter output. When S_1 and S_2 are turned OFF (S_3 and S_4 are ON), the inverter generates $-V_{dc}$. The power switches S_1 and S_2 remain ON till the current error of shunt APF crosses the upper hysteresis band at point $i_s^* + h$. The shunt APF error modifies from –h to +h with a progressive slope during OFF period. The OFF period for S_2 can be calculated as per Eq. (3.37):

$$T_{OFF} = \frac{2hL_c}{V_{dc} + V_c} \tag{3.37}$$

By adding Eq. (3.36) and Eq. (3.37), which gives the total switching period $T_{Sw}=T_{ON}+T_{OFF}$. Hence, the switching frequency can be calculated as per Eq. (3.38), where m is the modulation index and L_c is the interfacing inductor.

$$T_{sw} = T_{ON} + T_{OFF} = \frac{2hL_c}{V_{dc} + V_c} + \frac{2hL_c}{V_{dc} - V_c}$$

Solving the above equation for calculating the switching frequency (f_{sw}).

$$f_{sw} = \frac{1}{T_{ON} + T_{OFF}} = \frac{V_{dc}}{4hL_c}(1 - m^2 \sin\phi), \qquad 0 < \omega t < 2\pi \tag{3.38}$$

Since, $V_c = V_{dc} m * \sin\phi$ is the average inverter output voltage and m varies from 0 to 1. The average switching frequency ($f_{sw,avg}$) over one fundamental period can be calculated as:

$$f_{sw,avg} = \frac{V_{dc}}{4hL_c}(1 - 0.5m^2) \tag{3.39}$$

It is clear from Eq. (3.39) that when the modulation index becomes zero, the average switching frequency will be in maximum value. The disadvantages of this scheme is that it has higher switching frequencies with lower hysteresis band values, which lead to higher switching losses and higher switching frequency variations. These disadvantages can be overcome by the unipolar hysteresis current controller as mentioned in the next section.

3.4.2 Unipolar Hysteresis Current Controller

This PWM switching scheme offers low switching frequency as compared to SBHCC. It is easy to implement and robust in control. The switching pattern of UHCC has shown in Figure 3.5. This scheme has three voltage levels, which are zero, $+V_{dc}$ and $-V_{dc}$ utilized to control the active filter current. In this scheme, two legs of VSI are controlled separately with separate hysteresis bands as shown in Figure 3.5 (b). The upper power switches (S_1 and S_3) and lower power switches (S_2 and S_4) are controlled by different hysteresis bands. The performance of UHCC is carried out by turning ON and OFF of the power switches by means of shunt APF current error are shown in Figure 3.5 (c). The expression for S_1 to turn ON as follows:

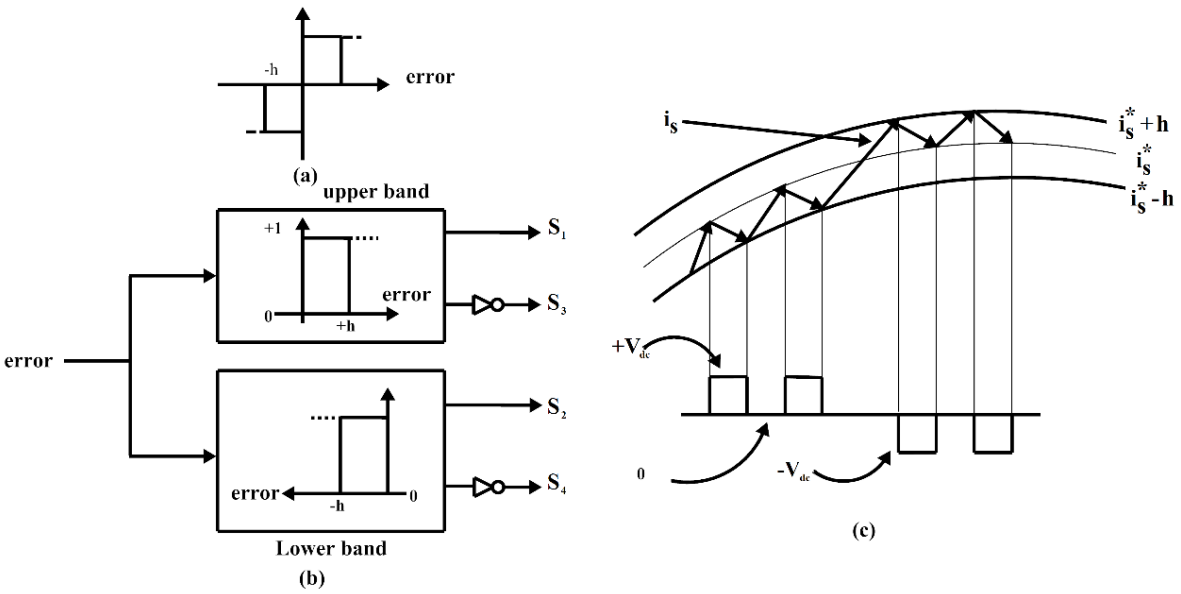


Figure 3.5 UHCC switching scheme (a) Unipolar hysteresis band function, (b) Two-level hysteresis function, and (c) Hysteresis switching pattern

$$T_{ON} = \frac{hL_c}{V_{dc} - V_c} \tag{3.40}$$

When the shunt APF current error reaches its lower band at point i_s^*−h, S_1 is switched OFF. When the shunt APF current error modifies from –h to 0 with progressive ramp, the power switch S_1 will turn OFF. The OFF period for S_1 can be written as follows:

$$T_{OFF} = \frac{hL_c}{V_c} \tag{3.41}$$

During positive half-cycle, the total switching period is given as:

$$T_{sw} = T_{ON} + T_{OFF} = \frac{hL_c}{V_{dc} - V_c} + \frac{hL_c}{V_c}$$

$$T_{sw} = T_{ON} + T_{OFF} = \frac{V_c hL_c}{(V_{dc} - V_c) * V_c} \tag{3.42}$$

Solving above equations for calculating the switching frequency (f_{sw}). The switching period obtained for S_1 and S_4 for one-half cycle where S_3 is OFF and S_2 is ON. Therefore, the switching frequency during one complete cycle is as follows:

$$f_{sw} = \frac{V_{dc}}{2hL_c}(m * \sin\phi - m^2 \sin^2\phi) \tag{3.43}$$

The average switching frequency for one complete fundamental period is as follows:

$$f_{sw.avg} = \frac{V_{dc}}{2hL_c}(\frac{2}{\pi} m - 0.5m^2) \tag{3.44}$$

In above Eq. (3.44), when the modulation index is zero, the average switching frequency will become zero, which ensures the lower switching frequency. The two hysteresis current controller switching schemes are explained in the above sections. The average switching frequency can be calculated from Eq. (3.39) and Eq. (3.44) for different values of h. Later, the same has been calculated in simulation and experimental sections which are also summarized in Table 3.2 and 3.2, respectively. The obtained switching frequency values under UHCC schemes give less switching frequency and switching frequency variations.

3.4.3 Design of Single-Phase Shunt APF System

In single-phase shunt APF system, the selection of interfacing inductor value, DC-link capacitor voltage and rating play a vital role in the efficient operation of shunt APF. The detailed device selection procedure is as follows:

Calculation of DC-link Capacitor Voltage (V_{dc}) and Capacitor (C_{dc}) value

The DC- side capacitor (C_{dc}) serves two purposes, one is to maintain a DC-link voltage with minimal ripple in steady state and the second is to serve as an energy storage element to supply real power difference during the transient state of the load. Therefore, the DC-link voltage (V_{dc}) of shunt APF should have enough to sustain disturbances during load perturbations. The DC-link voltage can be calculated as follows [107]:

$$V_{dc} = 1.25 * \sqrt{2}\, v_s \tag{3.45}$$

The DC-link capacitor is to absorb or supply the real power demand of the load during the transient condition of the load. The value of the capacitor depends on the following Eq. (3.46). The calculated values of V_{dc} and C_{dc} are mentioned in Appendix-B1.

$$C_{dc} = \frac{2P_{max} * 20 * 10^{-3}}{V_{dc}^2 \left[1 - \left(\frac{V_{dc,ref}}{V_{dc}}\right)^2\right]} \tag{3.46}$$

Where, V_{dc} and $V_{dc,\,ref}$ are the actual and reference DC-link voltages, respectively.

Calculation of Interfacing Inductor Value (L_c)

The interfacing inductance has to be selected in such a way that it should have lower flux density and enough ventilation between core and conductor of inductor. This inductor acts as a medium between single-phase VSI and grid to transfer the energy. The inductor value is calculated as per following equation [107].

$$L_c = \frac{V_{dc}}{4hf} \tag{3.47}$$

Where, h is the hysteresis band value and f is the switching frequency.

3.5 System Modelling using MATLAB®/ Simulink Environment

The single-phase VSI based shunt APF consists of four MOSFET switches with a DC-link capacitor and connected through the interfacing inductor at PCC. The interfacing inductor acts as a medium between shunt APF and grid to transfer the energy and suppress the higher order harmonics caused by switching action of MOSFET switches. The DC-link capacitor acts as an active energy storage element for VSI and also supplies extra real power demand of the load during transient condition of the load. The single-phase VSI based shunt APF is implemented with SimPowerSystem tools of MATLAB®/ Simulink software. The parameters used for simulation are tabulated in Appendix-B1.

3.5.1 Single-Phase Diode Bridge Rectifier with R-L Load

In order to verify the performance of the modified control algorithm along with SBHCC and UHCC switching schemes, a single-phase shunt APF has been developed in

MATLAB®/ Simulink environment. A single-phase diode bridge rectifier with R-L (resistive and inductive)-type load is connected as non-linear load which distort the source current by injecting the harmonic components into the system. The performance of single-phase shunt APF with modified control algorithm is tested under the sinusoidal and distorted supply voltage conditions.

3.5.1.1 Simulation under Sinusoidal Supply Voltage Condition

In this case, the compensation effectiveness and adaptability of Hilbert transform based ATF technique is tested under the sinusoidal supply voltage condition. The performance results of source voltage (V_S), source current (I_s), load current (I_L) and compensation current (I_c) are shown in Figure 3.6.

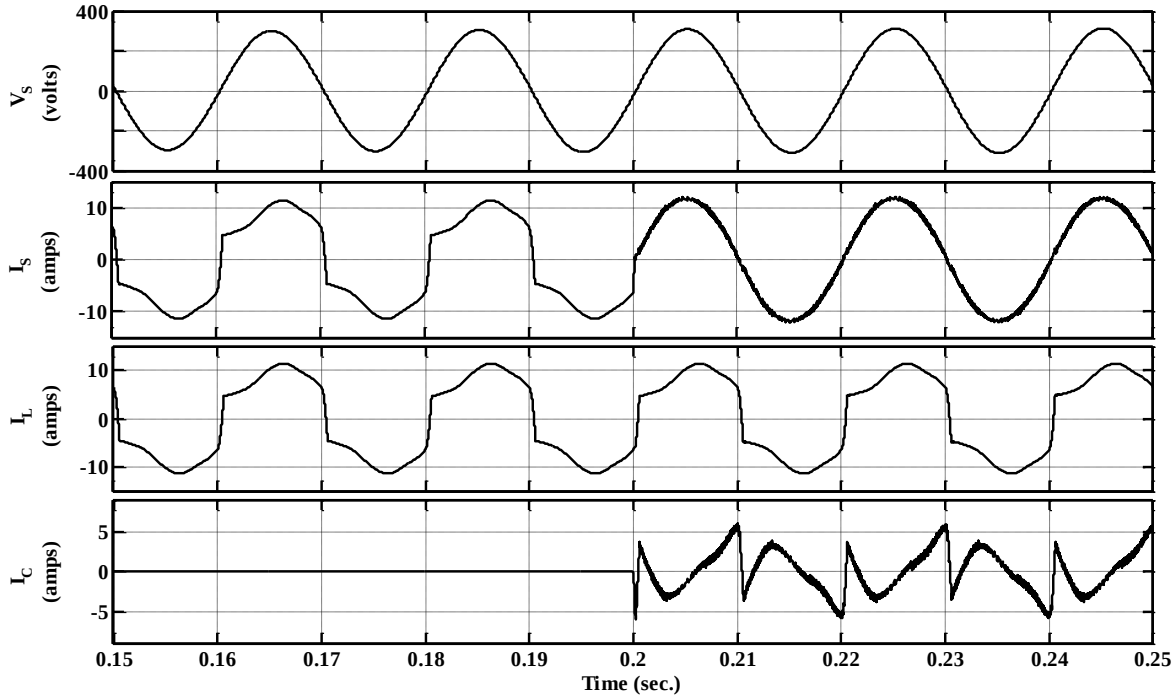
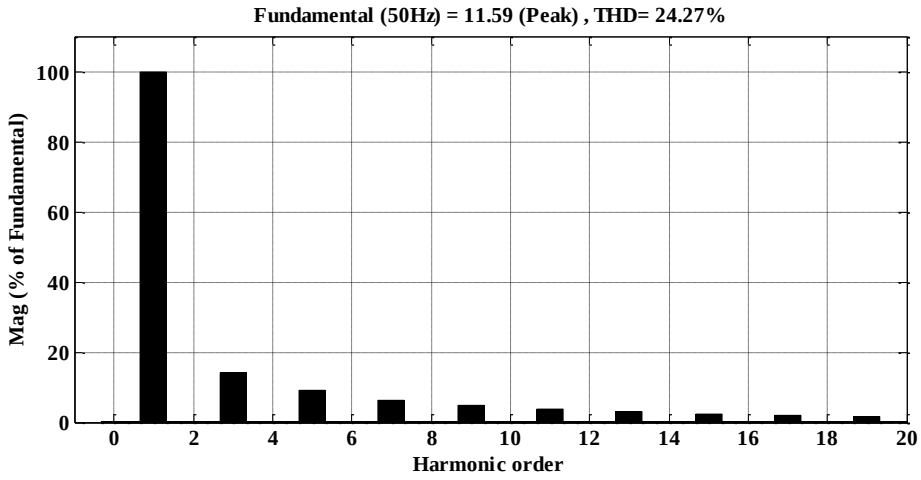
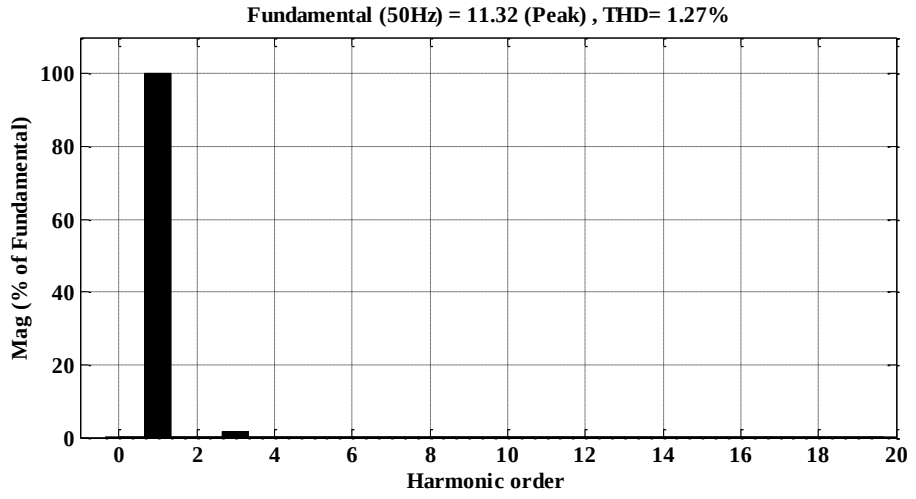


Figure 3.6 Shunt APF performance parameters of source voltage (V_S), source current (I_S), load current (I_L), and compensating current (I_C) under sinusoidal supply voltage condition

The source current has become sinusoidal as soon as the shunt APF is switched ON at 0.2 sec. and mitigated the current harmonics and reactive power requirement of non-linear load which shows that the presented control algorithm is efficient and robust. The frequency spectrum of source current before and after compensation are shown in Figure 3.7 (a) and (b), respectively. It is found that the source current THD is reduced from 24.27% to 1.27%.



(a)



(b)

Figure 3.7 Harmonic spectrum of source current (a) Before compensation, and (b) After compensation

3.5.1.2 Simulation under Distorted Supply Voltage Condition

Practically, the supply voltage in electrical distribution is not sinusoidal but it has a significant amount of harmonic contents. The significant feature of the presented Hilbert transform based ATF control scheme is able to extract the fundamental frequency component of supply from the distorted supply in synchronism with grid. The simulation performance of this modified scheme is tested by introducing distorted supply voltage having THD of 12.16% with considering 3^{rd}, 5^{th} and 7^{th} harmonic components, as shown in Eq. (3.48).

$$V_s = 325.27 * \sin(\omega t) + 65.05 * \sin(5\omega t) + 46.47 * \sin(7\omega t) \quad (3.48)$$

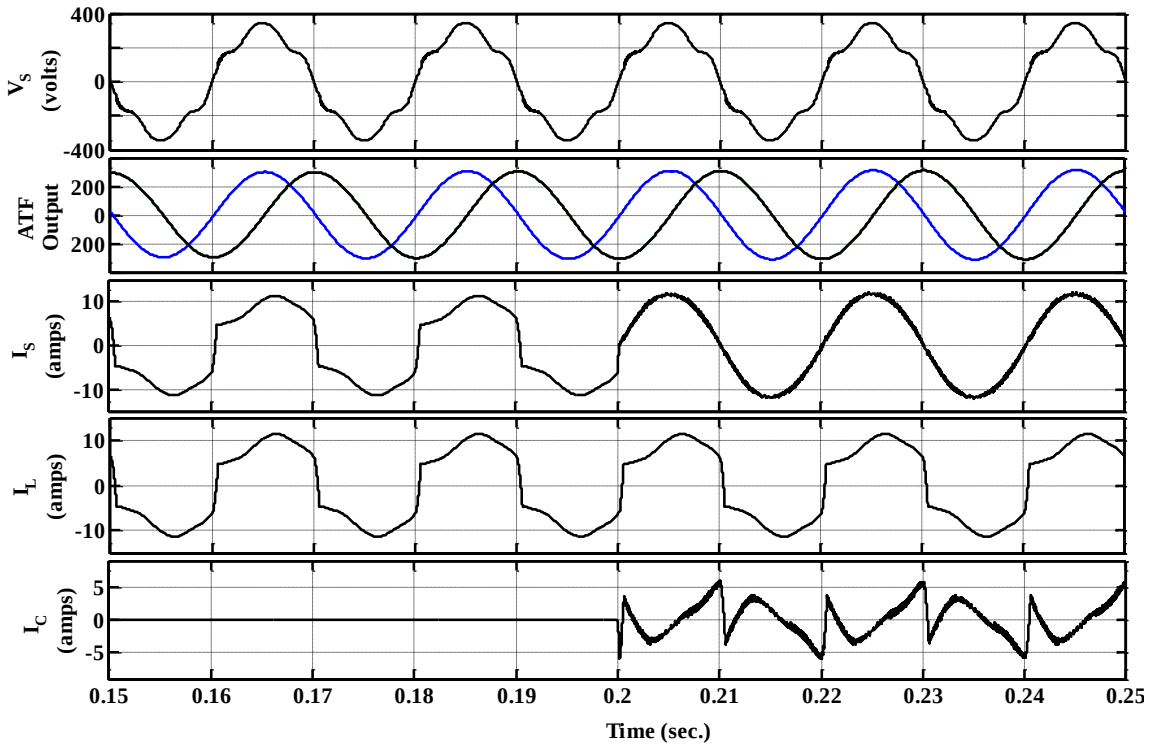
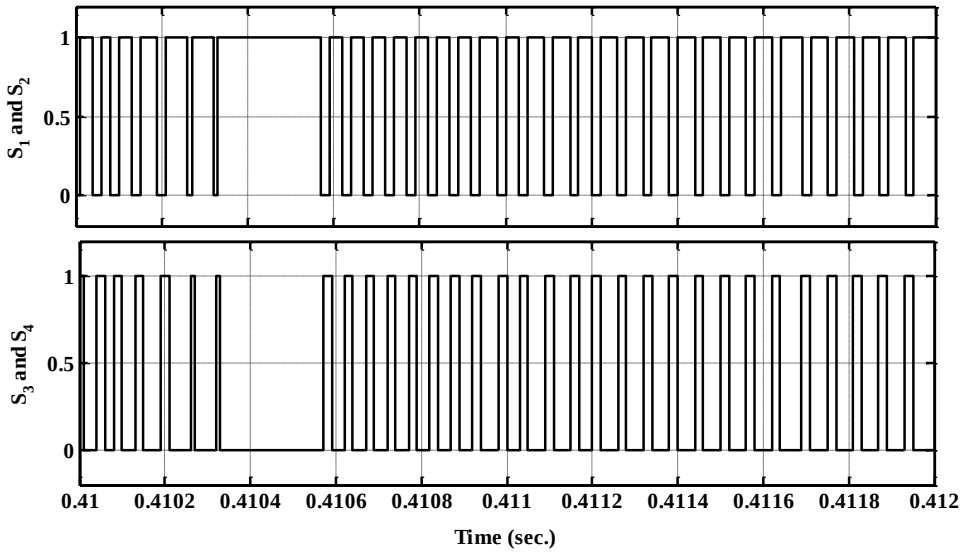
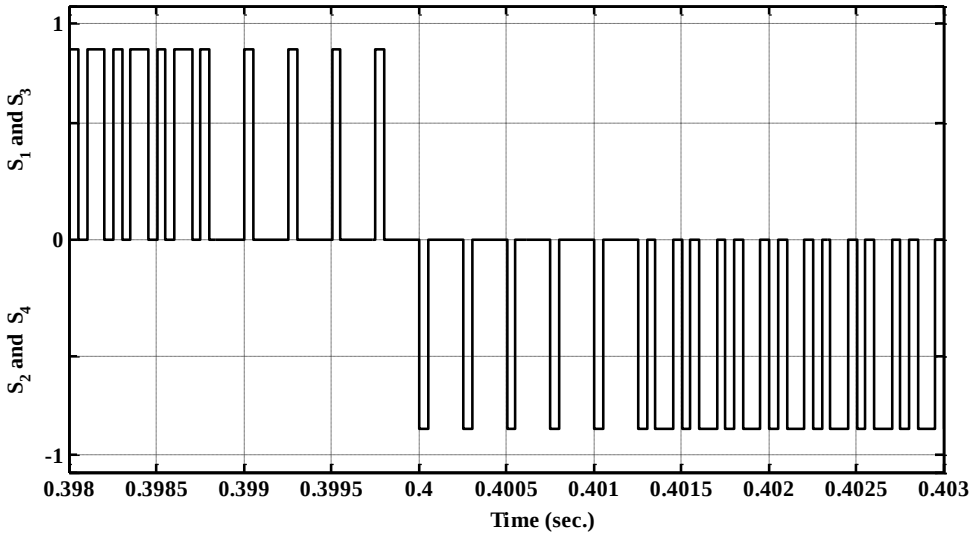


Figure 3.8 Performances under distorted supply voltage conditions Vs, Hilbert transform based ATF output ($\bar{v}_\alpha$ - $\bar{v}_\beta$), I_S, I_L, I_c

The distorted supply voltage is divided into two components (v_α and v_β) in 90º phase with each other by Hilbert transform function. These two signals are further processed in the ATF for the extraction of the fundamental component from the distorted supply voltage. The outputs of ATF $\bar{v}_\alpha$ and $\bar{v}_\beta$ are have same amplitude as the ideal supply voltage. Further, DC-link energy balance theorem is used for reference current generation. The source current becomes sinusoidal immediately after switching on of single-phase shunt APF at 0.2 sec. The performance waveforms of distorted supply voltage, $\bar{v}_\alpha - \bar{v}_\beta$, I_s, I_L and I_c are shown in Figure 3.8. The Hilbert transform based ATF is extracted the fundamental component of supply from the distorted supply without phase delay which further used for mitigating the harmonic currents in the system. In addition, the performance is analyzed for both SBHCC and UHCC switching schemes. According to SBHCC switching scheme as shown in Figure 3.9 (a), the generated switching pulses are of two levels, i.e. +1 and 0. Therefore, the switches S_1 & S_2 are switched on and off during one complete cycle. Similarly, S_3 & S_4 are switched on and off.



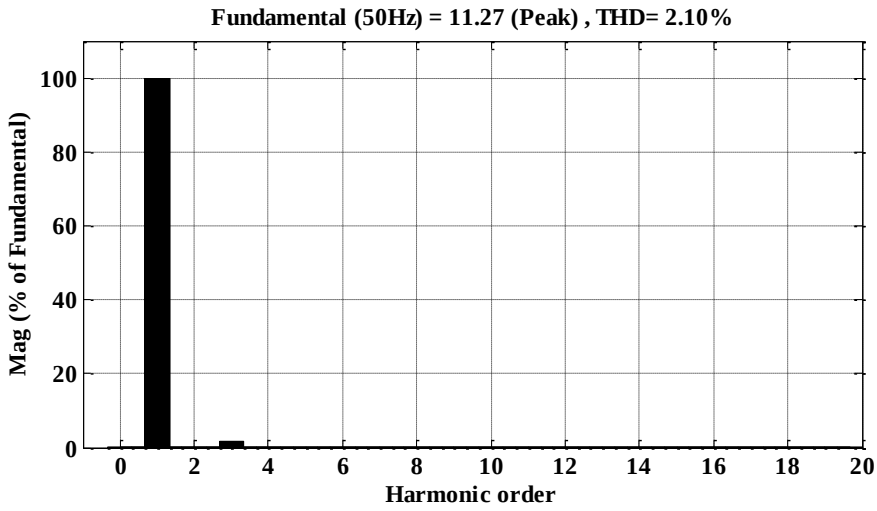
(a)



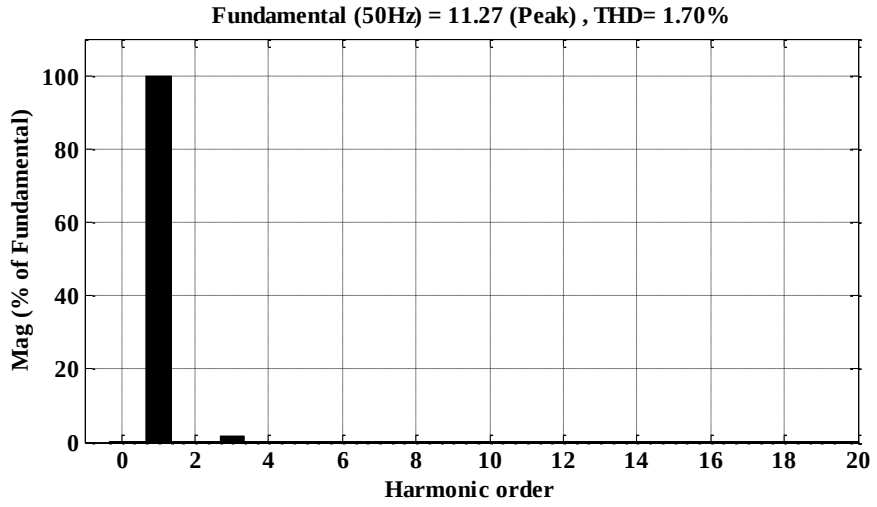
(b)

Figure 3.9 Shunt APF switching pattern under: (a) SBHCC scheme, and (b) UHCC scheme

The average switching frequency is calculated as per Eq. (3.39) for the hysteresis band of 0.3 by the SBHCC scheme as 19.7 kHz. Also, in the UHCC switching scheme as shown in Figure 3.9 (b), the generated switching pulses are of three levels, i.e. +1, 0 and -1. Therefore, the switches S_1 & S_2 are switched on while S_3 & S_4 always off state during positive half cycle and S_3 & S_4 are on during negative half cycle while S_1 & S_2 are off. The calculated average switching frequency as per Eq. (3.44) by UHCC scheme is 10.97 kHz for the same hysteresis band parameters as SBHCC.



(a)



(b)

Figure 3.10 Simulated harmonic spectrum of source current (a) by SBHCC switching scheme, and (b) by UHCC switching scheme

It can be concluded that, the UHCC provides the lower switching frequency compared to SBHCC scheme. Even though, the THD is almost equal in both switching schemes but, switching frequency is drastically reduced which further reduces the switching losses by UHCC scheme as compared to SBHCC scheme. A fair performance comparison study has been analyzed between both SBHCC and UHCC schemes for different hysteresis band parameters which are tabulated in Table 3.2. It is observed from Table 3.2 that as lower the hysteresis band value, increase the switching frequency and improves the THD of source current. Also, the switching frequency is drastically reduced with UHCC scheme compared

to SBHCC scheme for the same hysteresis band values. The Figures 3.10 (a) and (b) shows the supply current THD which has been reduced from 24.27% to 2.10%, 1.70%, respectively by using SBHCC and UHCC schemes. It can be observed from these results that the Hilbert transform based ATF control algorithm is able to mitigate the current harmonics and reactive power burden even under distorted supply voltage conditions, which improved the source current THD and power factor as per IEEE-519 standards.

Table 3.2

Simulated results of %THD, average switching frequency and power factor for various hysteresis band values in SBHCC and UHCC schemes

Hysteresis band (h)	**SBHCC (Simulation)**		**UHCC (Simulation)**		**Power factor (Simulation)**
	THD (%)	$f_{sw.a}$ (kHz)	THD (%)	$f_{sw.a}$ (kHz)	
0.1	1.38	59.13	1.01	32.90	0.995
0.2	1.45	29.56	1.1	16.45	0.988
0.3	1.67	19.7	1.35	10.97	0.985
0.4	1.8	14.78	1.5	8.22	0.98
0.5	2.8	11.82	2.1	6.58	0.97

3.5.1.3 Transient Performance under Distorted Supply Voltage Condition

Figure 3.11 shows the simulated performance parameters of V_s, I_s, I_L, I_c and DC-link voltage under distorted supply voltage and transient condition of the load. Initially load current is 11.48 A and DC-link voltage is stable at its steady-state value. The transient performance of shunt APF with Hilbert transform based ATF based control technique is observed by increasing & decreasing the load value. At t = 0.4 sec. the load is increased from 11.48 A to 26.09A and subsequently, the load is decreased from 26.09 A to 11.48 A at t = 0.7 sec. It is observed from Figure 3.11 that the source current is sinusoidal under distorted supply voltage condition which shows the effectiveness of Hilbert transform based adaptive filter. During applying and removal of load, DC-link capacitor voltage decreases and increases respectively. But, DC-link voltage quickly reverts back to its steady-state value due to the fast action of compensator and Hilbert transform based ATF controller.

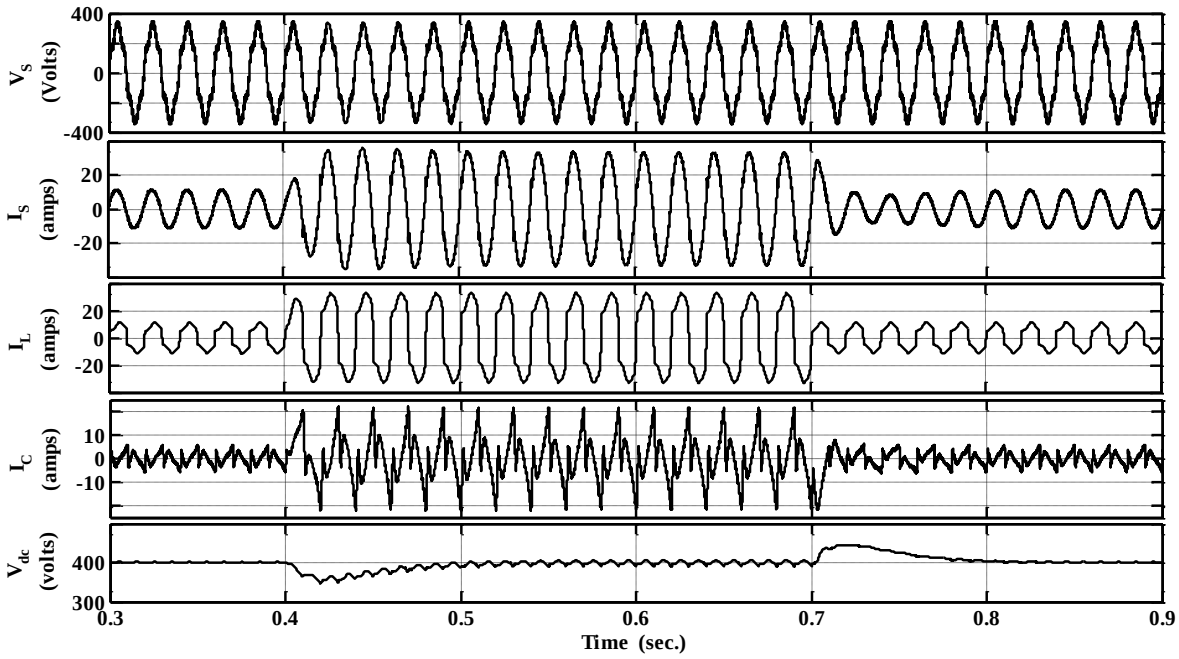


Figure 3.11 Transient performance of Hilbert transform based ATF control scheme under distorted supply voltage conditions and load change at t = 0.4 sec. and t = 0.7 sec

3.6 Implementation of System Hardware

The complete block diagram of single-phase shunt APF is shown in Figure 3.12. The single-phase shunt APF is a VSI made of power MOSFET switches (S_1, S_2, S_3, S_4) with anti-parallel diodes. An energy storage DC-link capacitor (C_{dc}) is presented at the DC side of VSI. A single-phase uncontrolled bridge rectifier is exhibited as a non-linear load with resistive and inductive element (R-L load). The shunt APF is connected near to the non-linear load at the PCC through interfacing filter inductors (L_c, R_c) which is used to mitigate the ripples in the compensating current and act as an interface between grid and shunt APF for transferring the energy. The smoothening inductor (L_{sm}, R_{sm}) are connected along with the diode bridge rectifier for eliminating high switching noise due to switching of VSI.

3.6.1 Power Circuit Configuration

Single-Phase Voltage Source Inverter

The single-phase voltage source inverter is implemented using IRFP 460 MOSFET switches as shown in Appendix-A5. The single-phase shunt APF has four MOSFET switches (S_1 to S_4). MOSFET switch has internal inbuilt body diodes with fast reverse

recovery capability. The body diodes are used for charging the DC-link capacitor (C_{dc}). Each MOSFET is mounted on the heat sink for proper heat dissipation.

Single-Phase Diode Bridge Rectifier

A Single-Phase diode bridge rectifier with R-L load is commonly used as non-linear load. A Single-phase diode bridge rectifier is developed in the laboratory for experimental purpose as shown in Appendix-A7.

3.6.2 dSPACE Controller Platform

DSPACE platform affords an entire solution for electronic control unit (ECU) software development. It is an effective development tool for devoted services within the area of developing prototype models and testing. The dSPACE easily interfaces with common software like MATLAB/Simulink platform. The additional feature of the dSPACE is its graphical user interface (GUI) environment in which real-time activities can be performed. Real-time Interface (RTI) acts as an interface between dSPACE real-time systems and the MATLAB/Simulink software model. It extends real-time workshop (C-code generation) for the continuous and automatic implementation of Simulink models on the dSPACE real-time hardware. This allows us to concentrate fully on the actual design process and to carry out fast design iterations. To implement a real-time control loop using dSPACE and MATLAB, the following items are needed. (a) DS1104 DSP of dSPACE R&D controller board (b) CLP1104 Connector Panel.

DS1104 DSP of dSPACE DS1104 R&D Controller Board

A schematic description of the features input and output ports of the DS1104 Board are given in Figure 3.13. Some of the main features of the board include the main processor, a PowerPC603e with a 250MHz CPU clock frequency and a slave DSP from Texas instruments (DSP TMS 320F240). The dSPACE1104 board also consists of Digital I/O ports, Slave I/O PWM ports, ADC and DAC channels, an incremental encoder interface and a UART interface. The DS1104 R&D controller board can be plugged into a PCI slot of a PC. The DS1104 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations in various fields. It is a complete real-time control system based on a 603 Power PC floating-point processor running at 250 MHz.

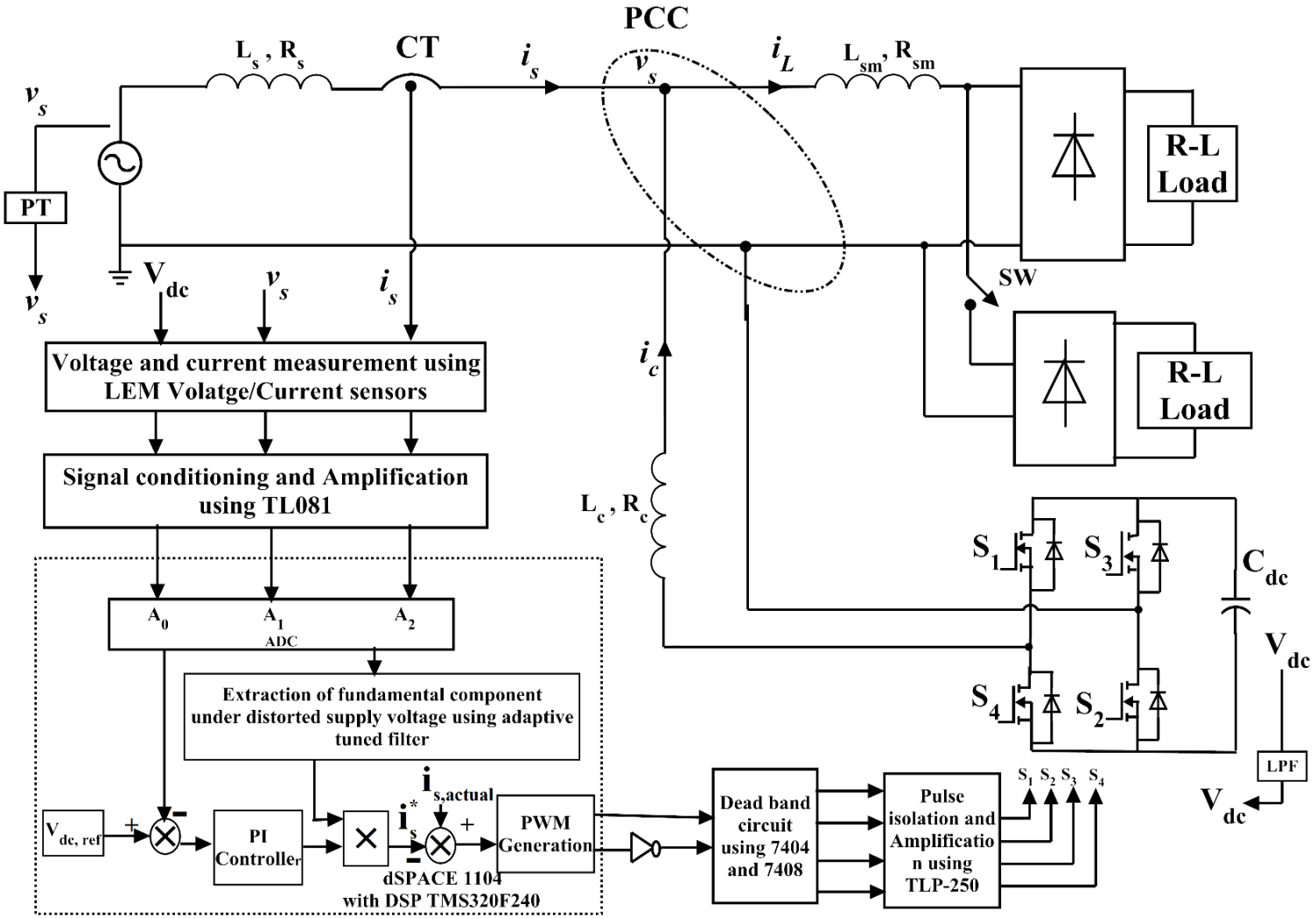
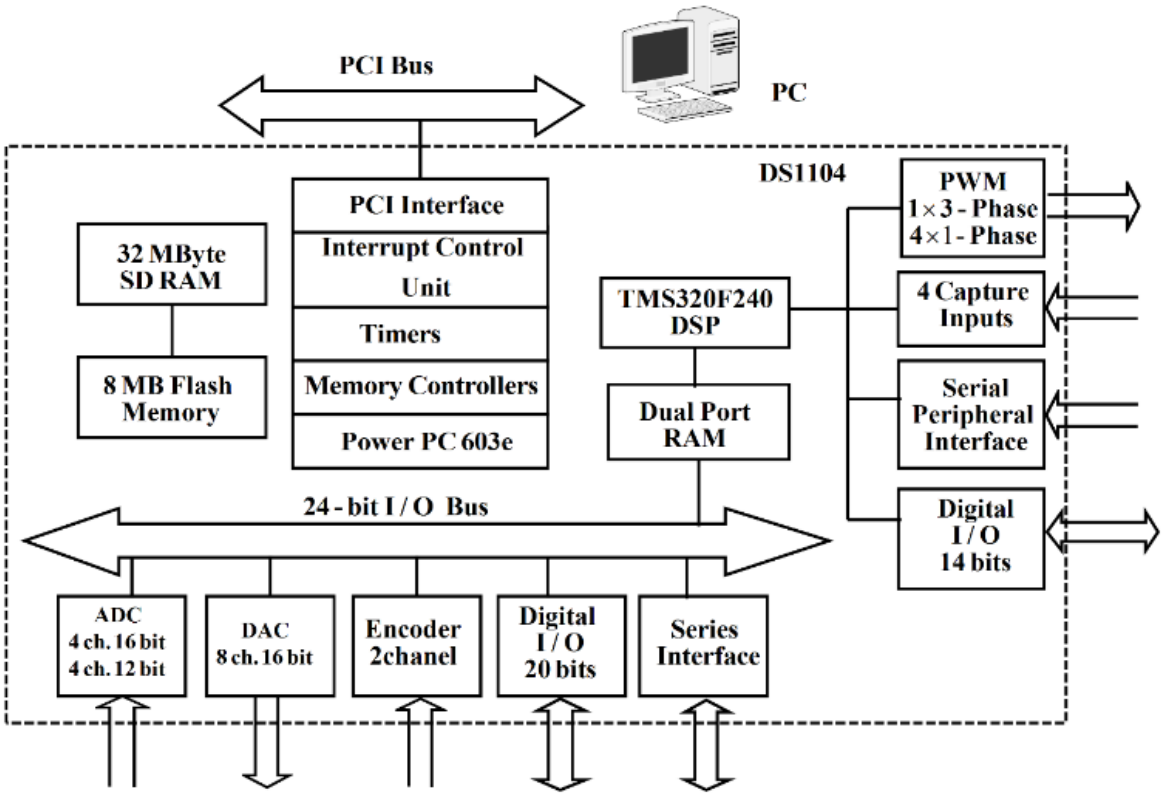


Figure 3.12 Schematic laboratory set-up of VSI based single-phase shunt active power filter

The TMS320F240 DSP microcontroller board includes a slave DSP subsystem for advanced I/O purposes. The rapid control prototyping (RCP), specific interface connectors and connector panels described below provide easy access to all input and output signals of the board. Thus, the DS1104 R&D controller board is the ideal hardware for the dSPACE prototype development system for cost-sensitive RCP applications. It executes all computational and control tasks for the shunt connected converter [156].

The CLP1104 Combined Connector Panel

Specific interface connector panels provide easy access to all the input and output signals of the DS1104 R&D controller board. The CLP1104 connector panel provides connections between the DS1104 R&D controller board and devices. The devices can be individually connected, disconnected or interchanged without soldering via BNC connectors. This simplifies system construction, testing and troubleshooting. The currents and voltage signals are taken into the DS1104 using BNC connectors CP1-CP8 on the CLP1104 connector panel.



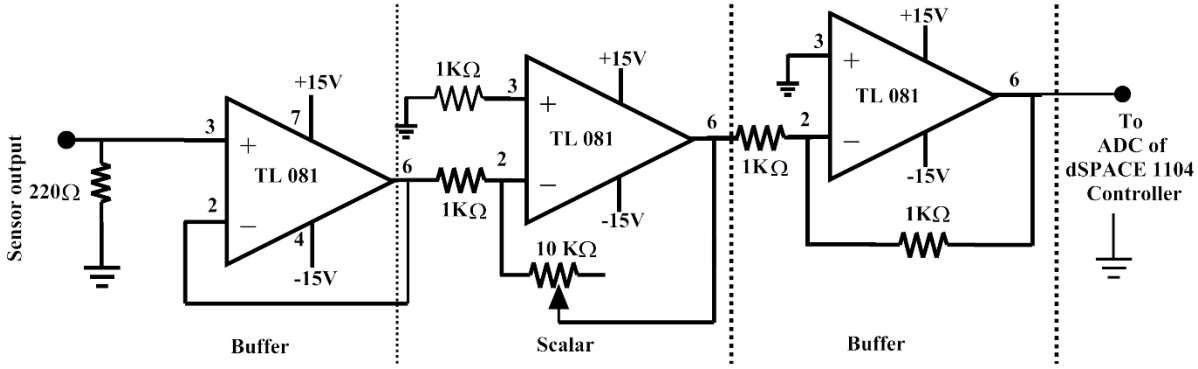
(a)

Figure 3.13 Schematic architecture of dSPACE 1104 controller [157]

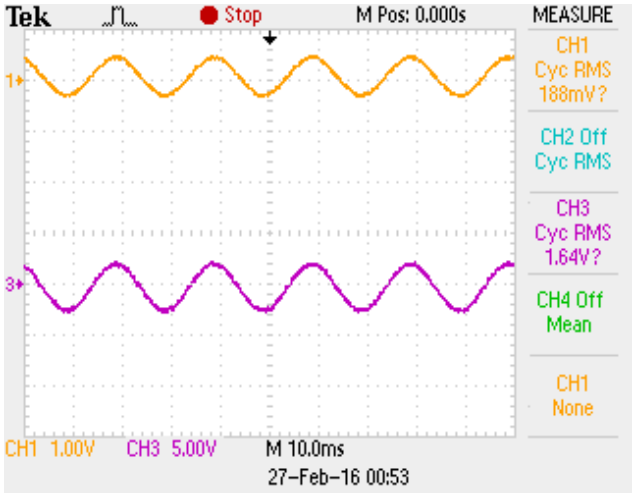
3.6.3 Hall Effect Sensors

The voltages and currents are sensed by using Hall Effect voltage and current sensor to compute the reference current generation in the controller. These Hall Effect sensors convert the high-level voltage and current quantities to low-level analog signals in the range of ±5V. Also, these will provide isolation between power circuit and signal circuit (controller). Single-phase supply voltage, source current and dc-link voltage are sensed for Hilbert transform based DC-link energy balance theorem. The LEM LV25-P voltage and LEM LA 25-NP current sensors selected which have high accuracy, precision, wide frequency band and low-temperature drift. The voltage and current sensing with a signal conditioning board are shown in Appendix-A1 and-A2, respectively.

3.6.4 Signal Conditioning and Amplification



(a)



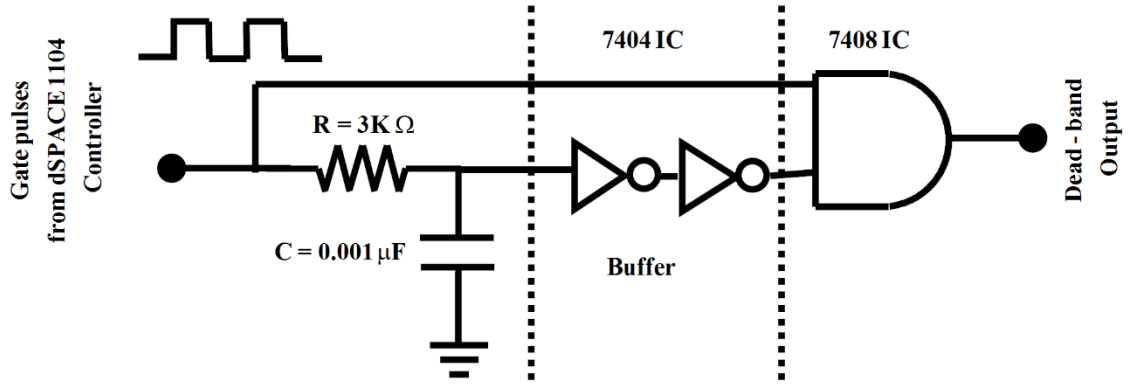
(b)

Figure 3.14 (a) Circuit configuration of signal conditioning board using TL081 ICs, and (b) Sensor output in volts and amplified output in volts

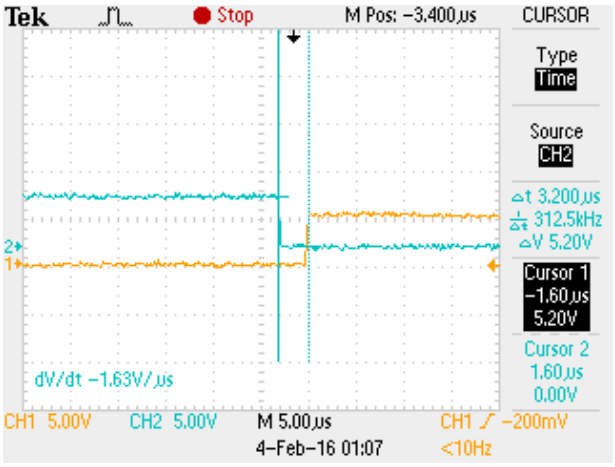
The voltage and current sensor signals are low-level bipolar signals. These signals have to be amplified to a certain range so that the controller is able to detect. The circuit diagram is implemented using TL081 ICs as shown in Figure 3.14 (a). The sensor output voltage and signal conditioning circuit output are shown in Figure 3.14 (b). It is observed from Figure 3.14 (b) that the output voltage of sensor is in the range of mV (188 mV), which is amplified to 1.64 V. Therefore the ADC of dSPACE controller is able to detect the signal accurately.

3.6.5 Dead-band Circuit

In single-phase VSI topology, the switches (S_1 and S_4) are switched ON and OFF complementarily by each other.



(a)



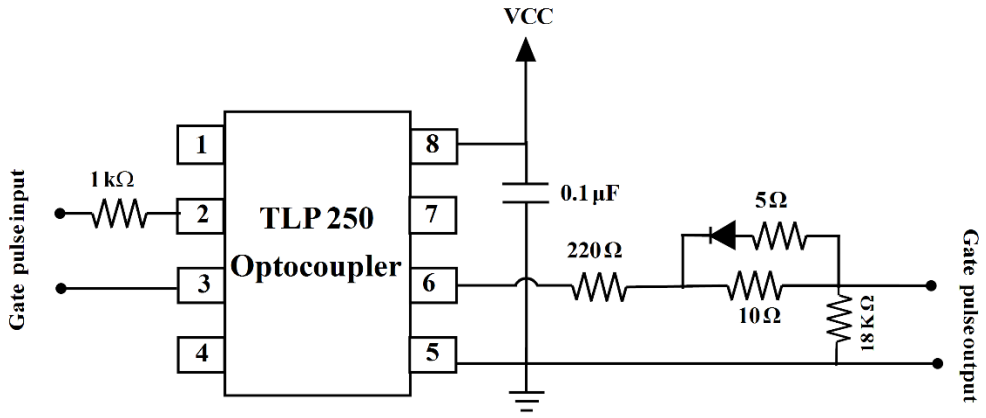
(b)

Figure 3.15 (a) Dead band circuit using 7408 and 7404 ICs, and (b) Generated dead-band created for switching pulses

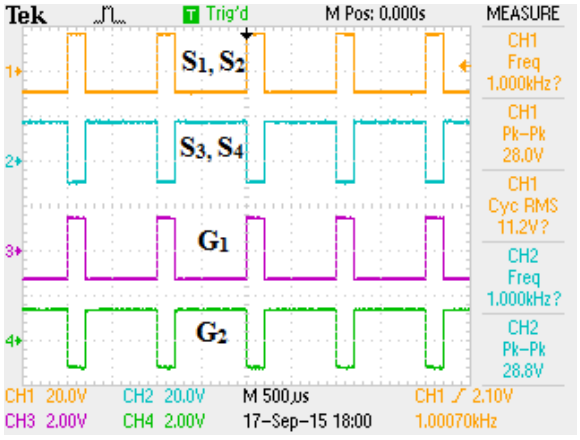
The moment the S_1 turns OFF, the S_4 starts conducting. Practically, the power electronic switches (either MOSFET or IGBT) are not ideal but have slow turn of time. Hence, dead-time is necessary for safe operation of the inverter topology. Dead-time is a small interval time period where both upper and lower switches of the same leg are off. The dead-band circuit is implemented with the help of 7404 and 7408 ICs as shown in Figure 3.15 (a). The dead-time of 3.2 µsec as shown in Figure 3.15 (b) is provided for each leg of VSI switches to avoid shoot-through problems.

3.6.6. Gate Driver Circuit

The primary function of the gate driver circuit is to switch the device from the OFF state to the ON state and vice versa.



(a)



(b)

Figure 3.16 (a) Gate driver circuit using TLP 250, and (b) dSPACE controller output signals G_1 and G_2, gate driver amplified signals S_1, S_2 and S_3 S_4

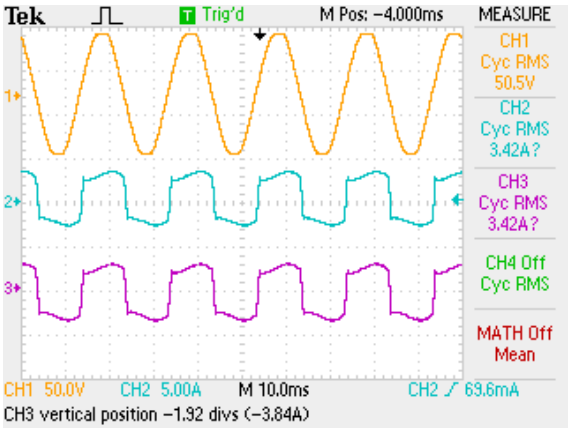
The TLP 250 optocoupler is used as a gate driver IC in this thesis. It provides the required level of amplification for the switching device as well as the electrical isolation between the control circuit and power circuit. The complete circuit configuration of the gate driver circuit is shown in Figure 3.16 (a). The dSPAC1104 controller card generated switching signals according to the control theory. The generated switching signals (G_1 and G_2) in the range of 3-5 V ranges as shown in Figure 3.16 (b) and amplified signals for VSI switches (S_1-S_4) are also shown in Figure 3.16 (b). The gate driver circuit provides amplification and isolation for triggering the MOSFET switches.

3.7 Experimental Results and Discussion

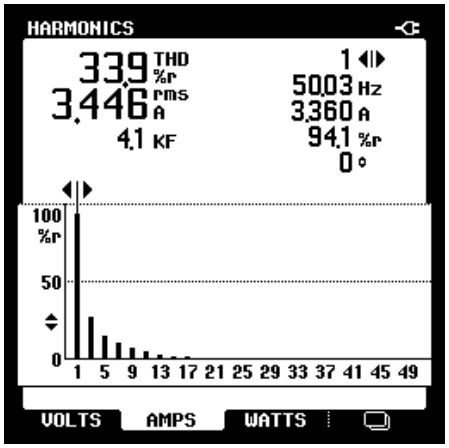
A prototype model of single-phase shunt APF system is implemented in the laboratory as shown in Appendix-A11. The Hilbert transform based ATF control technique and both SBHCC and UHCC switching schemes are implemented. The sensed voltage and current signals are processed through ADCs of dSPACE controller, the control technique is interfere through the MATLAB to the dSPACE 1104 controller. The hysteresis current controller is used for the generation of the switching pulses for the shunt APF. These switching pulses are provided for the MOSFET switches via general purpose I/O pins of the dSPACE 1104 controller through dead-band and gate driver circuit. The performance of the controller is tested under available and distorted supply voltage conditions.

3.7.1 Experimental Investigation under Available Supply Voltage

Initially, the performance of Hilbert transform based ATF control scheme along with UHCC switching scheme in comparison with conventional SBHCC switching schemes is tested under an available supply voltage (1.5 to 2% THD at the time of measurement) with single-phase uncontrolled bridge rectifier with R-L load. The non-linear load distorts the source current by injecting the harmonic components of currents into the system. The Figure 3.17 (a) shows V_S, I_L and source current before compensation. The frequency spectrum of source current is found to be 33.9 % before compensation and power factor is 0.92 as shown in Figure 3.17 (b) and (c), respectively. The Hilbert transform based ATF with DC-link energy balance theorem is used for the reference current generation. When the shunt APF is switched on, the compensated current injected into the system and makes the non-sinusoidal source current to sinusoidal.



(a)



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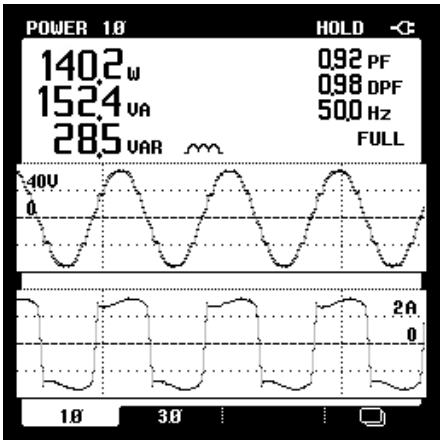
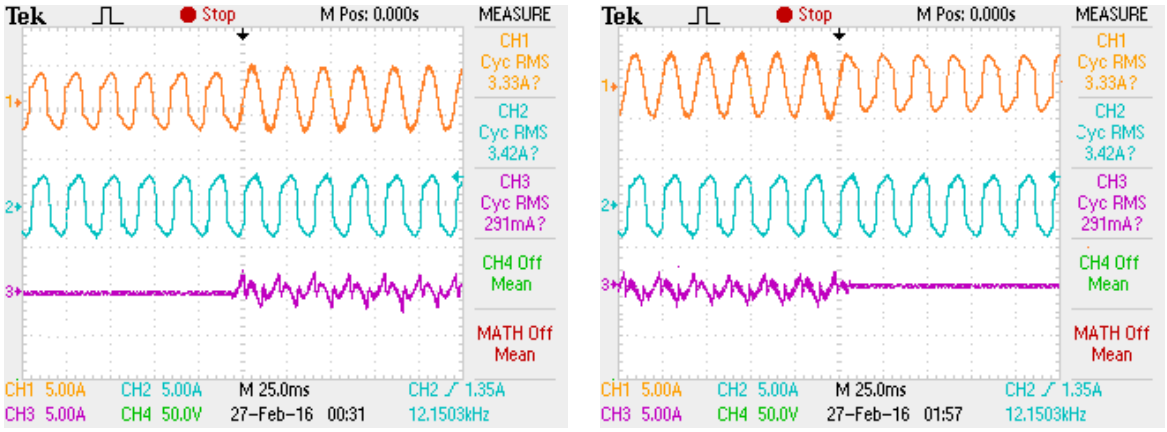


(c)

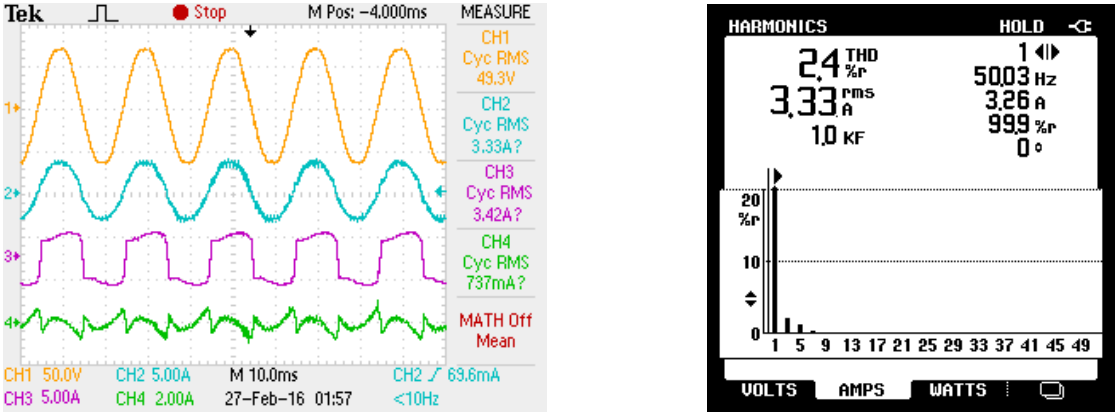
Figure 3.17 (a) Supply voltage, source current before compensation and load current (b) Frequency spectrum of source current before compensation, and (c) Power factor calculation

The switch-ON and switch-OFF response of shunt APF are shown in Figures 3.18 (a) and (b) which show that the shunt APF response is spontaneous and has no delay with this control scheme. The experimental waveforms of V_S, I_S and I_L under the steady-state condition is shown in Figures 3.19 (a) and the harmonic spectrum of source current which reduced from 33.9% to 2.4% have shown in Figure 3.19 (b). It concluded from these results that the single-phase shunt APF is able to compensate load harmonic current successfully. The switching pattern of both SBHCC and UHCC are shown in Figures 3.20 (a) and (b), respectively. The error in SBHCC scheme varies hence, switching frequency as shown in Figure 3.20 (a). It can be concluded that, the control signals generated for switches (S_1, S_2, S_3, S_4) are of a complete cycle. The average switching frequency is calculated as 4.93 kHz using SBHCC scheme.



(a) (b)

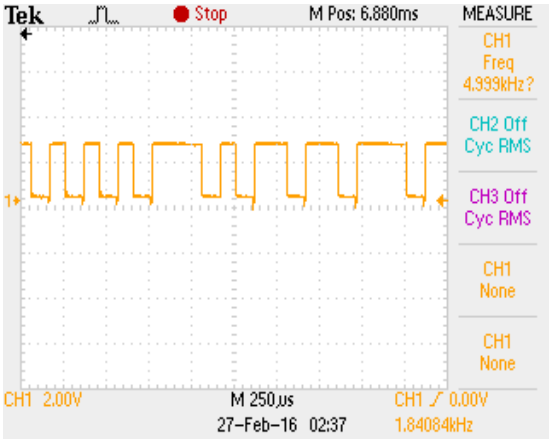
Figure 3.18 (a) Switch-in response of shunt APF, and (b) Switch-off response of shunt APF



(a) (b)

Figure 3.19 (a) Experimental results of source voltage, source current, load current and compensating current at available PCC voltage after compensation, and (b) Harmonic spectrum of source current after compensation

In UHCC scheme as shown in Figure 3.20 (b), the switching pulses are generated for switches S_1 & S_2 for positive half-cycle of error and S_3& S_4 are for negative half-cycle of error. Therefore, the average switching frequency is calculated as 2.74 kHz which is lower compared to the conventional SBHCC scheme. It is found that the switching frequency is less in UHCC scheme as compared to SBHCC scheme for the same hysteresis band parameter value which is tabulated in Table 3.3. It is concluded that the UHCC switching scheme has less switching frequency and switching ripples over SBHCC switching scheme. The unity power factor operation of single-phase shunt APF has been achieved by improving the power factor which is shown in Figure 3.20 (c) and (d), respectively.



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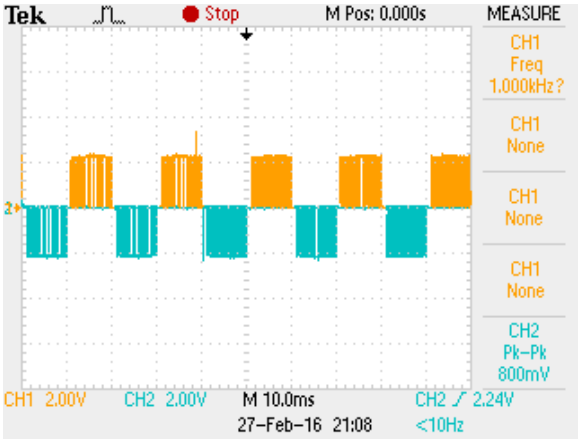
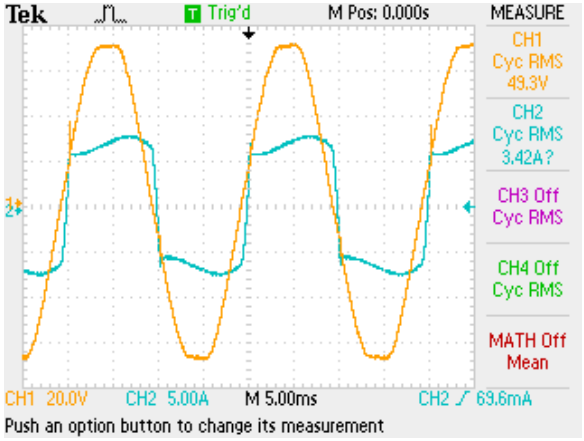


(b)



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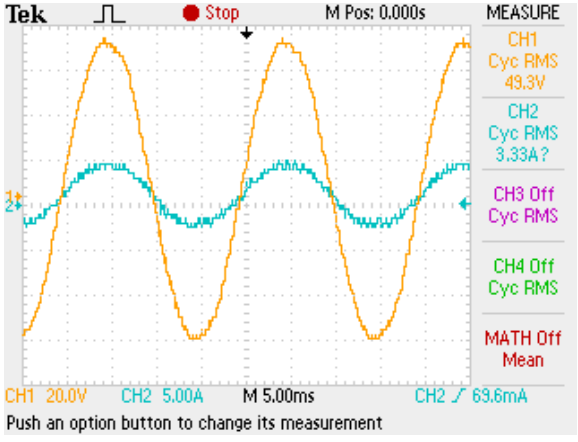


(d)

Figure 3.20 Experimental results of switching pattern (a) SBHCC scheme, (b) UHCC scheme, (c) Supply voltage and load current, and (d) Supply voltage and source current at unity power factor operation

Table 3.3

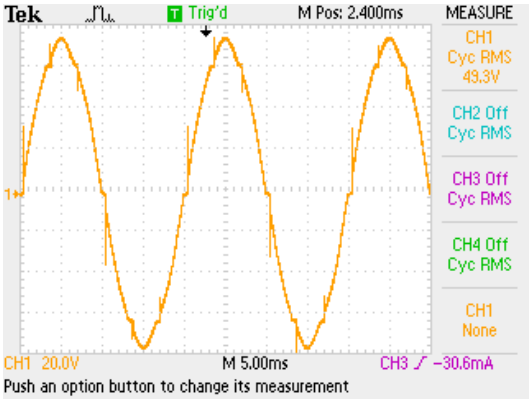
Experimental results of %THD, average switching frequency and power factor for various hysteresis band values in SBHCC and UHCC schemes

Hysteresis band (h)	**SBHCC (Experimental)**		**UHCC (Experimental)**		**Power factor (Experimental)**
	THD (%)	$f_{sw.a}$ (kHz)	THD (%)	$f_{sw.a}$ (kHz)	
0.1	3.7	14.78	2.4	8.2	0.99
0.2	5.2	7.39	4.1	4.11	0.98
0.3	5.5	4.93	4.5	2.74	0.97
0.4	6.1	3.69	5	2.05	0.96
0.5	6.5	2.95	5.2	1.64	0.94

3.7.2 Experimental Investigation under Distorted Supply Voltage

In this case, the performance of the Hilbert transform based ATF control algorithm has been tested under the distorted supply voltage condition. A single-phase diode bridge rectifier with high inductive R-L load is connected near the auto-transformer which creates distortions in the supply voltage. The distorted supply voltage and its harmonic spectrum are shown in Figure 3.21 (a) and (b), respectively. The supply voltage contains harmonics which is recorded THD as 9.6%. Figures 3.21 (c) shows the output waveforms of Hilbert based ATF. It can be concluded from Figure 3.21 (c) that the extracted voltage component from distorted supply voltage using Hilbert transform based ATF is sinusoidal and balanced in nature with zero phase delay. The performance waveforms of V_S, I_S after compensation, I_L and I_C are shown in Figure 3.22 (a). It can be perceived that I_S is sinusoidal even in distorted supply voltage condition. The supply voltage and source current are in-phase after compensation as shown in Figure 3.22 (b). In Figures 3.23 (a) and (b), the power factor before and after compensation respectively, shows that the presented control technique compensated reactive power demand and improved the power factor. The control scheme verified with different gain parameters as shown in Figures 3.24 (a)-(h) with respective harmonic spectrum. It can be concluded from Figures 3.24 (a)-(h) that the Hilbert transform based ATF is robust, effective and works in a wide range of gain parameter values (i. e. 30-70). A complete comparison of different gain parameters in effect of source current THD is

tabulated in Table 3.4 which shows that the source current THD is well within IEEE 519 standards for a wide range of operation of shunt APF.



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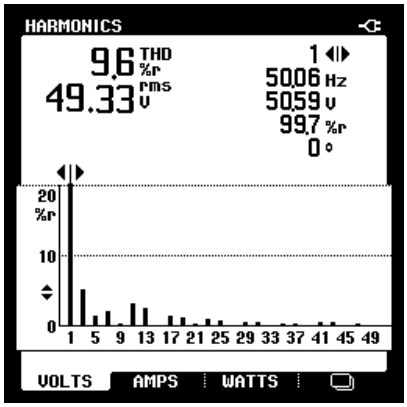

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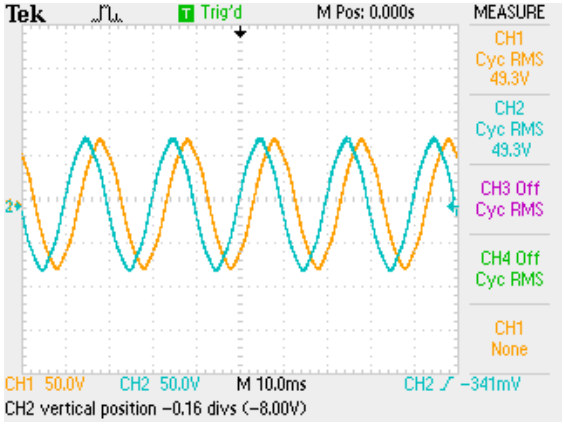
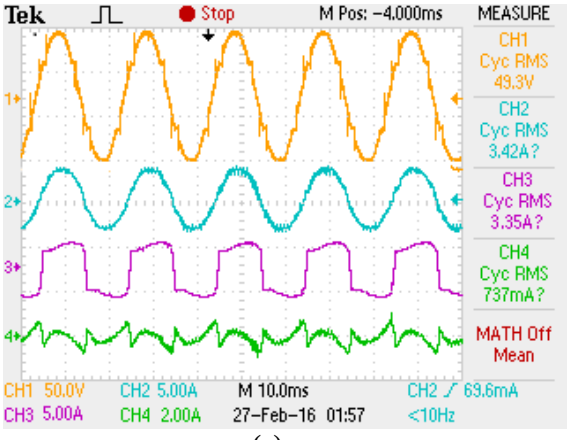


(c)

Figure 3.21 (a) Distorted supply voltage, (b) Harmonic spectrum of supply voltage, and (c) Experimental waveforms of Hilbert transform based ATF output



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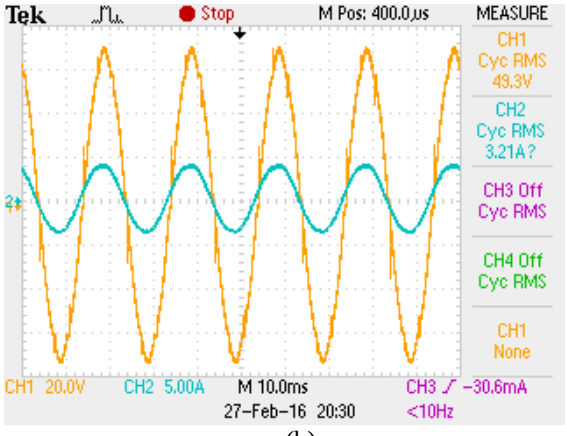
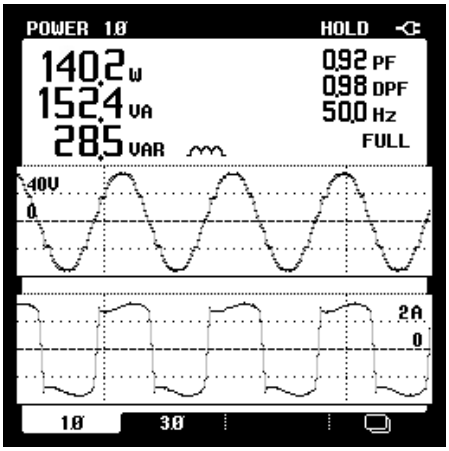
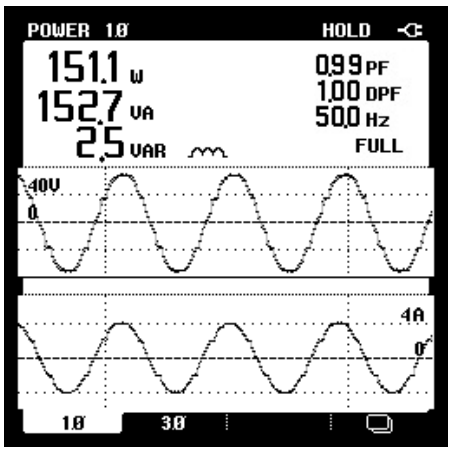


(b)

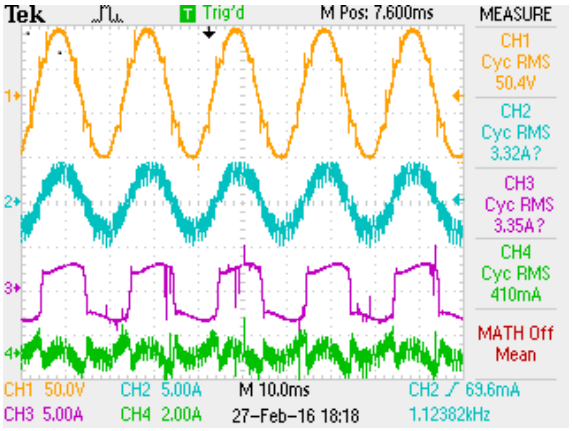
Figure 3.22 Experimental results under distorted supply voltage (a) V_S, I_S, I_L and I_C, and (b) V_S and I_S are in-phase

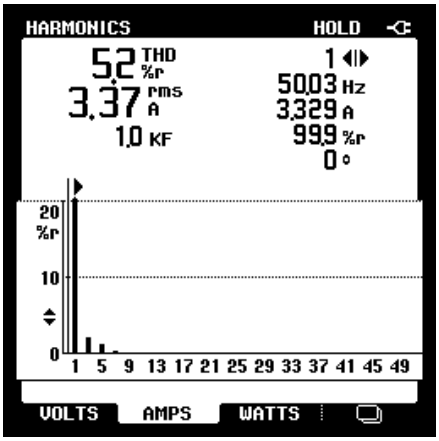




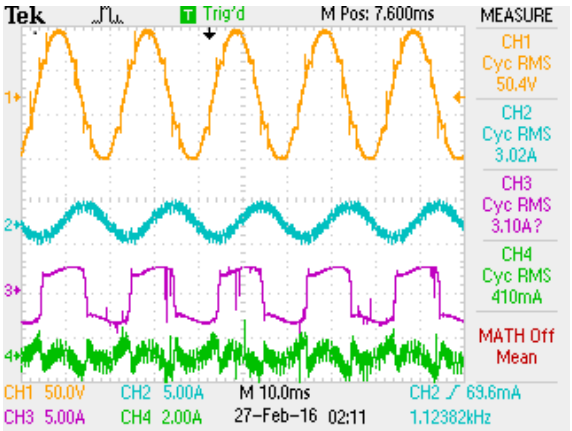
(a) (b)

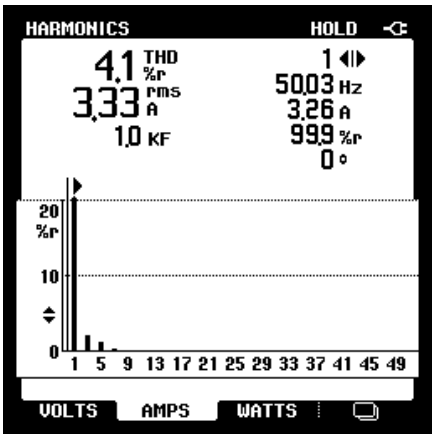
Figure 3.23 Experimental performance of source current with power factor improvement (a) Before compensation, and (b) After compensation



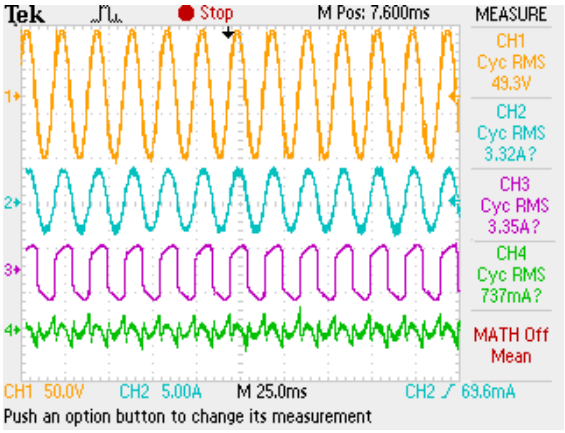


(a) (b)

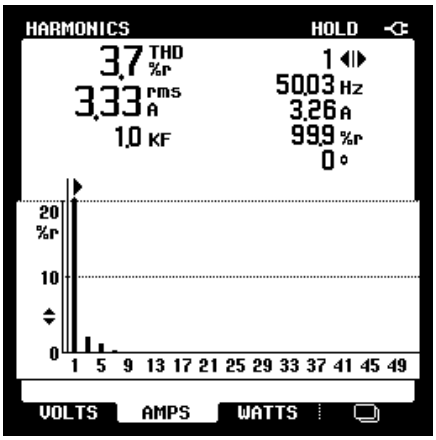




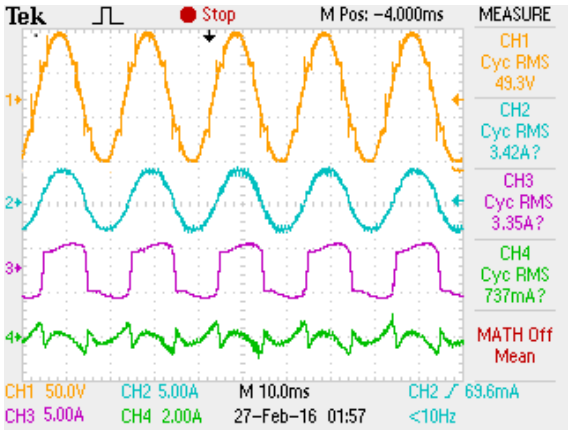
(c) (d)



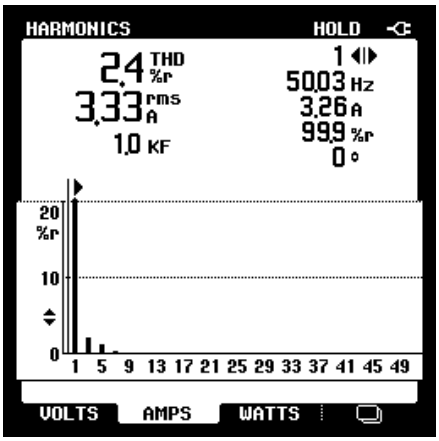
(e)



(f)



(g)



(h)

Figure. 3.24 Experimental waveforms of V_S, I_S, I_L and I_C for altered gain (k) parameters (a) k=100, (c) k=70, (e) k=50, (g) k=30, and (b)-(d)-(f) (h) Represent %THD of compensated source current for different k values

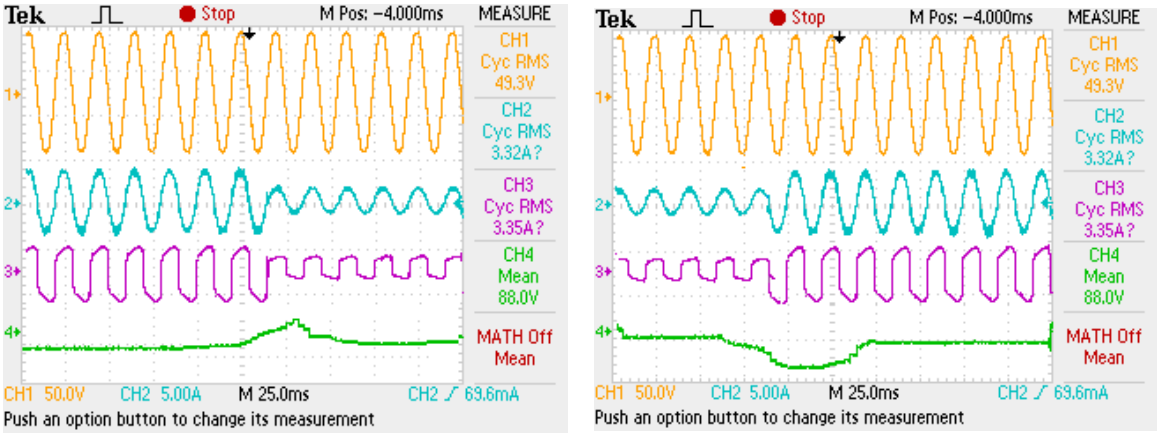
Table 3.4

Simulated and Experimental results of %THD for different values of gain parameters (k)

The gain values	**THD (%) (Simulation)**	**THD (%) (Experimental)**
k_1=100	2.5	5.2
k_2=70	2.3	4.1
k_3=50	1.38	3.7
k_4=30	1.01	2.4
k_5=20	2.5	6.3

3.7.3 Transient Behavior Study in Concern with Distorted Supply Mains

Figures 3.25 (a) and (b) show the transient response of shunt APF under load change with distorted supply voltage condition. The efficiency of control technique is tested in two transient cases. One is load increase and the other one is load decrease. The load current increased from 1.5 A to 3.2 A or decreased from 3.2 A to 1.5 A. To balance the real power between the load demands and supplied by the source can be achieved by DC-link voltage decreases or increases, respectively. This change in DC-link capacitor voltage stabilizes to reference value by PI controller. Figures 3.25 (a) and (b) show the load decrease and load increase, respectively. The DC-link voltage stabilizes at its close reference value due to fast action of controller, which shows the superiority of the controller even in distorted supply voltage condition. It shows the Hilbert transform based ATF control algorithm is robust under varying load conditions.



(a) (b)

Figure 3.25 Load perturbation response under distorted supply mains voltage (a) Step increase in load, and (b) Step decrease in load

3.8 Conclusion

Hilbert transform based ATF control strategy for single-phase shunt APF has been implemented to compensate current harmonics and reactive power burden in the single-phase distribution system. The efficiency of the control algorithm is highly affected by the supply voltage distortions. In order to solve this problem, a Hilbert transform based adaptive tuned filter has been developed to extract the fundamental frequency signal from the distorted supply voltage. Further, the DC link energy balance theorem is implemented

for reference current generation. It gives a reliable solution to the challenging issues of grid synchronization like accurate grid voltage detection, proper gain selection and fast transient response of the tuned filter. A unipolar hysteresis band current controller switching scheme is presented to overcome the switching frequency problems. It uses different hysteresis bands to control the upper and lower switches of the VSI. This approach has successfully reduced the switching frequency and switching frequency variations. Various simulation studies have been accomplished to test the efficiency of the control technique under the steady-state and transient condition of the load for the sinusoidal and distorted supply voltages. The extensive experimental analysis have been carried out by developing a single-phase shunt APF prototype model using the dSPACE1104 controller to validate the simulation results. The simulated and experimental results shows that the Hilbert transform based ATF with UHCC control scheme mitigates the current harmonics, reactive power burden and switching frequency problems under the ideal and distorted sinusoidal voltage conditions with improved power factor.

CHAPTER 4

INTERLEAVED INVERTER BASED SHUNT ACTIVE POWER FILTER

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "PTF based control algorithm for Three-phase Interleaved Inverter based SAPF," *International Journal of Electronics, Taylor & Francis Publications,* Taylor & Francis Publications, Jan. 2019. (In Press)
2. **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Three-Phase Interleaved SAPF with Modified Indirect Current Control Algorithm," *International Journal of Power Electronics*, Inderscience Publishers, Nov. 2018. (In Press)
3. **V. Gali**, N. Gupta and R. A. Gupta, "Predictive Tuned Filter based Reference Current Generation for Shunt Active Power Filter under Distorted and Unbalanced Supply Voltage," in Proc. of IEEE National Power Engineering Conference (NPEC), Thiagarajar College of Engineering, Madhurai, pp. 188-193, March 8^{th} -10^{th}, 2018.
4. **V. Gali**, N. Gupta and R. A. Gupta, "Real-Time Implementation of Shunt Active Power Filter with Enhanced Control Algorithm using dPSACE1104 Controller", in Proc. of dSPACE Academic Conference, Indian Institute of Technology (IIT), Delhi, September 16^{th} , 2017.
5. **V. Gali**, N. Gupta and R. A. Gupta, "Distortion free Improved Reference Current Generation Algorithm for Interleaved Inverter based Shunt APF", in Proc. of 9^{th} IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Indian Institute of Science Bangalore, pp. 1-6, November 8^{th} -10^{th}, 2017.

CHAPTER4

INTERLEAVED INVERTER BASED SHUNT ACTIVE POWER FILTER

4.1 Introduction

Electrical power is distributed to many commercial and industrial applications, through the three-phase system. The modern society has come to depend heavily upon the continuous and reliable availability of electricity. Computer and telecommunication networks, railway network, banking, post offices, emergency medical care centres, defence system, industries, etc. are a few applications that just cannot function without electricity. Apart from that the industrial development totally depends upon the electrical supply and quality of electricity [7].

Continuous proliferation of power electronic based converters in many commercial and industrial applications leads to serious PQ problems in the electrical power system. A three-phase VSI based shunt APF is very popular and a reliable solution to mitigate the PQ problems in the 3P3W and 3P4W electrical distribution system [47]. However, the conventional VSI based shunt APF encounters one of the hazardous conditions i.e. shoot-through problem which further introduces ringing problem, temperature rise in the power switches, causing higher EMI, etc. [67]. The shoot-through mode occurs when the two power switches of the same leg are inadvertently switched ON at the same time period. Therefore, extremely high current flows through it which damage the power devices. To avoid shoot-through problem, a dead-time has been created when both the switches of the same leg are switched OFF. However, adding the dead-time in the switching control signal leads to an increase complexity of the circuit. In addition, the harmonic compensation level decreases, hence decrease the efficiency of the system [68-69]. In contrary to the above issues of shoot-through problems, an interleaved inverter is introduced as a shunt APF in this chapter to mitigate current harmonics and reactive power burden to improve the power factor of the system without shoot-through problems.

4.2 Operating Principle of Interleaved Inverter based SAPF

The interleaved inverter is one of the best topologies over conventional VSI to overcome the shoot-through problems. The effect of dead-band circuitry and operating principle of the interleaved inverter can be elaborated by considering the half-bridge topology in the following sections.

4.2.1 Shoot-through and Dead-Time Effects

The shoot-through defined as when both the upper and lower switches of the same leg being turned on abruptly at the same time, a huge current flows through the circuit which damages the power semiconductor switches. To avoid the shoot-through effect, a dead-time is being introduced in the switching signals. The conventional VSI single-leg and dead-time effect timing diagrams are shown in Figure 4.1 (a) and (b), respectively. The switches (S_1 and S_6) are switched ON and OFF complementarily by each other. The moment S_1 turns OFF, the S_6 starts conducting.

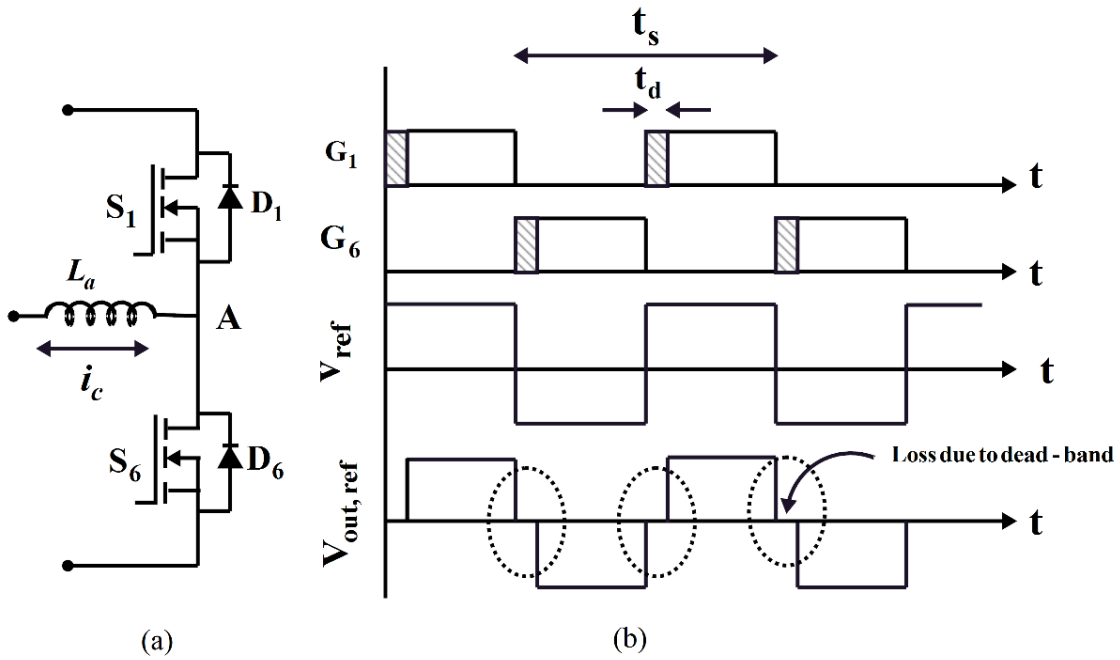


Figure 4.1 Effect of dead-time on conventional voltage source inverter (a) Single-leg, and (b) Timing diagram

Practically, the power electronic switches (either MOSFET or IGBT) are not ideal but having a slow turn of time. Hence, dead-time is necessary for safe operation of the inverter topology. Dead-time is a small interval of time period where both upper and lower switches

of the same leg are OFF. The dead-time provided as shown in Figure 4.1 (b), which decreases the modulated output voltage where the actual output voltage is deviated from the reference output voltage. Further, it introduces magnitude and phase errors in the output voltage, degrades the energy transfer capability and compensation performance in the active power filters.

4.2.2 Description of Interleaved Inverter Cell

The upper and lower cells of interleaved inverter leg are shown in Figure 4.2 (a) and (b), respectively. This interleaved cell consists of one power switch and series diode. The direction of current into the phase-leg is taken as a reference current. If the reference current (or compensating) is positive, the switch S_1 is ON and if the reference current direction is negative, the switch S_1 will be OFF and diode D_1 will be switched ON. It can be observed that this type of connection doesn't lead to any shoot-through problem in the circuit operation.

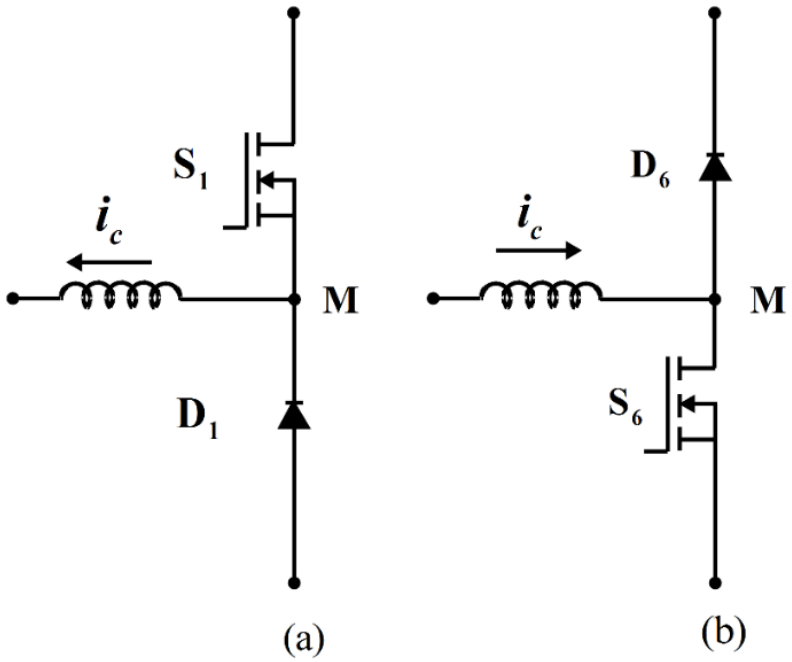


Figure 4.2 Equivalent circuit of interleaved inverter leg (a) Upper cell, and (b) Lower cell

4.2.3 Interleaved Inverter as Shunt APF

The interleaved inverter is introduced as a shunt APF to mitigate current harmonics and reactive power burden to improve the power factor of the system close to unity. The operating principle of the interleaved SAPF relies on the half-bridge topology with four

switching states as shown in Figure 4.3. The capacitor (C_{dc}) is divided into two parts for better understanding, i.e. upper capacitor (C_1) and lower capacitor (C_2) with their capacitor voltages V_{c1} and V_{c2}, respectively. The compensating current (i_{ca}) has two cycles, i.e. positive cycle and negative cycle.

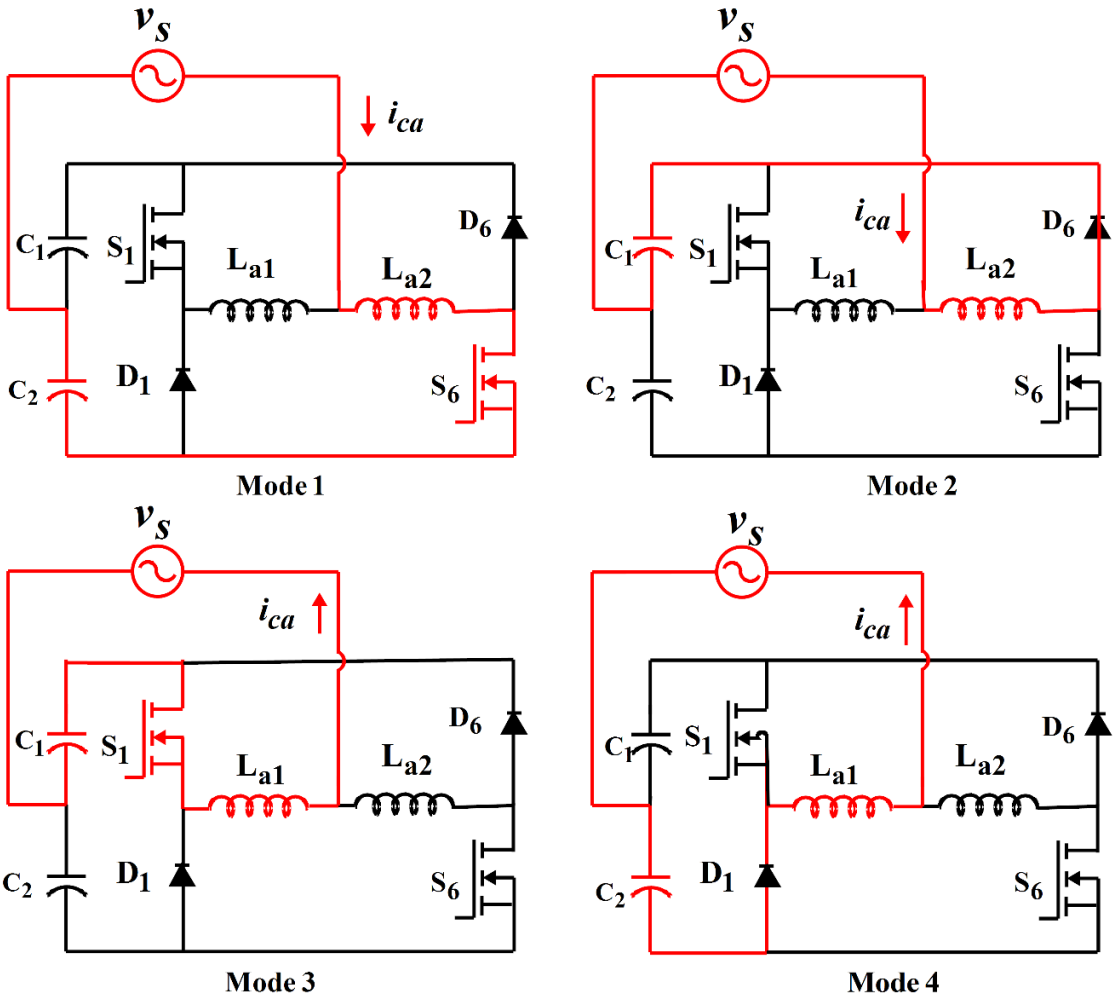


Figure 4.3 Different operating modes of interleaved SAPF

When compensating current is positive during one half-cycle, the following modes can be observed.

Mode 1: The rate of change of compensating current is greater than zero, the switch S_6 is switched ON and C_2 supplies the power.

Mode 2: The rate of change of compensating current is less than zero, the diode D_1 conducts and C_1 is in charging mode.

When compensating current is negative during other half-cycle, mode 3 and mode 4 can be observed as follows:

Mode 3: Switch S_1 is switched ON and C_1 supplies power when rate of change of compensating current is greater than zero.

Mode 4: Diode D_6 conducts, C_2 is in charging mode when the rate of change of compensating current is less than zero.

Similarly, the charging and discharging of the capacitor will be observed from the switching action of other switches (S_2, S_3, S_4, S_5). It is evident from all these four modes of operation that at any instant of time one switch will be in conducting state and all other switches will be in OFF state. Thus, there is no shoot-through mode in the circuit operation. Therefore, the interleaved SAPF works without external dead-band circuit which improves the reliability and efficiency of the system.

4.3 Investigation on Symmetrical Components of Supply Voltage under Distorted and/ or Unbalanced Supply Voltages

The compensated source currents can be balanced, in-phase with supply voltage and harmonic free, if the three-phase supply voltages are balanced and distortions free. Practically, the supply voltage will be distorted and unbalanced due to the large use of non-linear loads. Therefore, the performance of the control algorithm will be degraded and affects the compensation capability of the interleaved SAPF. The symmetrical positive- and negative-sequence components of supply voltages and source currents have been investigated for the three-phase three-wire system to analyse the phase quantities. The unbalanced and/ or distorted voltages and currents include fundamental and harmonic components, respectively. This can be represented as follows:

$$\left.\begin{aligned} v_{sa} &= \underbrace{V_{am1}\sin(\omega t+\theta_{va1})}_{\text{Fundamental component}} + \underbrace{V_{am5}\sin(5\omega t+\theta_{va5})+\sum_{k=7}^{M} V_{amk}\sin(k\omega t+\theta_{vak})}_{\text{Distorted and unbalanced component}} \\ v_{sb} &= \underbrace{V_{bm1}\sin(\omega t+\theta_{va1})}_{\text{Fundamental component}} + \underbrace{V_{bm5}\sin(5\omega t+\theta_{vb5})+\sum_{k=7}^{M} V_{bmk}\sin(k\omega t+\theta_{vbk})}_{\text{Distorted and unbalanced component}} \\ v_{sc} &= \underbrace{V_{cm1}\sin(\omega t+\theta_{vc1})}_{\text{Fundamental component}} + \underbrace{V_{cm5}\sin(5\omega t+\theta_{vc5})\sum_{k=7}^{M} V_{cmk}\sin(k\omega t+\theta_{vck})}_{\text{Distorted and unbalanced component}} \end{aligned}\right\} \quad (4.1)$$

$$\left.\begin{aligned} i_{sa} &= \underbrace{I_{am1}\sin(\omega t+\varphi_{ia1})}_{\text{Fundamental}} + \underbrace{I_{am5}\sin(5\omega t+\varphi_{ia5})+\sum_{k=7}^{M} I_{amk}\sin(k\omega t+\varphi_{iak})}_{\text{Distorted and fundamental component}} \\ i_{sb} &= \underbrace{I_{bm1}\sin(\omega t+\varphi_{ib1})}_{\text{Fundamental}} + \underbrace{I_{bm5}\sin(5\omega t+\varphi_{ib5})+\sum_{k=7}^{M} I_{bmk}\sin(k\omega t+\varphi_{ibk})}_{\text{Distorted and fundamental component}} \\ i_{sc} &= \underbrace{I_{cm1}\sin(\omega t+\varphi_{ic1})}_{\text{Fundamental}} + \underbrace{I_{cm5}\sin(5\omega t+\varphi_{cb5})+\sum_{k=7}^{M} I_{cmk}\sin(k\omega t+\varphi_{ick})}_{\text{Distorted and fundamental component}} \end{aligned}\right\} \quad (4.2)$$

Here, k, s, m, M, θ and φ are the harmonic order, supply, peak value of the signal, upper limit of harmonics, phase angle of supply voltage and currents, respectively. Three voltages are unbalanced, therefore, the Eq. (4.1) and Eq. (4.2) also can be represented as follows:

$$\dot{V}_{sn} = \sum_{k=1}^{M} V_{nmk}\angle\theta_{nk} = \sum_{k=1}^{M}\dot{V}_{nmk}, \qquad \dot{I}_{sn} = \sum_{k=1}^{M} I_{nmk}\angle\varphi_{nk} = \sum_{k=1}^{M}\dot{I}_{nmk} \quad (4.3)$$

The three-phase three-wire system is unbalanced and distorted. Therefore, the supply voltage can be divided into positive- and negative-sequence components. The positive- and negative-sequence components can be represented as follows:

$$\begin{bmatrix} \dot{V}_{a1k} \\ \dot{V}_{a2k} \\ 0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & b & b^2 \\ 1 & b^2 & b \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} \dot{V}_{sak} \\ \dot{V}_{sbk} \\ \dot{V}_{sck} \end{bmatrix} \quad (4.4)$$

Where, the subscripts 1 and 2 represent the positive- and negative-sequence components, respectively. Here, b is the complex operator in the matrix which has the value of $e^{j.2\pi/3}$. The sequence components depend on the value of the harmonic content in the supply voltage. The following analysis has been made by assuming that the fifth and seventh harmonic components are presented in supply along with the fundamental component of voltages. The supply voltage can rewrite as follows:

$$\begin{bmatrix} \dot{V}_{a11} \\ \dot{V}_{a21} \\ 0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & b & b^2 \\ 1 & b^2 & b \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} \dot{V}_{sa1} \\ \dot{V}_{sb1} \\ \dot{V}_{sc1} \end{bmatrix}, \begin{bmatrix} \dot{V}_{a15} \\ \dot{V}_{a25} \\ 0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & b & b^2 \\ 1 & b^2 & b \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} \dot{V}_{sa5} \\ \dot{V}_{sb5} \\ \dot{V}_{sc5} \end{bmatrix},$$
$$\begin{bmatrix} \dot{V}_{a17} \\ \dot{V}_{a27} \\ 0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & b & b^2 \\ 1 & b^2 & b \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} \dot{V}_{sa7} \\ \dot{V}_{sb7} \\ \dot{V}_{sc7} \end{bmatrix} \quad (4.5)$$

The inverse transformation of the Eq. (4.4) can be written as shown in Eq. (4.6) with three-sets of voltages

$$\begin{cases} v_{sak} = V_{a1k}\sin(k\omega t + \theta_{1k}) + V_{a2k}\sin(k\omega t + \theta_{2k}) \\ v_{sbk} = V_{b1k}\sin(k\omega t + \theta_{1k} - 2\pi/3) + V_{b2k}\sin(k\omega t + \theta_{2k} + 2\pi/3) \\ v_{sck} = V_{c1k}\sin(k\omega t + \theta_{1k} + 2\pi/3) + V_{c2k}\sin(k\omega t + \theta_{2k} - 2\pi/3) \end{cases} \quad (4.6)$$

As per the symmetrical sequence component theory,

$$\begin{aligned} V_{a1k} &= V_{b1k} = V_{c1k} \\ V_{a2k} &= V_{b2k} = V_{c2k} \end{aligned} \quad (4.7)$$

$$\begin{cases} v_{sak}(t) = V_{a1k}\sin(k\omega t + \theta_{1k}) + V_{a2k}\sin(k\omega t + \theta_{2k}) \\ v_{sbk} = V_{a1k}\sin(k\omega t + \theta_{1k} - 2\pi/3) + V_{a2k}\sin(k\omega t + \theta_{2k} + 2\pi/3) \\ v_{sck} = V_{a1k}\sin(k\omega t + \theta_{1k} + 2\pi/3) + V_{a2k}\sin(k\omega t + \theta_{2k} - 2\pi/3) \end{cases} \quad (4.8)$$

The above three-phase equations are the sum of distorted positive- and negative-sequence voltage components but, balanced three-phase system. The balanced positive-sequence components of voltages can be used for the further process of reference source current generation. The three-phase positive-sequence component of voltages $\ddot{v}_{sak}$, $\ddot{v}_{sbk}$, $\ddot{v}_{sck}$ written as follows:

$$\begin{cases} \ddot{v}_{sak}(t) = V_{a1k}\sin(k\omega t + \theta_{1k}) \\ \ddot{v}_{sbk}(t) = V_{a1k}\sin(k\omega t + \theta_{1k} - 2\pi/3) \\ \ddot{v}_{sbk}(t) = V_{a1k}\sin(k\omega t + \theta_{1k} + 2\pi/3) \end{cases} \quad (4.9)$$

The above three-phase equations are balanced however, it contains 5^{th} and 7^{th} harmonic components. Hence, before processing these signals further, the fundamental frequency component of the voltage signal has to be extracted by a fundamental frequency signal extraction technique.

4.4 Control Scheme for Three-Phase Interleaved SAPF

The three-phase interleaved SAPF works to improve the wave shape of supply currents that are to be in-phase and well balanced with the supply voltages irrespective of the non-linear load characteristics with shoot-through protection. To improve the performance of the system under distorted and unbalanced supply voltages, the control technique has been divided into three major parts. The first includes the calculation of the positive-sequence component using instantaneous symmetrical component theory. Secondly, the elicitation of the fundamental component of the voltage signal from the positive-sequence component of the supply voltage is achieved by predictive tuned filter (PTF). The third is to calculate the reference current generation using instantaneous reactive power theory (IRPT) which is also known as generalized *p-q* theory. Further, the switching pulse generation is achieved by hysteresis current controller.

4.4.1 Predictive Tuned Filter based Fundamental Frequency Signal Extraction Technique

The electrical power system network loads vary with time, therefore the distortion level in the supply voltage varies in terms of frequency and amplitude. The predictive filter is designed for eliciting the fundamental frequency voltage signal from the distorted voltage. This filter is sensitive to detect time-varying distortions in the supply voltage and calculate accurately in terms of magnitude and frequency. It has simple structure with simple gain and integral blocks. Therefore, the computational time on the dSPACE1104 DSP processor will be less which enhances the real-time operation. This filter calculates fundamental component along with DC component in-phase and quadrature component of the supply voltage. The signal is periodic in nature and angular frequency of ω_1 having harmonics with dc bias. The N-dimensional vector is modelled as the sum of signal $z_0(t)$ and sine waves $z_p(t)$ of angular frequencies $p^*\omega_1$ as follows:

$$z(t) = [z_0(t), z_1(t), z_2(t), z_3(t), ...z_p(t)....z_N(t)] \tag{4.10}$$

$$z(t) = \sum_{p=0}^{p=N} z_p(t) \tag{4.11}$$

The outputs $z_{p(t)}$ derive from the dc block, a fundamental ($\dot{x}(t)$) and the N-1 harmonic oscillators $z(t)$, the state space model can be written as follows:

$$\begin{aligned} \dot{x}(t) &= B * x(t) \\ Z(t) &= F^t(t) * x(t) \end{aligned} \tag{4.12}$$

Where, B is an N-dimensional matrix can be represented as follows:

$$\begin{bmatrix} B_0 & 0 & 0 & - & 0 & - & 0 \\ 0 & B_1 & 0 & - & 0 & - & 0 \\ 0 & 0 & B_2 & - & 0 & - & 0 \\ - & - & - & - & - & - & - \\ 0 & 0 & 0 & - & B_p & - & 0 \\ - & - & - & - & - & - & - \\ 0 & 0 & 0 & - & 0 & - & B_N \end{bmatrix}; \quad B_0 = 0 \tag{4.13}$$

The p[th] sub-block in the B matrix is defined as:

$$B_p = \begin{bmatrix} 0 & j.\omega \\ -j.\omega & 0 \end{bmatrix} \tag{4.14}$$

$$[F]^t = [1\,1\,0\,1\,0 - - - 1\,0] \tag{4.15}$$

The p[th] sub-block is defined as:

$$\begin{aligned} \dot{x}_p(t) &= B_p x_p \\ z_p(t) &= F_p^t x_p \end{aligned} \tag{4.16}$$

Where, p=0, 1, 2,….N; and $F_p^t = [1\ 0]$; The state vector $x_p(t)$ and the output $z_p(t)$ of the sub-block are as follows:

$$x_p(t) = \begin{bmatrix} x_{p1}(t) \\ x_{p2}(t) \end{bmatrix} \tag{4.17}$$

Where, $z_p(t) = x_{p1}(t)$, the PTF has to be modelled for the closed loop linear system for estimating the harmonics of N+1 variables. The open-loop blocks of N+1 variables are organised in the parallel format as shown in Figure 4.4. The dc block consists of output $\dot{z}_0(t)$ from the G_0 and one state variable. Therefore, each of N block contains of one output variable and two state variables. The p[th] block has two state variables ($\dot{x}_{p1}, \dot{x}_{p2}$) and output variables $\dot{z}_p(t) = \dot{x}_{p1}$. Similarly, the N state variables, $[\dot{x}_{12}, \dot{x}_{22}, \dot{x}_{32} \ldots\ldots\ldots\ldots \dot{x}_{N2}]$ are orthogonal signals, which shifts various estimated harmonics in 90º out of phase. The scalar output of PTF for N+1 individual output variables is as follows:

$$\dot{z}(t) = \sum_{p=0}^{p=N} \dot{z}_p(t) \tag{4.18}$$

The closed-loop system error can be defined as

$$e(t) = [z(t) - \dot{z}(t)] \tag{4.19}$$

The PTF can be modelled as follows:

$$\begin{aligned} \dot{\hat{x}} &= B_p \dot{x}_p + D_p e(t) \\ \dot{z}(t) &= F_p^t \dot{x}_p; \quad p = 0,1,2,3,.....N \end{aligned} \tag{4.20}$$

The filter can be defined briefly as follows:

$$\begin{aligned} \dot{\hat{x}} &= B \dot{x} + De(t) \\ \dot{z}(t) &= F^t \dot{x}; \quad p = 0,1,2,3,.....N \end{aligned} \tag{4.21}$$

Where, D is the gain vector. The total PTF error ($\dot{E}$) can be defined as follows:

$$\dot{E}(t) = \left[B - DF^t \right] * E(t) \tag{4.22}$$

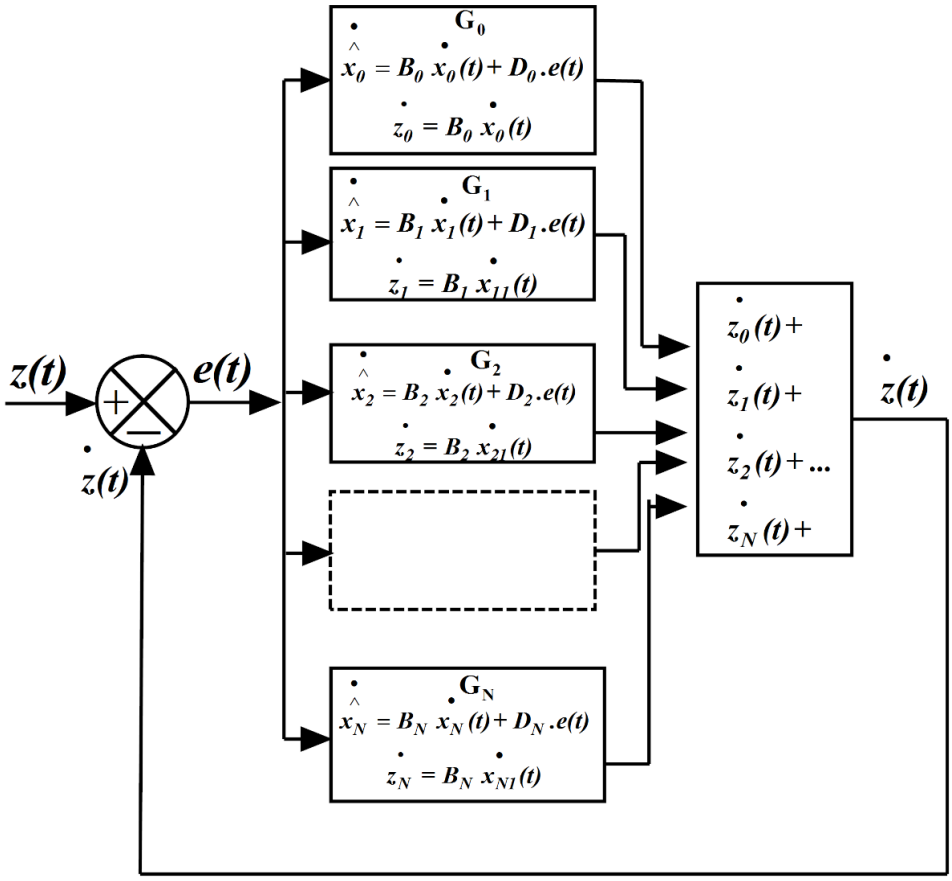


Figure 4.4 Structure of predictive tuned filter

The above error differential equation has (2N+1) roots, called PTF poles. These PTF poles located in the left side of the s-plane. Therefore, the magnitude of the individual error components will vanish exponentially. The sum of output variables of the various blocks of the PTF i.e $\dot{z}(t) = \left[\dot{\hat{x}}_0, \dot{\hat{x}}_{11}, \dot{\hat{x}}_{31} \dot{\hat{x}}_{41}, \ldots\ldots \dot{\hat{x}}_{p1}, \ldots\ldots \dot{\hat{x}}_{N1}, \right]^t$ is unify with the dc component and N-1 harmonic components. Therefore, the elicited harmonics are sine waves with different frequencies. The individual block would be controlled and tuned to various harmonic components. The harmonics are fixed at (p*f) Hz, p= 2, 3…….N. The PTF will be tracking these harmonic signals. The parameters are selected after observing the steady-state behaviour of the supply fundamental voltage, which are fully controllable and observable. The block diagram of PTF as shown in Figure 4.5, is used for extraction of fundamental frequency voltage signal from the distorted three-phase supply voltages. The gain G (s) is the open-loop gain of the PTF. Hence, the mason's gain formula is used for obtain open loop gain of PTF as follows:

$$\frac{\hat{v}_\alpha}{v_\alpha} = \frac{\frac{k}{s} + \frac{k\omega}{s^4}}{1 - \left\{ \frac{-k}{s} - \frac{\omega^2}{S^6} - \frac{k\omega}{S^4} \right\}} \tag{4.23}$$

$$\frac{\hat{v}_\alpha(s)}{v_\alpha(s)} = \frac{\frac{k}{s} + \frac{k\omega}{s^4}}{1 - \left\{ \frac{-k}{s} - \frac{\omega^2}{S^6} - \frac{k\omega}{S^4} \right\}} = \left[\frac{G(s)}{1 + G(s)} \right] \tag{4.24}$$

$$G(s) = \left[\frac{kS^5 + k\omega S^2}{S^6 + \omega^2} \right] \tag{4.25}$$

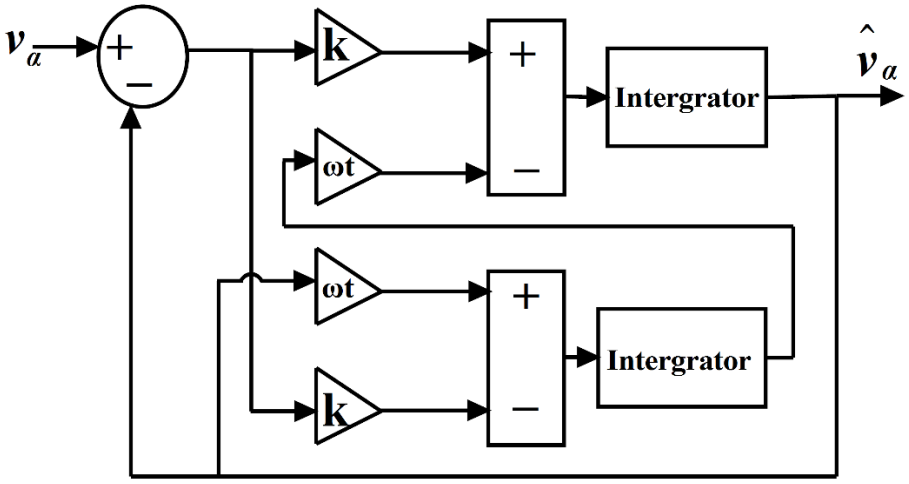
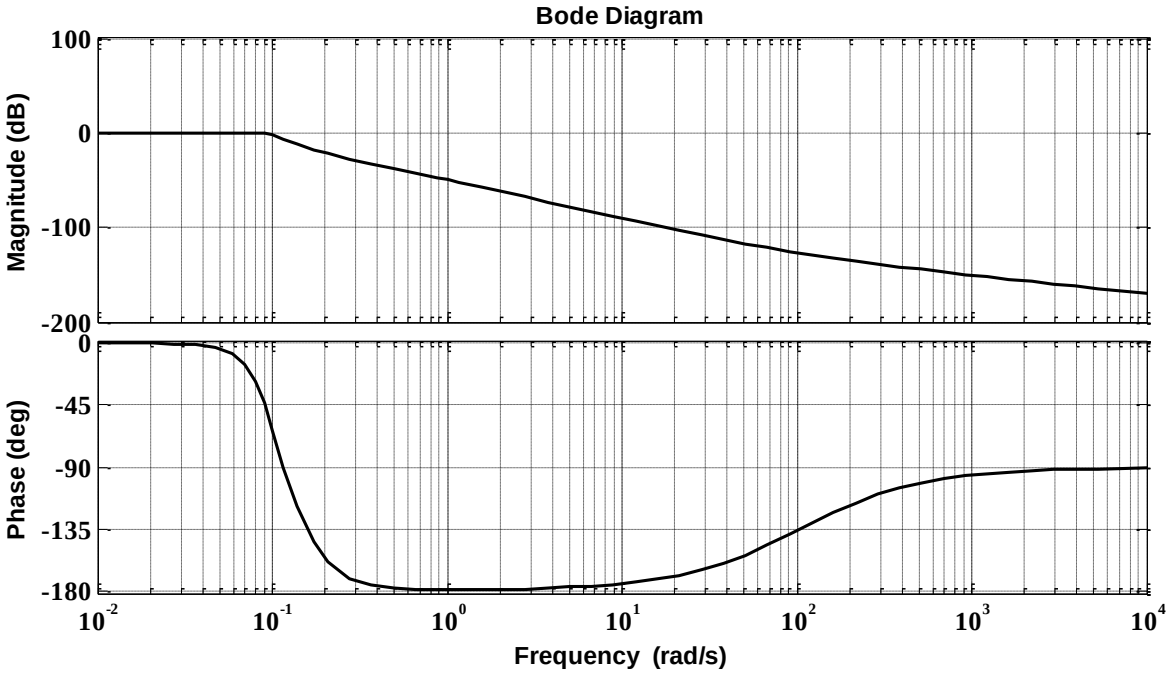


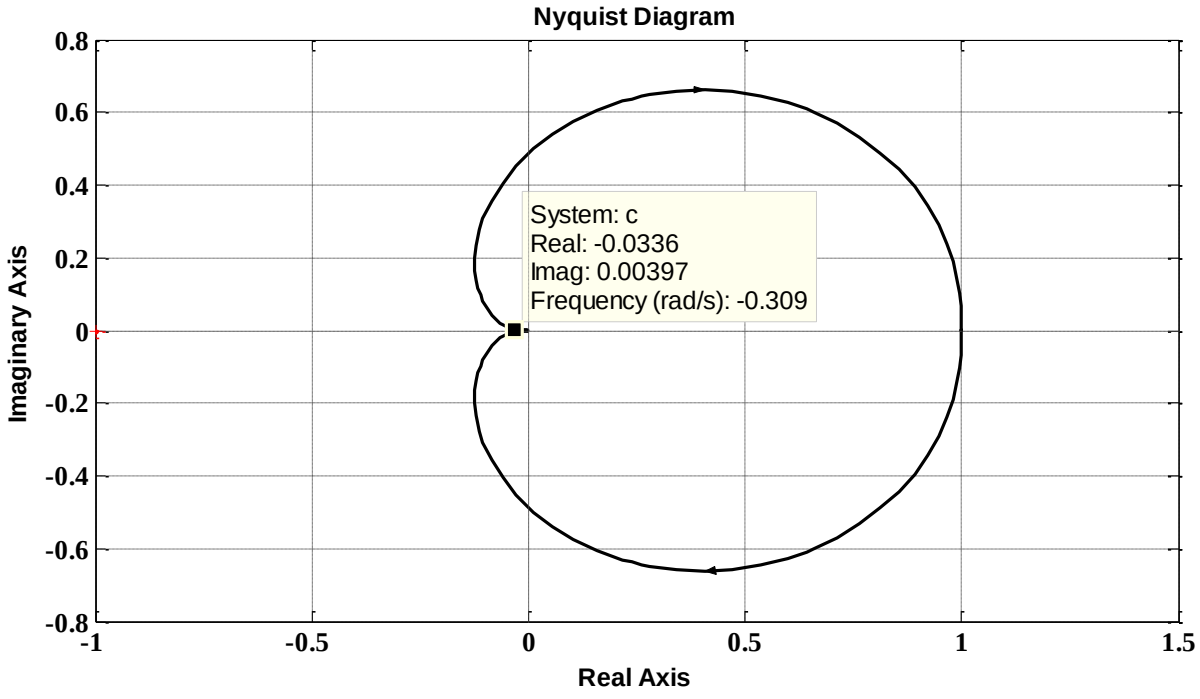
Figure 4.5 Block diagram of predictive tuned filter

The Bode and Nyquist plots are shown in Figure 4.6 (a) and (b), respectively. According to bode plot in Figure 4.6 (a), by increasing the phase margin, the response of the system will be improved with less overshoot and ringing. The phase margin is chosen 68º for the gain of 35 which gives the better response and minimum ripples in the extracted supply voltage. It is evident from Nyquist stability criteria in Figure 4.6 (b), the number of encirclement encloses the entire right half plane and therefore, the system is stable. The PTF poles are lying on the *s*-plane. The speed of process and bandwidth will increase with a constant factor in the real part of the PTF poles for different orders of harmonics. It is concluded from Eq. (4.23)-(4.25) that the selected real-part poles are 38, -3 for elicitation of fundamental frequency voltage components. The controllability and observability for the selected control parameters of the system, have been analysed. These values are selected

after analysing the steady-state behaviour of the estimated fundamental supply voltages. This PTF is used for extraction of fundamental frequency supply voltages in three-phases.



(a)



(b)

Figure 4.6 (a) Bode plot for the predictive tuned filter, and (b) Nyquist plot

4.4.2 Reference Current Generation using Three-Phase *p-q* theory

The instantaneous reactive power theory which is also called as three-phase *p-q* theory, developed by Akagi et al. in 1983 [17]. The idea behind this theory is that first instantaneous powers are calculated by transforming instantaneous voltages and currents of a-b-c coordinates to $\alpha-\beta$ coordinates by using Clarke's transformation as follows:

$$\begin{bmatrix} \bar{v}_\alpha \\ \bar{v}_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sa1} \\ v_{sb1} \\ v_{sc1} \end{bmatrix} \tag{4.26}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4.27}$$

The instantaneous active and reactive powers are calculated as follows:

$$p_L = \bar{v}_\alpha i_\alpha + \bar{v}_\beta i_\beta \tag{4.28}$$

$$q_L = \bar{v}_\alpha i_\beta - \bar{v}_\beta i_\alpha \tag{4.29}$$

The total instantaneous active and reactive powers can be disintegrated into fundamental and harmonic powers as follows:

$$p_L = \bar{p}_L + \tilde{p}_L = p_{DC} + p_{AC} \tag{4.30}$$

$$q_L = \bar{q}_L + \tilde{q}_L = q_{DC} + q_{AC} \tag{4.31}$$

It is clear from the Eq. (4.30) and Eq. (4.31) that p_{DC} and q_{DC} are the fundamental component of load active and reactive powers, respectively. Two possible approaches are presented in the literature using *p-q* theory to compensate reactive and harmonic currents which are direct and indirect current control techniques. In the direct current control technique, the reference currents are generated in terms of APF currents whereas in indirect current control (ICC) technique, reference currents are generated in terms of source currents. Indirect current control technique approach has been implemented in this chapter because of its advantages such as reduced sensor requirement, direct use of generated reference

source currents, etc. An LPF is introduced to separate the DC and AC components of instantaneous active powers in indirect current controller which is called as modified indirect current controller (MICC). An LPF has been designed in such a way that it eliminates the switching notches and distortions from the instantaneous active power which further help to generate the distortions free reference source currents. A detailed design of LPF is enumerated in the following section.

In addition, a fair comparison study of ICC and MICC techniques are observed in terms of performance improvement.

Design of Low Pass Filter

A LPF is being used for separating the instantaneous real power into two components, dc component of power ($\bar{p}$) and ac component of power ($\tilde{p}$). The transfer function of LPF can be written as follows:

$$H(s) = \frac{\mathrm{r}(s)}{x(s)} = \frac{\omega_c}{\mathrm{s} + \omega_c} \tag{4.32}$$

Where, ω_c is the cut-off frequency. The *s*-plane of Eq. (4.32) can be converted into *z*-plane by using bilinear transformation.

$$\mathrm{s} = \frac{2}{\mathrm{T}}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right) \tag{4.33}$$

Where, T is the sampling time, it has to be set for real-time implementation of interleaved SAPF. Substitute the value of s in the Eq. (4.33), the transfer function becomes as follows:

$$H(s) = \frac{r(s)}{x(s)} = \frac{\omega_c}{\omega_c + \frac{2}{\mathrm{T}}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)} \tag{4.34}$$

Rewriting the Eq. (4.35) as follows:

$$H(s) = \frac{r(s)}{x(s)} = \frac{\omega_c}{\omega_c + \frac{2}{\mathrm{T}}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)} = \frac{\omega_c \mathrm{T}\left(1 + z^{-1}\right)}{\omega_c \mathrm{T}\left(1 + z^{-1}\right) + 2\left(1 - z^{-1}\right)}$$

$$r(s)*\left\{\omega_c T\left(1+z^{-1}\right)+2\left(1-z^{-1}\right)\right\}=x(s)*\left\{\omega_c T\left(1+z^{-1}\right)\right\}$$

$$r(s)*\left\{\omega_c T+\omega_c T z^{-1}+2-2z^{-1}\right\}=x(s)*\left\{\omega_c T+\omega_c T z^{-1}\right\}$$

$$r(s)*\left\{z^{-1}\left(\omega_c T-2\right)+\omega_c T+2\right\}=x(s)*\left\{\omega_c T+\omega_c T z^{-1}\right\}$$

$$r(s)z^{-1}\left(\omega_c T-2\right)+r(s)\left(\omega_c T+2\right)=x(s)\omega_c T+x(s)\omega_c T z^{-1}$$

$$r(s)=\frac{-\left(\omega_c T-2\right)}{\left(\omega_c T+2\right)}r(s)z^{-1}+x(s)\omega_c T+x(s)\omega_c T z^{-1}$$

Now, convert into to time domain as follows:

$$\begin{aligned} r(\mathrm{n}) &= \frac{-\left(\omega_c T-2\right)}{\left(\omega_c T+2\right)}r(\mathrm{n}-1)+x(\mathrm{n})\omega_c T+x(\mathrm{n}-1)\omega_c T \\ &= \frac{-\left(\omega_c T-2\right)}{\left(\omega_c T+2\right)}r(\mathrm{n}-1)+\left\{x(\mathrm{n})+x(\mathrm{n}-1)\right\}\omega_c T \end{aligned} \tag{4.35}$$

T=0.1μs and the cutoff frequency 5 Hz to 20 Hz are taken for the modified control algorithm. The bode diagram is plotted for different LPF cutoff frequency as shown in Figure 4.7.

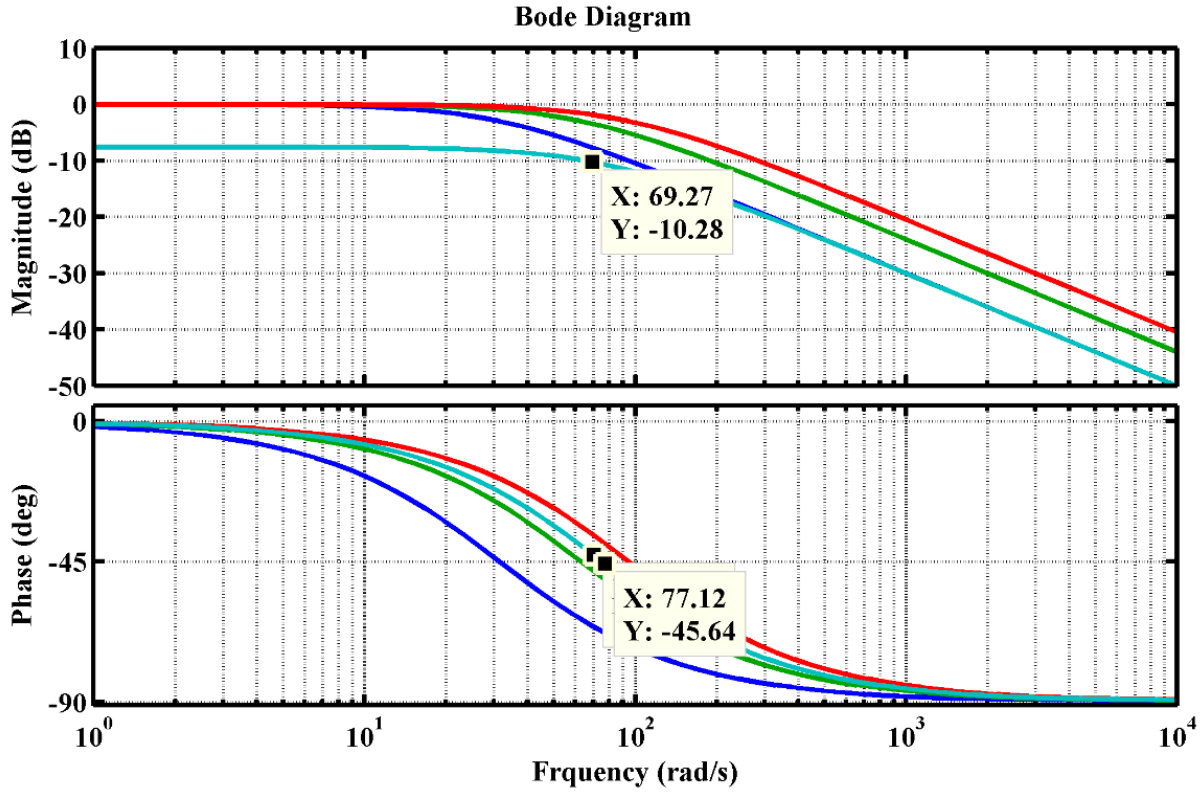


Figure 4.7 Bode plot for low pass filter with different cutoff frequencies

It is observed from Figure 4.7 that, the LPF works well at cut off frequency of 10.28 Hz and phase angle of 45.64º by eliminating the notches due to switching and ripples from the reference source current.

$$\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = \frac{1}{\bar{v}_\alpha^{\,2} + \bar{v}_\beta^{\,2}} \begin{bmatrix} \bar{v}_\alpha & \bar{v}_\beta \\ \bar{v}_\beta & -\bar{v}_\alpha \end{bmatrix} \begin{bmatrix} p_{DC} + p_{DC\_Link} \\ 0 \end{bmatrix} \tag{4.36}$$

Where, $i_{s\alpha}$ and $i_{s\beta}$ are reference source current in α-β coordinates. The p_{DC_Link} is the active power enforced to retain DC-link voltage at a reference value. A Proportional-integral (PI) controller is used for regulating the DC-link voltage which enhances the operation of shunt APF. The PI gain parameters K_p and K_i are chosen as 0.7 and 2.4, respectively from table 4.1. The reactive load component q_L is kept zero. Since, the source should supply only active load power. The three-phase reference source currents are generated by using inverse transformation by converting α-β to a-b-c coordinates as follows:

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{4.37}$$

The error will be generated by comparing the reference source currents with the actual source currents. This error is processed through hysteresis current controller which produces switching pulses for the interleaved inverter based SAPF.

Table 4.1

Selection of K_p and K_i values

K_p	**K_i**	**% Overshoot**	**Settling time (sec.)**
0.11	1.14	10.21	0.071
0.23	1.36	12.17	0.056
0.45	1.95	5.12	0.023
0.70	2.40	3.65	0.012
0.81	2.85	6.70	0.027
0.96	3.21	11.87	0.081

4.5 Design of Three-Phase Interleaved SAPF Parameters

The three-phase interleaved SAPF design comprises of interleaved inverter switches, DC-link capacitor, DC-link voltage, and interfacing inductor. The rating of interleaved SAPF is depend on the nonlinear load parameters with harmonic and reactive power compensation requirement. Hence, the selection of power electronic switch rating, DC-link capacitor and interfacing inductors are the key elements in the interleaved SAPF system.

Selection of Interleaved Inverter Switch

The interleaved inverter switch has to be selected precisely which is able to handle the maximum voltage stress during turn off period and maximum amount of current flowing during turn-on period. The power MOSFET switches have been proven prominent features like high power handling capability with high switching frequency. The voltage rating (V_d) and current rating (I_d) is as follows [8]:

$$V_d = V_{dc} + V_{dx} \tag{4.38}$$

$$I_d = 1.25 * (I_{cr\text{-}pp} - I_p) \tag{4.39}$$

Where,

V_{dx} = 10% of DC-link voltage overshoot

$I_{cr\text{-}pp}$ = current ripple,

I_P = peak value of phase current

Selection of DC-link capacitor voltage (V_{dc})

The DC-link voltage defines the rating of the interleaved SAPF. The minimum DC-link voltage has to be maintained for efficient operation of filter. In contrary, above the value of maximum voltage causes to increase voltage stress on power switches. Hence, the selection of DC-link voltage value is an important factor in the design of interleaved SAPF. The DC-link voltage value can be calculated as follows [8]:

$$V_{dc} \geq \frac{2\sqrt{2}V_L}{\sqrt{3}m} \tag{4.40}$$

Where, m is the modulation index, V_L is the line voltage, V_{dc} is the DC-link voltage

Selection of DC-link capacitor (C_{dc})

The DC-link capacitor serves two purposes in the operation of interleaved SAPF, it act as an active source to the interleaved inverter to supply sufficient amount of compensating currents and difference of real power demand required by the nonlinear load during transient condition of load. The DC-link capacitor has be chosen as follows [8]:

$$C_{dc} = \frac{E_1 * 6 * V_{rms} * I_p * a * t}{(V_{dc}^2 - V_{dc,\,ref}^2)} \tag{4.41}$$

Where,

V_{dc} = Minimal DC-link voltage

$V_{dc,ref}$ = reference DC-link voltage

V_{rms} = Phase RMS voltage

E_1 = Energy variation during transients

a = loading factor

t = DC-link voltage recovery time

I_p = phase current of interleaved inverter

Selection of Interfacing Inductor (L_f)

The interfacing inductor (L_f) is considerably used as a medium between interleaved SAPF and grid to transfer the energy. The switching frequency of SAPF and voltage across the inductor limits the wave shape of current. The interfacing inductor calculates as follows [5]:

$$L_f = \frac{\sqrt{3} * V_{dc}}{(12 * a * f_s * I_{cr\text{-}pp})} \tag{4.42}$$

Where,

a = loading factor

m = modulation index

f_s = switching frequency

$I_{cr\text{-}pp}$ is the current ripple across inductor

V_{dc} = DC-link voltage

4.6 System Modelling using MATLAB®/ Simulink Software

In order to test the compensation capability, the three-phase interleaved inverter based SAPF is modelled using MATLAB®/ Simulink software. A three-phase full wave controlled and uncontrolled bridge rectifiers with R-L loads are used as non-linear loads to test the robustness and effectiveness of interleaved inverter based SPAF. This non-linear load distort the source current waveform into non-sinusoidal due to injecting the harmonics and draws the reactive power from the system. The designed parameters of three-phase interleaved inverter based SAPF are tabulated in Appendix-B2. The simulation study has been carried out to test the effectiveness of interleaved inverter topology and control strategy.

4.6.1 Simulation Results for Different Supply Voltage and Non-Linear Load

A detailed simulation study of the three-phase interleaved SAPF is carried out to investigate the performance of interleaved SAPF. Different simulation studies have been carried out under sinusoidal, distorted, and distorted-unbalanced supply voltage conditions with controlled and uncontrolled rectifiers with R-L loads.

4.6.1.1 Simulation Results with Sinusoidal Supply Voltage

4.6.1.1.1 Switch Current Loss Analysis of Conventional VSI and Interleaved Inverter Based SAPF

The switch current loss analysis of conventional VSI and interleaved inverter based SAPF are analyzed to prove the novelty of the topology over conventional VSI. Figure 4.8 shows the relation between the polarities of the phase 'A' source current and phase 'A' compensating current waveforms of conventional VSI with switching operation. The compensating current of two cycles, i.e. positive and negative half cycles. During the positive half cycle of phase 'A' source current, when the rate of change of compensating current is greater than zero, D_6 (body diode of S_6) will be turned ON and capacitor charges. When the rate of change of compensating current is less than zero, S_1 will be turned ON and capacitor supplies the compensating current. Similarly, during the negative half cycle, when the rate of change of compensating current is less than zero, D_1 (body diode of S_1) will be turned ON and capacitor charges. When the rate of change of compensating current

is greater than zero, S_6 will be turned ON, and the capacitor supplies the compensating current. The same operating states can be applied to phase 'B' and phase 'C', respectively. It is observed from the above operation of conventional VSI based SAPF that as soon as the power switches (either S_1 or S_6) are ON or OFF, the body diodes (either D_1 or D_6) of the same leg will be switched ON or OFF for charging. Hence, there is a chance of shoot-through phenomena without the dead-band circuit. Since, the turn-ON time is small compared to turn OFF time of any power electronic device (either MOSFET or IGBT). Therefore, interleaved inverter topology is presented in the application of active filters.

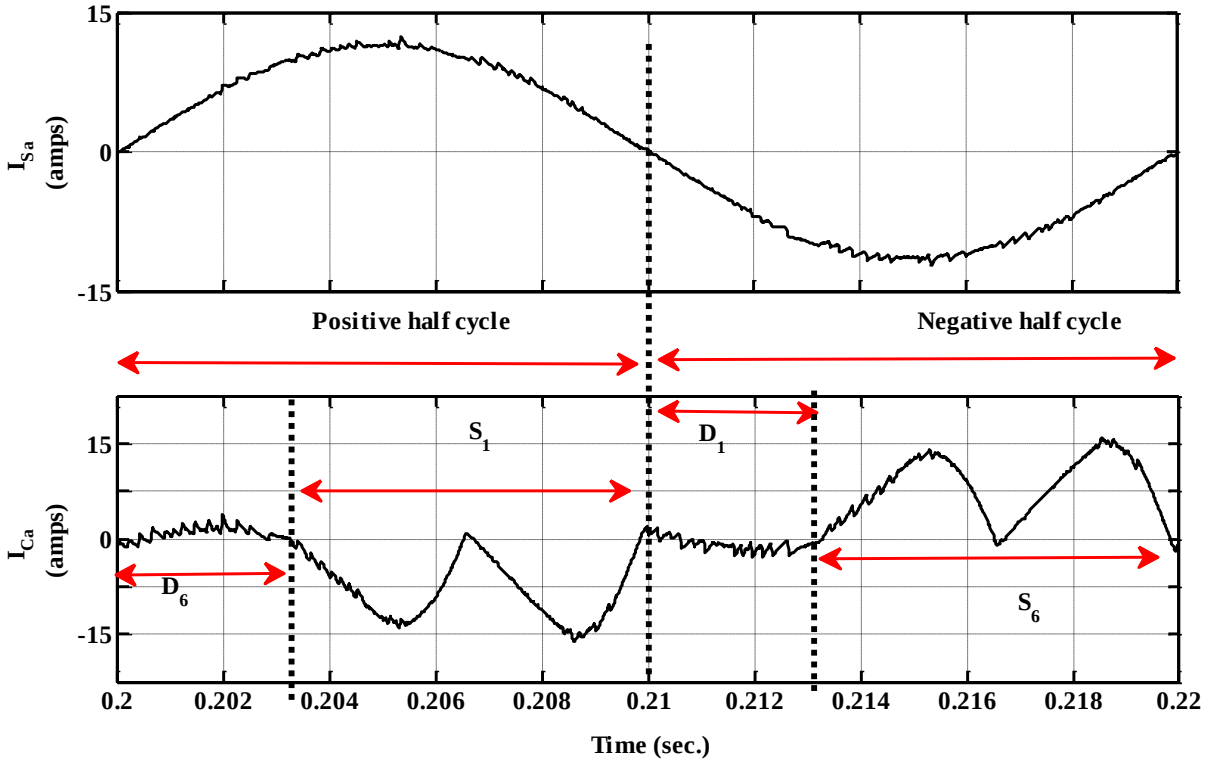


Figure 4.8 Conventional VSI switch current waveform

The construction of the interleaved inverter is different from the conventional VSI. Hence, the charging of a capacitor through power diodes of inverter leg (not body diodes of MOSFET) and discharging of the capacitor is through MOSFET switches. Figure 4.9 shows the phase 'A' source current and compensating current waveforms with respect to the switching action of the interleaved inverter based SAPF switches.

During the positive half cycle: When the rate of change of compensating current is less than zero, S_6 will be turned ON and capacitor supplies the compensating current.

When the rate of change of compensating current is greater than zero, D_6 will be turned ON and the capacitor charges.

During the negative half cycle: When the rate of change of compensating current is greater than zero, S_1 will be turned ON and the capacitor supplies the compensating current. When the rate of change of compensating current is less than zero, D_1 will be turned ON and the capacitor charges.

It is observed from the operation that the capacitor charges through series connected diodes instead of body diodes of MOSFETs. Hence, the switches S_1 and S_6 are never get a chance to conduct at the same time, which ensures the safe switching operation of power MOSFETs and no shoot-through phenomena.

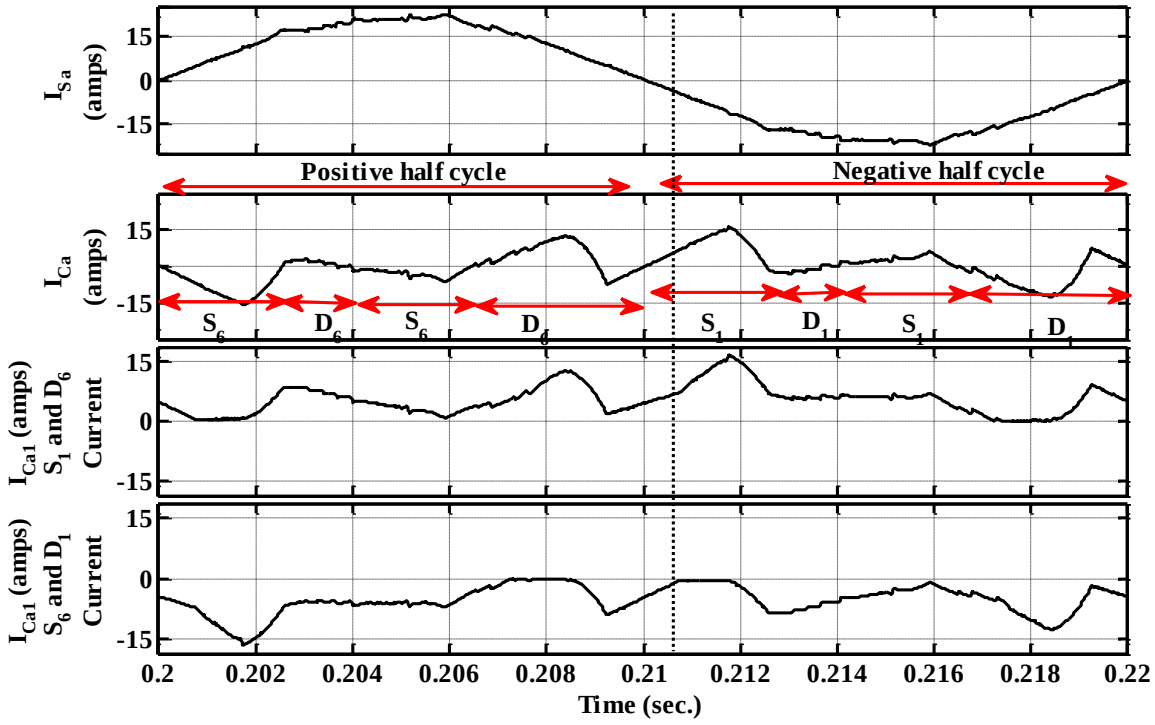


Figure 4.9 Analysis of interleaved inverter based SAPF switch current waveform

4.6.1.1.2 Diode Bridge Rectifier with R-L Load

The compensation effectiveness and robustness of the three-phase interleaved inverter based SAPF over conventional VSI based SAPF is tested under the sinusoidal three-phase supply voltage condition. The diode bridge rectifier with R-L load is connected as non-linear load which pollutes the power system network by injecting the current harmonics and draws the reactive power, thus leads to poor power factor. The performance parameters

of the three-phase supply voltages (V_S), source current (I_S), phase 'A' load current (I_{La}) and phase 'A' compensation current (I_{ca}) under the sinusoidal supply voltages are shown in Figure 4.10. The interleaved inverter based SAPF is switched on at 0.1 sec, the presented interleaved inverter topology starts working as an active power filter. Since, only one active power electronic switch per leg is conducting at a time, no chance of shoot-through state. It shows the successful operation of three-phase interleaved inverter as shunt active power filter.

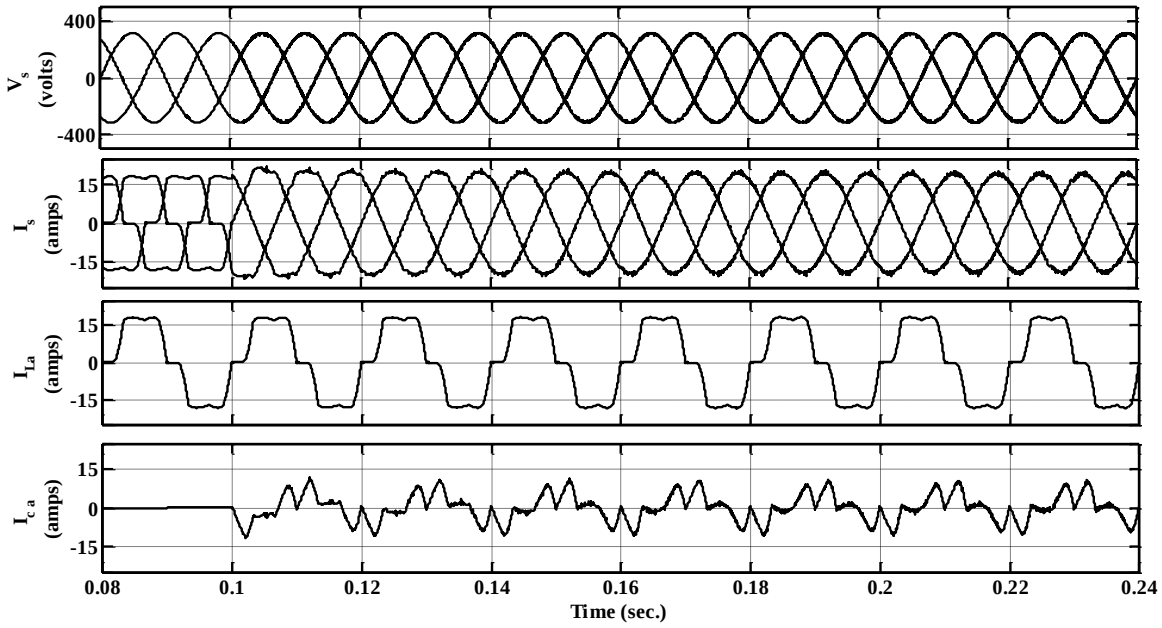


Figure 4.10 Performance of interleaved SAPF under sinusoidal supply voltage condition

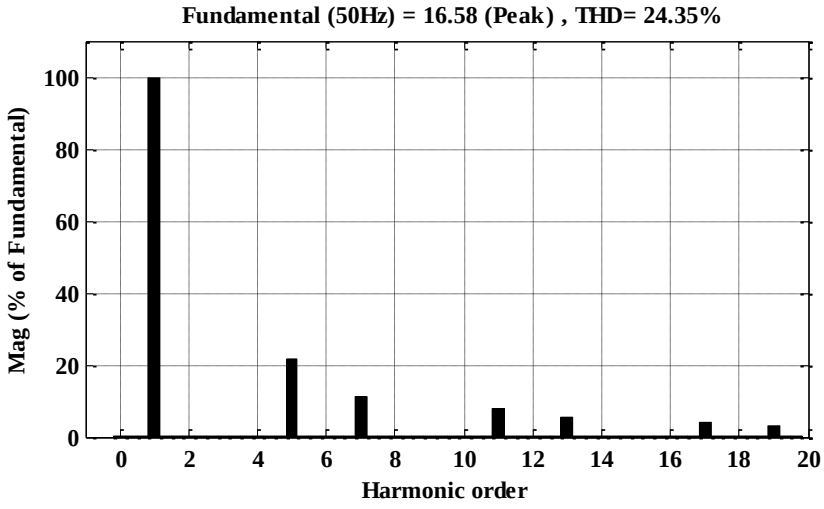


Figure 4.11 Frequency spectrum of source current before compensation

The source current harmonic spectrum before and after compensation are shown in Figure 4.11 and 4.12, respectively. These results validate the satisfactory performance of the interleaved SAPF for harmonic compensation confirming to IEEE-519 standards.

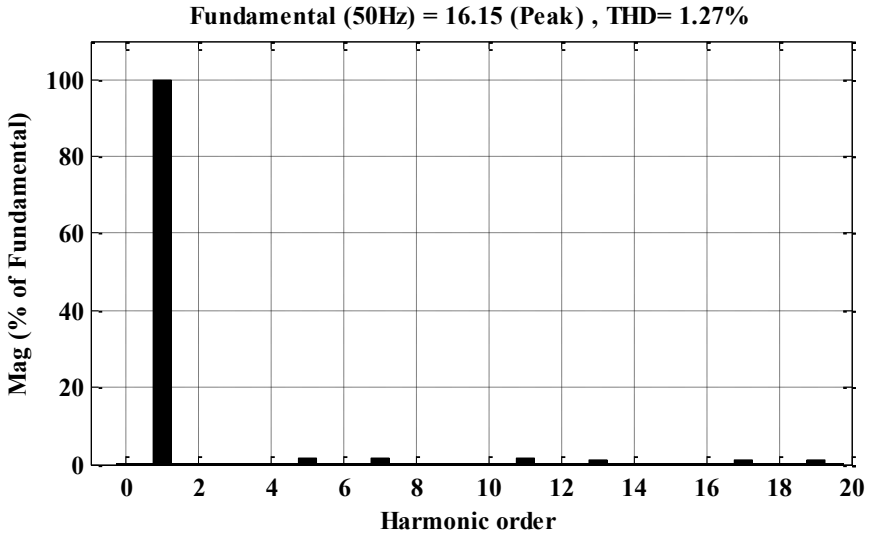


Figure 4.12 Frequency spectrum of source current after compensation

4.6.1.1.3 Controlled Bridge Rectifier with R-L Load

The phase controlled rectifiers are highly recommended to control the adjustable speed drives in high and medium power industrial systems. These phase controlled converters have significant characteristics as follows:

(i) It draws currents with sharp rising and falling edges which injects odd and even order harmonics into the system.

(ii) Phase controlled rectifiers draw a substantial amount of reactive power. The amount of reactive power drawing depends on the firing angle of the phase controlled rectifier. The power factor becomes poor and % THD also degrades with increasing the firing angle of the phase controlled rectifier. Various simulation studies have been performed to verify the effectiveness of interleaved inverter based SAPF with the phase-controlled rectifier. The simulation studies have been presented for a different firing angle of the phase controlled rectifier. The rating of the active filter depends on the reactive power to be compensated, and the reactive power drawn which increases with the increase in firing angle. Performance of interleaved SAPF using conventional ICC technique is shown in Figure 4.13. The phase controlled rectifier injects current harmonics and sharp rising and falling edges of current

into the system. Hence, the source currents possess the sharp rising and falling edges even after the compensation. The steady-state simulation results of the interleaved inverter based SAPF with a phase controlled bridge rectifier as shown in Figure 4.14 using MICC technique.

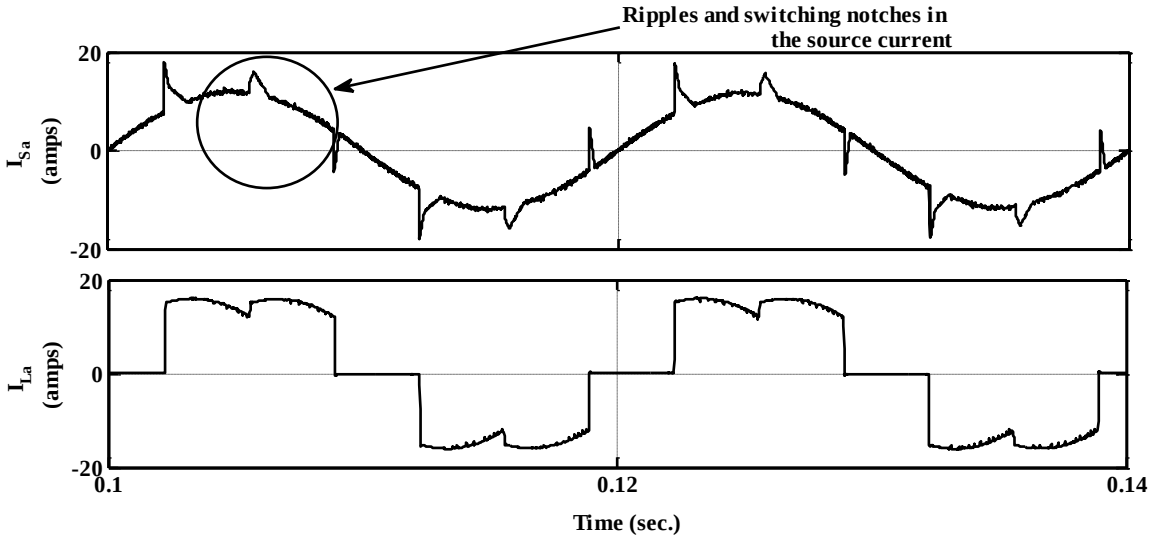


Figure 4.13 Simulation performance of phase 'A' source current after compensation and load current

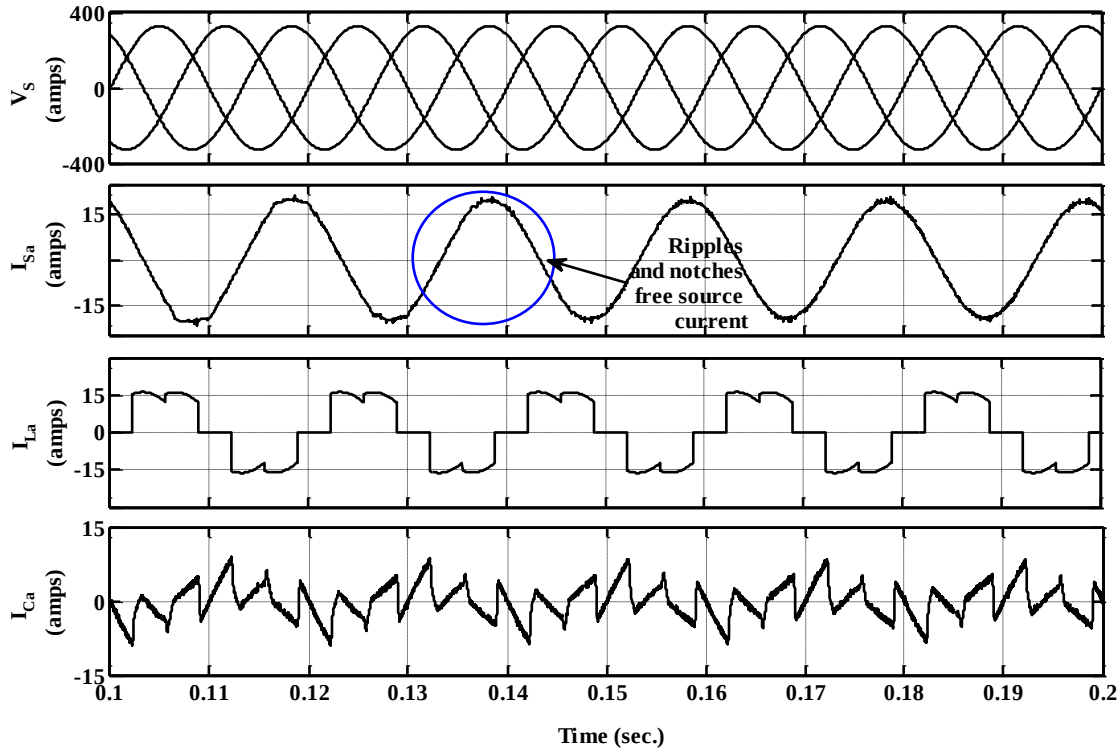


Figure 4.14 Simulation results of thyristor controlled bridge rectifier with R-L load in steady-state operation of interleaved SAPF

The LPF has been tuned to remove the switching notches and ripples from instantaneous active power as well as separates the dc and ac quantities of instantaneous active power. Therefore, the generated reference current will be distorted free. After compensation, the source current becomes sinusoidal and in phase with the respective phases of three-phase supply voltages. The harmonic spectrum of source current before and after compensation is shown in Figures 4.15 and 4.16, respectively. It is concluded from these results that the MICC control algorithm works in removing the ripples and notches from the power which is further used for generating the distorted free reference current generation. Hence, the THD of source current reduced from 34.27% to 2.82%. Detailed simulation results with respect to different phase angle of controlled bridge rectifier are tabulated in Table 4.2, which shows that the MICC is working wide range of operation by maintain the THD under IEEE standards.

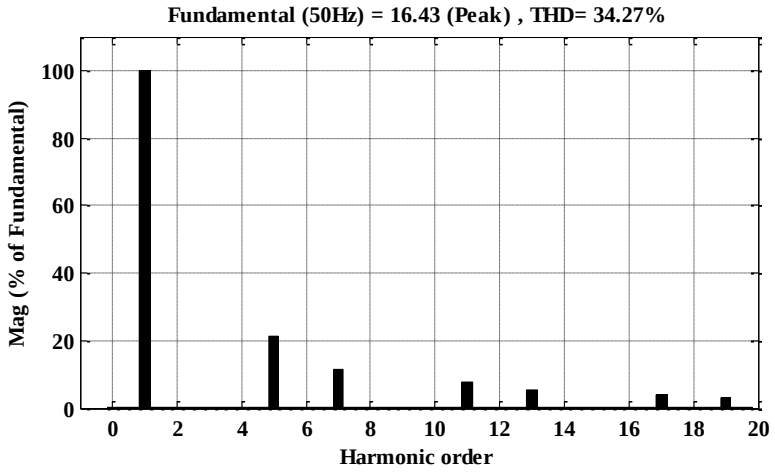


Figure 4.15 Harmonic spectrum of phase 'A' source current before compensation

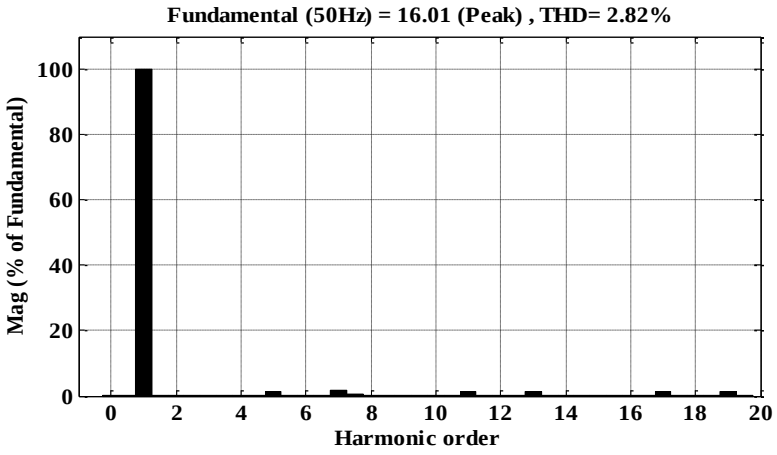


Figure 4.16 Harmonic spectrum of phase 'A' source current after compensation

Table 4.2

Harmonic compensation effectiveness in comparison to increment in firing angle

Firing angle	Before Compensation		After Compensation	
	%THD	P.F	%THD	P.F
5º	20.47	0.92	1.45	0.99
10º	26.14	0.90	2.12	0.99
20º	30.78	0.88	2.56	0.98
30º	34.27	0.82	3.86	0.98
40º	36.32	0.79	4.50	0.97

4.6.1.2 Simulation Results with Distorted Supply Voltage Case

4.6.1.2.1 Balanced Load Condition

Practically, the supply voltage wave shape is not a pure sinusoidal, but distorted, due to rapid use of non-linear loads. The supply voltage profile affects the compensation effectiveness of the control algorithm.

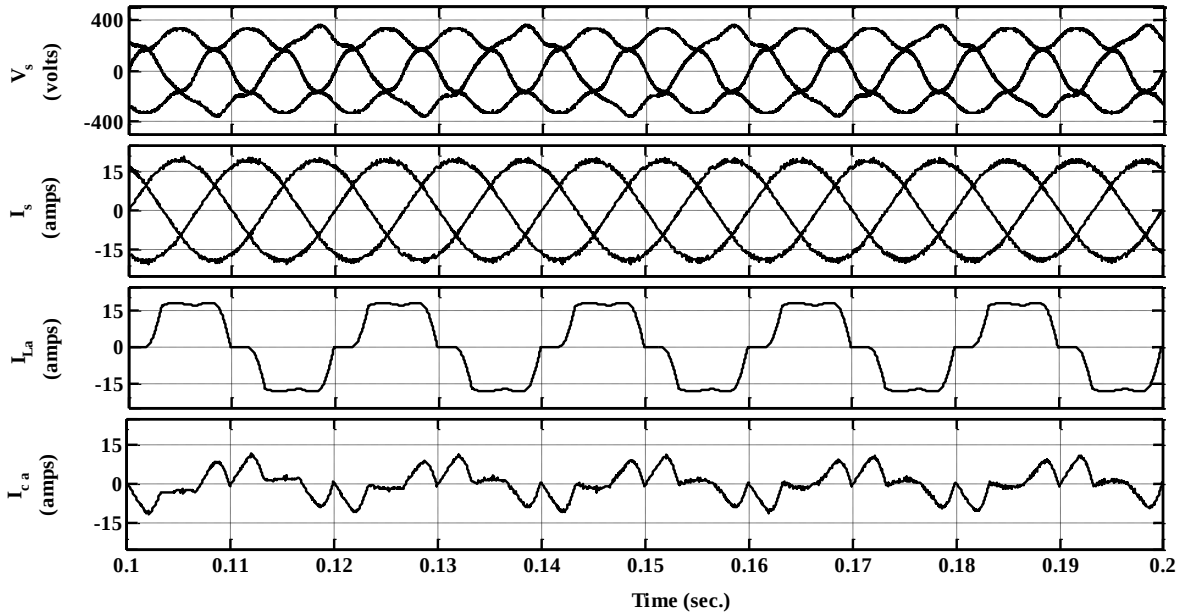
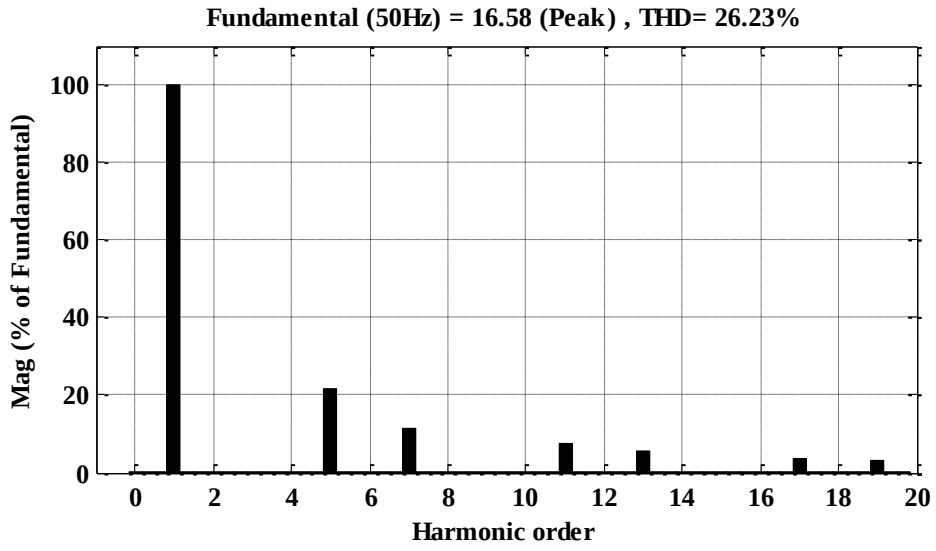


Figure 4.17 Performance parameters of distorted supply voltage (V_s), source current (I_s), phase 'A' load current (I_{La}), and phase 'A' compensation current (I_{ca})

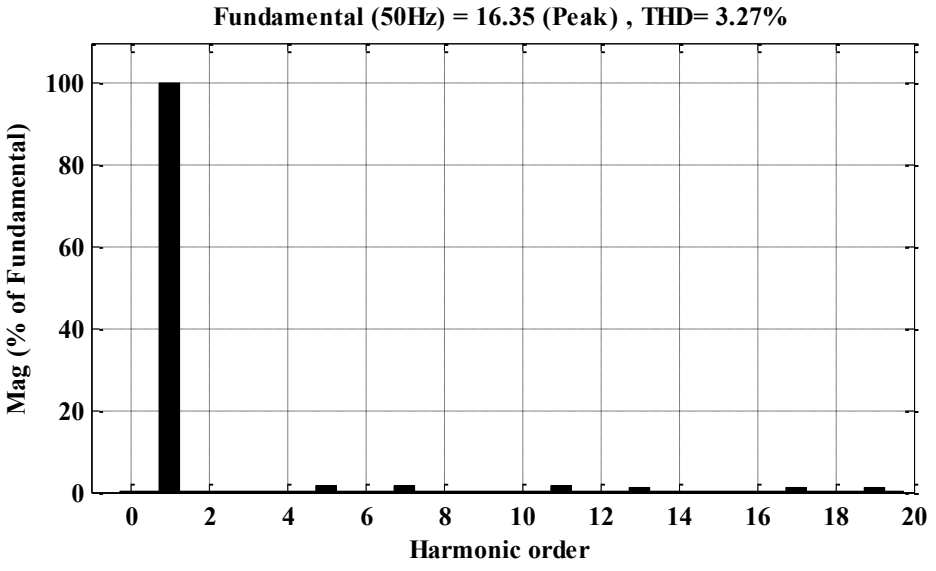
To prove the pre-eminence of the PTF based MICC scheme under the distorted supply voltage conditions, the supply voltage introduced with 20% of 5^{th} and 14% of 7^{th} harmonic contents as shown in Eq. 4.43. The fundamental component of voltage signal is extracted

by the PTF with minimum phase delay which is further processed for the reference current generation using MICC technique. The performance constraints of the modified control algorithm are shown in Figure 4.17.

$$\left.\begin{aligned} v_{sa} &= 325*\sin(\omega t) + 65*\sin(5\omega t) + 46*\sin(7\omega t) \\ v_{sb} &= 325*\sin(\omega t - 120^{\circ}) + 65*\sin(5\omega t - 120^{\circ}) + 46*\sin(7\omega t - 120^{\circ}) \\ v_{sc} &= 325*\sin(\omega t + 120^{\circ}) + 65*\sin(5\omega t + 120^{\circ}) + 46*\sin(7\omega t + 120^{\circ}) \end{aligned}\right\} \quad (4.43)$$



(a)



(b)

Figure 4.18 Harmonic spectrum of source current (a) Before compensation, and (b) After compensation

It is contemplated from these results that the PTF based MICC algorithm is significant and efficient under the distorted supply voltage conditions. The source current becomes sinusoidal, and its THD decreased from 26.23% to 3.27%. The harmonic spectrum of phase 'A' source current before and after compensation are shown in Figure 4.18 (a) and (b), respectively. This reflects the supremacy of designed PTF based MICC algorithm with interleaved SAPF.

4.6.1.2.2 Unbalanced Load Condition

The dynamic performance of the three-phase interleaved SAPF with the presented PTF based MICC is tested by disconnecting one phase (phase 'B') at 0.6 sec. to 0.7 sec. The performance parameters of three-phase voltages (V_S), balanced and distortion free source currents (I_S), unbalanced three-phase load currents (I_{La}, I_{Lb}, I_{Lc}) and compensating currents (I_{ca}, I_{cb}, I_{cc}) are shown in Figure 4.19. Smooth and distortion free supply currents without any over-shoot and under-shoot are observed during this condition. The source currents are balanced and sinusoidal after compensation, having 3.52%, 3.57% and 3.48% THD of phases 'A', 'B' and 'C', respectively as shown in Figure 4.20.

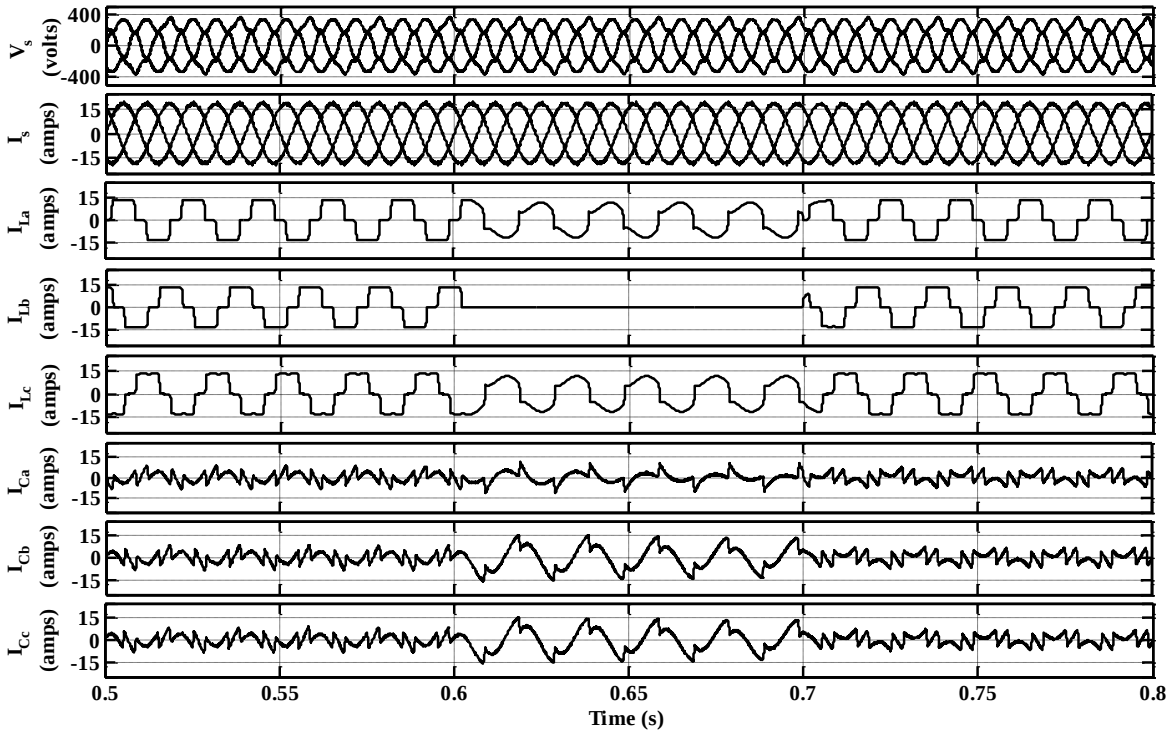
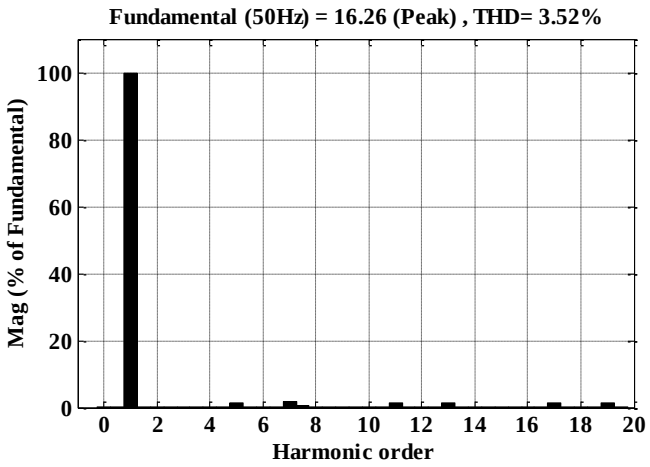
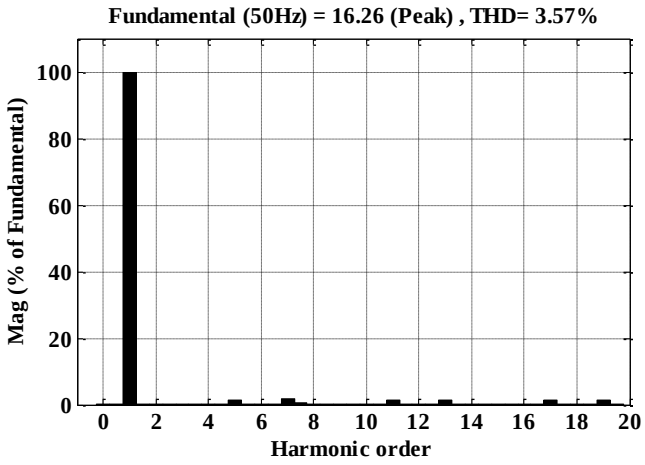


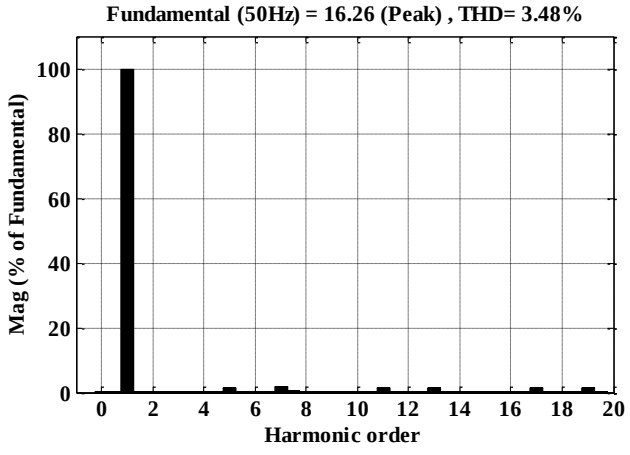
Figure 4.19 Dynamic performance under unbalanced non-linear load with distorted supply voltage



(a)



(b)



(c)

Figure 4.20 FFT analysis of three-phase source currents after compensation (a) Phase 'A', (b) Phase 'B', and (c) Phase 'C'

The amplitudes of the three-phase voltages are unchanged under this load changing condition. It can be observed that the harmonics of the source currents are well within IEEE-519 standard. These results showed the satisfactory performance of this control algorithm for compensating reactive power burden, load balancing of non-linear loads and harmonic mitigation. A complete system harmonic analysis results for different supply voltage and load conditions are given in Table 4.3. It is observed from these results that the PTF based MICC algorithm is fast in response and superior in compensation under different supply voltage and load conditions.

4.6.1.3 Distorted and Unbalanced Supply Voltage Case

The electrical power system becomes unbalance and distort due to sudden switch on/ off of heavy loads, unequal impedances in the distribution system, large interconnected non-linear loads, etc. Therefore, the supply voltage will be unbalanced and distorted which severely affect the source current profile. The superiority of the PTF based MICC algorithm is tested under the distorted and unbalanced supply voltage conditions. The supply voltage profile highly influences the compensation capability of interleaved SAPF. The distorted and unbalanced three-phase voltages have harmonic components and positive- and negative-sequence components.

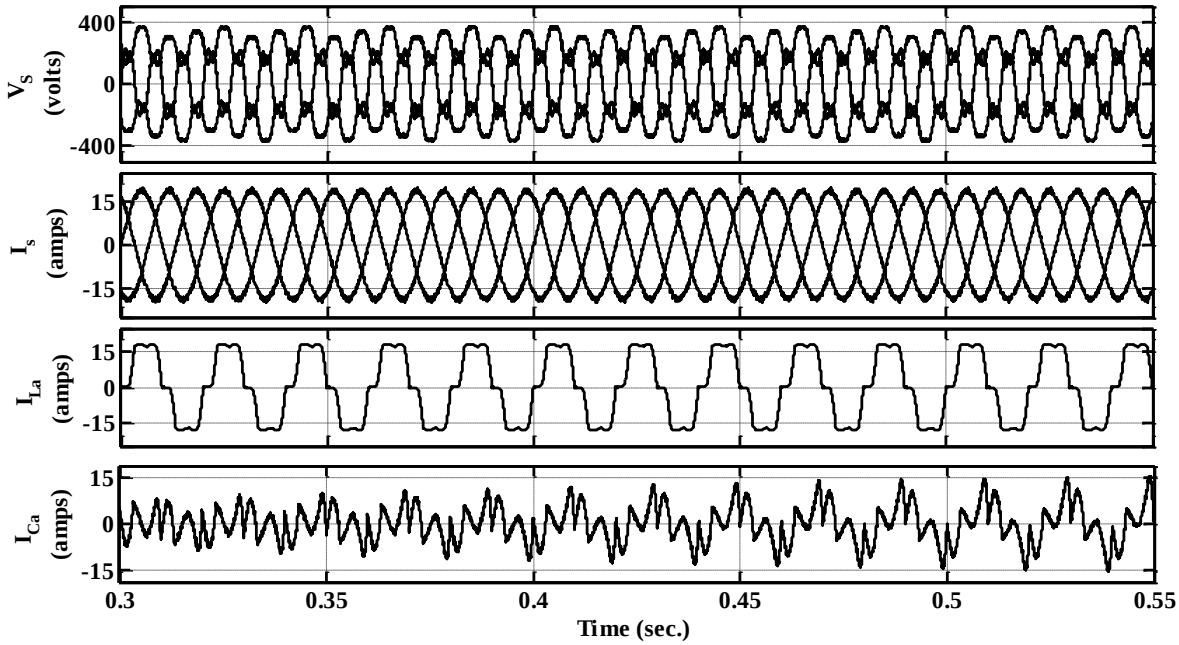


Figure 4.21 Performance of interleaved SAPF under distorted and unbalanced supply voltage

To test the robustness of this mdified control algorithm, 10% unbalance, 20% of 5th and 14% of 7th harmonic are imposed into the supply system as follows:

$$\left.\begin{aligned} V_{sa} &= 325*\sin(\omega t) + 65*\sin(5\omega t) + 46*\sin(7\omega t) \\ V_{sb} &= 292*\sin(\omega t - 120^{\circ}) + 58*\sin(5\omega t - 120^{\circ}) + 41*\sin(7\omega t - 120^{\circ}) \\ V_{sc} &= 350*\sin(\omega t + 120^{\circ}) + 70*\sin(5\omega t + 120^{\circ}) + 50*\sin(7\omega t + 120^{\circ}) \end{aligned}\right\} \quad (4.44)$$

In this case, the positive-sequence component of three-phase voltages are extracted using the symmetrical component theory as explained in Section 4.3. These extracted positive-sequence component voltages are well balanced but contained with 5th, 7th harmonic component of supply voltages including a fundamental component of voltages. Therefore, the PTF extracts the fundamental component of the positive-sequence supply voltage without phase distortion and delay which further processed for reference current generation using MICC.

Table 4.3

Simulation Performance of PTF based MICC algorithm under different supply voltage conditions

	Non-linear load under ideal supply			**Non-linear load Under distorted Supply voltage**			**Under distorted and Unbalanced Supply voltage**		
	Phase 'A'	***Phase 'B'***	***Phase 'C'***	***Phase 'A'***	***Phase 'B'***	***Phase 'C'***	***Phase 'A'***	***Phase 'B'***	***Phase 'C'***
i_s (A)	11.52	11.52	11.52	11.47	11.47	11.47	11.47	11.52	11.47
v_s (V)	230	230	230	230	230	230	230	206.5	247.5
Supply voltage % THD	0	0	0	10.74	10.74	10.74	10.74	9.85	11.79
Source current %THD before compensation	20.18	20.35	20.21	25.39	25.41	25.47	26.12	28.09	27.59
Source current %THD after compensation	1.27	1.68	1.72	3.27	3.38	3.24	3.71	3.81	3.69
i_5 (%)	1.594	1.594	1.594	1.547	1.547	1.547	1.547	1.594	1.547
i_7 (%)	1.138	1.138	1.138	1.113	1.113	1.113	1.113	1.138	1.113
I_{11} (%)	0.724	0.724	0.724	0.697	0.697	0.697	0.697	0.724	0.697
i_{13} (%)	0.613	0.613	0.613	0.585	0.585	0.585	0.585	0.613	0.585

The performance waveforms of three-phase unbalanced and distorted supply voltage (V_S), I_S after compensation, I_{La} and I_{ca} are shown in Figure 4.21. It is observed that the presented modified control algorithm is robust, fast response and superior in compensation under the unbalanced and distorted supply voltage conditions.

4.7 Implementation of Prototype and Experimental Results

This section presents the hardware prototype model and experimental investigation of three-phase interleaved inverter based SAPF. The main objective is to validate the simulation results by mitigating the harmonic pollution and reactive power burden along with shoot-through problem. The interleaved inverter model is implemented by using IRFP 460 MOSFET switches and MUR 460 fast recovery power diodes. The detailed description of the DS1104 DSP of dSPCE controller card, voltage and current sensors, signal conditioning circuits and gate driver circuits are elaborated in Section 3.6. The presented topology doesn't require the dead-band circuitry, hence it enhances the compensation efficiency. Thyristor controlled rectifier and diode bridge rectifiers with resistive and inductive loads (R-L) are used as non-linear loads to test the interleaved inverter topology and control technique. TYN612 thyristor and power diodes are used for making the bridge rectifier as shown in Appendix-A8 and A7, respectively. A Tektronix TPS 2014B digital signal oscilloscope (DSO; Beaverton, USA) and Fluke 43B power quality analyzer, are used for measurement of all waveforms and distortions. A complete hardware implementation of interleaved SAPF prototype and parameters used for experimentation are shown in Appendix-A12 and B2, respectively.

4.7.1 Experimental Verification under Available Supply Voltage

4.7.1.1 Switch Current Analysis of Interleaved Inverter based SAPF

The switch current waveform of the interleaved inverter is analyzed during the operation of active filtering. A diode bridge rectifier with R-L load is connected as non-linear load. The phase 'A' compensating current waveform is shown in Figure 4.22. There is only one active power switch per leg in the interleaved inverter, therefore the direction of the switch current is unchanged and provided the safe turn off of the MOSFET. It could be observed that the capacitor charging through power diodes and discharging through power MOSFETs

of interleaved SAPF. Therefore, it has a discontinuity in the compensating current, hence no shoot-through problem. It is evident that, the interleaved SAPF doesn't have any conduction state where the two power switches will be ON abruptly.

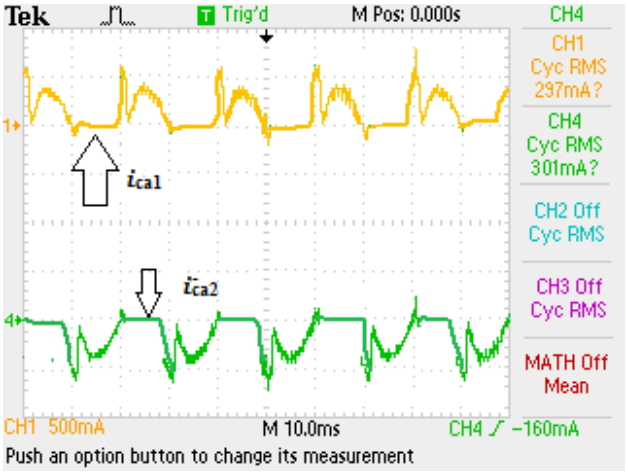
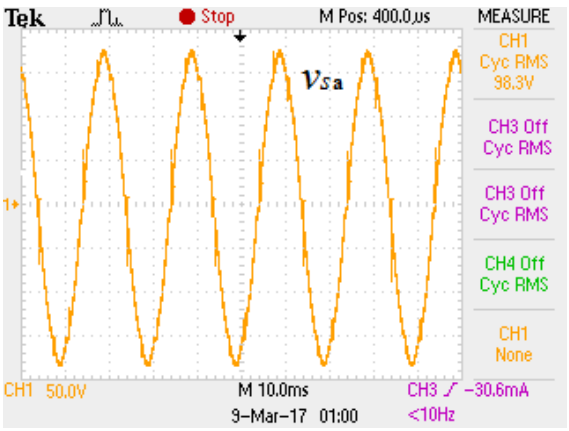


Figure 4.22 Phase 'A' interleaved SAPF switch current waveforms

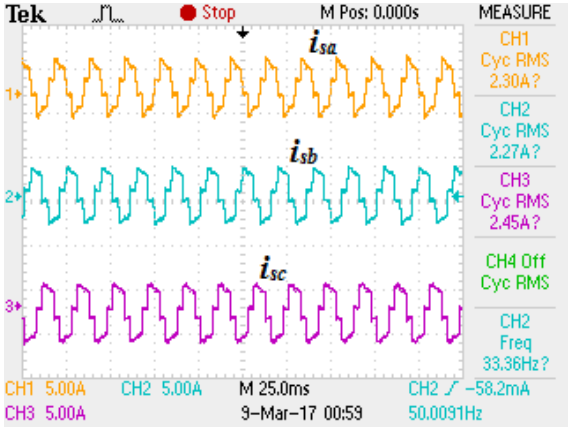
4.7.1.2 Diode Bridge Rectifier with R-L load

The performance of the interleaved SAPF is tested under the available supply voltage (1.2 to 2% measured THD at the time of experimentation). A three-phase full wave diode bridge rectifier with R-L load used as a non-linear load. This non-linear load pollutes the source currents profile by injecting current harmonics and draw the reactive power from the system. A modified *p-q* control algorithm is implemented for the reference current generation. The generated three-phase reference source currents are compared with the actual source currents and generate the error signals. These error signals will further process through hysteresis current controllers and produce switching pulses for the interleaved SAPF. Therefore, the interleaved SAPF provides the required harmonic and the reactive power compensation. The performance parameters of phase 'A' supply voltage (v_{sa}), three-phase source currents before compensation (i_{sa}, i_{sb}, i_{sc}), phase 'A' source current after compensation (i_{sa}), phase 'A' load current (i_{La}) and phase 'A' compensating current (i_{ca}) are shown in Figure 4. 23 (a) to 4.23 (c), respectively. The switch ON and OFF response of SAPF are shown in Figure 4.24 (a) and (b), respectively. It is observed from these results that the interleaved SAPF is fast in response and working effectively without shoot-through effect. The obtained experimental results under the steady-state indicates

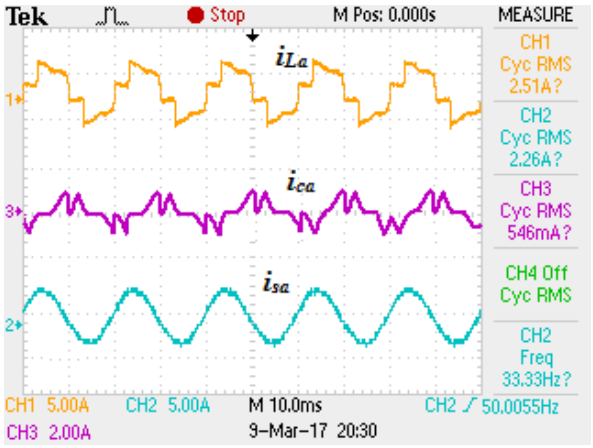
that the interleaved inverter based SAPF with PTF based MICC is superior solution to compensate current harmonics, reactive power burden without shoot-through effect. The reactive power burden has been compensated and the power factor is improved from 0.90 to 0.98 which is observed from Figure 4.25 (a) and (b), respectively. Therefore, the three-phase source currents are balanced and in-phase with supply voltages after compensation. The phase 'A' voltage and current are in-phase as shown in Figure 4.26 (a). Moreover, the source current THD is reduced from 27.4% to 2.9% as shown in Figure 4.26 (b) and (c), respectively. These results show the satisfactory results of interleaved inverter based SAPF by compensating the current harmonics and the reactive power burden.



(a)

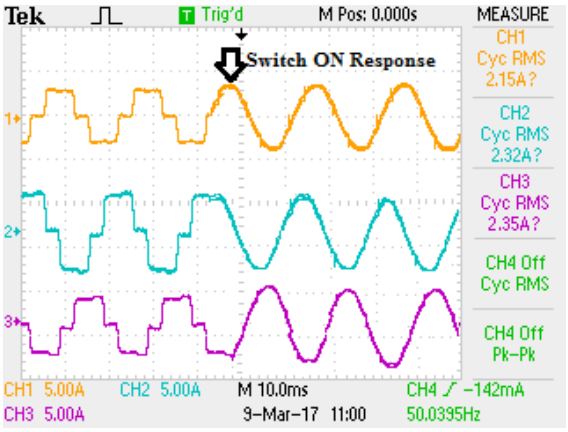


(b)

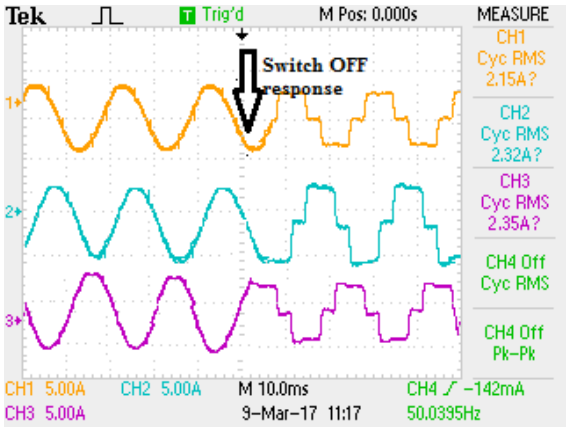


(c)

Figure 4.23 Performance of interleaved SAPF under available supply voltage (a) Supply voltage, (b) Three-phase source currents i_{Sa}, i_{Sb} and i_{Sc}, and (c) Phase 'A' source current after compensation, phase 'A' load current and phase 'A' compensation current

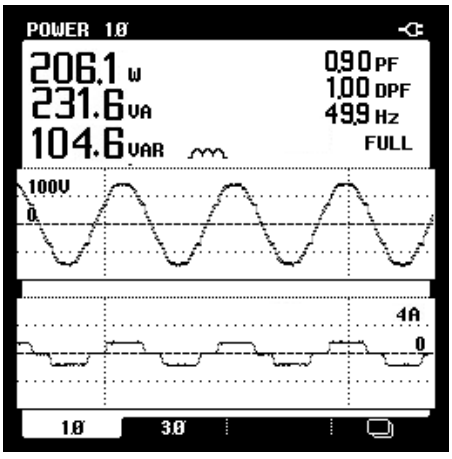


(a)



(b)

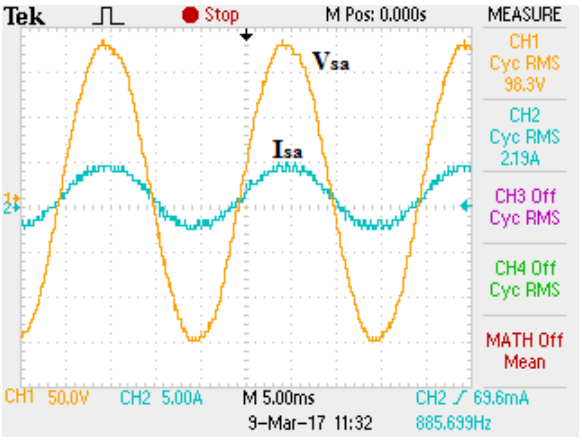
Figure 4.24 (a) Switch-ON response, and (b) Switch-OFF response of interleaved SAPF



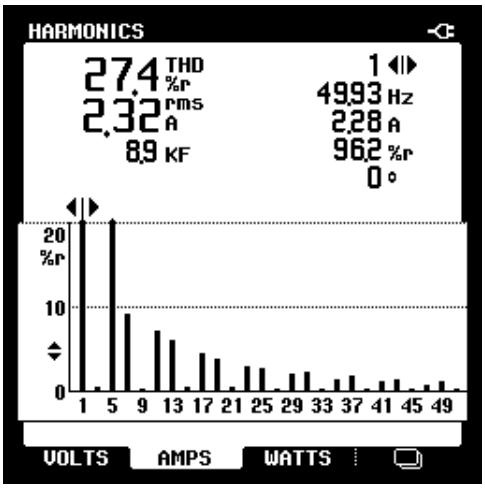
(a)

(b)

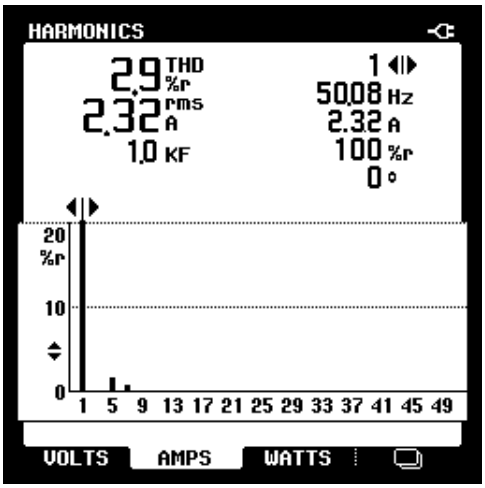
Figure 4.25 (a) Reactive power requirement of load, and (b) Improvement of power factor by reactive power compensation



(a)



(b)

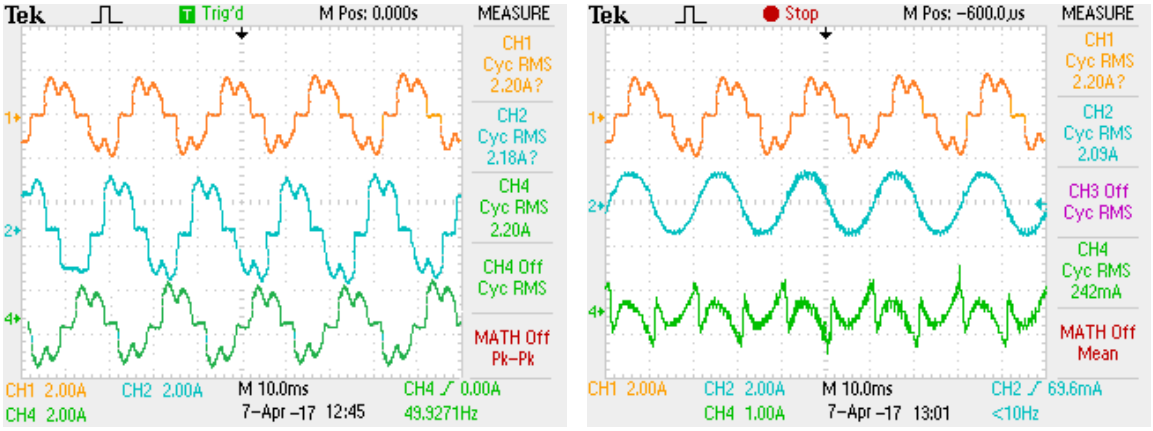


(c)

Figure 4.26 (a) Supply voltage and source current after compensation, (b)-(c) Harmonic spectrum of phase 'A' source current before compensation, and (c) After compensation

4.7.1.3 Thyristor Controlled Bridge Rectifier with R-L load

The three-phase controlled rectifier with R-L load injects current harmonics into the system hence, the source currents (i_{sa}, i_{sb}, i_{sc}) become distorted as shown in Figure 4.27 (a). The performance of interleaved SAPF parameters phase 'A' load current (i_{La}) phase 'A' source current (i_{sa}) and phase 'A' compensating current (i_{ca}) are shown in Figure 4.27 (b). The switch-on and-off response of MICC technique is shown in Figures 4.28 (a) and (b), respectively.



(a) (b)

Figure 4.27 Performance of interleaved SAPF (a) Three-phase source currents i_{sa}, i_{sb} and i_{sc}, and (b) Phase 'A' load current i_{La}, phase 'A' source current after compensation , compensating current i_{ca}

It is contemplated that as soon as interleaved SAPF switched ON, the source current becomes free of notches and distortions and hence, source current becomes sinusoidal which show that the presented interleaved SAPF has quick response and working effectively without shoot-through effect. The performance parameters of both conventional ICC and MICC techniques, phase 'A' source current (i_{sa}) and load current (i_{La}) are shown in Figures 4.29 (a) and (b), respectively. It is contemplated from Figure 4.29 (a) that the source currents still have distortions and switching notches. Hence, the source current THD by using conventional ICC technique is reduced from 32.8% to 6.95%. The harmonic spectrum of phase 'A' source current before and after compensation by using conventional ICC are shown in Figure 4.30 (a) and (b), respectively which doesn't meet the IEEE-519 standards. Whereas the MICC technique removes distortions and notches from the source currents therefore, the THD of source current become 4.0% as shown in Figure 4.30 (c).

Hence, the interleaved SAPF with MICC algorithm is effective, robust and gives satisfactory results by maintaining the IEEE-519 standards without shoot-through problems.

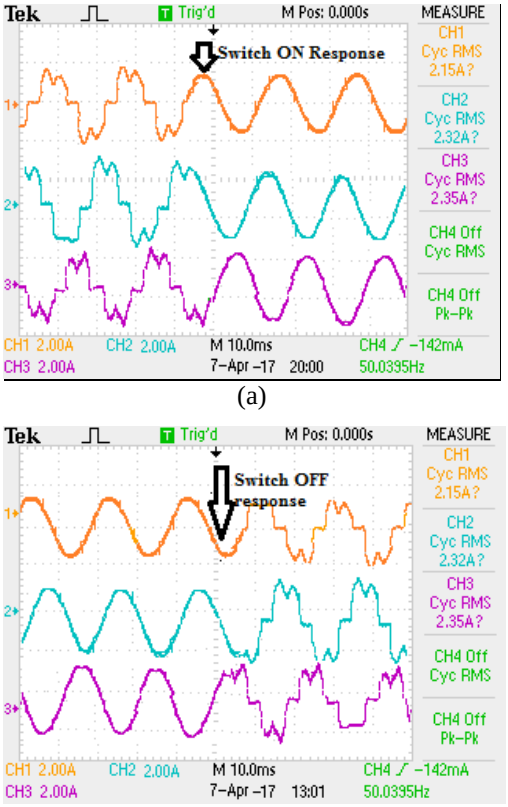


Figure 4.28 (a) Switch-on response: three-phase source currents (i_{sa}, i_{sb}, i_{sc}), and (b) Switch-off response: three-phase source currents (i_{sa}, i_{sb}, i_{sc}) of interleaved SAPF using MICC

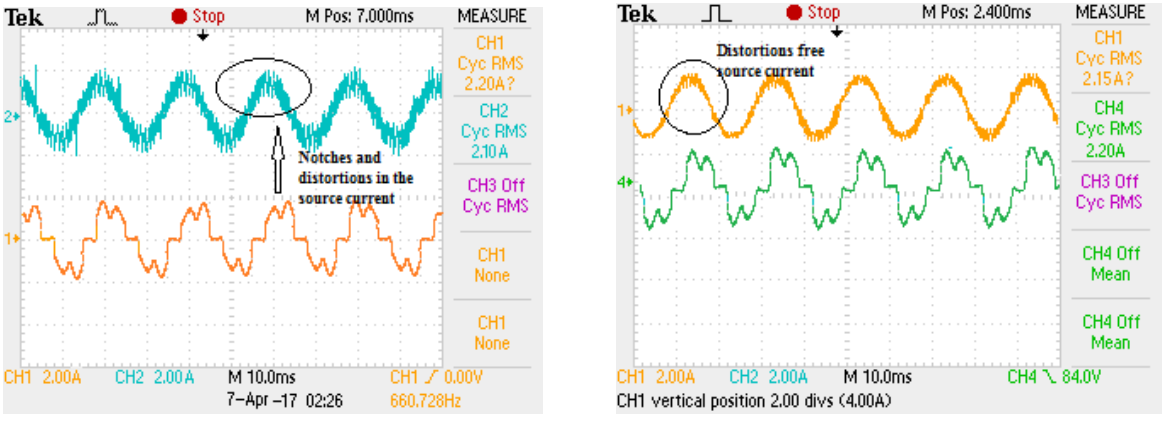


Figure 4. 29 Performance of interleaved SAPF (a) i_{sa}, i_{La}, using conventional indirect current control technique and, (b) i_{sa}, i_{La}, using modified indirect current control technique

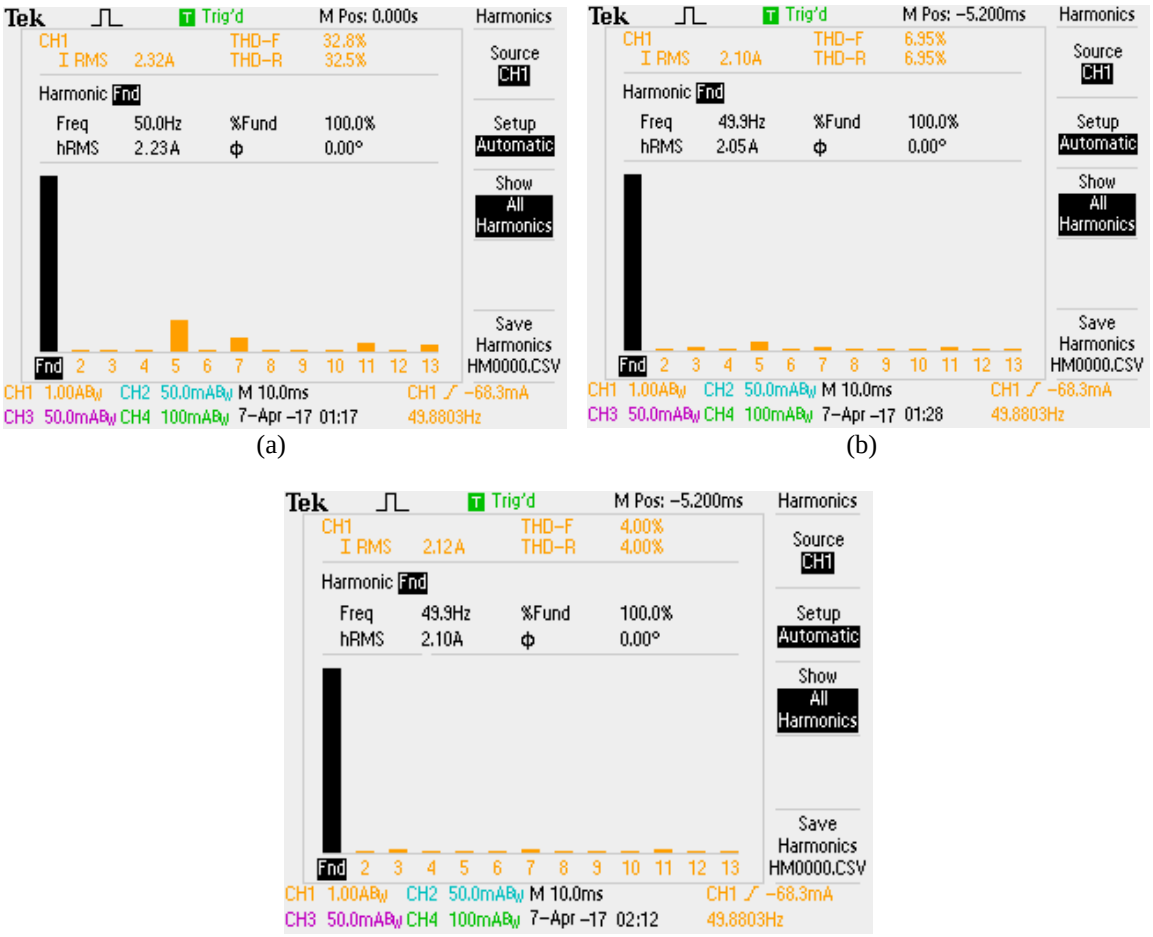
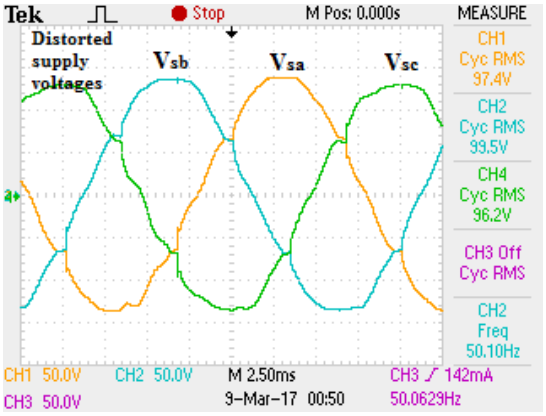


Figure 4.30 Harmonic spectrum of phase 'A' source current (a) Before compensation, (b) After compensation using conventional indirect current control, and (c) Modified indirect current controller

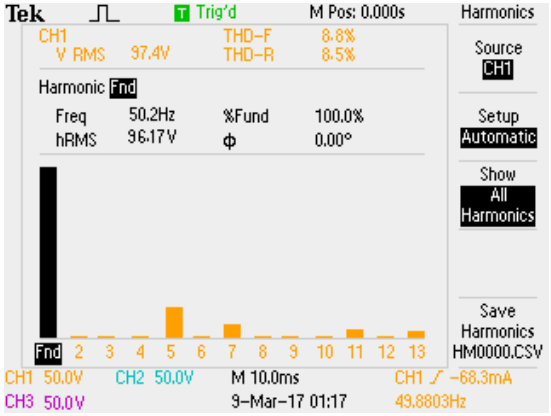
4.7.2 Experimental Verification under Distorted Supply Voltage

The superiority of the PTF based MICC control algorithm is tested under the distorted supply voltage conditions. The distorted three-phase voltages at PCC and their harmonic spectral diagrams are shown in Figure 4.31 (a)-(d), respectively. Figure 4.32 (a) shows the distorted supply phase 'A' voltage and extracted fundamental frequency component of signal. It is contemplated from the Figure 4.32 (a) that the presented PTF is extracted the fundamental component of voltage signal from the distorted supply voltage. The extracted fundamental voltage signal is further processed for the reference current generation using modified generalized *p-q* theory. The error will be generated by comparing reference current with actual source current. The generated error wi be further processed through hysteresis

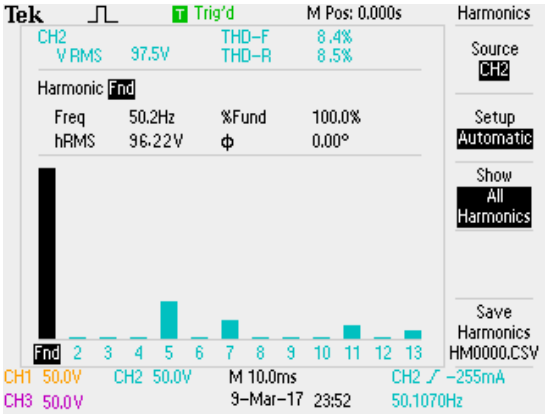
current controller and produces the switching pulses for the interleaved SAPF switches. Therefore, the flow of compensating current can be controlled which improves the compensation capability of interleaved SAPF. The performance parameters of three-phase source currents and phase 'A' load current are shown in Figure 4.32 (b) and their respective three-phase compensating currents are shown in Figure 4.32 (c). It is recognized from these results that, the three-phase source currents are sinusoidal as per IEEE-519 standards. The harmonic spectrum of three-phase source currents are shown in Figure 4.32 (d)-(f). It can be concluded that the PTF based MICC algorithm is well designed to compensate for current harmonics and reactive power burden under the distorted supply voltage conditions.



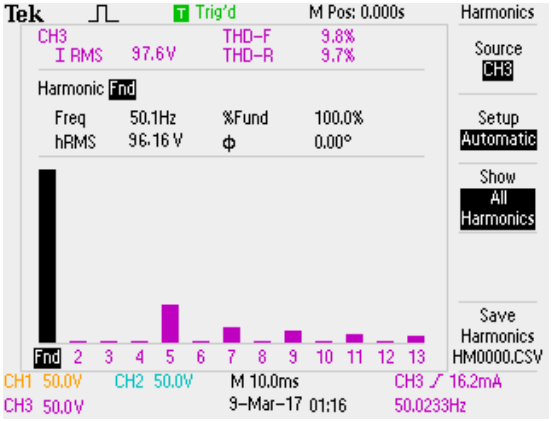
(a)



(b)

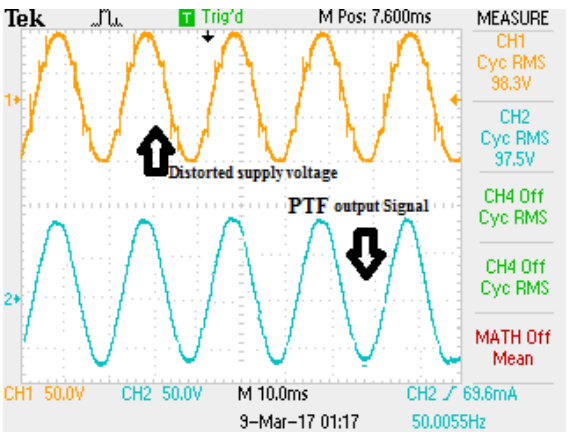


(c)

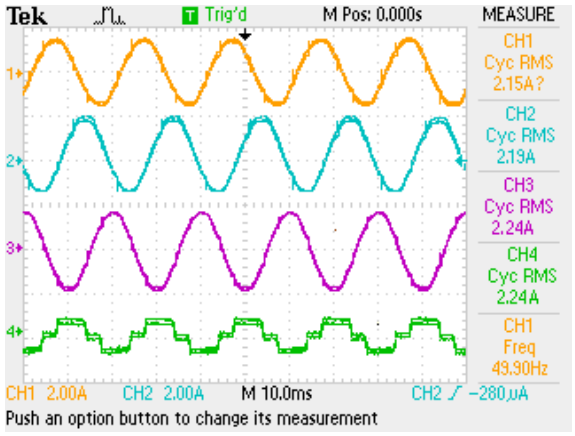


(d)

Figure 4.31 (a) Three-phase distorted supply voltages, (b)-(d) Harmonic pattern of three-phase supply voltages phase 'A', phase 'B' and phase 'C'



(a)



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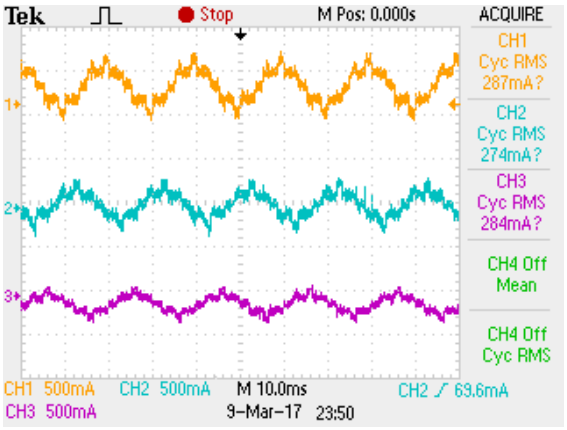
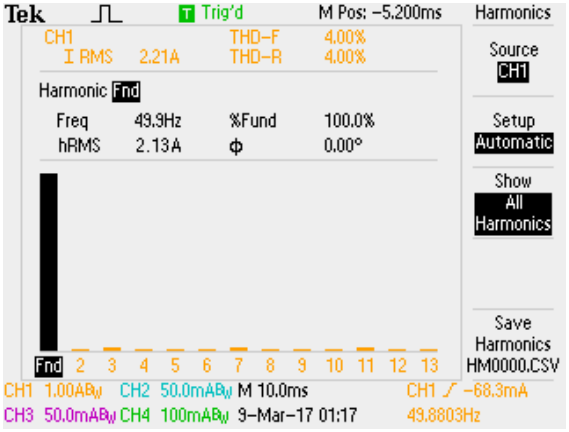
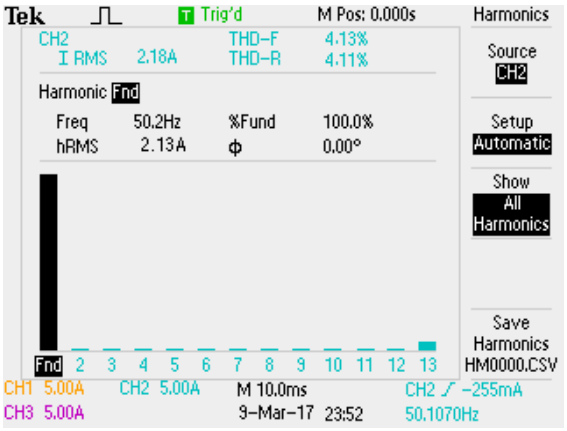


(c)



(d)



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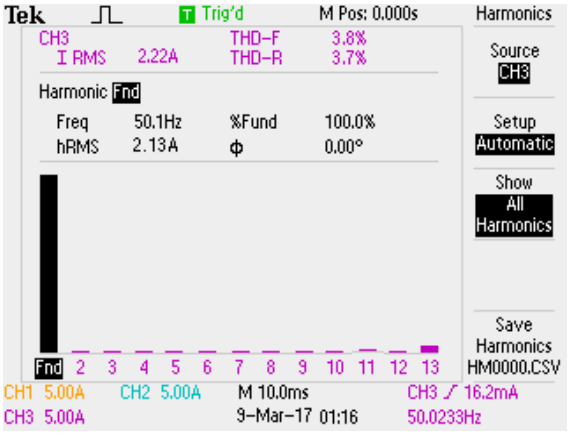


(f)

Figure 4.32 (a) Distorted phase 'A' supply voltage and PTF output signal, (b) Source currents after compensation i_{sa}, i_{sb} and i_{sc}, phase 'A' load current i_{La}, (c) Compensation currents: i_{ca}, i_{cb} and i_{cc}, and (d)-(f) Harmonic spectrum of source currents after compensation

4.7.3 Experimental Verification under Unbalanced and Distorted Supply Voltage

The dynamic attainment of PTF based MICC algorithm is tested under the distorted and unbalanced supply voltages with unbalanced load. The performance parameters of modified control algorithm with three-phase interleaved SAPF are shown in Figure 4.33 (a)-(c). The three-phase unbalanced and distorted supply voltages are shown in Figure 4.33 (a) and unbalanced load current are shown in Figure 4.33 (b).

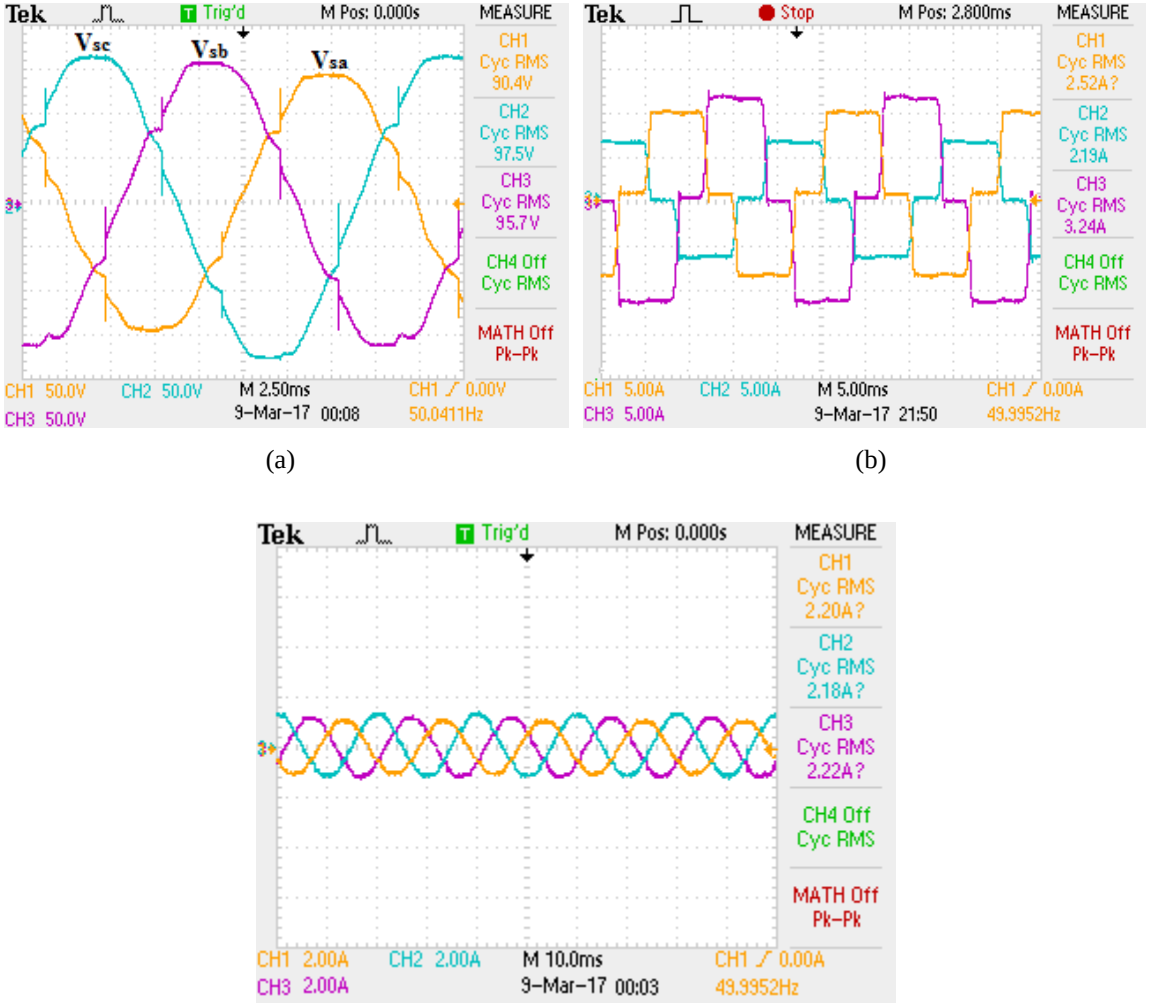


Figure 4.33 Performance parameters of (a) Three-phase distorted with unbalanced supply voltages, (b) Three-phase unbalanced load currents, and (c) Three-phase source currents after compensation

It is observed from Figure 4.33 (b) that, the unbalanced load current imposes the unbalancing nature in the source side. Therefore, the PTF based MICC technique is sensitive

to detect the unbalanced nature of the load currents. Further, this control algorithm is able to balance all three-phase source currents as shown in Figure 4.33 (c). It is concluded from the Figure 4.33 (c) that all three-phase source currents are balanced under the unbalanced load condition. It is evident that the PTF based MICC algorithm is able to work by balancing the source currents and compensating the harmonics in the source currents under this condition. A complete harmonic analysis under different supply and load conditions are tabulated in Table 4.4. It is observed that the presented control algorithm is sensitive to detect the various harmonics in the system and able to extract the fundamental component of voltage signal accurately without phase delay under different load and supply voltage conditions.

Table 4.4

Experimental Performance of PTF based MICC algorithm under different supply voltage conditions

	Non-linear load under ideal supply			**Non-linear load Under distorted Supply voltage**			**Under distorted and Unbalanced Supply voltage**		
	Phase 'A'	***Phase 'B'***	***Phase 'C'***	***Phase 'A'***	***Phase 'B'***	***Phase 'C'***	***Phase 'A'***	***Phase 'B'***	***Phase 'C'***
i_s (A)	2.30	2.32	2.35	2.15	2.19	2.24	2.20	2.18	2.22
v_s (V)	98.3	99.1	98.5	97.4	99.5	96.2	97.4	97.5	98.7
Supply voltage % THD	1.5	1.4	1.7	8.8	8.4	9.8	8.7	8.5	8.9
Source current %THD before compensation	27.4	26.8	27.5	28.4	27.7	28.7	27.7	25.3	26.5
Source current %THD after compensation	4.0	4.2	3.7	4.0	4.13	3.8	3.5	4.1	3.8
i_5 (%)	0.439	0.439	0.439	0.396	0.412	0.446	0.412	0.291	0.446
i_7 (%)	0.314	0.314	0.314	0.295	0.295	0.295	0.295	0.295	0.295
i_{11} (%)	0.199	0.199	0.199	0.199	0.199	0.199	0.199	0.199	0.199
i_{13} (%)	0.169	0.169	0.169	0.169	0.169	0.169	0.169	0.169	0.169

4.8 Conclusion

In this chapter, design and implementation of three-phase interleaved SAPF is presented to mitigate shoot-through and power quality problems under the sinusoidal and distorted supply voltage conditions. In present power system network, lot of inevitable linear and non-linear loads are connected which cause variable harmonic contents, affects the compensation effectiveness of the interleaved SAPF due to the large variation in supply voltage and loads. The PTF based modified *p-q* control algorithm has been presented and implemented in this chapter to enhance the operation of the interleaved inverter based SAPF. The presented system with modified control technique has been modelled in MATLAB®/ Simulink environment and tested under various conditions of the supply voltage and load. The simulation results show that three-phase interleaved SAPF is working successfully without a dead-band circuit which eliminates the shoot-through state, EMI effect and ringing problem along with PQ problems. In addition, the interleaved inverter based SAPF with PTF based MICC algorithm have been proved to be an effective solution to mitigate power quality problems like harmonic pollution, poor power factor and load unbalancing. The simulation results are validated by developing the prototype model in the laboratory. The overall simulation and hardware performance showed that the three-phase interleaved SAPF with PTF based modified *p-q* control technique is able to maintain the supply currents sinusoidal and balanced at unity power factor.

CHAPTER 5

MULTITUDINAL SLIDING MODE CONTROLLER FOR DC-VOLTAGE REGULATION

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Multitudinal Sliding Mode Controller based Interleaved Shunt APF to Mitigate Shoot-through and PQ Problems under Distorted Supply Voltage Conditions," *International Transactions on Electrical Energy Systems*, Wiley publications, vol. 29, no. 1, pp. 1-23, Jan. 2019.
   DOI: https://doi.org/10.1002/etep.2701

CHAPTER 5

MULTITUDINAL SLIDING MODE CONTROLLER FOR DC-VOLTAGE REGULATION

5.1 Introduction

In shunt active power filters, the accuracy of harmonic and reactive power compensation highly depends on DC-link capacitor voltage stabilization. In other words, the proper DC-link voltage regulation ensures the accurate injection of compensating currents by shunt APF. Unrelenting propagation of power electronic based devices in industrial, commercial and residential applications create harmonic pollution in the distribution system. Over a period of decade, this proliferation of harmonic pollution has been increased drastically. In addition, due to continuing variation of these non-linear loads and requirement of harmonic compensation, the DC-link voltage stabilization has become a great concern for the researchers [112].

PI controllers are well-established controllers to stabilize the DC-link voltage because of its simplicity, reliability and ease of implementation with low-cost controllers. However, it has demerits like sluggish response in the transient condition of the load, difficult to adjust the PI controller gain values. Sliding mode controllers were acknowledged as an impressive controllers in the application of APF. The SMC afford system access to formulate problem to maintain stability in the presence of system uncertainty [113-114]. The main advantage of the SMC is that it is insensitive to parameter uncertainty and external disturbances. Therefore, the SMC is most suitable for the closed-loop control of the converters. Many researchers across the globe use this SMC in the field of the grid-tied system which enhances the system stability under the steady and dynamic state of the system. However, the conventional SMC has demerits like poor response under mismatched system uncertainties/ disturbances [115-117]. To overcome these problems of conventional SMC, multitudinal sliding mode control (MSMC) has been presented in this chapter. The MSMC uses multiple surfaces for mismatched system disturbances/

uncertainties. Moreover, it uses to control the mismatched disturbances/uncertainties using inertial delay control.

5.2 Conventional Sliding Mode Controller

The sliding mode control theory has to be developed for single-phase interleaved SAPF to maintain constant DC-link voltage under the steady-state and transient condition of the load. The equivalent control concept of the sliding surface can be implemented for the interleaved SAPF model. To derive the control equation, consider the equivalent circuit model of the single-phase interleaved SAPF as shown in Figure 5.1. The sliding control law gives the switching function to track the sliding surface. Based on the switching action of the power switches (S_1, S_2, S_3, and S_4) and diodes (D_1, D_2, D_3 and D_4), the DC-link voltage charges and discharges. Let μ is the switching state of the interleaved SAPF. When μ=0, either D_1 or D_4 will be in conduction mode which charges the capacitor through diodes. When μ=1, either S_1 or S_4 will be in conducting mode, therefore, capacitor discharges. To derive the equivalent control concept for the interleaved SAPF, the switching states of a single leg of half bridge switches (S_1 and D_4) are considered.

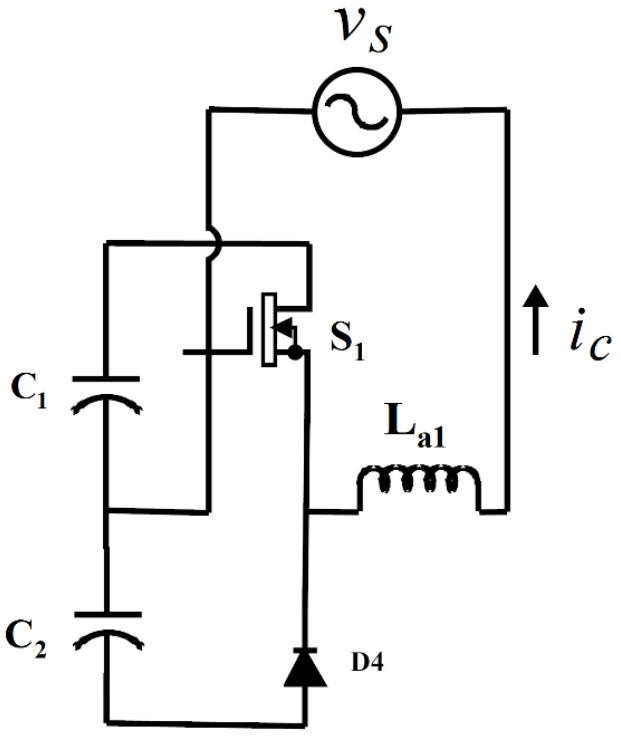


Figure 5.1 Switching action for capacitor DC-link voltage stabilization

The state space equation has to be derived for the interleaved SAPF. When μ=0, the switch D_4 will be ON and hence capacitor C_2 charges with charging current of i_c. As per Kirchhoff's voltage law (KVL), the following equation can be written:

$$L_{a1}\frac{di_c}{dt} = -r_{a1}i_c - v_{c2} + v_s \tag{5.1}$$

$$\text{Let } x_1 = i_c; x_2 = v_{c1}; x_3 = v_{c2}; \tag{5.2}$$

$$\dot{x}_1 = -\frac{r_{a1}}{L_{a1}}x_1 - \frac{1}{L_{a1}}x_3 + \frac{v_s}{L_{a1}} \tag{5.3}$$

$$C_2\dot{x}_3 = x_1, \text{and } \dot{x}_2 = 0 \tag{5.4}$$

Where, x_1, x_2 and x_3 are three variables which consist of compensating current (i_c), upper capacitor voltage (v_{c1}) and lower capacitor value (v_{c2}), respectively. When μ=1, the switch S_1 will be ON, and the compensating current can be supplied through capacitor C_1. The following equations can be derived during this mode of operation.

$$L_{a1}\frac{di_c}{dt} = -r_{a1}i_c + v_{c1} + v_s \tag{5.5}$$

$$\dot{x}_1 = -\frac{r_{a1}}{L_{a1}}x_1 + \frac{1}{L_{a1}}x_2 + \frac{v_s}{L_{a1}} \tag{5.6}$$

$$C_1\dot{x}_2 = x_1, \text{ and } \dot{x}_3 = 0 \tag{5.7}$$

From Eq. (5.1)-(5.7), the state space equation for the interleaved SAPF can be written as follows:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\end{bmatrix} = \begin{bmatrix}-\frac{r_{a1}}{L_{a1}} & 0 & -\frac{1}{L_{a1}}\\ 0 & 0 & 0\\ \frac{1}{C_2} & 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} + \begin{bmatrix}0 & \frac{1}{L_{a1}} & \frac{1}{L_{a1}}\\ \frac{1}{C_1} & 0 & 0\\ -\frac{1}{C_2} & 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}\mu + \begin{bmatrix}\frac{v_s}{L_{a1}}\\ 0\\ 0\end{bmatrix} \tag{5.8}$$

The DC-link voltage and current through inductor are considered as the state of the system. To derive the sliding surface, one has to find out the output function. The output function can be obtained as follows:

$$y(t) = \int v_S i_C dt \tag{5.9}$$

The derivation of the output function y(t) is as follows:

$$\begin{aligned} \dot{y}(t) &= v_s i_c \\ U_{eq} = \ddot{y}(t) &= \dot{v}_s i_c + v_s \dot{i}_c = v_s \left\{ \frac{-r_{a1}}{L_{a1}} x_1 - \frac{v_{c2}}{L_{a1}} - \frac{\mu v_{c1}}{L_{a1}} + \frac{\mu v_{c2}}{L_{a1}} + \frac{v_s}{L_{a1}} \right\} \end{aligned} \tag{5.10}$$

Where U_{eq} is the equivalent surface model of the interleaved SAPF. The mismatch disturbance stated from the state space model as follows:

$$\left.\begin{aligned} \dot{x}_1 &= -\frac{r_{a1}}{L_{a1}} x_1 - \frac{\mu}{L_{a1}} x_2 - \left(\frac{1}{L_{a1}} + \frac{\mu}{L_{a1}}\right) x_3 + e_1(t) \\ \dot{x}_2 &= \frac{\mu}{C_1} x_1 + e_2(t) \\ \dot{x}_3 &= x_1 \left(\frac{1}{C_2} - \frac{\mu}{C_2} \right) + e_3(t) \\ y &= x_1 \end{aligned}\right\} \tag{5.11}$$

Where, $e_2(t)$ and $e_3(t)$ are the system disturbances, $e_1(t)$ is the lumped uncertainty and y is the output. Assume that these disturbances have boundaries.

5.2.1 Lyapunov Theorem

According to Lyapunov theorem, the stability can be defined as the system stability in the neighbourhoods of equilibrium, in simple terms, if the solution of the equilibrium point near to stable, then it stays forever in that stability point. The block diagram of the sliding mode controller is shown in Figure 5.2 (a).

5.2.2 Relay Function

In this conventional SMC, the sliding surface is designed by imposing the desired dynamic behaviour of the system which allows the determination of the parameters for conventional SMC. The relay function is shown in Figure 5.2 (b). The stability of the sliding surface can be verified by using the Lyapunov theorem. The signum function can be applied to the equivalent control surface as shown in Eq. (5.12)

$$U_{eq} = k.sign[S(x)] \tag{5.12}$$

Where, *sign* is an odd mathematic function which extracts the sign of the real number and S is the sliding surface. The Lyapunov function works if the U_{eq} function is negative, the Lyapunov function must decrease to zero. The switching function of the hysteresis controller always controls the chattering phenomena of the sliding surface which helps to move the state of the controller in the surface. The equivalent control model U_{eq} boundaries can be written as shown Eq. (5.13).

$$U_{eq} = \begin{cases} \dfrac{k}{\lambda} & \text{if } |S(x)| < \lambda \neq 0 \\ k.sign[s(x)] & \text{if } |S(x)| > \lambda \end{cases} \tag{5.13}$$

Where k is gain of the conventional SMC taken in the range of admissible value, and λ is the surface boundary. In order to regulate the DC-link voltage, the error generated by comparing the V_{dc} and synthesizes a current command.

The output of the conventional SMC is as follows:

$$I_{sm}^{*} = k * sign(\varepsilon) \tag{5.14}$$

Where ε an error, and k is the gain which must be satisfy the sliding mode condition.

The sliding mode condition can be express as follow:

$$k > \max \left| \frac{2}{3} I_{sm}^{*} \frac{V_{dc}}{V_s^2} \right| \tag{5.15}$$

The control actions for the sliding surface can be written as follows:

$$\mu = \begin{cases} 1 \text{ for } S \geq 0 \\ 0 \text{ for } S \leq 0 \end{cases} \tag{5.16}$$

This conventional SMC gives better results when the system fulfils matching conditions like disturbances present in the inputs. However, the system may not always under matching conditions, as the demand of the non-linearity increases, at the same time mismatched uncertainties/ disturbances increases. The research is progressing to solve these type of problems. Hence, MSMC has been presented in this chapter to overcome the problems of conventional SMC.

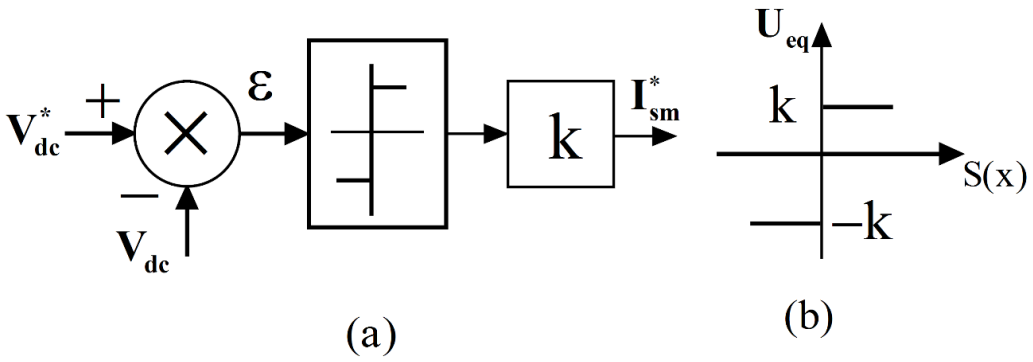


Figure 5.2 (a) Block diagram of sliding mode controller for DC-voltage regulation, and (b) Relay function

5.3 Multitudinal Sliding Mode Controller

5.3.1 Inertial Delay Control

Many real-time systems are significantly affected by uncertainties and large unmeasurable external disturbances. One of the methods to design robust control for such real-time system is by estimating the consequence of the uncertainties and disturbances performing on the system and compensate for the same. Various techniques such as uncertainty and disturbance estimator (UDE), disturbance observer (DO), and unknown input observer (UIO) are used for estimation of the effects of the uncertainties and disturbances. However, in this thesis work IDC is used for handling the mismatched uncertainties in the system. It is a simple controller with a reduced number of state derivative calculations. This IDC is used in sliding mode controller to estimate the mismatched uncertainties in the system and calculate the sliding surfaces in the following sections.

5.3.2 Determination of Multitudinal Sliding Surface

MSMC is used for controlling the mismatched uncertainties using inertial delay control. The IDC is used to estimate the number of mismatched disturbances. Moreover, it allows the sliding controller to design in such a way that it reduces the relative degree by the system state as artificial input. These artificial inputs are controlled by the second controller to confirm that the artificial controller tracks the defined profile. The main purpose of the controller is to confirm x_1 track the anticipated trajectory x_{1j}. The first sliding mode surface can be defined as follows:

$$S_1 = \dot{x}_1 - x_{1j} \tag{5.17}$$

The modified sliding surface can be written to minimize the initial control as

$$S_1^* = S_1 - S_1(0)\, e^{-\beta t} \tag{5.18}$$

Where $S_1(0)$ is the initial value

$$\left.\begin{aligned} S_1^* &= x_2 - e_1 - \dot{x}_{1j} + \beta S_1(0)\, e^{-\beta_1 t} \\ e_1 &= S_1^* - x_2 + \dot{x}_{1j} - \beta S_1(0)\, e^{-\beta_1 t} \end{aligned}\right\} \tag{5.19}$$

From the IDC law, the estimation of e_1 as follows:

$$\hat{w} = \frac{1}{\tau s + 1} e_1 \tag{5.20}$$

$$S_2^* = S_2 - S_2(0)\, e^{-\beta_2 t} \tag{5.21}$$

$$\dot{S}_2^* = x_2 + \dot{x}_{2j} - \beta S_2(0)\, e^{-\beta_2 t} \tag{5.22}$$

Where, τ is the time constant. The artificial input x_{2j} is to be designed in such a way that it will make $S_1^* \dot{S}_1^* < 0$ and make ineffective the uncertainty e_1. The artificial input x_{2j} can be derived from Eqs. (5.19), (5.20) and (5.22) as follows:

$$x_{2j} = \dot{x}_{1j} - \hat{w}_1 - \beta_1 S_1(0) e^{-\beta t} - k\ S_1^* \tag{5.23}$$

$$\hat{w}_1 = \frac{1}{\tau_1}\left[S_1^* + \int (k\ S_1^* - S_2^* - S_2(0) e^{-\beta_2 t} \right] \tag{5.24}$$

The solution for the control input μ, which drives S_2^* to zero and hence influence the e_2. Therefore, the desired control input μ as follows:

$$\mu = -b^{-1}(x)\left[a(x) + \beta_2 S_2(0)\, e^{-\beta_2 t} + \hat{w}_2 + k\ S_2^* \right] \tag{5.25}$$

Where, a and b are the constants

The $\hat{w}_2$ can be written as

$$\hat{w}_2 = \frac{1}{\tau_2}\left[S_2^* + \int k\ S_2^*\right] \tag{5.26}$$

Once the sliding surface is defined by the MSMC, the output of MSMC is further processed for the reference current generation. Similarly, the control law for other switches (S_3 and S_4) can be derived.

5.3.3 Bode Diagram and Stability Criteria

The Lyapunov stability criteria can provide the boundaries. The Bode plot for the different MSMC gain parameters is shown in Figure 5.3.

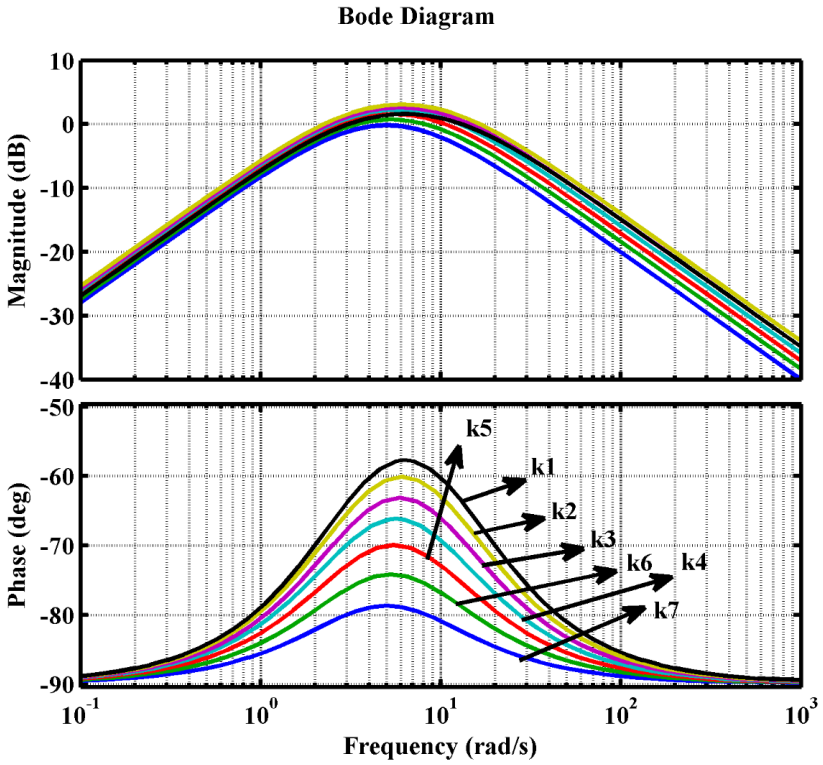


Figure 5.3 Bode plot for multitudinal sliding mode controller

According to the bode plot, increase in the phase margin, improves the transient response of the system with less overshoot and ringing. The phase margin is chosen 68º for the sliding gain of 35 (k_4) which gives the better transient response and minimum ripples in the DC-link voltage. The improvement in source current THD for the different MSMC gain parameters are tabulated in Table 5.1.

5.4 Control Strategy and PWM Switching Generation

The reference current generation is achieved by MSMC based DC-link energy balance theorem and extraction of fundamental signal from distorted voltage signal is achieved by Hilbert transform based ATF as explained in Section 3.3. The block diagram of modified controller is shown in Figure 5.4.

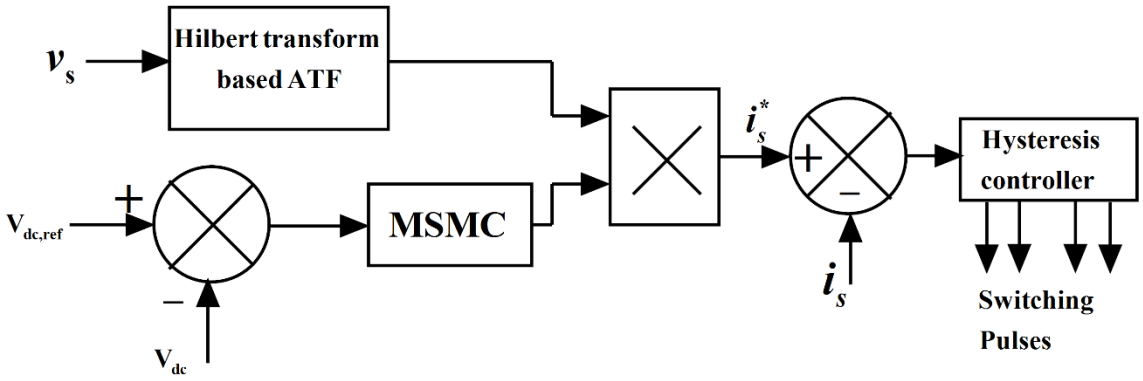


Figure 5.4 Block diagram of MSMC based control algorithm

The Hilbert transform based ATF is extracts the fundamental component of supply voltage from distorted supply voltage. Also, it generates the unit template which is sinusoidal and synchronized to the grid without phase delay. The generated unit template is multiply with output of MSMC which produces reference source current. This generated reference current is compared with the actual source current which gives error output. The switching pulses for the switches of interleaved SAPF are produced by hysteresis current controller. The switching pulses are obtained as:

If $i_{sj} > (i_{sj}^* + \mathrm{HB})$, upper interleaved SAPF switch of j^{th} leg is switched ON and lower switch is OFF.

If $i_{sj} < (i_{sj}^* + \mathrm{HB})$ upper interleaved SAPF switch of j^{th} leg is switched OFF and lower switch is ON, Where, the HB is the hysteresis band around the reference current.

5.5 Modelling of Single-Phase Interleaved SAPF using MATLAB®/Simulink Environment

The feasibility analysis and comparative study of PI, conventional SMC and MSMC based control algorithm with interleaved SAPF are simulated in MATLAB®/ Simulink

environment with extension of SimPowerSystem library. The model consist of single-phase AC source, interleaved inverter made up of MOSFET switches, interfacing inductor which split into two, DC-link capacitor, a non-linear load and a developed MSMC control scheme. The source voltage, non-linear load parameters, feeder impedance and controller parameters for the simulation studies have been tabulated in Appendix-B3.

5.6 Simulation Results

The performance of the MSMC based modified control algorithm is tested under the sinusoidal and distorted supply voltage conditions. Rigorous simulation studies have been carried out under the steady-state and transient condition of the load with sinusoidal and distorted supply voltage conditions.

5.6.1 Simulation under Ideal Supply Voltage Condition

The performance parameters of supply voltage (V_S), source current (I_S), load current (I_{Load}) and compensating current (I_C) are shown in Figure 5.5. In order to test the compensation competence, a single-phase full wave diode bridge rectifier with R-L load is connected as non-linear load.

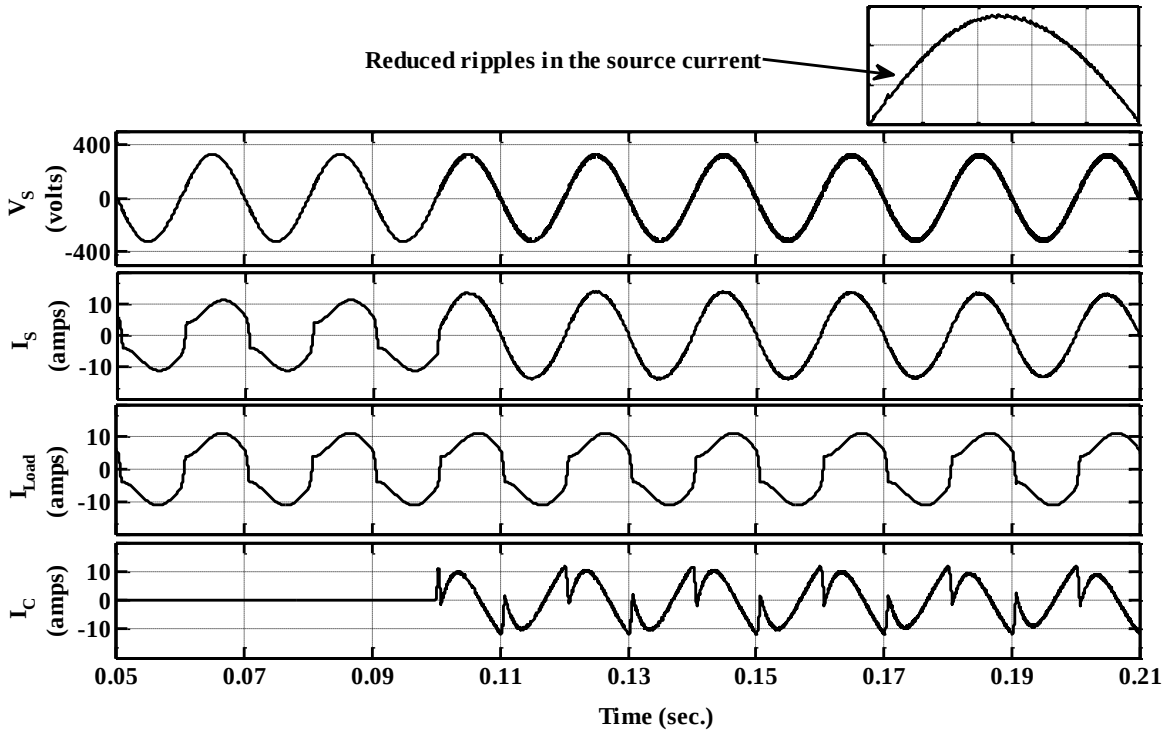
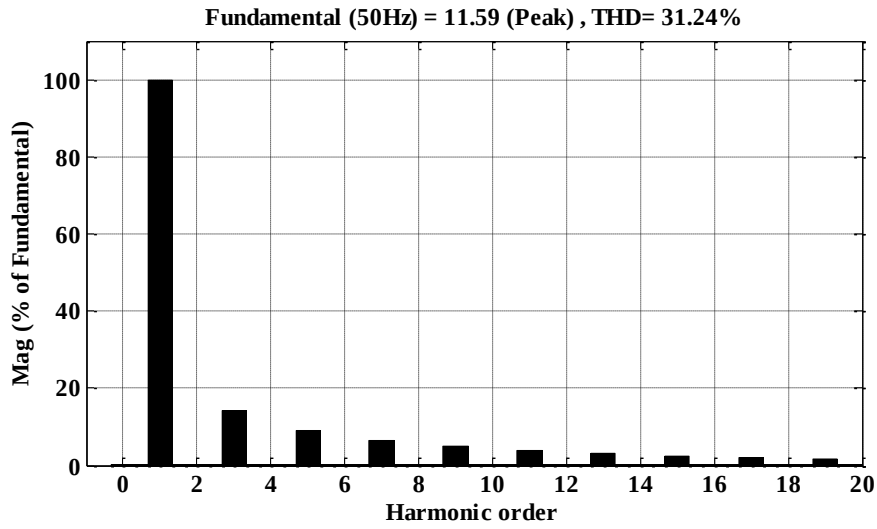
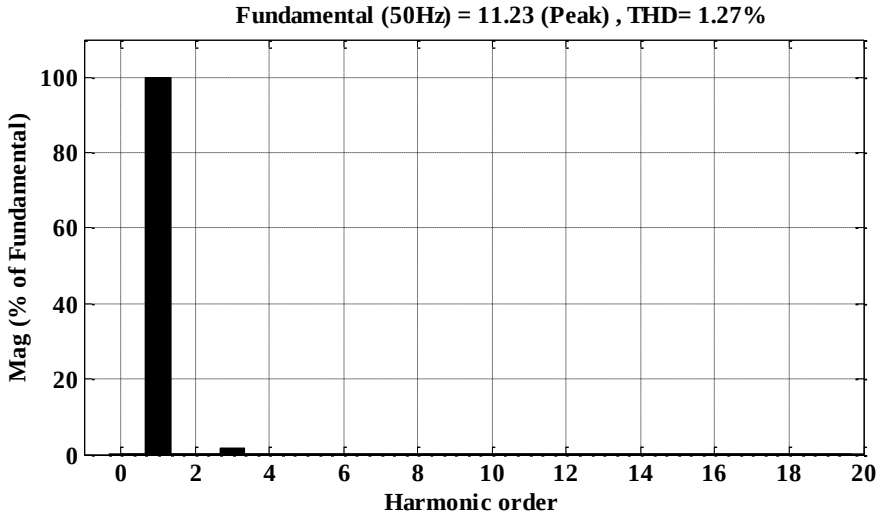


Figure 5.5 Performance of interleaved SAPF under the sinusoidal supply voltage condition

This non-linear load injects the current harmonics and draws the reactive power, therefore the power factor of the system becomes poor. The source current has the same amount of THD levels as the load current possess due to this non-linear load. The MSMC based modified control technique is implemented for the reference current generation in this chapter.



(a)



(b)

Figure 5.6 Harmonic spectrum of source current (a) Before compensation, and (b) After compensation

The unit template will be generated by dividing the supply voltage by its peak value which further multiplies with the output of MSMC for the reference current generation. The

generated reference current is compared with the actual source current and produce an error. The generated error is fed through the hysteresis band current controller and produce switching pulses for the interleaved SAPF. The flow of compensating current can be controlled by these switching pulses. These switching pulses given to the MOSFET switches of interleaved inverter. At the instant, when the interleaved SAPF is switched on at 0.1 sec. as shown in Figure 5.5, the source current profile becomes sinusoidal with reduced ripples and brings back to the harmonic level from 31.24% to 1.27%. It can be concluded that the MSMC based modified control algorithm is quick and able to compensate harmonics injected by the nonlinear load. Figure 5.6 (a) and (b), respectively show the harmonic spectrum of the source current before and after compensation. It can be contemplated from these results that the performance of interleaved SAPF is satisfactory in maintaining the unity power factor at the supply side and bringing back the non-sinusoidal source current to sinusoidal by maintaining the IEEE-519 standards which shows the compensation capability of the control algorithm.

5.6.2 Performance Evaluation under Distorted Supply Voltage Condition

To verify the robustness of the MSMC based interleaved SAPF, the performance analyzed under the distorted supply voltage condition. Practically, the supply voltage is not pure sinusoidal, but having distinct harmonic contents. The simulation performance has been conducted by introducing 5^{th} and 7^{th} harmonic contents in the supply voltage with THD of 11.74% as shown in Figure 5.8 (a), which is as follows:

$$V_S = 325.26 * \sin(\omega t) + 65.05 * \sin(5\omega t) + 46.46 * \sin(7\omega t) \tag{5.27}$$

The distorted supply voltage has fundamental and harmonic component of voltage in the waveform. The Hilbert transform based ATF alters the frequency of the SAPF output voltage if the grid voltage and SAPF output voltage are out of phase due to sudden change in load and distortion in the supply voltage. Moreover, Hilbert transform based ATF is used to generate sinusoidal unit template signal from the distorted supply voltage by extracting fundamental component. Further, this unit template multiply with output of MSMC for generating the reference source current. The switching pulses generated for interleaved SAPF when the difference of actual and reference source goes to through hysteresis current controller. A complete block diagram of control algorithm is shown in Figure 5.4.

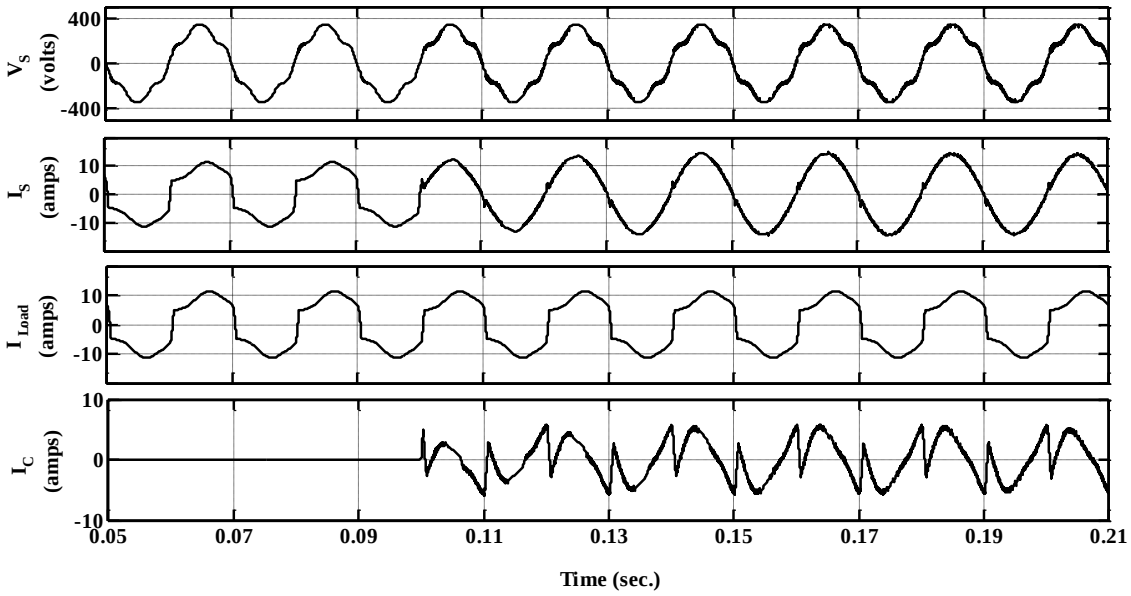
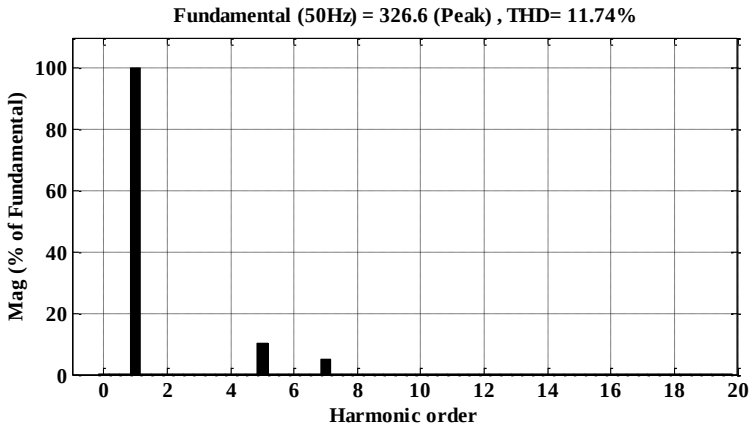
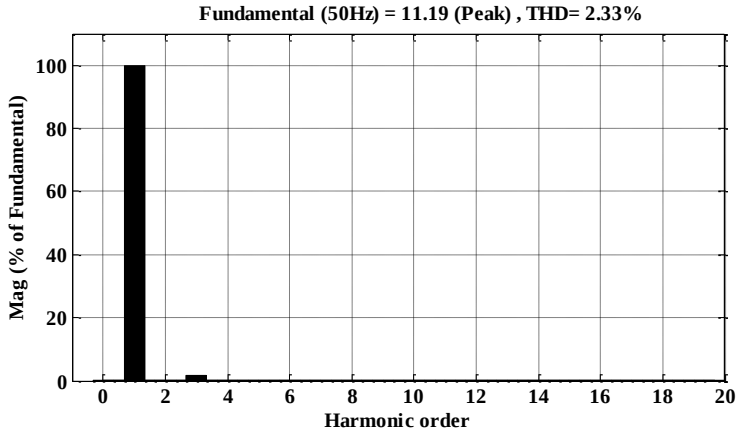


Figure 5.7 Performance parameters of interleaved SAPF under the distorted supply voltage



(a)



(b)

Figure 5.8 Harmonic spectral waveforms (a) Distorted supply voltage, and (b) Source current after compensation

The simulation performance of MSMC based interleaved SAPF under the distorted supply voltage is shown in Figure 5.7. It can be concluded from these results that the MSMC based modified control algorithm is able to compensate current harmonics and reactive power to ensure unity power factor under the distorted supply voltage condition. The harmonic spectral diagram of source current after compensation are shown in Figure 5.8 (b), which shows the superiority of this presented control algorithm. The variations in the source current wave shape is not differentiable but, these different MSMC gain parameters impact the source current THD which are tabulated in Table 5.1.

Table 5.1

Simulation results of %THD for different values of gain parameters (k)

MSMC gain (k) values	**THD (%) of the source current (Simulation)**
k_1=90	3.5
k_2=80	3.1
k_3=40	1.84
k_4=35	1.04
k_5=30	3.3

5.6.3 Simulation Study under Transient Condition of Load

The amount of loads in the electrical power system are not constant but changes abruptly. The DC-link voltage tracking capability of presented MSMC based modified control algorithm is tested under the transient load in comparison with conventional SMC and PI controllers. The real power supplied by the source to load during transient condition is not equal, the capacitor has to supply required amount of power during this condition. The load is increased to 200% from the normal value at 0.9 sec. and released at 1.4 sec. as shown in Figure 5.9. The FFT analysis also observed before and after load perturbations using powergui tool in SimPowerSystem. The harmonic spectrum of load current is changed from 30.23% to 32.14% as shown in Figure 5.10 (a) and (b) due to % change in non-linear load. The DC-link voltage stabilization during load perturbation using PI controller is shown in Figure 5.11 (a). The moment when load increased suddenly to 200% of its baseload at 0.9 sec, the DC-link capacitor undergone to its reference value and settled

at 400 V after 10 cycles. Similarly, load decreased to the normal value at 1.4 sec, the DC-link voltage rises over to its reference value and setback to its reference value after 10 cycles. The FFT analysis of source current after load change is observed as shown in Figure 5.11 (a) and (b), respectively. The harmonic compensation is degraded from 4.11% to 6.18% due to more steady state error which leads to ripples in the DC-link voltage. Similar load perturbation test has been conducted to test the performance of conventional SMC based control algorithm. During load increased at 0.9 sec, the DC-link voltage has undergone to below its reference value to supply active power demand of the load. The SMC is designed to achieve reduced steady-state error under load perturbations.

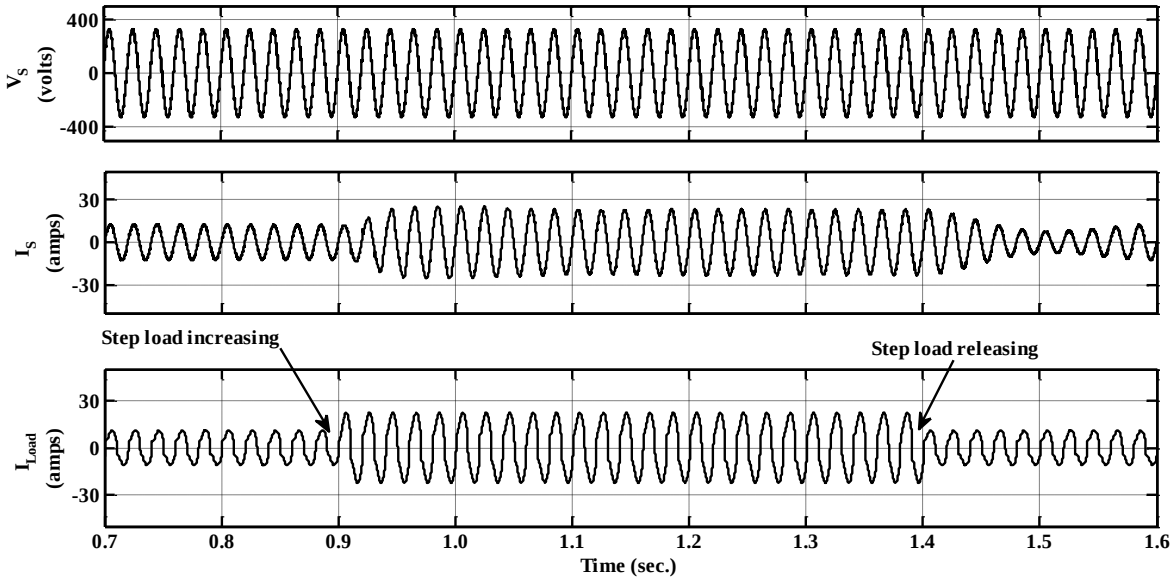
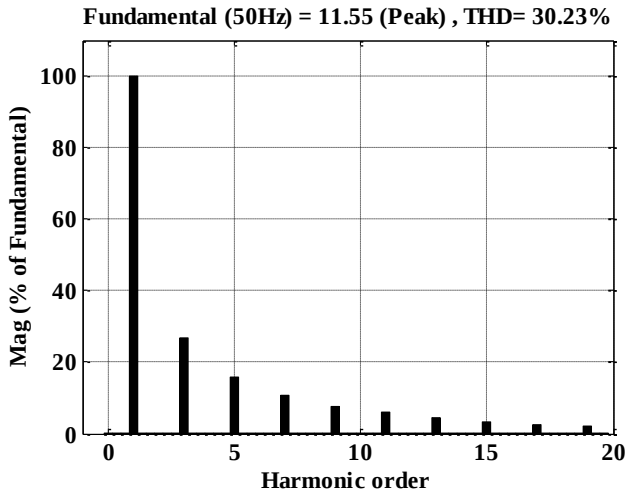


Figure 5.9 Load perturbation response of interleaved SAPF for load increase and load decrease case

The DC-link voltage stabilization during load perturbation using conventional SMC is shown in Figure 5.12 (a). The DC-voltage has undergone below to its reference value and settled at 400 V after 6 cycles and similarly when load removed at 1.4 sec, the DC-link voltage has gone above the reference value and settled at 400 V after 6 cycles. The FFT analysis of source current also observed before and after load change as shown in Figure 5.12 (b) and (c), respectively. It can be observed from Figure 5.12 (b) and (c) that the source current still have harmonic contains above limit value due to the uncertainty in the controller which creates undesirable ripples in the DC-link voltage. Hence, the source current waveform below the standard shape. The MSMC based modified control algorithm is designed to overcome the uncertainty while tracking the DC-link voltage during load

perturbations and reduce the steady-state error. The DC-link voltage stabilization performance of MSMC is shown in Figure 5.13 (a). The MSMC based modified algorithm improves the system performance by reducing steady-state error and forced oscillations therefore, the overall system stability will be improved. It is observed from Figure 5.13 (a) that the DC-link voltage achieved to its reference value during both load increase and load decrease cases. It can be concluded that, the MSMC has good dynamic response under the transient condition of the load with less overshoot.



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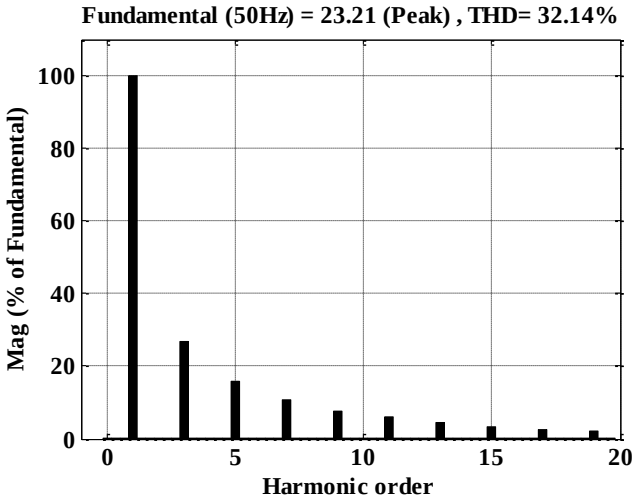
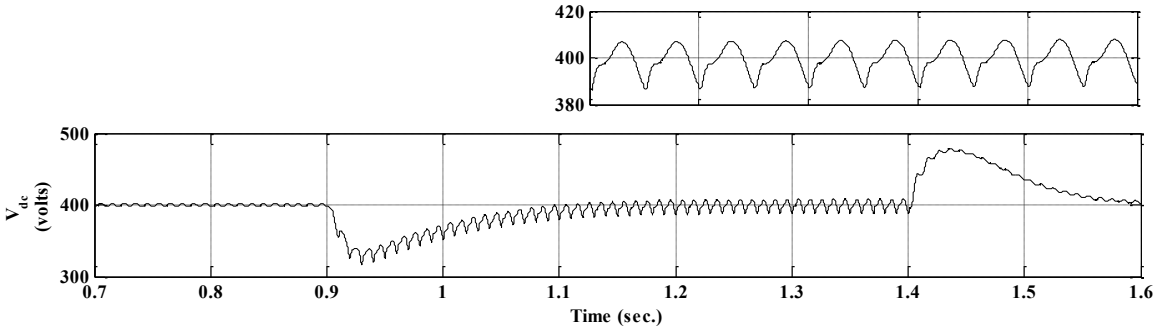


(b)

Figure 5.10 (a) Harmonic spectrum of load current before, and (b) After load change



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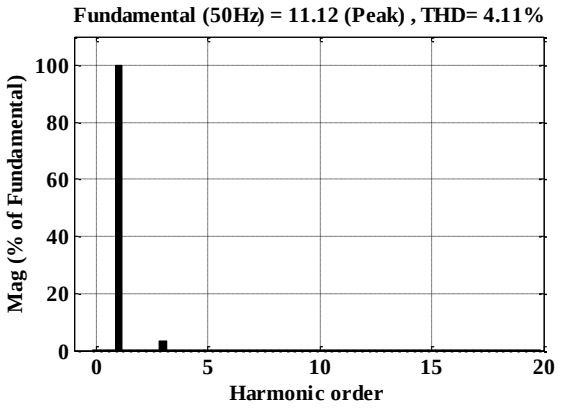

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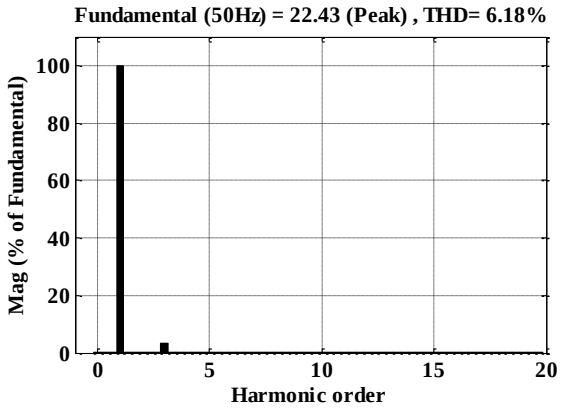
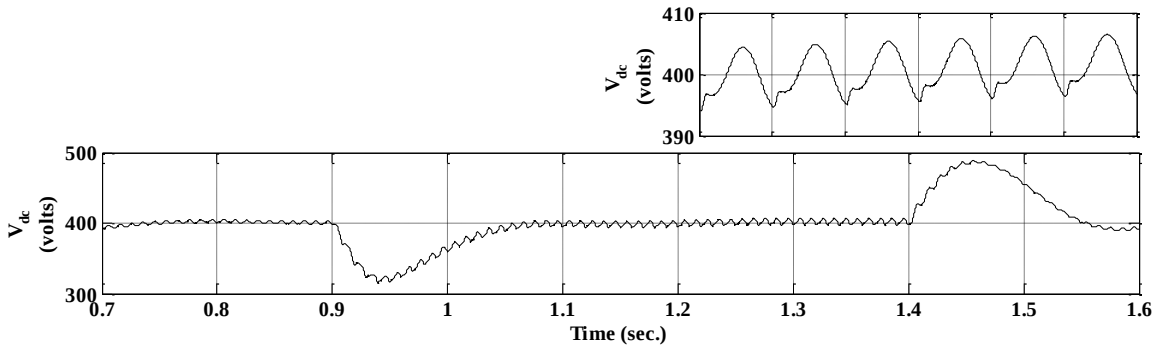


(c)

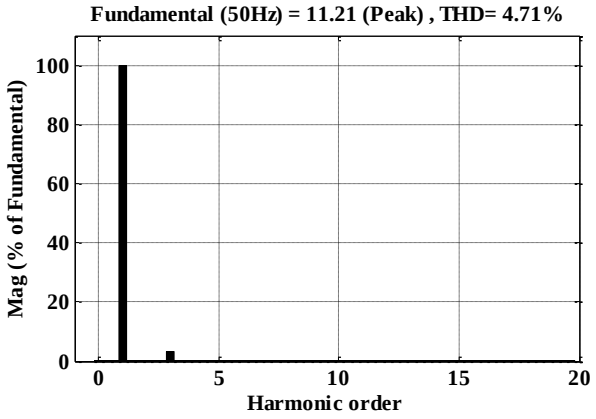
Figure 5.11 (a) DC-link voltage stabilization during load perturbations using PI controller, (b) Frequency spectrum of compensated source current before, and (c) After load change

The DC-link voltage settled back to its original value within two cycles with less ripples where, conventional SMC and PI controller have slow responses and more ripples in DC-link voltage. The harmonic spectral analysis of source current before and after load change are shown in Figure 5.13 (b) and (c), respectively.

It is observed from Figures 5.13 (b) and 5.13 (c), that the source current THD below 5% as per IEEE-519 standards. The complete comparison of PI, conventional SMC and MSMC are shown in Table 5.2, which confirms that the MSMC is effective and robust under the transient condition of the load.



(a)



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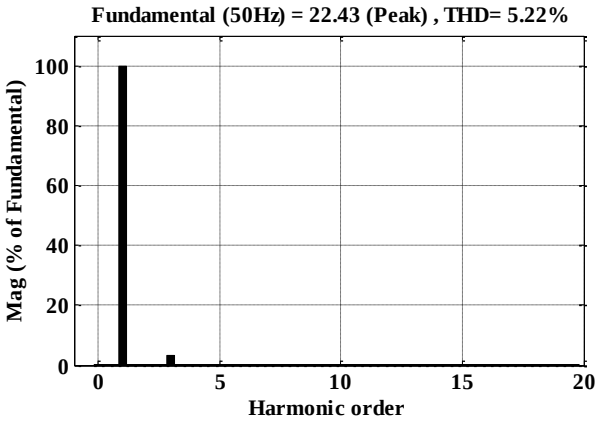
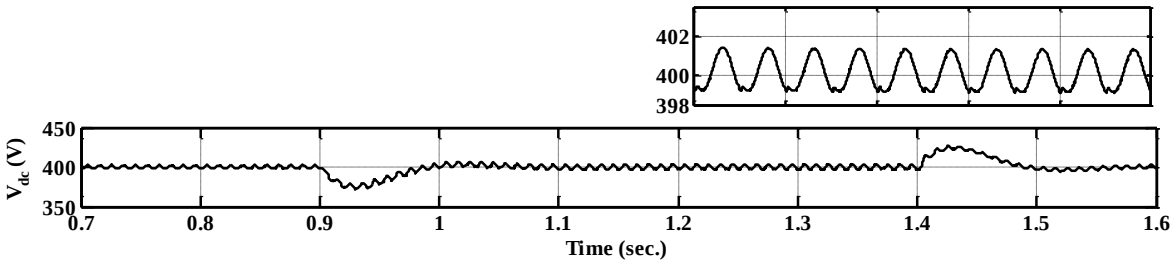


(c)

Figure 5.12 (a) DC-link voltage stabilization using conventional SMC based algorithm, (b) FFT analysis of source current before load change, and (b) After load change



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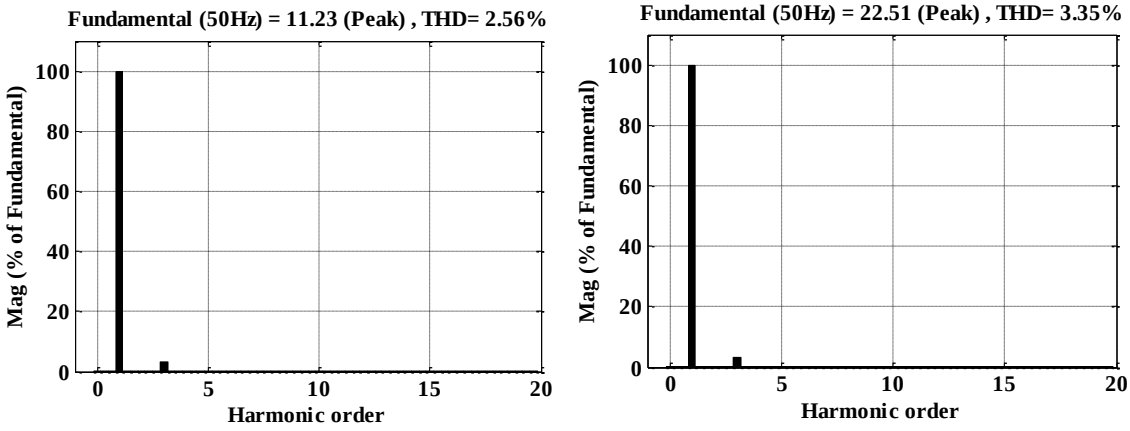


(b) (c)

Figure 5.13 (a) DC-link voltage stabilization using MSMC based modified algorithm (b) FFT analysis of source current before load change, and (b) After load change

Table 5.2

Simulation comparison of PI, SMC and MSMC based interleaved SAPF

Control strategy	**Value of capacitance (μF)**	**DC-link voltage ripple (V)**	**No. of cycles for stabilizing the DC-link voltage under transient load condition**	**%THD of source current (i_s)**
PI	1000	15	10	4.3%
Conventional SMC	1000	10	6	3.84%
MSMC	1000	3	2	1.5%

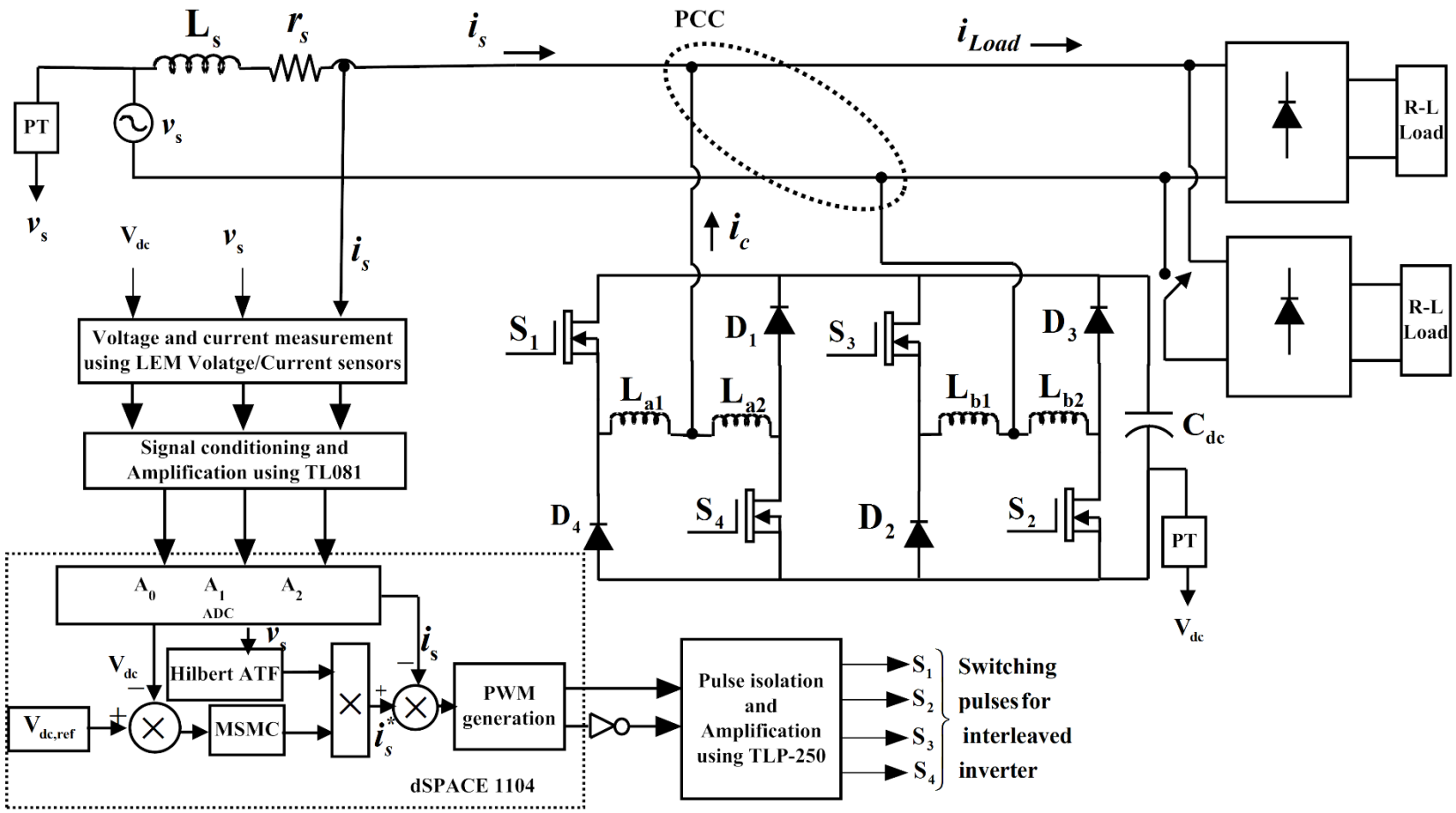


Figure 5.14 Block diagram of single-phase interleaved SAPF

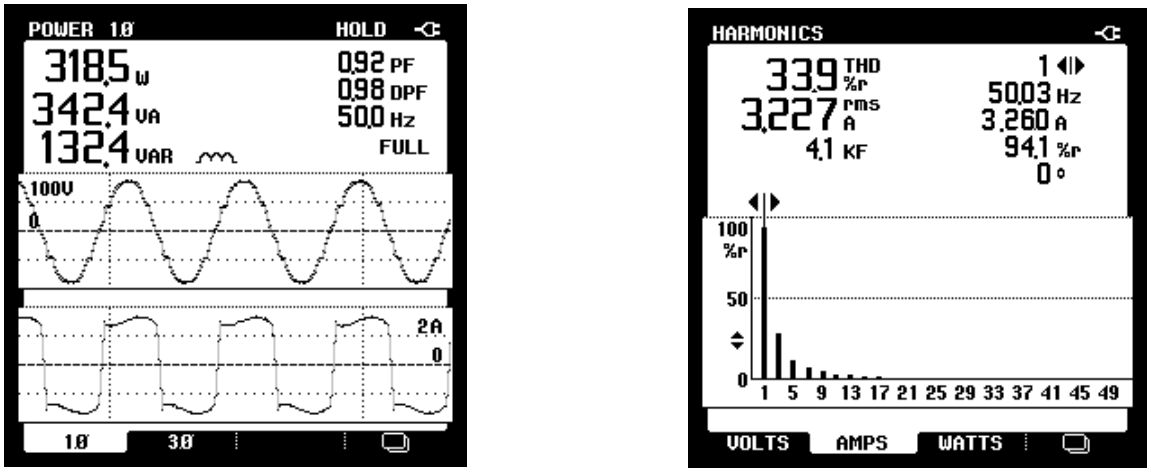
5.7 Hardware Implementation and Experimental Investigation

The significance of MSMC based modified reference current generation technique for single-phase interleaved SAPF in comparison with the PI controller based and conventional SMC based control techniques are tested in the laboratory prototype model. The block diagram of the suggested system is shown in Figure 5.14. A diode bridge rectifier with R-L is used as a non-linear load to test the MSMC based modified control technique under the steady-state and transient condition of the load. Voltage and current sensors, gate driver circuit, dSPACE1104 controller board, signal condition board are already discussed in section 3.6. The interleaved inverter does not require dead-band circuit which enhances the operation of shunt active filtering capability.

5.7.1 Experimentation under Steady-State Condition of Load

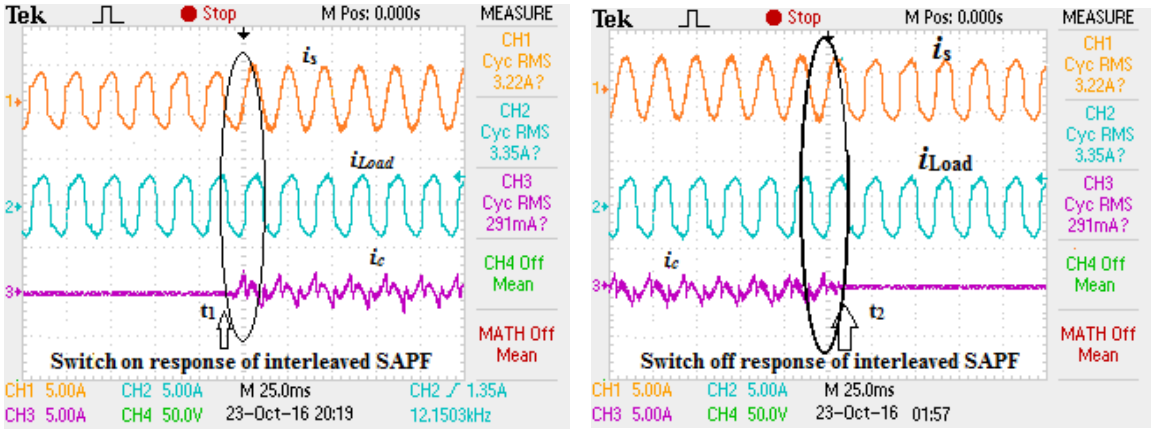
The performance of MSMC based interleaved SAPF is tested under normal available grid supply voltage (1 to 2 % measured THD at the time of experimentation) by connecting single-phase full wave diode bridge rectifier with R-L load as non-linear load. This non-linear load is injecting the current harmonics and draws the reactive power, therefore, the source current will be distorted. The source current wave shape and its %THD pattern are shown in Figure 5.15 (a) and (b), respectively. It can be depicted from Figure 5.15 (b) that source current having 33.9% THD before compensation as load current possess due to this non-linear load. When the interleaved SAPF switched on as shown in Figure 5.16 (a) at time t_1, the harmonic compensating current injects into the system at PCC which makes distorted source current into sinusoidal. When the interleaved SAPF is switched off as shown in Figure 5.16 (b) at time t_2, the source current retrieve to its original shape as load current wave shape which shows that the MSMC based modified controller is fast. The reactive power is reported by the power quality analyzer before and after compensation are shown in Figure 5.15 (a) and 5.18 (a), respectively. The reactive power requirement of the load is compensated by the interleaved SAPF from 132.4 VAR (inductive) to 69.4 VAR (capacitive). The interleaved SAPF undergoes slightly over compensation to supply extra reactive power for maintaining the PCC voltage under this steady-state operation. The experimental performance waveforms of supply voltage (v_s), source current (i_s) and compensating current (i_c) are shown in Figure 5.17 (a). The Figure 5.17 (b) shows the

source current after compensation (i_s), load current (i_{Load}) and compensating current (i_c). It can be observed from these results that the interleaved inverter with MSMC based control algorithm is working successfully by compensating of current harmonics and reactive power burden. The interleaved SAPF improves the harmonic pattern of the source current and it becomes 3.7% from 33.9% as shown in Figure 5.18 (b). It is evident that interleaved SAPF does not require any dead band circuit, fast in response, no time delay and good in harmonic compensation.



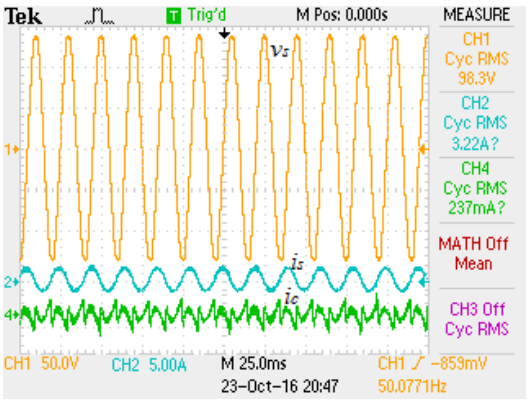
(a) (b)

Figure 5.15 (a) Source voltage and current waveforms before compensation, and (b) Harmonic spectrum of source current before compensation



(a) (b)

Figure 5.16 Experimental performance of the interleaved SAPF under available supply voltage**:** source current, load current and compensating current (a) Switch-on response, and (b) Switch-off response



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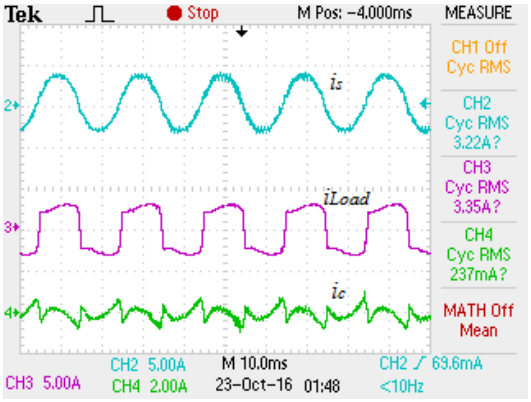
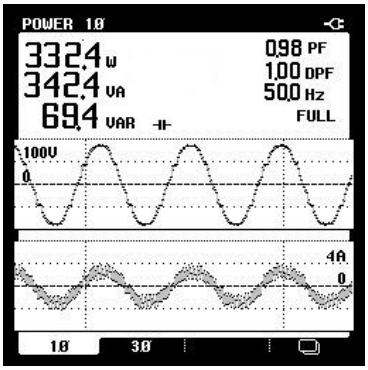


(b)

Figure 5.17 Experimental performance of (a) Source voltage, source current after compensation, compensating current, and (b) Source current after compensation, load current and compensating current



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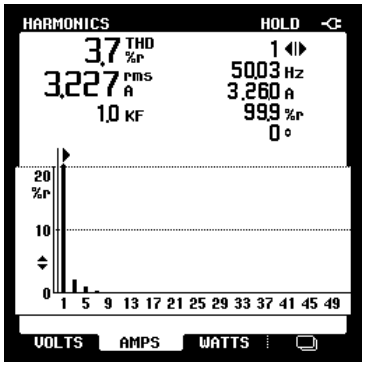


(b)

Figure 5.18 (a) Reactive power compensation to ensure unity power factor, and (b) Harmonic spectrum of source current after compensation

5.7.2 Performance Analysis under Distorted Supply Voltage Condition

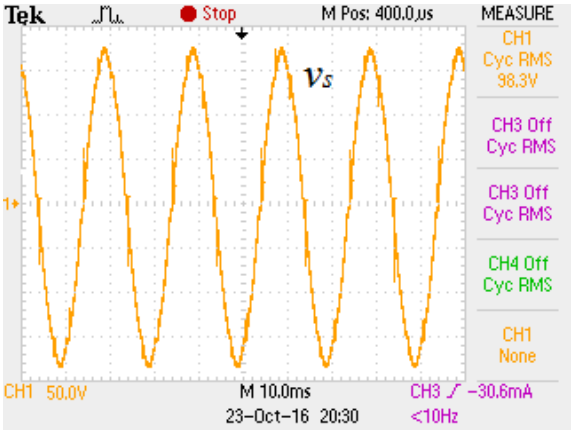
The compensation capability of single-phase MSMC based interleaved SAPF tested under the distorted supply voltage condition. In order to create distorted supply voltage at

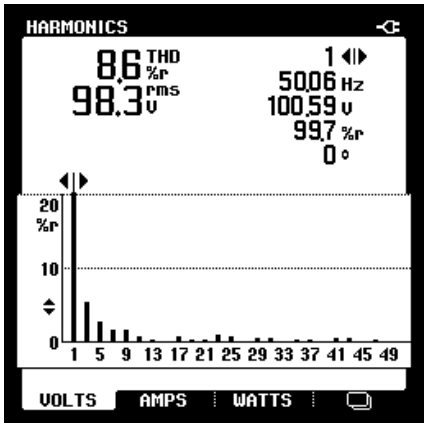
PCC in the laboratory, a separate single-phase diode bridge rectifier with higher value of R-L load is connected nearer to the auto transformer therefore, the supply voltage profile will be distorted. The distorted supply voltage profile and its respective harmonic spectrum are shown in Figure 5.19 (a) and (b), respectively. The performance waveforms of source current (i_s), load current (i_{Load}) and compensation current (i_c) are observed with the different MSMC gain parameters as shown in Figure 5.20 (a) to (c) and with respective improvement in %THD are shown in Figure 5.20 (b) and (d). It can be contemplated from these results that the MSMC based modified control algorithm is effective for synchronization with the grid and generation of sinusoidal unit template from the distorted voltage signal for the generation of reference current. It can be observed from the Figure 5.20 (b) and (d) that, the MSMC gain parameters are influencing the source current THD by reducing the DC-link voltage ripples. The effect of sliding gain parameters in the performance of source current THD are tabulated in Table 5.3. The combined waveforms of distorted supply voltage and source current are shown in Figure 5.21 (a). It is observed from Figure 5.21 (a) that the non-linearity of load and distortions in the supply voltage are imposed into the source current which affect the source current waveform. Figure 5.21 (b) and (c), respectively show the reactive power demand of the load and reactive power compensation by the interleaved SAPF. The interleaved SAPF compensates reactive power from 131.3 VAR (inductive) to 12.4 VAR (inductive) to improve the power factor from 0.9 (lagging) to 0.98 (lagging). The harmonics presented in the source current are well within the IEEE 519 standard. It is evident that the MSMC based modified control technique is capable to compensate current harmonics and reactive power burden to ensure unity power factor even under the distorted supply voltage condition.

Table 5.3

Experimental results of %THD for different values of gain parameters (k)

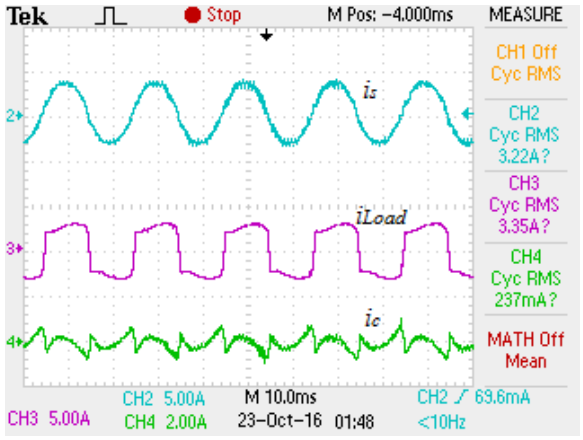
MSMC gain (k) values	**% THD of the source current (Experimental)**
k_1=90	6.2
k_2=80	3.7
k_3=40	3.3
k_4=35	2.6
k_5=30	5.3

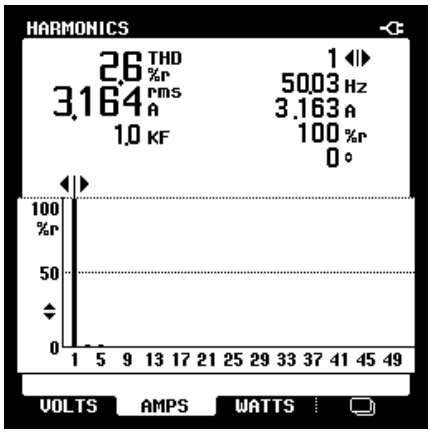




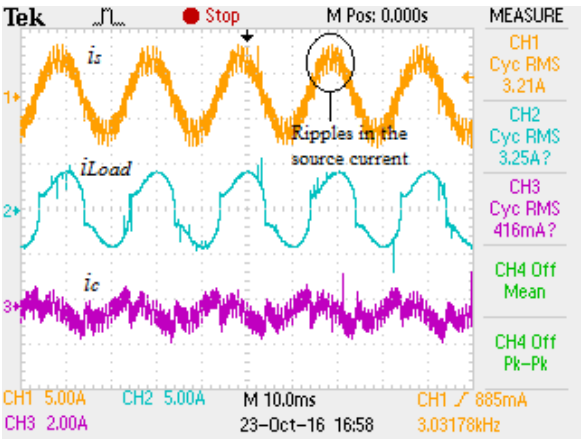
(a) (b)

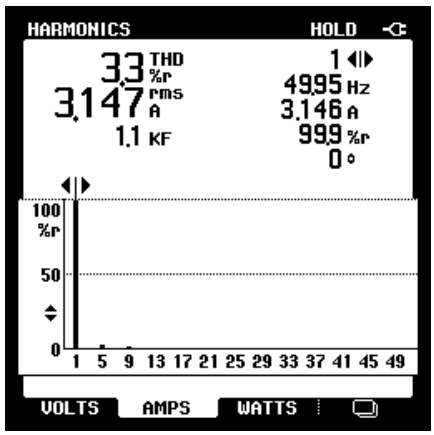
Figure 5.19 (a) Distorted supply voltage, and (b) Distorted supply voltage THD





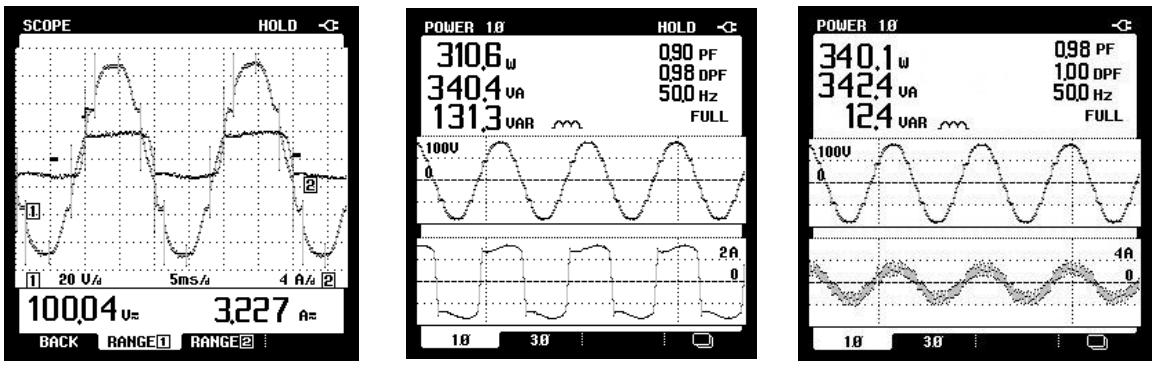
(a) (b)





(c) (d)

Figure 5.20 Experimental results for different MSMC gain parameters (a) &(c) Source current (i_S), load current (i_{Load}), compensating current (i_c), and (b) & (d) Represent %THD of compensated source current

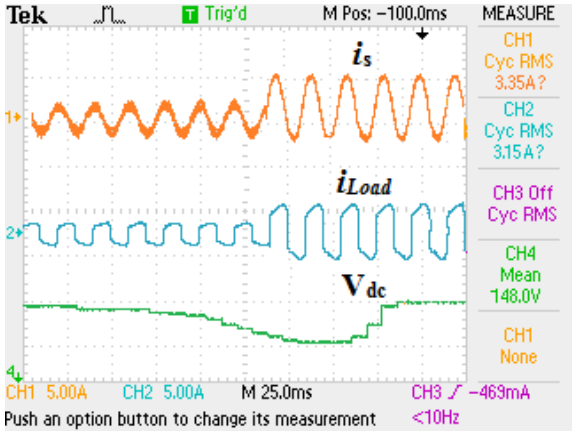


(a) (b) (c)

Figure 5.21 Experimental results of reactive power compensation (a) Distorted supply voltage and source current before compensation, (b) Load reactive power requirement before compensation, and (c) Improvement of power factor by compensation of reactive power under the distorted supply voltage after compensation

5.7.3 Experimentation under Transient Condition of Load

The effectiveness and robustness of the MSMC based interleaved SAPF is tested under the step load change condition. During this transient condition, the real power difference between load and source are not equal which can be compensated by the DC-link capacitor. The DC-link capacitor voltage has to recover quickly to its reference value to balance the real power demand of the load. The transient condition of the load is conducted in two cases, one is step load increase and the second one is step load decrease. The load increases from 1.5 A to 3.35 A, and load decreases from 3.35 A to 1.5 A. Figure 5.22 (a) and (b), respectively show the response of the PI-based system for the load increase and load decrease. When step load increase, the capacitor voltage decreases to supply a sufficient amount of real power to the load and settled to its reference value. When step load decrease, the capacitor voltage increases to maintain real power difference. It is observed that the PI controller has sluggish response under the transient load change conditions. The conventional SMC based system performance is tested in sudden load increase and load decrease conditions are shown in Figure 5.22 (c) and (d), respectively. The conventional SMC tracks the DC-link voltage to stabilize with its reference value within four cycles even under the distorted supply voltage case, which shows the superiority and robustness of the controller. However, due to uncertainty in the load profile, the conventional SMC fails to track reference value of the DC-link voltage quickly. The step load increase and decrease response of the MSMC are shown in Figure 5.22 (e) and (f), respectively.



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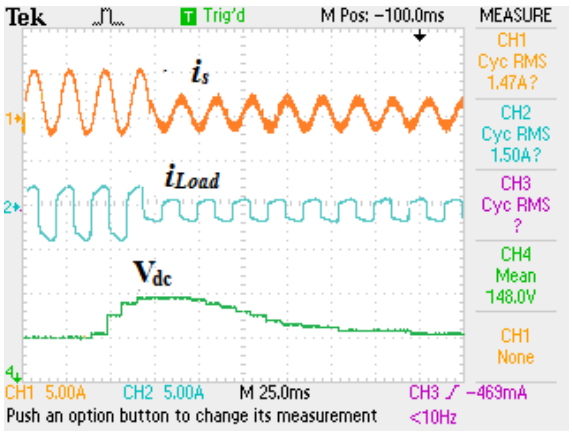

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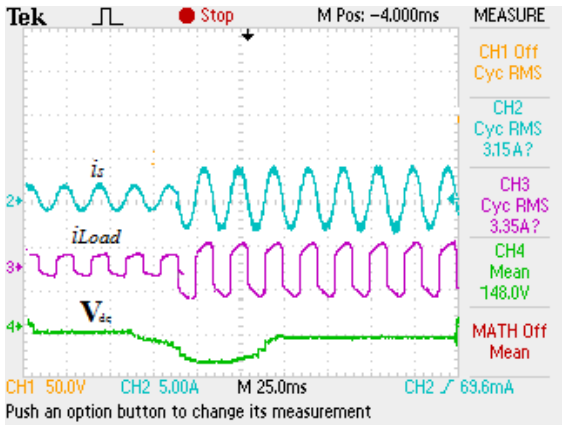

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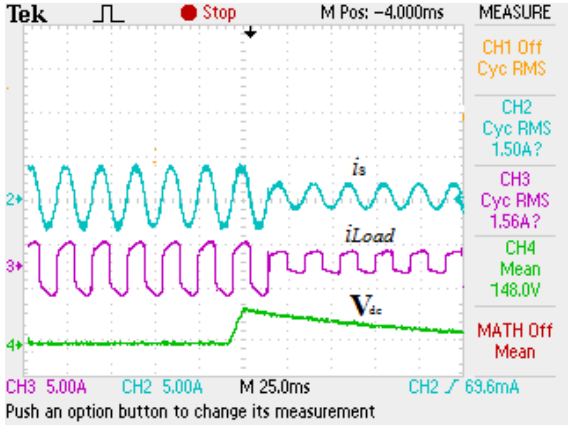

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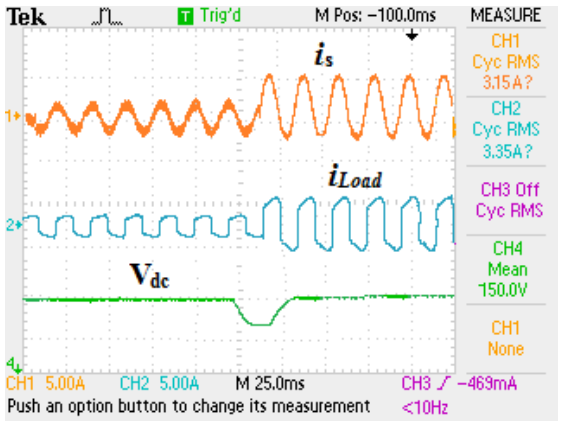

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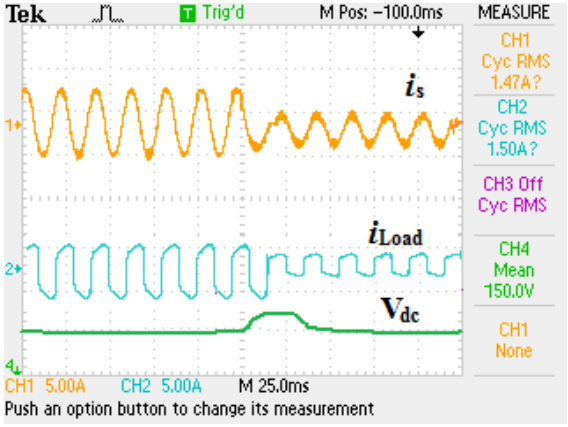


(f)

Figure 5.22 Performance parameters of interleaved SAPF source current, load current and DC-link voltage response under transient condition of the load (a)-(b) PI controller (CH4 50 V/div), (c)-(d) Conventional SMC (CH4 50 V/div), and (e)-(f) Multitudinal sliding mode controller (CH4 50 V/div)

The MSMC based interleaved SAPF is sensitive to the load changing under the distorted supply voltage condition and good DC-link voltage tracking capability under uncertainty in load and mismatched load profile. A fair performance comparison of PI controllers, conventional SMC and MSMC are tabulated in Table 5.4.

Table 5.4

Experimental comparison of PI, SMC and MSMC based interleaved SAPF

Control strategy	**Value of capacitance (μF)**	**DC-link voltage ripple (V)**	**No. of cycles for stabilizing the DC-link voltage under transient load condition**	**% THD (Experimental)**
PI Controller	1000	20	10	4.6
Conventional SMC	1000	10	4	3.7
MSMC	1000	5	2	2.4

5.8 Conclusion

A multitudinal sliding mode controller based reference current generation is presented in this chapter for effective harmonic and reactive power compensation under steady-state and transient condition of the load. The DC-link voltage plays a pivotal role in the compensation of harmonics generated due to the presence of non-linear loads. Various simulation studies have been carried out to test the compensation competence of the MSMC technique. A fair comparison study has been carried out between MSMC, conventional SMC and PI controllers based control algorithms under sudden load changing conditions. The MSMC successfully rectify the effect of mismatched uncertainties under the sudden load changing condition where conventional SMC and PI controller are failed. The MSMC has good tracking capability to stabilize the DC-link voltage and reduce the steady-state error under the transient condition of the load as compared to the conventional SMC and PI controllers. A laboratory prototype model of the interleaved SAPF has been designed, developed and tested successfully in the laboratory. The control techniques have been realized using a dSPACE1104 controller. It can be concluded from the exhaustive simulated and experimental results that the harmonic compensation process can be achieved easily by MSMC based interleaved SAPF with the good dynamic response with reduced DC-link voltage ripples and improved efficiency of the system.

CHAPTER 6

ENHANCED PARTICLE SWARM OPTIMIZATION BASED CONTROL TECHNIQUE FOR THREE-PHASE SHUNT APF

List of Published Papers

1. **V. Gali**, N. Gupta and R. A. Gupta, "Enhanced Particle Swarm Optimization Based Dc-Link Voltage Control Algorithm for Interleaved SAPF" *Journal of Engineering Science and Technology*, Taylors University Press, vol. 13, no. 10, pp. 3393-3418, Oct. 2018.
2. **V. Gali**, N. Gupta and R. A. Gupta, "Enhanced Particle Swarm Optimization Technique for Interleaved Inverter tied Shunt Active Power Filter", in *Proc. of 7th International Conference on Soft Computing for Problem Solving (SocProS-2017)*, Indian Institute of Technology Bhubaneswar, Bhubaneswar, pp. 571-583, December 23rd – 24th, 2017. (Published in book chapter; Soft computing for problem solving, springer publishers)
3. **V. Gali**, N. Gupta and R. A. Gupta, "Improved Dynamic Performance of Shunt Active Power Filter using Particle Swarm Optimization," in Proc. of IEEE International Conference on Intelligent Techniques in Control, Optimization & Signal Processing (INCOS), Kalasalingam University, Srivilliputtur, pp. 505-511, March 23rd-25th, 2017.

CHAPTER 6

ENHANCED PARTICLE SWARM OPTIMIZATION BASED CONTROL TECHNIQUE FOR THREE-PHASE SHUNT APF

6.1 Introduction

The DC-link voltage plays a significant role in the compensation performance of active power filters. It supplies harmonic component of currents, switching losses, reactive power under the steady-state and real power under the transient condition of the load. During a transient condition of the load, there is a large variation between reference and actual values of DC-link voltage. The DC-link voltage has to be maintained at reference value irrespective of load changes [119-120]. The PI controllers have been used in the industry because of its simple structure, low cost, less design complexity. The proportional gain value (k_p) helps to improve the system performance by reducing steady-state error and forced oscillations whereas integral gain value (k_i) enhance the overall system stability [121]. The variable non-linear loads inject different harmonic components into the system which violate the DC-link voltage from its reference value. Hence, this serious undesirable oscillations (overshoot and undershoot) lead to the dielectric breakdown of the DC-link capacitor under the transient condition of the load. In another hand, the DC-link capacitor has to supply instant, real power to meet the load requirement which leads to a sharp decrement in DC-link capacitor voltage when load increased and vice versa [124-125]. It is important for the controller to adopt the changes in the system and maintain the DC-link voltage at its reference value. Therefore, tuning of PI controller gain values has become very much important for efficient operation of the interleaved shunt APF. In 1942, Ziegler and Nichols were employed in the Tylor Instruments, developed a mathematical model for tuning of PI controller gain values. This method of tuning is having rugged response under the transient condition of load and supply distorted voltages. Various optimization techniques have been proposed by the researchers to optimise the PI controller gain values [118]. The FLC have found to be an impressive tool because of its high robustness, insensitive to parameters

changes, treating non-linearity, etc. However, this has disadvantages like (i) lack of accuracy to select optimum number of rules since various factors are involving in the assessment like performance of controller, compensation efficiency, choice of linguistic variables, etc. (ii) the knowledge of human operator is repeatedly inadequate and non-methodical, (iii) the rules are not assured to be coherent hence, arises mismatch between rules, and (iv) large computational time for fuzzification and defuzzification [128-129]. Passino has motivated BFO algorithm, foraging behaviour of bacteria that observes the chemical gradients in the environment and move towards or away from the specific signal [131]. The enactment of the bacteria progressed into four sections, chemotaxis, swarming, reproduction, and elimination & dispersal [134-135]. The speed of the convergence to obtain maximum at the lower search space for saving the time and memory is the big challenge for the researchers. Particle swarm optimization technique has been introduced by Eberhart and Kennedy in the year 1995 by understanding the swarming behavior of the bird and fish flock [136]. The PSO has advantages like solving multi-objective function, non-linearity and non-differentiability with the multi-diametrical problem. A swarm processed in the search space to discover optimal solutions. The particles in the search space try to reach its optimal solution by updating position on own best position obtained by each particle. Due to its simplicity, ease of implementation with low-cost controllers and a well-balanced mechanism to reach out local and global best, it became more popular in various applications [137-139]. However, it has disadvantages like exploring all local best position obtained by the all particles in the search space which increase the complexity of the computation, reduce the speed of the processors and increase the number of iterations. By considering the above issues of optimization problems, an enhanced particle swarm optimization (EPSO) technique is presented in this thesis work to solve multi-objective function by eliminating the local best opposition and improve the converge speed obtained by the particles in the search space. Also, the performance improvement is compared with conventional techniques.

6.2 Enhanced Particle Swarm Optimization Control Scheme

6.2.1 Analysis on Minimum DC-Link Voltage Requirement and Problem Formulation

The DC-link voltage plays a remarkable role in the harmonic compensation process. In practical scenario, the system harmonic currents vary frequently with a change in non-

linear loads. In steady-state operation, the real power supplied by the source is equal to load demand and power losses in the interleaved SAPF switches, inductors. There is a real power difference between the source and load demand during a transient condition of the load. The DC-link capacitor can supplies this extra real power during the transient condition of the load. Hence, the DC-link capacitor acts as an energy source to maintain the energy balance in the interleaved SAPF. The DC-link capacitor voltage has to be maintained its reference value irrespective of load changes. The objective function of minimum DC-link voltage requirement for three-phase interleaved inverter based SAPF can be derived from the circuit operation. The equivalent model of interleaved inverter system is shown in Figure 6.1. The following equation can be derived by applying Kirchhoff's voltage law as follows:

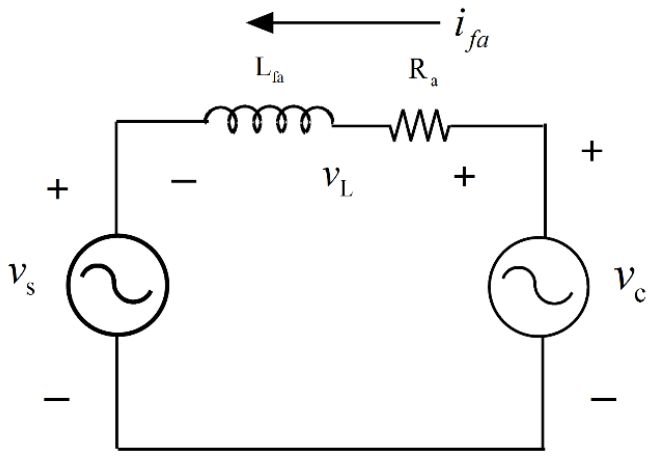


Figure 6.1 Equivalent circuit model of the three-phase interleaved inverter based SAPF

$$v_c = v_s + v_L \tag{6.1}$$

$$v_c = v_s + \mathrm{R_a} * i_{fa} + \mathrm{L}_{af} \frac{di_{fa}}{dt} \tag{6.2}$$

To simplify, the detailed analysis of the supply and inverter voltages are defined as follows:

$$v_s = \sqrt{2}\, \mathrm{V_{sn}} \cos(\omega t + \phi_1) \tag{6.3}$$

$$v_c = \mathrm{V_{c1}} \cos(\omega t + \varphi_1) + \sum_{n=2}^{\infty} \mathrm{V_{cn}} \cos(n\omega t + \varphi_n) \tag{6.4}$$

Where, $\mathrm{V_{sn}}$ is the peak value of supply voltage, $\mathrm{V_{c1}}$ and $\mathrm{V_{cn}}$ are the effective fundamental and n^{th} components of the inverter voltages, respectively. ω is the fundamental

angular frequency, ϕ and φ signify the initial phase components of supply and inverter voltages, respectively. Assume that the non-linear load current (i_{Load}) consists of fundamental and harmonic components.

$$i_{Load} = i_{Load1} + i_{Load,h} \tag{6.5}$$

$$= I_{Load1}\cos(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_{Load,n}\cos(n\omega t + \phi_{n1}) \tag{6.6}$$

Where, I_{Load1} and $I_{Load,n}$ are the fundamental and nth harmonic component of load current, respectively. Assume that the interleaved inverter based SAPF compensating current is composed of a fundamental i_{f1} and harmonic component i_{fh} of currents, respectively.

$$i_f = i_{f1} + i_{fh} \tag{6.7}$$

$$= i_{f1}\cos(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_{f,n}\cos(n\omega t + \phi_n) \tag{6.8}$$

The fundamental component of interleaved inverter output current is very small ($i_{f1}\approx 0$) to maintain the DC-link voltage and system power loss under the steady-state operation of the SAPF. Therefore, the fundamental interleaved inverter current can be neglected under the steady-state operation. If the interleaved SAPF generates compensated currents whose magnitudes are equal to load harmonic currents, the total harmonics injected into the source vanishes. Therefore, the phase 'A' compensating current can be written as follows:

$$i_{fa} = i_{fa,h} = i_{Load,h} = \sum_{n=2}^{\infty} I_{\mathrm{Load},n}\cos(n\omega t + \phi_n) \tag{6.9}$$

The voltage equation can be written by substituting Eqs. (6.3), (6.4) and (6.9) in the Eq. (6.1).

$$\left.\begin{aligned} &\mathrm{V}_{c1}\cos(\omega t + \varphi_1) + \sum_{n=2}^{\infty}\mathrm{V}_{cn}\cos(n\omega t + \varphi_n) = \\ &= \sqrt{2}\,\mathrm{V}_{sn}\cos(\omega t + \phi_1) + \mathrm{R}_a * \sum_{n=2}^{\infty} I_{Load,n}\cos(n\omega t + \phi_n) + L_a \frac{\sum_{n=2}^{\infty} d\left\{I_{Load,n}\cos(n\omega t + \phi_n)\right\}}{dt} \end{aligned}\right\} \tag{6.10}$$

The supply voltage, interleaved inverter based SAPF output voltage and compensating current can be expressed according to Euler's formula as follows:

$$\left.\begin{aligned}
\sqrt{2}\,\mathrm{V}_{sn}\cos(\omega t+\phi_1) &= \sqrt{2}\,\mathrm{V}_{sn}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\phi_1)}\right\}\\
\mathrm{V}_{c1}\cos(\omega t+\varphi_1) &= \mathrm{V}_{c1}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\varphi_1)}\right\}\\
\sum_{n=2}^{\infty}\mathrm{V}_{cn}\cos(\mathrm{n}\omega t+\varphi_n) &= \sum_{n=2}^{\infty}\mathrm{V}_{cn}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\varphi_1)}\right\}\\
\sum_{n=2}^{\infty}I_{Load,n}\cos(\mathrm{n}\omega t+\phi_n) &= \sum_{n=2}^{\infty}I_{Load,n}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\phi_1)}\right\}
\end{aligned}\right\} \tag{6.11}$$

Substituting the Eq. (6.11) into the Eq. (6.10), the voltage equations will become as follows:

$$\left.\begin{aligned}
&\mathrm{V}_{c1}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\varphi_1)}\right\}+\sum_{n=2}^{\infty}\mathrm{V}_{cn}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\varphi_1)}\right\}\\
&=\sqrt{2}\,\mathrm{V}_{sn}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\phi_1)}\right\}+R*\sum_{n=2}^{\infty}I_{Load,n}\,\mathrm{Re}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\phi_1)}\right\}\\
&+L*\sum_{n=2}^{\infty}I_{Load,n}\,\mathrm{Re}\left\{\mathrm{jn}\,\omega\,\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\phi_1)}\right\}
\end{aligned}\right\} \tag{6.12}$$

It is clear that the corresponding real parts on both sides of the equation are same sinusoidal frequency vector. Hence, real parts symbol on both sides can be removed.

$$\left.\begin{aligned}
&\mathrm{V}_{c1}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\varphi_1)}\right\}+\sum_{n=2}^{\infty}\mathrm{V}_{cn}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\varphi_1)}\right\}\\
&=\sqrt{2}\,\mathrm{V}_{sn}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\phi_1)}\right\}+R*\sum_{n=2}^{\infty}I_{Load,n}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\phi_1)}\right\}+L_{af}*\sum_{n=2}^{\infty}I_{Load,n}\left\{\mathrm{jn}\,\omega\,\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\phi_1)}\right\}
\end{aligned}\right\} \tag{6.13}$$

The real parts and imaginary parts on both sides are equal in Eq. (6.13). Thus, the following equation can be obtained:

$$\begin{aligned}
&\mathrm{V}_{c1}=\sqrt{2}\,\mathrm{V}_{sn}\\
&\sum_{n=2}^{\infty}\mathrm{V}_{cn}=\mathrm{R}*\sum_{n=2}^{\infty}I_{Load,n}+\omega L_{af}*\sum_{n=2}^{\infty}nI_{Load,n}
\end{aligned} \tag{6.14}$$

The mold length of the interleaved inverter output voltage vector can be defined as follows:

$$\mathrm{V}_{c}=\left\|\mathrm{V}_{c1}\left\{\mathrm{e}^{\mathrm{j}(\omega t+\varphi_1)}\right\}+\sum_{n=2}^{\infty}\mathrm{V}_{cn}\left\{\mathrm{e}^{\mathrm{j}(\mathrm{n}\omega t+\varphi_1)}\right\}\right\| \tag{6.15}$$

The efficient compensation is achieved by interleaved inverter based SAPF if the sufficient DC-link voltage is supplied. The maximum and minimum mold length of the interleaved inverter output voltage can be expressed from Eq. (6.14) and (6.15) in vector form as follows:

$$\left.\begin{aligned} V_{c\_max} &= V_{c1} + \sum_{n=2}^{\infty} V_{cn} \\ &= \sqrt{2}\, V_{sn} + R * \sum_{n=2}^{\infty} I_{Load,n} + \omega L_{af} * \sum_{n=2}^{\infty} n I_{Load,n} \end{aligned}\right\} \tag{6.16}$$

$$\left.\begin{aligned} V_{c\_min} &= \frac{2}{m} V_{c\_max} \\ &= \frac{2}{m}\left\{\sqrt{2}\, V_{sn} + R * \sum_{n=2}^{\infty} I_{Load,n} + \omega L_{af} * \sum_{n=2}^{\infty} n * I_{Load,n}\right\} \end{aligned}\right\} \tag{6.17}$$

Where, m is the modulation index of the interleaved inverter. The interleaved inverter based SAPF produces maximum output voltage that higher than the maximal value of interleaved inverter voltage mold vector. Therefore, harmonics produced by the non-linear loads are compensated completely. The minimum DC-link voltage is derived by substituting Eqs. (6.16) into (6.17) as follows:

$$\left.\begin{aligned} V_{dc\_min} &= \frac{2}{m} V_{c\_max} \\ &= \frac{2}{m}\left\{\sqrt{2}\, V_{sn} + R_a * \sum_{n=2}^{\infty} I_{Load,n} + \omega L_{af} * \sum_{n=2}^{\infty} n * I_{Load,n}\right\} \end{aligned}\right\} \tag{6.18}$$

The important factors can be concluded from the Eq. (6.18) that the minimum DC-link voltage influenced by the supply voltages, interfacing inductors, effective resistance of inductor values, non-linear load currents and modulation index values. Therefore, the stabilising the DC-link voltage is the key factor in the compensation process. The three-phase harmonic currents are independently compensated with three-phase three-wire interleaved inverter based SAPF. The equivalent DC-link voltage objective function can be written by considering required minimum DC-link voltage for each of three-phases as follows:

$$V_{dc} = \max\left\{V_{dc,a\_min}, V_{dc,b\_min}, V_{dc,c\_min}\right\} \tag{6.19}$$

6.2.2 Enhanced Particle Swarm Optimization

In conventional PSO, the particle has the capability to know the best position obtained by all the group particles. The particle has to find the global best instead of finding local best positions obtained by the all group particles. By making some modifications in the conventional PSO by using simulated annealing algorithm, the EPSO algorithm is formulated. The EPSO eliminates premature convergence and reduces the computational complexity. This divided into two parts, firstly, it chooses maximum fitness particles while iterating and initializing the position arbitrarily. Therefore, the particle can choose more search domains. Secondly, the idea of simulating annealing has been used to achieve the convergence PSO. It improves the convergence speed of the particle to obtain the best solution. The EPSO equations for the i^{th} particle's position after $(k+1)^{th}$ iterations can be written as follows:

$$x_{k+1}^{i} = x_{k}^{i}(1-\lambda_2) + \lambda_2 q_{gbest} + \eta\beta \tag{6.20}$$

Where, λ_2 Learning factor;

β =Acceleration coefficient, which accelerate the particle towards its best position;

x =position of particle;

η is the random number which decreases after successive iterations and can be defined as follows:

$$\eta = \eta_0 e^{-\alpha t} \qquad (0<\alpha<1),\ (0.5<\eta_0<1) \tag{6.21}$$

Where, η depends on scale of each variable. Value of α =0.5 and η_0 =0.8 are taken for the present study

The flow chart of EPSO is shown in Figure 6.2 and process is as follows:

Step 1: Initialize the position and velocities of each particle

Step 2: Find the fitness of each particle

Step 3: Find the best position obtained by each particle

Update the particles with the best position obtained, re-initialise the position of each particle and analyse the lowest value obtained whether its new position is suitable, if it is yes, update its position otherwise assign other position randomly.

Step 4: Compare each particle global best fitness value with the q_{gbest}, if the present value is greater, update its fitness value.

Step 6: Check whether Eq. (6.20) and (6.21) are satisfied, quit the iteration otherwise, return to step 3.

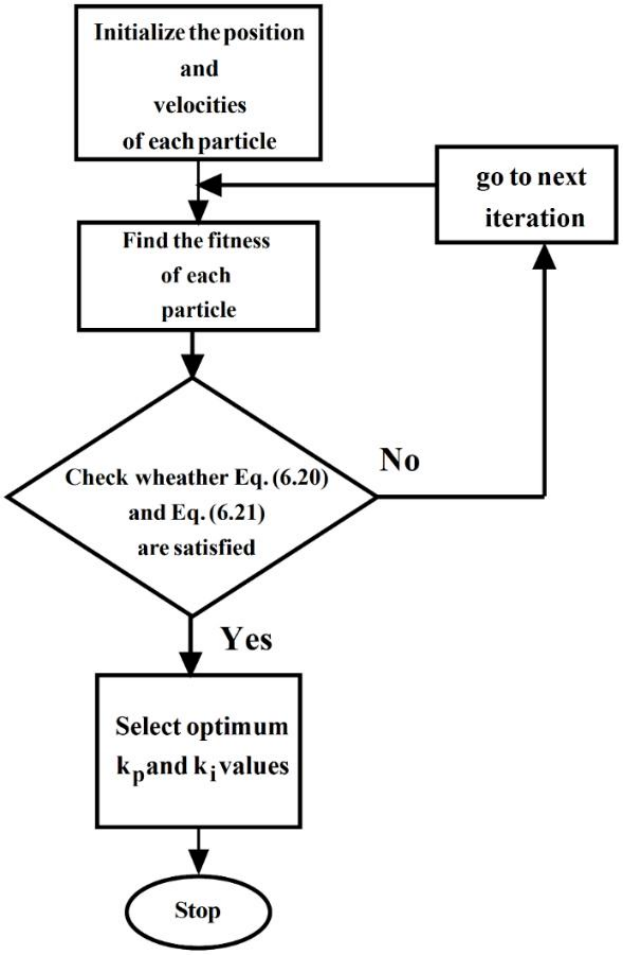


Figure 6.2 Flow chart of EPSO

6.3 Reference Current Generation Technique

The reference current generation technique deals with two important aspects. One is regulating the DC-link voltage in a closed loop to maintain at its reference value irrespective of load changes. Secondly deals with the reference current generations, which further used for controlling the flow of compensating current in harmonic mitigation. The PI controller gain values are tuned by EPSO and further reference current generation is achieved by MICC technique. The MICC technique is explained in the Section 4.4. The

switching pulse generation is achieved by hysteresis current controller which is explained in Section 3.4.

6.4 Comparative Simulation Study of PI, PSO and EPSO

The three-phase interleaved inverter based SAPF is modelled using MATLAB®/ Simulink environment. The simulation performance is conducted under the steady-state and transient conditions of load. The non-linear load is a full wave diode bridge rectifier with R-L load. Practically, the loads in the electrical power system are varying nature therefore, the requirement of compensation varies. The amount of generating compensating current highly influenced by the DC-link voltage stabilisation. The non-linear load and interleaved inverter based SAPF parameters are tabulated in Appendix-B4. The performance of interleaved inverter topology is tested under the steady state and the transient conditions of the non-linear load in comparison with PI, PSO and EPSO based control algorithms.

6.4.1 Steady-State Performance of Interleaved SAPF

The performance parameters of the three-phase interleaved SAPF V_s, I_s, $I_{Load,a,}$ and I_{ca} under the steady-state are shown in Figure 6.3. When the interleaved SAPF is switched on at t= 0.1 sec. in Figure 6.3, the interleaved inverter is started working as a shunt active power without shoot-through problem.

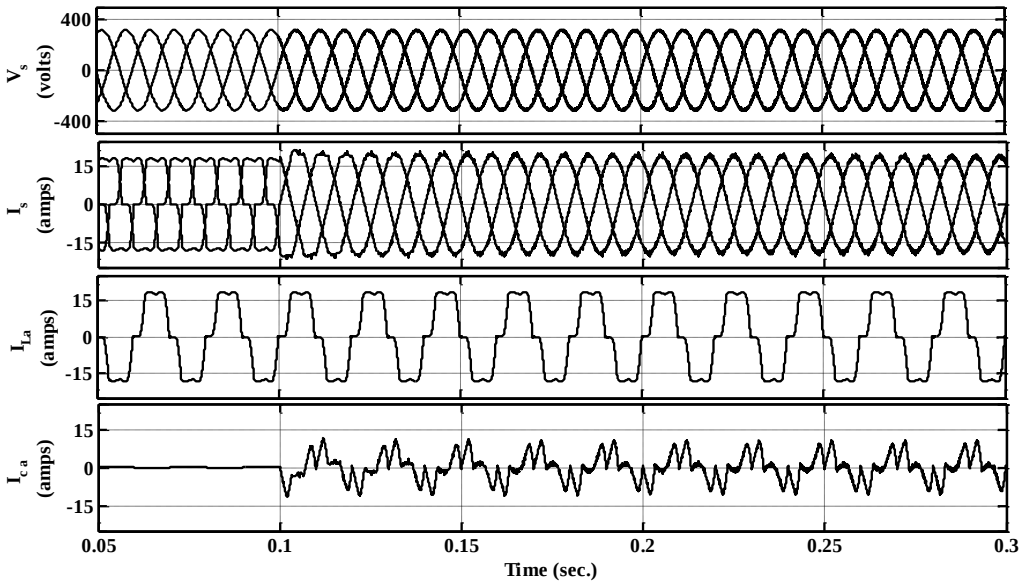


Figure 6.3 Performance parameters of three-phase interleaved SAPF under the steady-state condition of the load

The harmonic spectrum of source current before compensation is 24.68% as shown in Figure 6.4 (a). The performance of EPSO based p-q control algorithm is tested in comparison with the conventional PI and PSO based control algorithms in terms of harmonic compensation and % accuracy of DC-link voltage. The DC-link voltage stabilisation has been reflected on the amount of harmonic compensation. The %THD level using EPSO, conventional PI and conventional PSO based control algorithms are shown in Figure 6.4 (b), (c) and (d), respectively. The EPSO based p-q control algorithm adequately gives best-optimised solution for time-varying harmonics

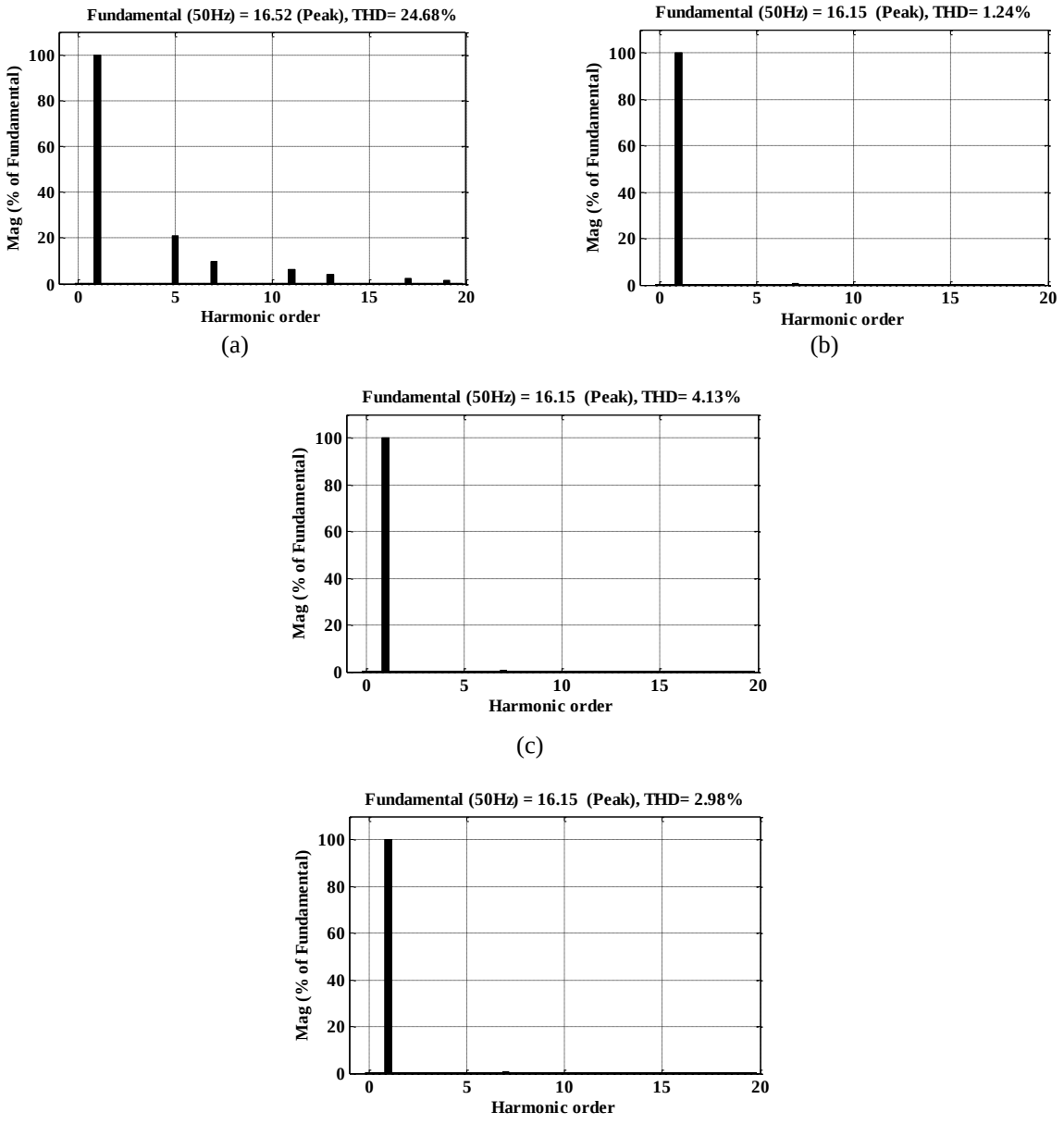


Figure 6.4 Harmonic spectrum of source current (a) Before compensation, (b) After compensation using EPSO, (c) PI controller, and (d) PSO

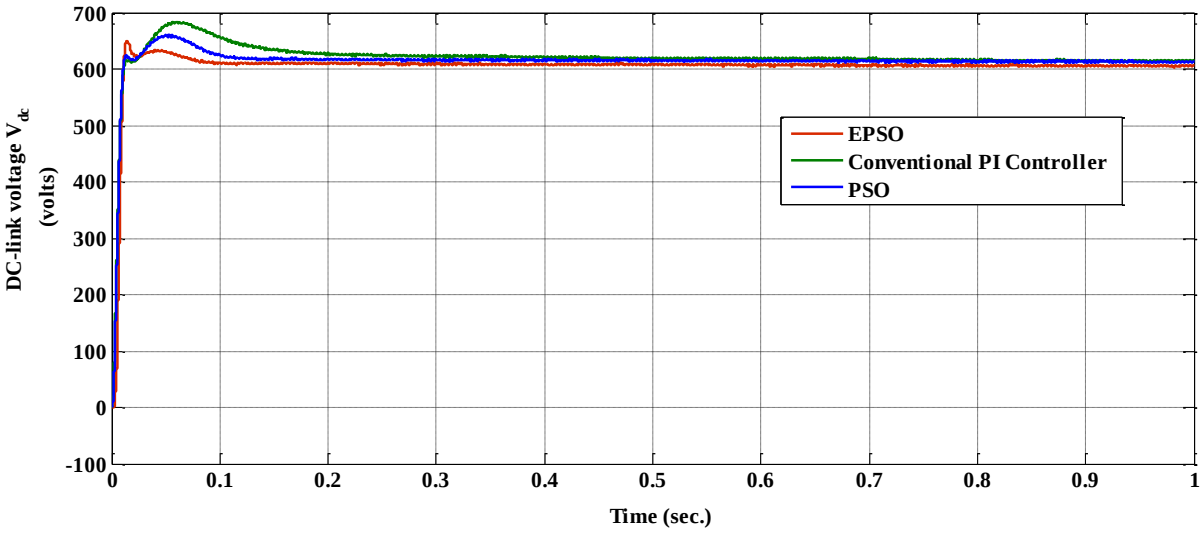


Figure 6.5 DC-link voltage stabilization

. Moreover, if any change in the harmonic currents and supply voltage, the DC-link voltage will be settled fast as compared to the conventional PI and PSO based control algorithms. The convergence characteristics of the PI, PSO and EPSO based gain tunings are shown in Figure 6.5. The DC-link voltage has overshoot of 75 V, 50 V and 10 V, respectively with conventional PI tuning, PSO-PI tuning and EPSO-PI tunings. The DC-link voltage has settled at 0.8 sec. by using conventional PI, 0.3 sec. by using PSO and 0.05 sec. by using EPSO. Hence, the EPSO is achieved less overshoot and settling time. It is contemplated that the EPSO convergences faster due to the elimination of finding local maxima, where the PSO searches for local maxima. The %DC link voltage accuracy achieved by PI, conventional PSO and EPSO are 95.42%, 98.71% and 99.97%, respectively. A complete performance comparison table of EPSO, conventional PI and PSO based control algorithms are tabulated in Table 6.1. It has been concluded that the EPSO based control algorithm performed outstandingly by achieving the good harmonic compensation and % accuracy of DC-link voltage in comparison with the PI and PSO based algorithms.

6.4.2 Simulation Results with Distorted Supply Voltage Case

Practically, the supply voltage wave shape is not a pure sinusoidal, but distorted, due to rapid use of non-linear loads. The supply voltage profile affects the compensation effectiveness of the control algorithm. To prove the pre-eminence of the EPSO based control scheme under the distorted supply voltage condition, the supply voltage has been introduced with 20% of 5^{th} and 14% of 7^{th} harmonic contents as shown in Eq. 6.22. The

distorted supply voltages contain 5th and 7th harmonics including fundamental components as shown in Figure 6.7 (a). The fundamental component of voltage signal is extracted by the PTF with minimum phase delay which is further processed for the reference current generation using EPSO based generalized p-q theory. The performance constraints of this modified control algorithm are shown in Figure 6.6. It is contemplated from these results that this control algorithm is significant and efficient under the distorted supply voltage conditions by making the distorted source currents to sinusoidal. The source current becomes sinusoidal which reduces the THD of source current from 25.31% to 2.63%.

$$\left.\begin{aligned} v_{sa} &= 325*\sin(\omega t) + 65*\sin(5\omega t) + 46*\sin(7\omega t) \\ v_{sb} &= 325*\sin(\omega t - 120^{\circ}) + 65*\sin(5\omega t - 120^{\circ}) + 46*\sin(7\omega t - 120^{\circ}) \\ v_{sc} &= 325*\sin(\omega t + 120^{\circ}) + 65*\sin(5\omega t + 120^{\circ}) + 46*\sin(7\omega t + 120^{\circ}) \end{aligned}\right\} \quad (6.22)$$

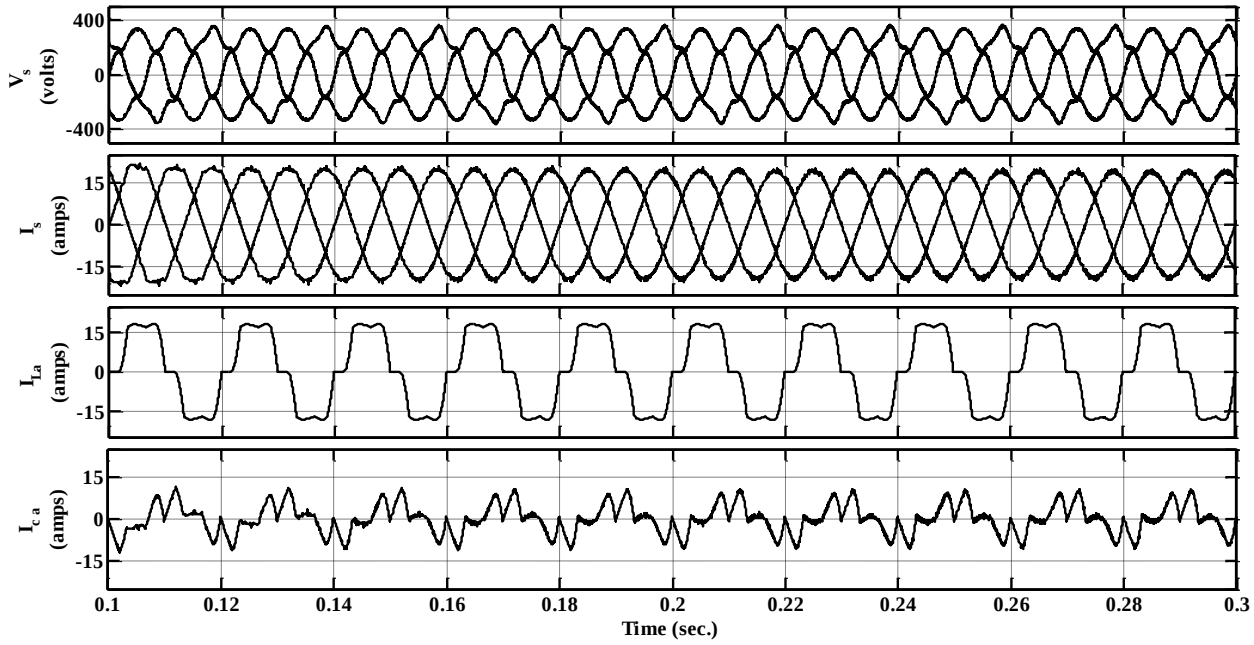
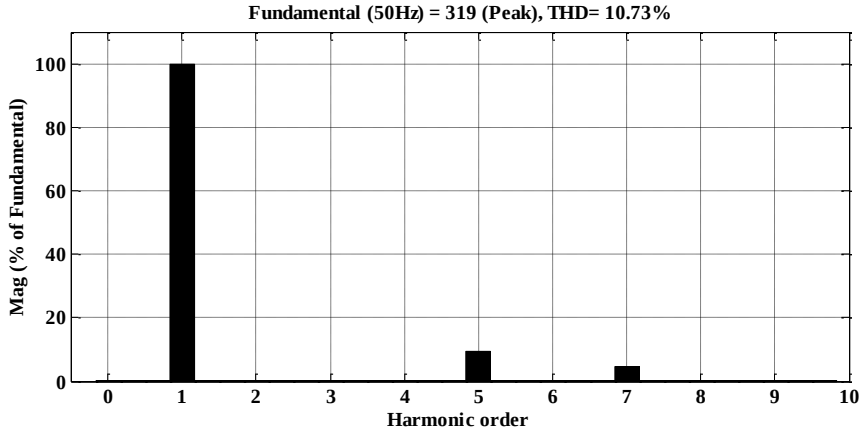
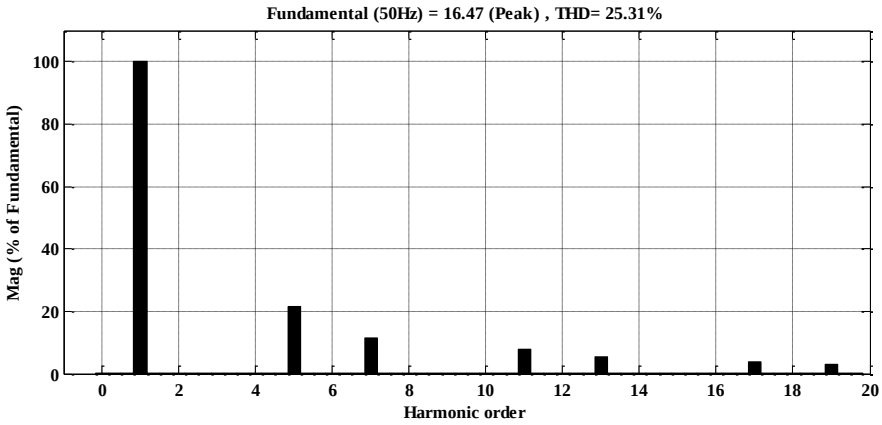


Figure 6.6 Performance parameters of distorted supply voltage (V_s), source current (I_s), phase 'A' load current (I_{La}), and phase 'A' compensation current (I_{ca})

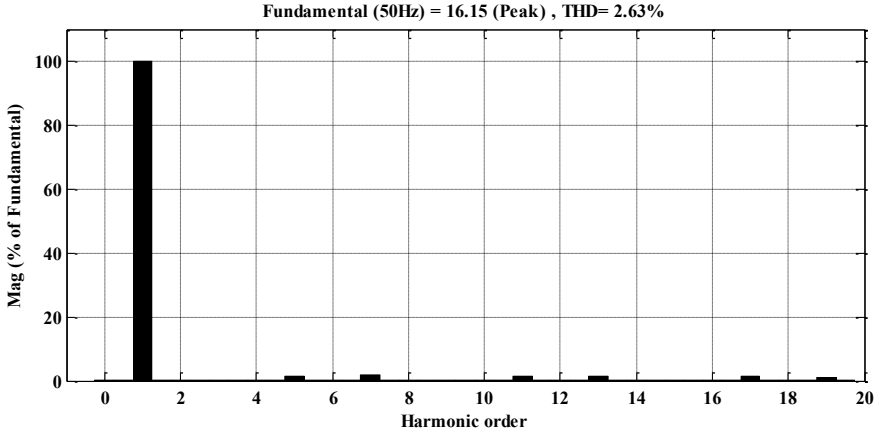
The harmonic spectrum of phase 'A' source by using EPSO based modified control algorithm before and after compensation are shown in Figure 6.7 (b) and (c), respectively. It is observed from these results that the source current became sinusoidal and well within the IEEE-519 standards.



(a)



(b)

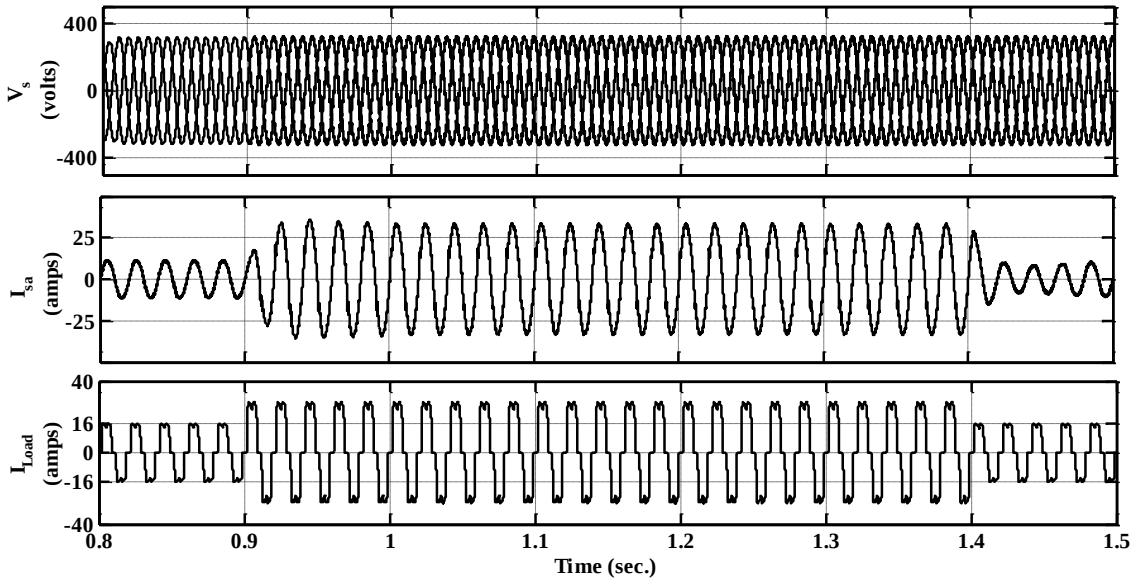


(c)

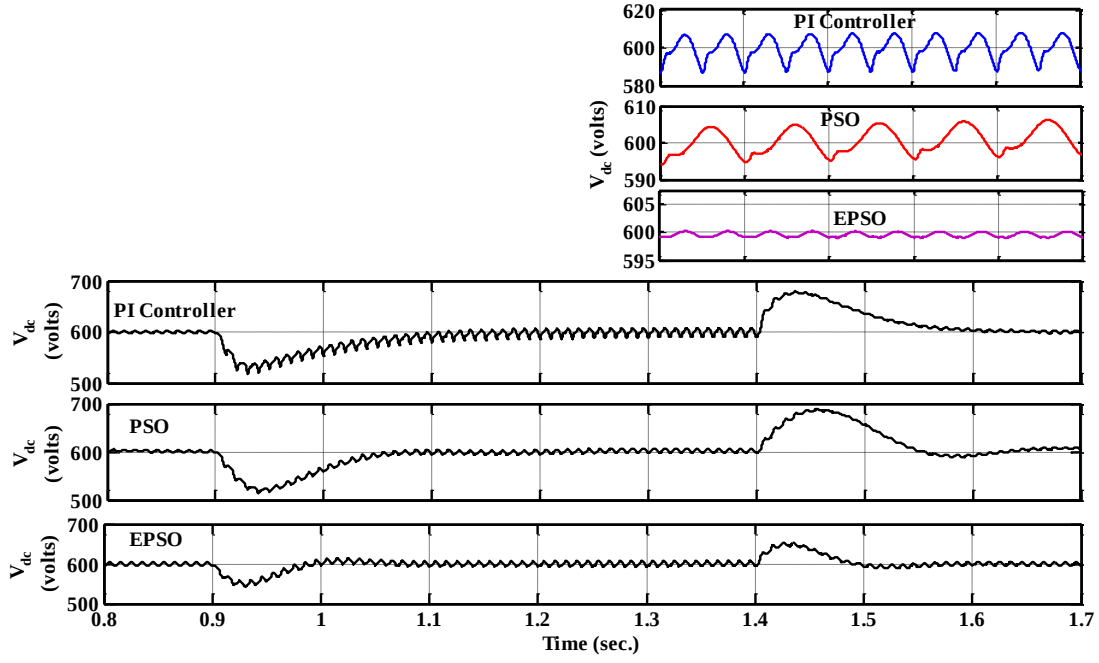
Figure 6.7 Harmonic spectrum (a) Distorted phase 'A' supply voltage (b) Phase 'A' source current before compensation, and (c) Phase 'A' source current after compensation

6.4.3 Transient Performance of Interleaved SAPF

The supremacy of the EPSO based modified control algorithm compared to conventional techniques under the transient condition of nonlinear load in Figure 6.8 (a). The performance has been investigated in terms of overshoot, undershoot, response time, settling time and ripple voltage.



(a)



(b)

Figure 6.8 (a) Performance of interleaved SAPF under transient condition of load, and (b) DC-link voltage stabilization using PI, PSO-PI, and EPSO-PI control algorithms

The performance of interleaved inverter based SAPF under sudden increase 50% of load at t=0.9 sec. and load removal at t=1.4 sec. is shown in Figure 6.8 (a). In Figure 6.8 (b), it shows the DC-link voltage stabilisation of EPSO, conventional PI and PSO based control algorithms. When the load increases, the capacitor voltage goes down to its reference value and vice versa. The conventional PI controller based algorithm performs overshoot of 10 V, undershoot of 10 V and response time of 2.27 sec. with 20V ripples in DC-link voltage. Similarly, the PSO based control algorithm performs overshoot of 5 V, undershoot of 5 V and response time of 1.32 sec. with 10 V ripples in DC-link voltage whereas, the EPSO based control algorithm performs outstandingly with the lowest overshoot of 2V, under shoot of 3V and fastest response time of 0.02 sec. with 4 V ripples in DC-link voltage. Since, the search process terminates once the predefined maximum number of iterations completed or additional best solution is not obtained in conventional PSO. Moreover, the number of iterations and increase number of premature convergence of particle's best position will increase the complexity of the program and degrade the convergence speed. In contrary, the EPSO eliminates the premature convergence and reduce the computational complexity by avoiding each particle's best position obtained during the search process. It is proven that EPSO based modified *p-q* control algorithm performs outstandingly under transient condition of the load with lower source current %THD, good accuracy, less overshoot, less undershoot and fast response time as tabulated in Table 6.1.

Table 6.1

Simulation comparison of algorithms on DC-voltage Regulation

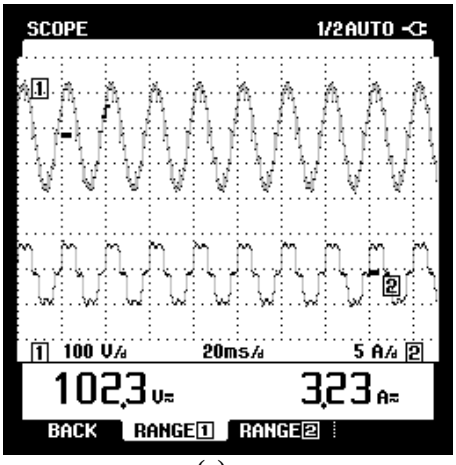
Control algorithm for DC-voltage regulation	**The steady-state condition of the load**					**Transient condition of the load**			
	%Accuracy of DC voltage	**%THD**			**Settling Time (sec.)**	**Overshoot (V)**	**Undershoot (V)**	**Response Time (sec.)**	**Ripple Voltage (V)**
		I_a	I_b	I_c					
PI controller	95.42	4.13	3.56	3.82	0.8	10	10	2.27	20
PSO	98.71	2.98	2.45	3.21	0.3	5	5	1.32	10
EPSO	99.97	1.24	1.25	1.29	0.05	2	3	0.02	4

6.5 Experimental Verification

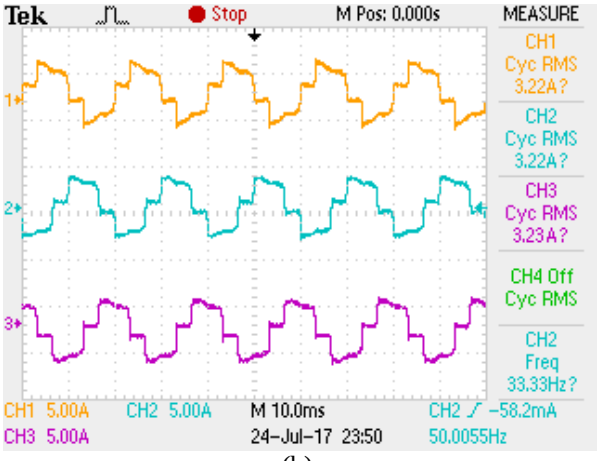
The substantial simulation results of conventional PI, PSO and EPSO are verified by experimental results. The laboratory prototype model of three-phase interleaved SAPF is shown in Appendix-A12.

6.5.1 Steady-State Performance of Interleaved SAPF

The performance of interleaved inverter based SAPF is tested under the steady-state condition of the non-linear load with EPSO based modified control algorithm in comparison with conventional PI and conventional PSO based *p-q* control algorithms. The phase 'A' supply voltage and distorted source current before compensation are shown in Figure 6.9 (a). The three-phase distorted source currents are shown in Figure 6.9 (b) and their respective phase harmonic spectrums are shown in Figure 6.10 (a)-(c), respectively. The performance parameters of three-phase source currents ($i_{sa,}$ $i_{sb,}$ i_{sc}) after compensation using EPSO based *p-q* control algorithm is shown in Figure 6.11 (a) and their respective compensation currents are shown in Figure 6.11 (b). It is contemplated that the interleaved inverter is working as a shunt active power filter. The comparative analysis of PI, conventional PSO and EPSO based control algorithms are tested to show the compensation effectiveness of the EPSO based modified control technique. The harmonic spectrum of source current after compensation using EPSO, PI and conventional PSO are shown in Figure 6.12 (a), (b) and (c), respectively.

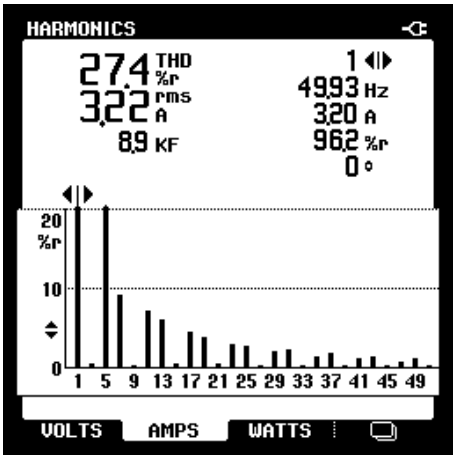


(a)

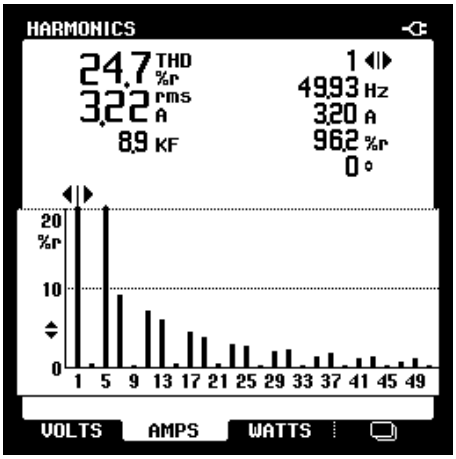


(b)

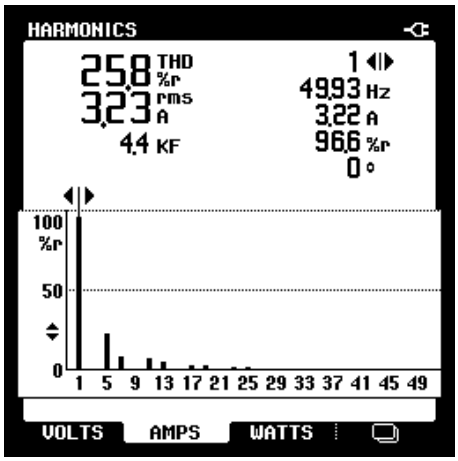
Figure 6.9 (a) Phase 'A' Supply voltage and phase 'A' current, and (b) Three-phase source currents before compensation



(a)

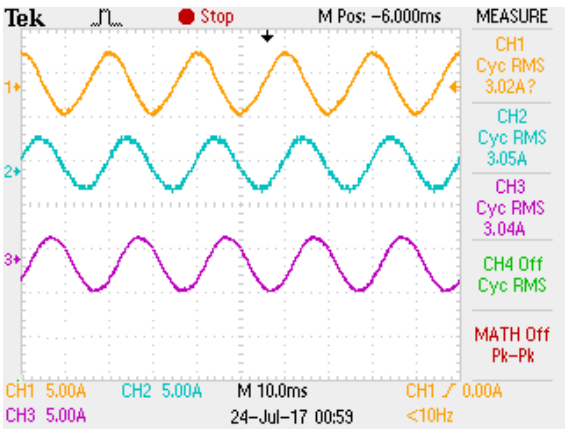


(b)

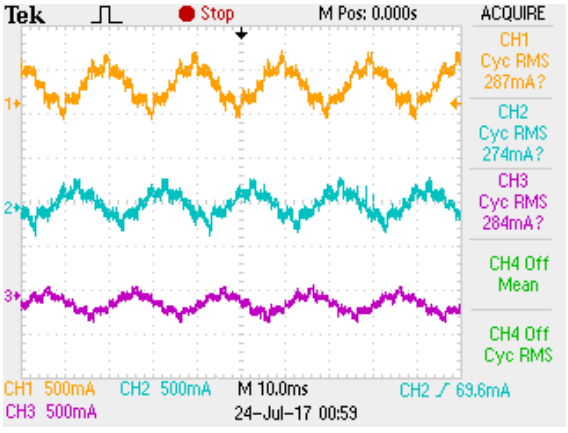


(c)

Figure 6.10 Harmonic spectrum of source currents before compensation (a) Phase 'A', (b) Phase 'B', and (c) Phase 'C'

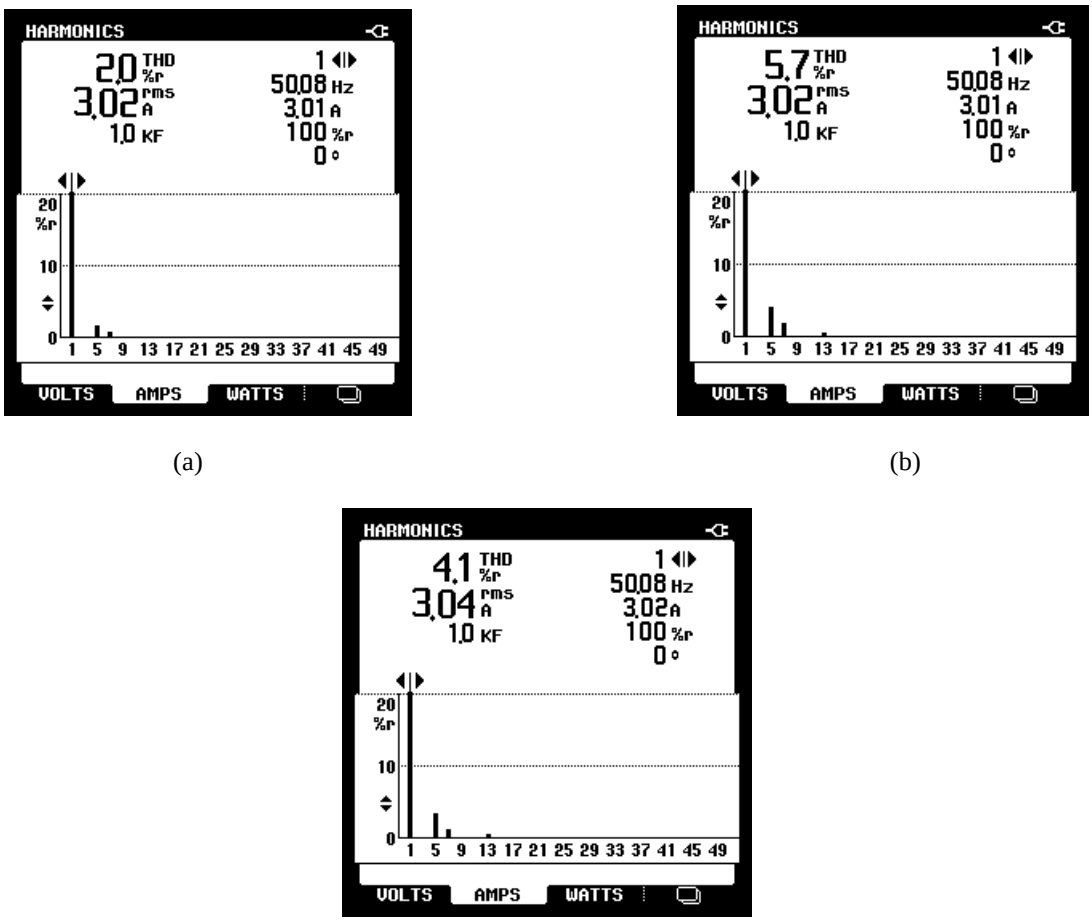


(a)



(b)

Figure 6.11 Performance parameters interleaved SAPF after compensation (a) i_{sa} , i_{sb} , i_{sc}, and (b) i_{ca} , i_{cb}, i_{cc}



(a) (b)

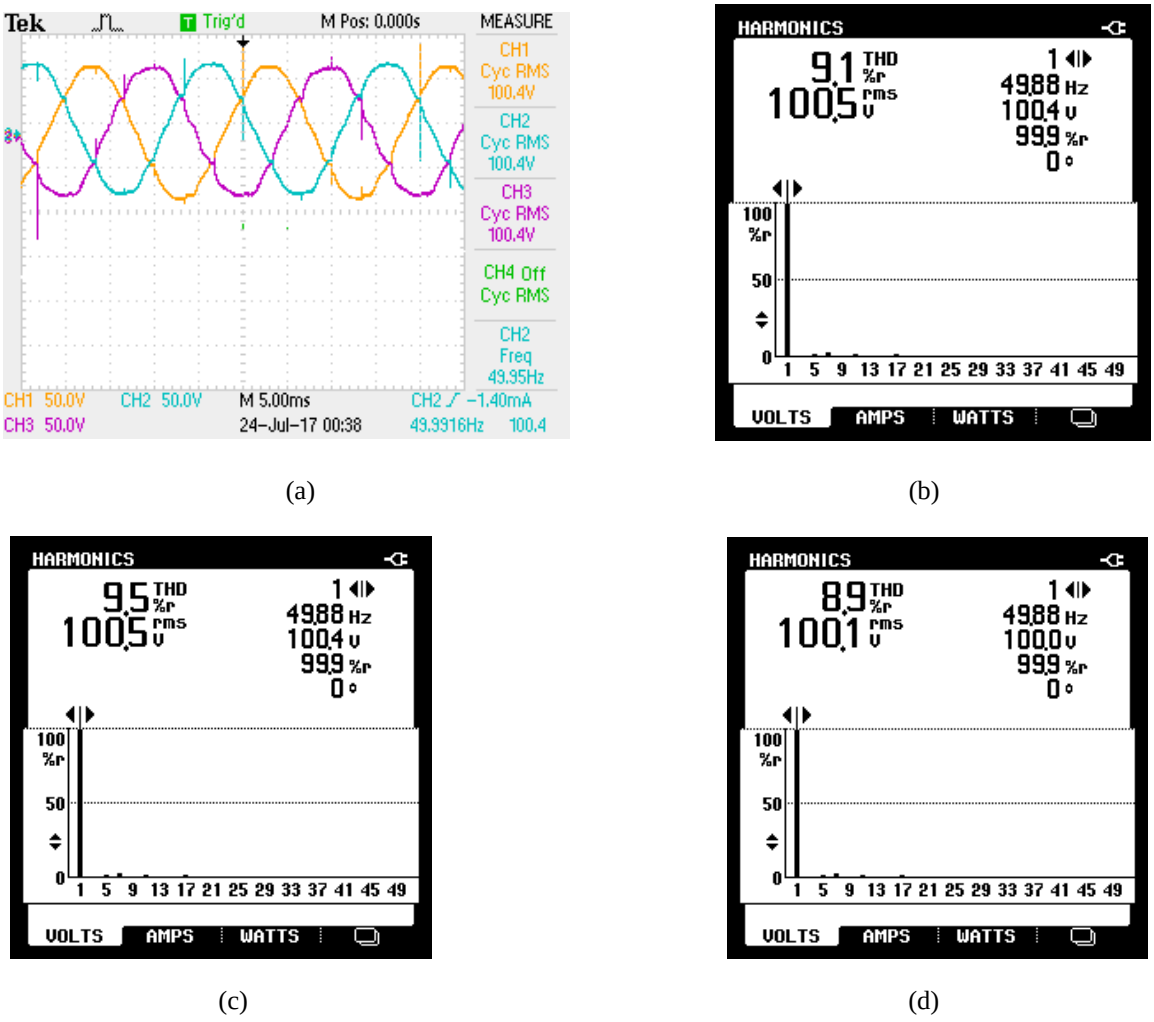
(c)

Figure 6.12 Harmonic spectral analysis of phase 'A' source current after compensation using (a) EPSO, (b) PI, and (c) Conventional PSO

It observed from Figure 6.12 (a) that the EPSO based control algorithm eliminates the premature convergence and reduces the computational complexity by avoiding each particle's best position obtained during the search process. It optimises the gain parameter values for variable harmonics presented in the system to tracks the DC-link reference voltage value. Therefore, the harmonic compensation level and %accuracy of DC-link voltage are improved. Whereas the PI controller fails to stabilize the DC-link voltage at its reference value due to variable harmonics presented in the system. Hence, affect the harmonic compensation level as shown in Figure 6.12 (b). It observed from Figure 6.12 (c) the PSO based tuning requires more of iterations to track the optimum values of gain values which affect the dSPACE controller speed. Hence, gives atrocious results due to failing to track its desire reference DC-link voltage value. A complete performance comparison table of conventional PI, PSO, and EPSO based control algorithms are shown in Table 6.2.

6.5.2 Experimental Verification under Distorted Supply Voltage

In this case, the distorted supply voltage and nonlinear loads are used to validate the performance of the EPSO based modified control technique. Continue proliferation of nonlinear loads in the power system network, inject the harmonic currents into the system also distort the supply voltage. The effectiveness of the presented EPSO based modified control algorithm is tested under distorted supply voltages. The distorted three-phase supply voltages are shown in Figure 6.13 (a).



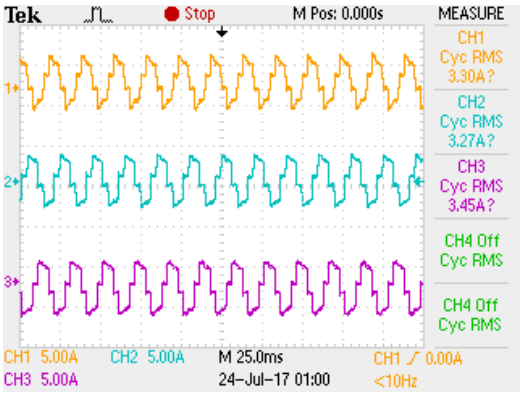
(a) (b)

(c) (d)

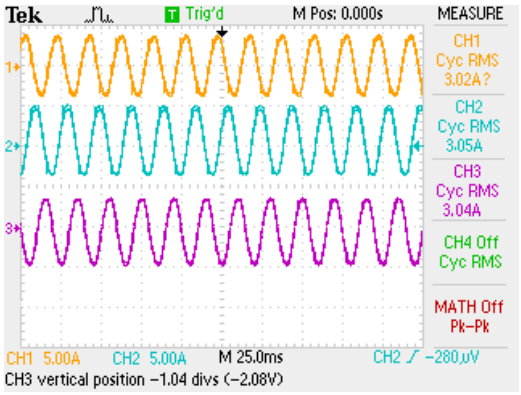
Figure 6.13 (a) Three-phase distorted supply voltages, and (b)-(d) Their respective harmonic spectral diagram

The THD of their respective phase voltages recorded as 9.1%, 9.5% and 8.9% are shown in shown in Figures 6.13 (b)-(d), respectively. The distortions in the supply voltages affects the wave shape of the reference currents which eventually degrade the compensation

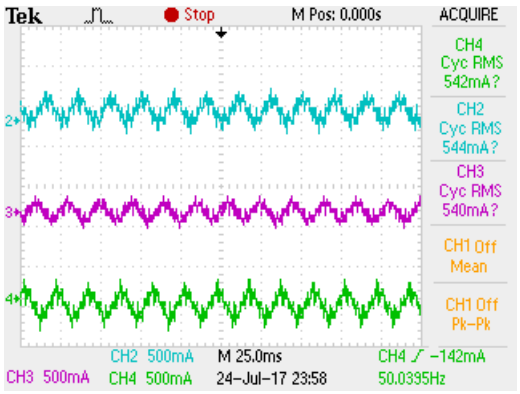
efficiency of the control technique. Hence, the control technique is divided into two parts, one is to extracts the fundamental frequency component from the distorted supply voltage using PTF as explained in Section 4.4. Secondly, the reference current generation using EPSO based generalized *p-q* control technique. The PTF extracts the fundamental component of voltage signal from the distorted supply which further processed for the reference current generation. The performance parameters of three-phase source currents before and after compensation with their respective phase compensating currents using modified control technique are shown in Figure 6.14 (a), (b) and (c), respectively. It is concluded from Figure 6.14 (b) that the source currents became sinusoidal and recorded THD of phase 'A' source current as 3.4%. It is concluded that the EPSO based modified control technique is effective in compensation even under distorted supply voltage conditions, robust.



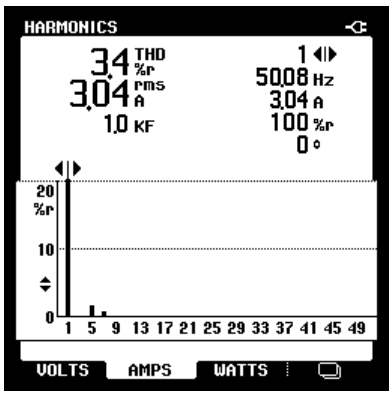
(a)



(b)



(c)

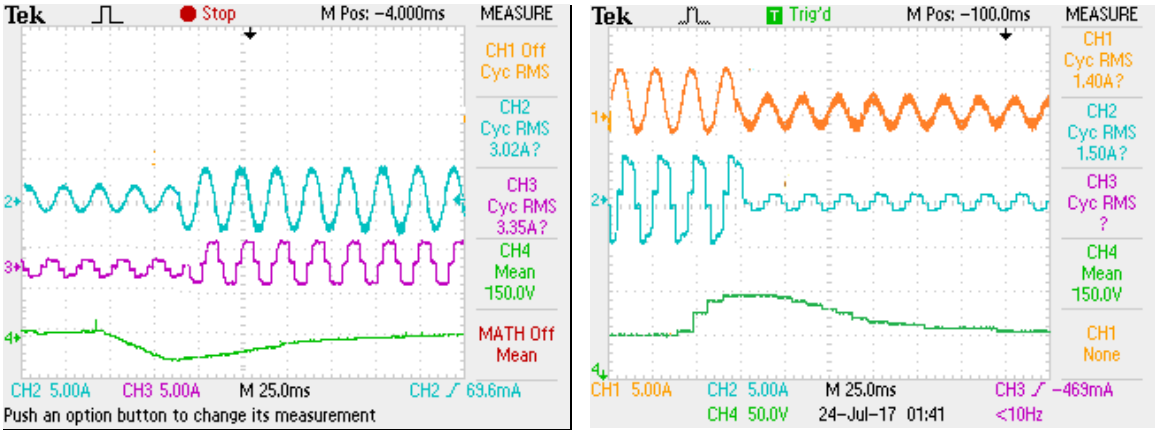


(d)

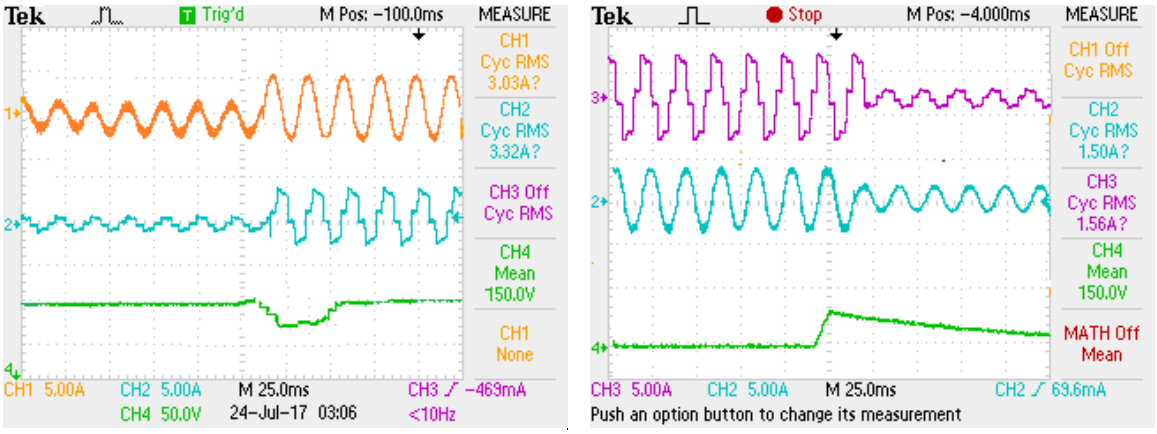
Figure 6.14 Performance of three-phase interleaved SAPF under distorted supply voltage condition (a) Three-phase source currents before compensation, (b) Three-phase source currents after compensation, (c) Three-phase compensating currents, and (d) FFT analysis of phase 'A' source current after compensation

6.5.3 Transient-State Performance of Interleaved SAPF

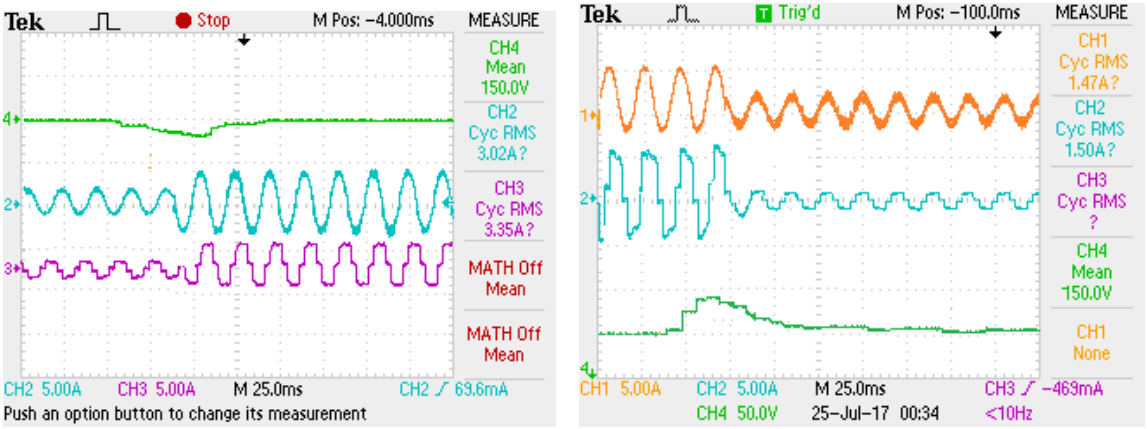
Extensive experimental analysis has been conducted on interleaved SPAF to test the robustness and effectiveness of the EPSO based modified control algorithm during a transient condition of load. The practical electrical power system experiences different hazardous load disturbances due to varying power demand, therefore the DC-link capacitor undergoes inevitable disturbances. In such scenario, the DC-link voltage has to be regulated at its normal reference value to ensure reliable and effective harmonic compensation. The effectiveness of EPSO based modified control algorithm is tested by sudden increment and decrement of the non-linear load. The 56% of decrement and step load increment have been conducted in the laboratory. Hence, the load current increases from 1.5 A to 3.35 A and decreases from 3.35 A to 1.5 A. The response of conventional PI-based control algorithm is shown in Figure 6.15 (a) and (b), respectively. It is contemplated from these results that the when the load increases, the DC-link capacitor voltage undergoes down off its reference value to supply sufficient amount of real power to the load. It is recorded undershoot of 10 V and response time of 2.5 sec. When the load decrement, the DC-link capacitor voltage increases with an overshoot of 12 V and settle down to its reference value with a response time of 3.01 sec. Therefore, the harmonic compensation affected in both dynamic conditions of the load with poor %THD. The step load increased and decreased are performed to test the PSO based control algorithm as shown in Figure 6.15 (c) and (d). When the step load increases, the difference between the reference and real values of DC-link voltages are fed through PSO algorithm to generate the optimised gain values to reduce the overshoot, undershoot and settling time. In this case, the PSO explores to new domains in the searching space to entrap in local optimisation and causes to premature phenomena. Therefore, the PSO gives inevitable results under sudden step load increase which undershoot of 10V and settling time of 1.25 sec. When step load decrease, the overshoot of 8 V and settling time of 1.02 sec. Thus, the harmonic compensation affected in both dynamic condition of the load with poor %THD of both step load increment and decrement. The performance of EPSO based modified control algorithm under both step load increment and decrement are shown in Figure 6.15 (e) and (f), respectively. The EPSO reduces the convergence time by eliminating the search process to find the local best position obtained by all the particles.



(a) (b)



(c) (d)



(e) (f)

Figure 6.15 DC-link voltage stabilization under transient condition of the load by using (a)-(b) Conventional PI controller (CH4-50 V/div), (c)-(d) PSO based PI controller (CH4-50 V/div) and (e)-(f) EPSO based PI controller (CH4-50 V/div)

The DC-link voltage undergo down to its reference value under step load increment, the EPSO able to track the DC-link voltage to settle back to its reference value in 0.02 sec. with less undershoot voltage of 3 V. Similarly, DC-link voltage increases over reference value under step load decrease case. The EPSO gives best results to bring back to its reference value with less overshoot of 3.2 V and settling time 0.01 sec. It is observed from all these results the EPSO based control algorithm performed excellently under both steady-state and dynamic-state load change conditions with high accuracy, very less response time, less overshoot and undershoot. By taking advantage of eliminating the best solution obtained by all particles in the search process which reduces the convergence speed and improve system efficiency. A complete performance comparison table is tabulated in Table 6.2.

Table 6.2

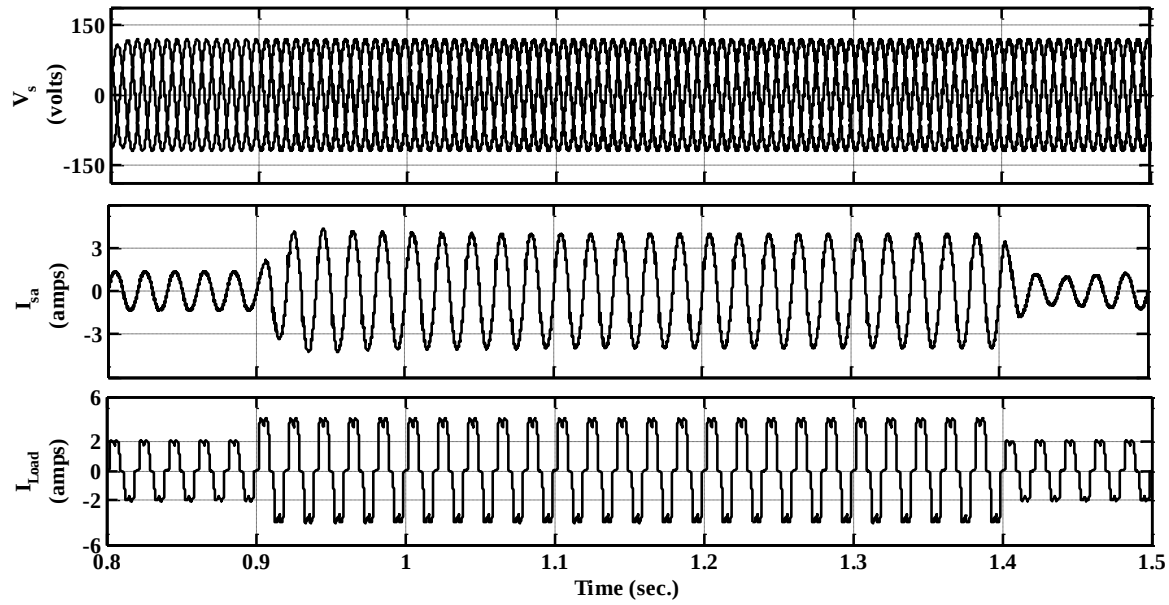
Experimental comparison of algorithms on DC-voltage regulation

Control algorithm for DC-voltage regulation	Steady-state condition of the load			Transient condition of the load							
				Experimental				Simulation			
	%Accuracy of DC voltage	%THD Source current after compensation	Settling Time (s)	Overshoot (V)	Response Time (sec.)	Undershoot (V)	Ripples in DC-link voltage (V)	Overshoot (V)	Response Time (sec.)	Undershoot (V)	Ripples in DC-link voltage (V)
PI	95.42	5.7	2	12	2.5	10	15	9	2.1	10	12
PSO	98.71	4.1	0.7	8	1.25	10	10	7	1.12	6	8
EPSO	99.97	2.0	0.05	3.2	0.02	3	0.4	2.1	0.02	2.2	0.5

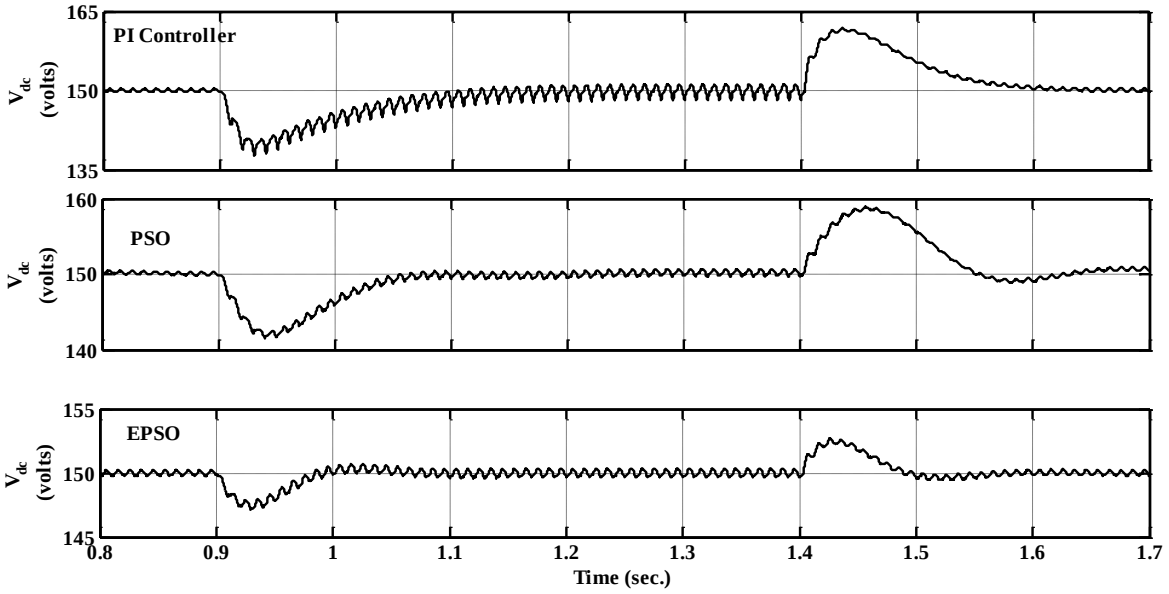
6.5.3.1 Validation of Simulation Results

The simulation model of three-phase interleaved SAPF is carried out again with the parameters used in the experimental and simulation to compare the simulation and laboratory experimental results. The sampling time, source voltage, smoothening inductors values, interfacing inductor values, DC-link voltages and nonlinear load are kept same as experimental. The performance parameters of V_s, I_s and I_{Load} are shown in Figure 6.16 (a) under transient condition of nonlinear load. The transient behaviour of load is observed during 0.9 sec. to 1.4 sec. by sudden increase and removal of second nonlinear load. The

DC-link voltage stabilization is observed for PI, PSO-PI and EPSO-PI-based control techniques as shown in Figure 6.16 (b). It is observed from Figure 6.16 (b) (simulation results) and Figure 6.15 (experimental results) that the DC-link voltage stabilization using PI, PSO-PI and EPSO-PI-based control techniques compliance each other.



(a)



(b)

Figure 6.16 Transient condition of nonlinear load (a) Simulation performance parameters of three-phase supply voltage, phase 'A' source current and phase 'B' load current, and (b) DC-link voltage stabilization using PI, PSO-PI and EPSO-PI control techniques

6.6 Conclusion

Swarm intelligence techniques are applied to solve the multi-objective function of DC-link voltage stabilisation in interleaved SAPF. The PI controller has been used for stabilising the DC-link voltage under the steady-state and transient conditions of the load. But, it gives poor results under sudden changing of loads. The PI controller gain parameters have been tuned to regulate the DC-link voltage using PSO and EPSO approaches. The performance improvement of EPSO is compared with conventional PI tuning and PSO approaches using MATLAB®/ Simulink environment. A prototype model has been developed in the laboratory to validate the simulation results. It can be concluded from both simulation and hardware results that the EPSO converges fast to find the best optimum PI gain parameters under the steady-state and transient condition of the load with less overshoot and undershoot.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

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7.1 Conclusion

Continue proliferation of power electronic converters as embedded devices in the industrial applications, household and commercial equipment, etc. give enormous advantages like flexible control, reduced cost and size, increase the robustness, etc. However, rapid use of these power electronic based converters are lead to produce nonlinearity in the supply system due to switching action of power electronic devices. Subsequently, creates various PQ problems like harmonics, reactive power burden which degrade the power factor of the system. These PQ problems affect the protection system which results mal-operation of protective devices, etc. Also, interrupt many operations and processes in the industries and other establishments, affect different measuring instruments and metering of the various quantities such as voltage, current, power and energy. Moreover, it affects the monitoring systems of critical, emergency, and costly equipment, etc. Hence, the study of the PQ becoming a more important subject for both suppliers and end users. Many International standards such as IEEE, IEC, etc. are recommended, developed and enforced voltage and current distortions limits for different voltage levels so that the PQ of an electrical system can be maintained. It is recommended to install proper compensation devices like CPDs or APFs at proper location. To design and placement of APF in the distribution system at proper location, first need to analyze the harmonic pattern and level of harmonics penetrating into the system. The harmonic survey has been conducted on various critical lab and commercial equipment such as variable frequency drive, rectifier, dip-coater, magnetic stirrer, spin coating unit, ultrasonicator, syringe pump, computer loads, , fluorescent lamps, etc. to understand the existing level of harmonics in the system.

Low-pass filters are used for harmonic filtering because of their less expensive, ease of installation, no maintenance, etc. However, these filters are suffering from resonance

problem, size and poor compensation which are included in chapter 1. Researchers have come with new solutions to overcome the problems of conventional low pass filtering i.e. active power filters. APFs are found to be a viable solution over conventional methods of filters due to its low cost, effective, robust, no resonance problems, etc. Various topological aspects of shunt APFs are proposed and developed in 3P3W and 3P4W including single-phase system. The rapid advancement in microelectronic technology leads to the development of high-speed processors, semiconductor devices with high power handling capability. An improved sensor technology create an interest in the development of shunt APFs with new control techniques which could able to work under adverse condition of supply voltage and load conditions.

In this thesis, shunt APF is designed and implemented to compensate current related problems, like current harmonics, reactive power burden for unity power factor operation, etc. The shunt APF with proper control algorithm compensates major PQ problems under sinusoidal and distorted supply voltage conditions. A PWM voltage source inverter is used as a shunt APF with the DC-link capacitor on DC-side. In shunt APF, control algorithms play a substantial role in harmonic compensation under sinusoidal and distorted supply voltage conditions. Continue proliferation of power electronic based equipment in the present power system network, the supply voltage also gets distorted. A Hilbert transform based adaptive tuned filter is presented to extract the fundamental frequency component of voltage signal from the distorted voltage. This Hilbert transform based ATF is tuned to extract fundamental frequency component from the distorted voltage signal and synchronize with the grid without phase delay. This works effectively over conventional LPF and PLL. A DC-link energy balance theorem is used for the reference current generation. The error will generate by comparing the reference source current with the actual source current, which further processed through hysteresis current controller for switching pulse generation. A unipolar hysteresis current controller is introduced in SAPF applications to eliminate the switching frequency problems over single-band hysteresis current controller. The shunt APF system with these control techniques are developed in MATLAB/ Simulink environment. A single-phase full-wave uncontrolled bridge rectifier with R-L load used as a nonlinear load which injects harmonics and draws reactive power. An additional, rectifier with R-L load connected near to the supply to which distort the supply voltage. The Hilbert

transform based ATF control algorithm is tested under sinusoidal and distorted supply voltage conditions. In addition, a performance comparison study also made between SBHCC and UHCC switching schemes. Various simulation studies have been presented under sinusoidal and distorted supply voltage conditions. The Hilbert transform based ATF with DC-link energy balance theorem has been tuned to extract fundamental frequency component from the distorted supply voltage without phase delay compared to PLL based technique. Also, The UHCC switching scheme reported lower switching frequency and frequency variations compared to SBHCC scheme. A laboratory prototype model is developed to test the Hilbert transform based modified control algorithm with SBHCC and UHCC schemes. ADS 1104 of dSPACE is used for implementation of control algorithms. This DS 1104 having TMS320F240 DSP processor with Control desk feature. It also interfaces with MATLAB software to implement the control algorithms. The LEM voltage sensors (LV 25-P) and current sensors (LA 25-NP) have been used for sensing the voltage and current, respectively. A signal conditioning board has been prepared by using TL081 IC, gate driver circuit by TLP250 ICs and dead-band circuitry by 7404 and 7408 ICs. A diode bridge rectifier with R-L load is used as a nonlinear load. The single-phase VSI is prepared by using IRFP460 MOSFET switches. Rigorous experimental studies have been conducted to validate the simulation results under sinusoidal and distorted supply voltage conditions. The simulated and experimented observations in the form of the source current wave shape and %THD indicated that the Hilbert transform based modified control technique with UHCC scheme mitigate the current harmonics, reactive power burden and switching frequency problems under sinusoidal and distorted voltage conditions with improved power factor.

The most of the researchers used VSI based shunt APF topology for mitigating the current related PQ problems. However, the VSI based shunt APF is severely suffering from hazardous conditions i.e. shoot-through problem which further introduces the ringing problem, the temperature rise in the power switches causes to higher EMI and reduce the efficiency of the circuit. The shoot-through mode occurs when the two power switches of the same leg are inadvertently switched on. Therefore, extremely high current flows through it which damage the power devices. To overcome these shoot-through problems, a three-phase interleaved inverter based topology is introduced to act as a shunt APF in three-phase

distributed system. Also, the present power system is having inevitable sensible non-linear which create large variations in the supply voltage distortions and unbalance. Therefore, the compensation capability and efficiency of the shunt APF degrades. The symmetrical component theory used to calculating positive sequence component from the unbalanced three-phase supply voltages and currents. The extracted positive sequence components still have harmonic components. Therefore, a novel predictive tuned filter is introduced to estimate the variations in the amplitude of supply voltage, frequency and harmonics for extracting the fundamental voltage signal. The extracted fundamental frequency is well balanced and distorted free. This extracted signal is further processed for reference current generation using modified generalized *p-q* theory. Further, modified indirect current control technique is introduced with a tuned low pass filter to separate the ac and dc components of the instantaneous power and the dc component of power is used for reference source current. A controlled and uncontrolled rectifier with R-L loads is used as a non-linear load for testing the effectiveness of the interleaved inverter topology with the PTF based mfied control technique. Various simulation results have been presented to verify the compensation effectiveness under different supply and load conditions. The simulation results are experimentally validated which shows that the interleaved inverter based SAPF with a modified indirect current controller is effective in harmonic and reactive power compensation without shoot-through problem.

DC-link capacitor voltage plays a significant role in the compensation performance of active filters. It supplies the harmonic component of currents, switching losses, reactive power under the steady-state and real power under the transient condition of the load. During a transient condition of the load, there is a large variation between the reference and actual values of DC-link voltages. The DC-link voltage has to be maintained at its reference value for accurate compensation. The PI controllers are well-established controllers to stabilize the DC-link voltage because of its simplicity, reliability and ease of implementation with low-cost controllers. It requires precious mathematical modelling of system for obtaining the gain parameters. Hence, the tuning of PI controller gain values during adverse condition of load and supply voltage is a big challenge for the researchers. Sliding mode controllers are acknowledged as a remarkable controller in the application of APF over PI controllers. The main advantage of the SMC is that, it is insensitive to

parameter uncertainty and external disturbances. Therefore, the SMC is the most suitable for the closed-loop control of the converters. However, the conventional SMC has demerits like poor response under mismatched system uncertainties/ disturbances. Therefore, multitudinal sliding mode controller is developed to overcome the problems of conventional SMC. The MSMC uses multiple surfaces for mismatched system disturbances/ uncertainties. Moreover, it uses inertial delay control to control the mismatched disturbances/uncertainties. The output of MSMC is multiplied with the unit template which is generated by using Hilbert transform based ATF. Various simulation and experimental studies have been conducted to verify the compensation competence of MSMC in comparison to conventional SMC and PI controllers. The test is conducted under the steady-state and transient condition of load with different supply voltage conditions.

The power system network is having different types of linear and non-linear loads which continuously switches on and off. The efficiency of control technique depends on how fast the control technique helps to stabilize the DC-link voltage after load perturbation. PI controllers are well established controllers, used for stabilizing the DC-link voltage under the steady-state and transient condition of load. The PI controller gain values i.e. k_i and k_p are tuned to certain load parameters to operate the shunt APF successfully. However, the loads connected to the power system network change frequently. Hence, tuning of PI controller gain values is a multi-objective function. An Enhanced particle swarm optimization is presented to solve multi-objective function by eliminating the local best opposition and improve the converge speed obtained by the particles in the search space. The performance pre-eminence of EPSO-PI technique is tested in comparison with the conventional PI and PSO-PI based control techniques. Various simulation and experimental studies have been conducted under different load and supply voltage conditions to show the performance improvement of EPSO based modified control technique.

7.2 Future Scope

The innovation in research is the combination of already work done and hypothesis for new innovative thought which provides a path to future research work. The research is a continuous process which contributes to developing technology and helps the society. Every step of the research work is to find different ways for future research work. However, there

are some issues to be solved for a future point of view in applications of power electronics converters for power quality improvement. There are some important points found out during the research works which further investigated and to be solved as mentioned as follows.

1. The presented Hilbert transform based ATF control strategy could be used in the control and integration of renewable energy sources to the grid.
2. Practical implementation of interleaved inverters for high power shunt APF applications could be tested with suitable control techniques in multifunctional operation.
3. The power system network continually experiences uncertainty in supply voltage and load harmonics due to integration of micro-producers of renewable energy into the system. Hence, the extraction of fundamental frequency components of supply voltage for the calculation of the reference current generation without phase delay is still a major problem. Therefore, simple control techniques to could be investigated.
4. Continue increasing in the microelectronic technology, chip technology, invention of many smart power electronic equipment create even order harmonics into the system. A proper control technique could be designed for this type of harmonic components.
5. The MSMC based control technique could be further explored for three-phase system to reduce the uncertainty of DC-link voltage under the steady-state and the transient condition of load.
6. Selection of optimal hardware components in the design and implementation of laboratory prototype model is a big challenge. The efficiency of the system is highly influenced by the components used in the hardware system.
7. High-speed DSP kits like FPGA, Micro toolbox of dSPACE platforms, etc. could be used for the implementation of control technique with reduced sampling time.

LIST OF PUBLICATIONS FROM RESEARCH WORK

International Journals (Accepted/ Published)

[1] **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Multitudinal Sliding Mode Controller based Interleaved Shunt APF to Mitigate Shoot-through and PQ Problems under Distorted Supply Voltage Conditions", *International Transactions on Electrical Energy Systems*, Wiley publications, vol. 29, no. 1, pp. 1-23, Jan. 2019.
DOI: https://doi.org/10.1002/etep.2701

[2] **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Single-Phase Shunt APF to Mitigate Current Harmonics and Switching Frequency Problems under Distorted Supply Voltage," *IETE Journal of Research*, Taylor & Francis Publications, Nov. 2018.
DOI: https://doi.org/10.1080/03772063.2018.1542351

[3] **V. Gali**, N. Gupta and R. A. Gupta, "PTF based control algorithm for Three-phase Interleaved Inverter based SAPF," *International Journal of Electronics, Taylor & Francis Publications*, Taylor & Francis Publications, Jan. 2019. (In Press)

[4] **V. Gali**, N. Gupta and R. A. Gupta, "Enhanced Particle Swarm Optimization Based Dc-Link Voltage Control Algorithm for Interleaved SAPF" *Journal of Engineering Science and Technology*, Taylors University Press, vol. 13, no. 10, pp. 3393-3418, Oct. 2018.

[5] **V. Gali**, N. Gupta and R. A. Gupta, "Experimental Investigations on Three-Phase Interleaved SAPF with Modified Indirect Current Control Algorithm," *International Journal of Power Electronics*, Inderscience Publishers, Nov. 2018. (In Press)

International and National Conferences

[1] **V. Gali**, N. Gupta and R. A. Gupta, "Predictive Tuned Filter based Reference Current Generation for Shunt Active Power Filter under Distorted and Unbalanced Supply Voltage," in *Proc. of IEEE National Power Engineering*

Conference (NPEC), Thiagarajar College of Engineering, Madhurai, pp. 188-193, March 8th -10th, 2018.

[2] **V. Gali**, N. Gupta and R. A. Gupta, "Enhanced Particle Swarm Optimization Technique for Interleaved Inverter tied Shunt Active Power Filter", in *Proc. of 7th International Conference on Soft Computing for Problem Solving (SocProS-2017)*, Indian Institute of Technology Bhubaneswar, Bhubaneswar, pp. 571-583, December 23rd – 24th, 2017. (Published in book chapter; Soft computing for problem solving, springer publishers)

[3] **V. Gali**, N. Gupta and R. A. Gupta, "Real-Time Implementation of Shunt Active Power Filter with Enhanced Control Algorithm using dPSACE1104 Controller", in *Proc. of dSPACE Academic Conference*, Indian Institute of Technology (IIT), Delhi, September 16th , 2017.

[4] **V. Gali**, N. Gupta and R. A. Gupta, "Distortion free Improved Reference Current Generation Algorithm for Interleaved Inverter based Shunt APF", in *Proc. of 9th IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Indian Institute of Science Bangalore, pp. 1-6, November 8th -10th, 2017.

[5] **V. Gali**, N. Gupta and R. A. Gupta, "Mitigation of Power Quality Problems using Shunt Active Power Filters: A Comprehensive Review", in *Proc. of 12th IEEE Conference on Industrial Electronics and Applications (ICIEA 2017)*, Cambodia, pp. 1100-1105, June 18th-20th, 2017.

[6] **V. Gali**, N. Gupta and R. A. Gupta, "Improved Dynamic Performance of Shunt Active Power Filter using Particle Swarm Optimization," in *Proc. of IEEE International Conference on Intelligent Techniques in Control, Optimization & Signal Processing (INCOS)*, Kalasalingam University, Srivilliputtur, pp. 505-511, March 23rd-25th, 2017.

[7] **V. Gali**, N. Gupta and R. A. Gupta, "Application of Shunt Active Power Filters in Medical Diagnosis and Critical Lab Equipment", in *Proc. of IEEE International Conference on Power and Embedded Drive Control (ICPEDC)*, SSN College of Engineering, Chennai, pp. 290-295, March, 2017.

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APPENDIX-A

Hardware Circuit and Laboratory Prototype Photograph

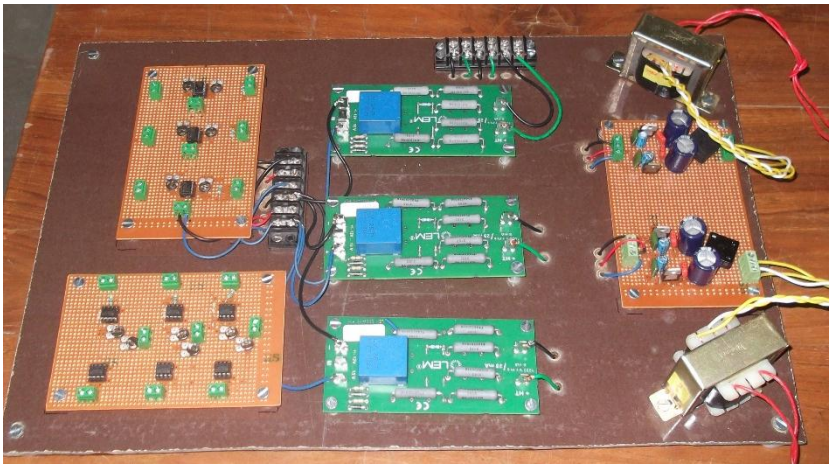


Figure A1. LEM LV25-P voltage sensor card with signal amplification

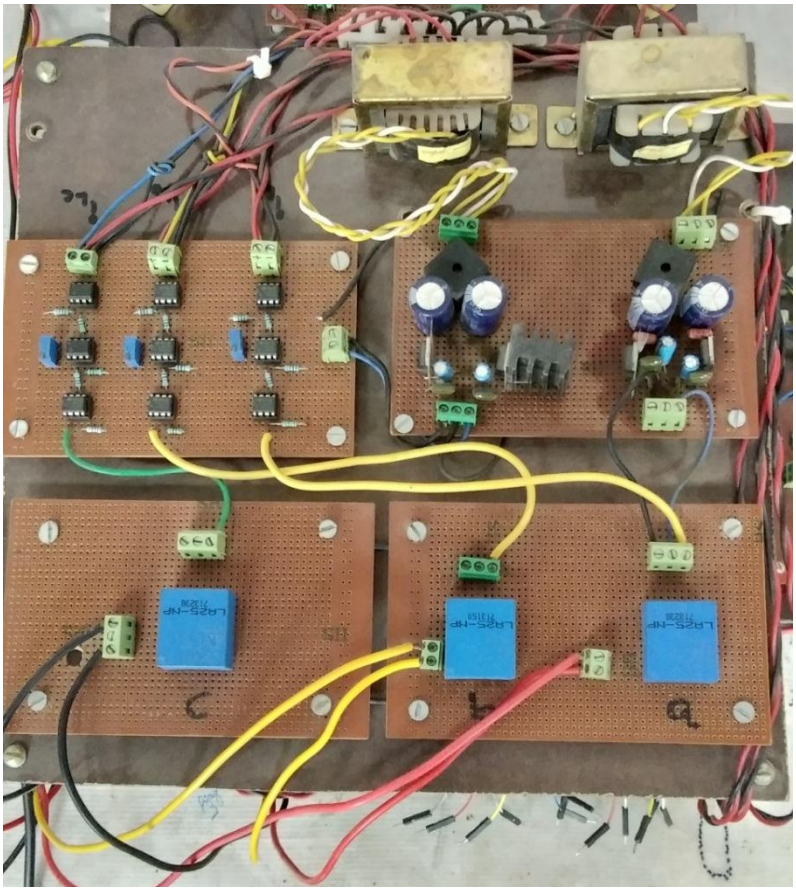


Figure A2. LEM LA25-NP Current sensor card with signal amplification

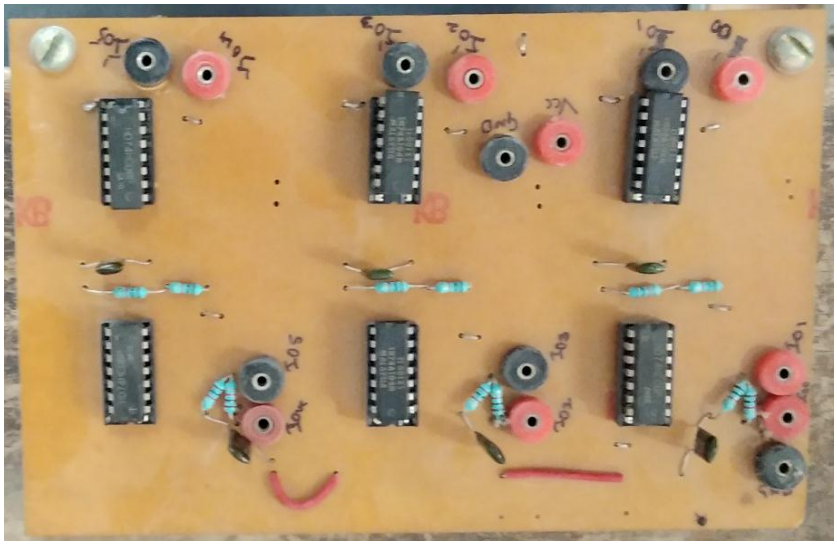


Figure A3. Dead-band circuit using 7404 and 7408 ICs

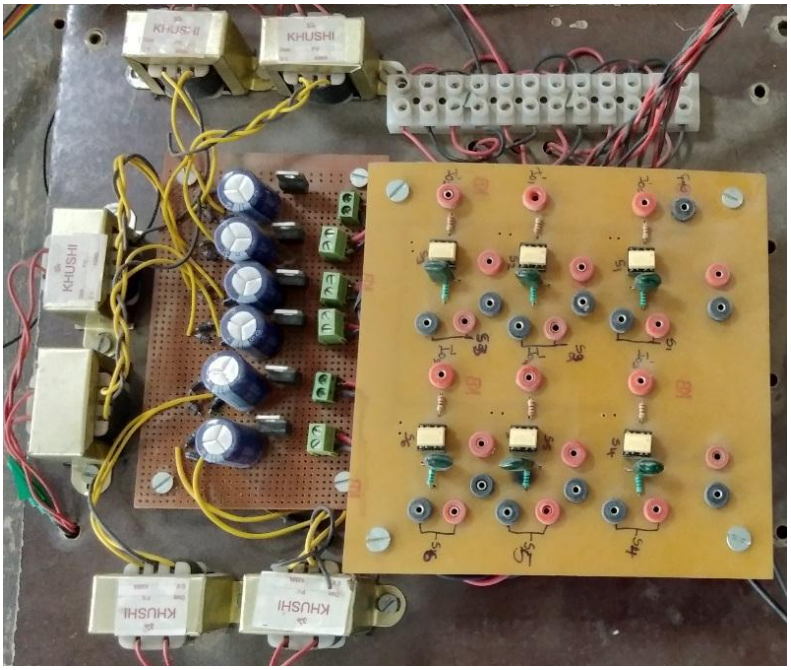


Figure A4. Pulse isolation and amplification circuit using TLP-250

Figure A5. Multi-purpose voltage source inverter using IRFP460 MOSFET

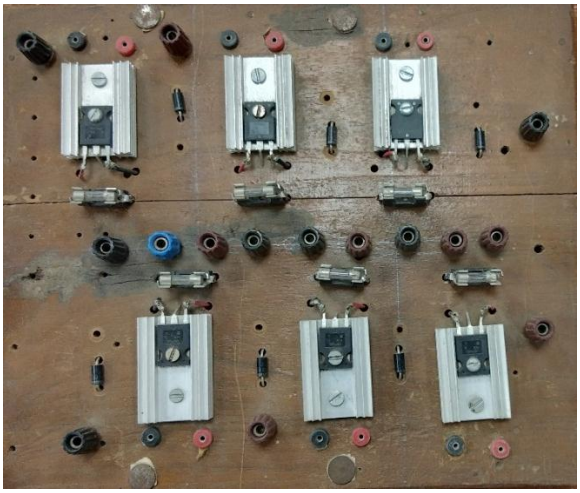


Figure A6. Multi-purpose interleaved inverter

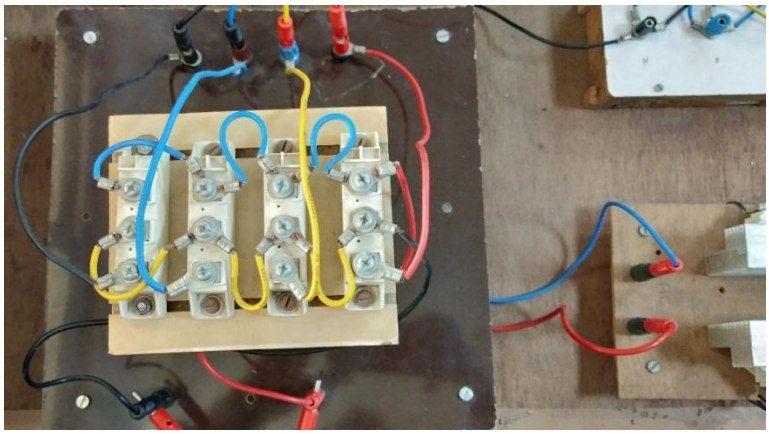


Figure A7. Diode bridge rectifier

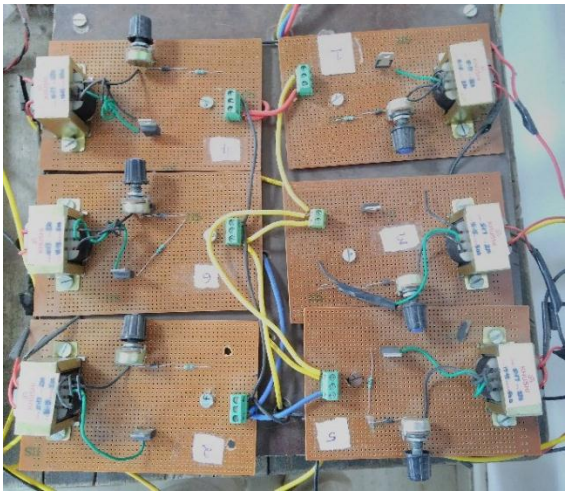


Figure A8. Thyristor controlled bridge rectifier

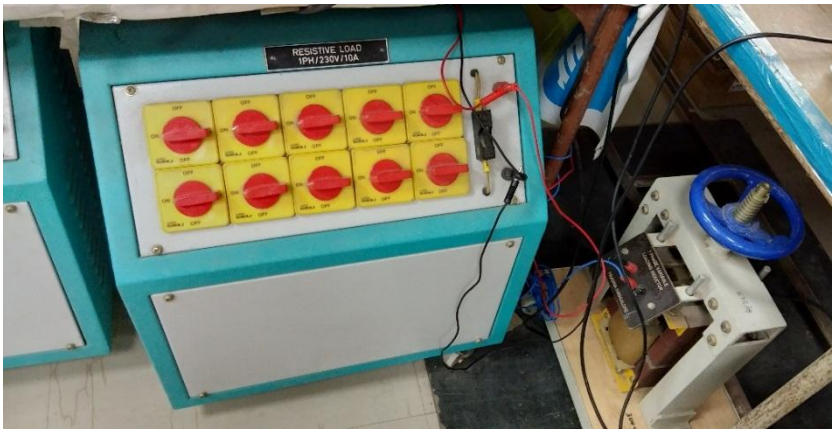


Figure A9. Resistive-inductive load

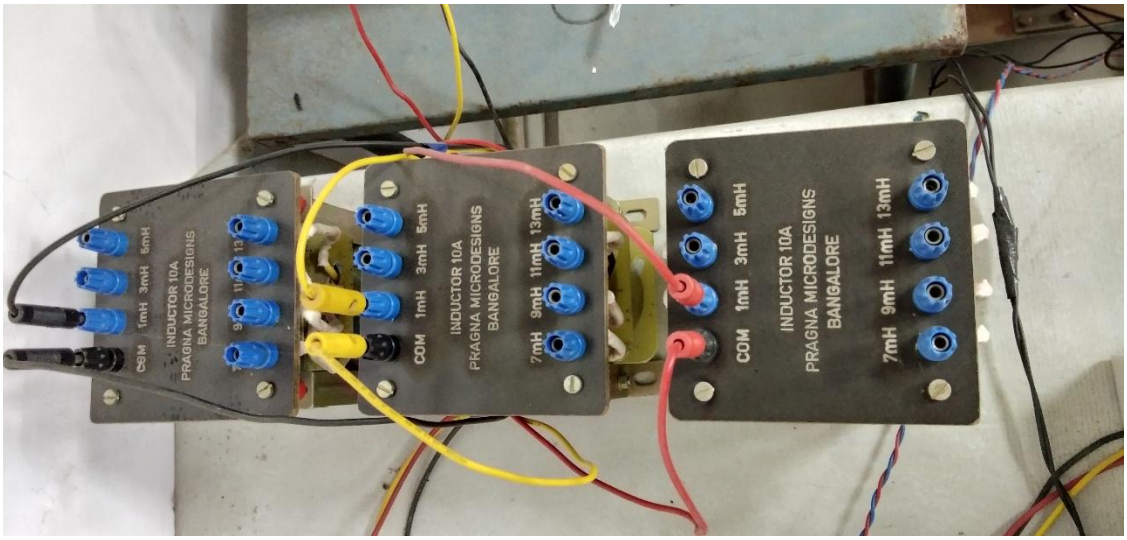


Figure A10. Interfacing inductors

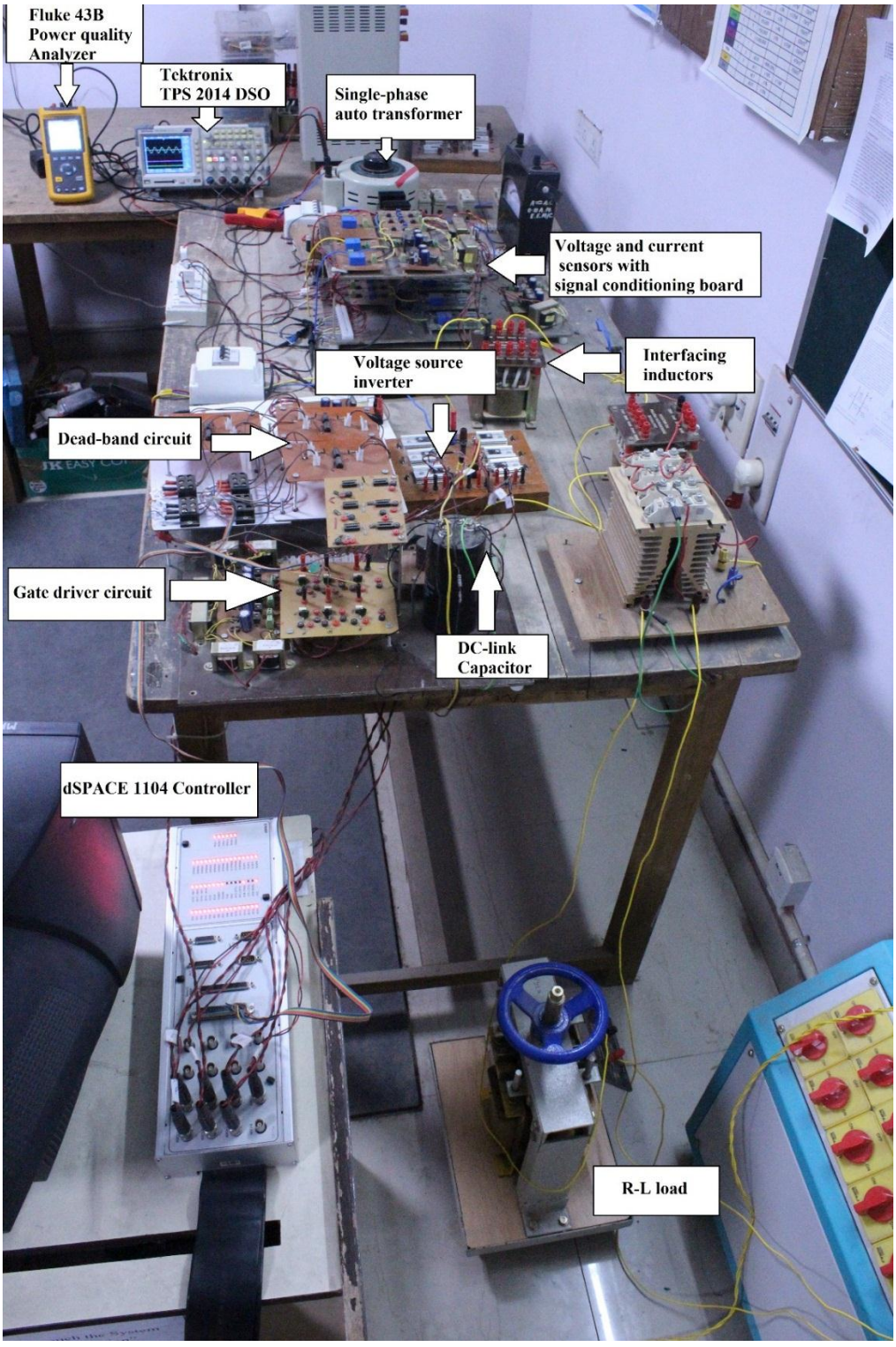


Figure A11. Single-phase voltage source inverter based shunt APF

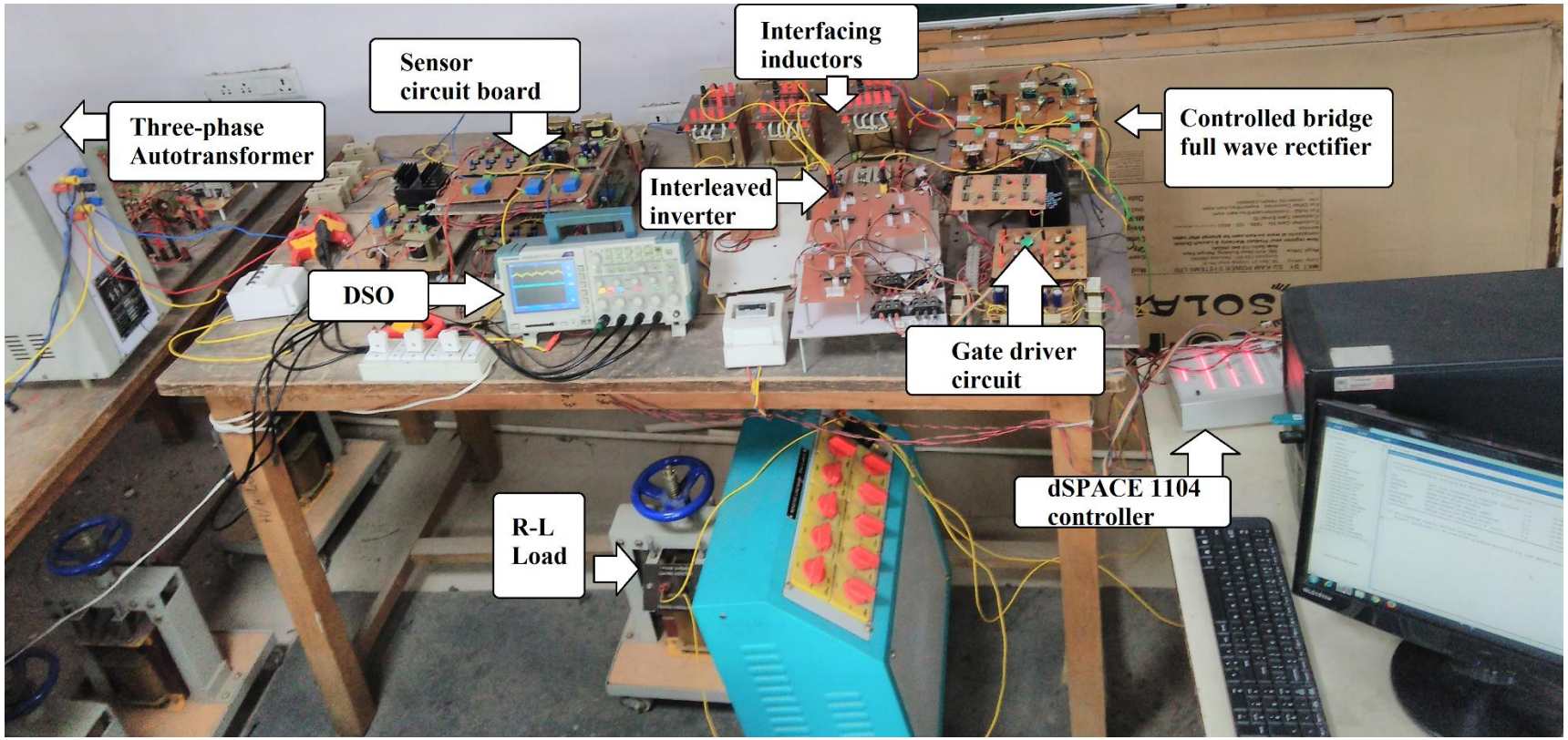


Figure A12. Three-phase interleaved inverter based shunt SPF

APPENDIX-B

Parameters used in Simulation and Experimental Study

Table-B1

The single-phase VSI based shunt APF simulation and experimental study parameters:

Parameters	**Symbol**	**Simulation**	**Experimental**
Supply Voltage	v_s	230 V RMS (50 Hz)	50 V RMS (50Hz)
Source resistance	R_S	0.1Ω	0.1 Ω
Source inductance	L_S	0.5mH	0.5mH
Interfacing resistance	R_{a1}, R_{a2}, R_{b1}, R_{b2}	0.7 Ω	0.7 Ω
Interfacing inductor	$L_{a1,}$ L_{a2}, L_{b1}, L_{b2}	11.5 mH	5 mH
DC-link capacitor	C_{dc}	1000 µF	1000 µF
DC-link capacitor voltage	V_{dc}	400 V	90V
PI controller values	k_p, k_i	0.1, 1	0.1, 1
Non-linear load case I Resistance	R_L	25 Ω	16 Ω (initially)
Inductor inductance	L_L	50 mH	30 mH
Transient Condition Non-linear load case II			
Resistance	R_L	50 Ω	32 Ω (when load decreased)
Inductor inductance	L_L	100 mH	30 mH

Table-B2

The three-phase interleaved SAPF simulation and experimental study parameters:

Parameters	**Symbol**	**Simulation**	**Experimental**
Supply Voltage	v_s	415 V RMS (50 Hz) (L-L)	100 V RMS (50Hz)
Series resistance	R_S	0.1Ω	0.1 Ω
Series inductance	L_S	1mH	0.5mH
Interfacing resistance	R_{a1}, R_{a2}, R_{b1}, R_{b2}	0.7 Ω	0.7 Ω
Interfacing inductor	L_{a1}, L_{a2}, L_{b1}, L_{b2}	5mH	2mH
DC-link capacitor	C_{dc}	1500 µF	1000 µF
DC-link capacitor voltage	V_{dc}	600V	150V
PI controller values	k_p, k_i	0.3, 2.1	0.1, 1
Non-linear load Resistance	R_L	25Ω	16 Ω (initially)
Inductor inductance	L_L	50mH	30 mH

Table-B3

The simulation and experimental study parameters for single-phase interleaved SAPF

Parameters	**Symbol**	**Simulation**	**Experimental**
Supply Voltage	v_s	230 V RMS (50 Hz)	100 V RMS (50Hz)
Source resistance	R_S	0.1Ω	0.1 Ω
Source inductance	L_S	0.5mH	0.5mH
Interfacing resistance	R_{a1}, R_{a2}, R_{b1}, R_{b2}	0.7 Ω	0.7 Ω
Interfacing inductor	$L_{a1,}$ L_{a2}, L_{b1}, L_{b2}	5mH	2mH
DC-link capacitor	C_{dc}	1500 µF	1000 µF
DC-link capacitor voltage PI controller Conventional SMC MSMC	U_{dc}	400V	150V
PI controller values	k_p, k_i	0.3, 2.1	0.1, 1
Non-linear load case I Resistance	R_L	25Ω	16 Ω (initially)
Inductor inductance	L_L	50mH	30 mH
Transient Condition Non-linear load case II			
Resistance	R_L	50Ω	32 Ω (when load decreased)
Inductor inductance	L_L	100mH	30mH

Table-B4

The simulation and experimental study parameters for three-phase interleaved SAPF

Parameters	**Symbol**	**Simulation**	**Experimental**
Supply Voltage	v_s	415 V RMS (50 Hz) (L-L)	100 V RMS (50Hz)
Series resistance	R_S	0.1Ω	0.1 Ω
Series inductance	L_S	1mH	0.5mH
Interfacing resistance	R_{a1}, R_{a2}, R_{b1}, R_{b2}	0.7 Ω	0.7 Ω
Interfacing inductor	$L_{a1,}$ L_{a2}, L_{b1}, L_{b2}	5mH	2mH
DC-link capacitor	C_{dc}	1500 µF	1000 µF
DC-link capacitor voltage	V_{dc}	600 V	150V
PI controller values	k_p, k_i	0.3, 2.1	0.1, 1
Non-linear load Resistance	R_L	10 Ω	10 Ω (initially)
Inductor inductance	L_L	50mH	40 mH

APPENDIX-C

DS1104 R&D Controller Board

Cost-effective system for controller development

Highlights

- Single-board system with real-time hardware and comprehensive I/O
- Cost-effective
- PCI/PCIe (PCI Express) hardware for use in PCs

Application Areas

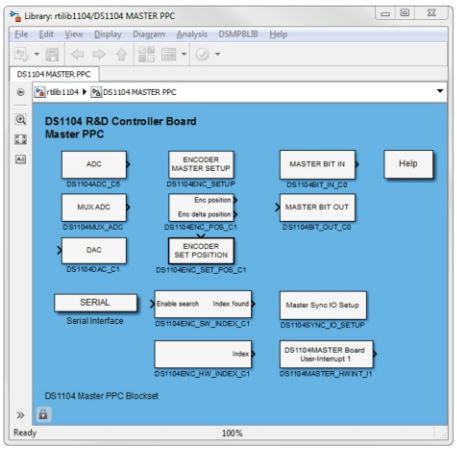
The real-time hardware based on PowerPC technology and its set of I/O interfaces make the controller board an ideal solution for developing controllers in various fields, such as drives, robotics, and aerospace. The board is used in many university laboratories.

Key Benefits

The DS1104 R&D Controller Board is a cost-effective entry-level system with I/O interfaces and a real-time processor on a single board that can be plugged directly into a PC. It upgrades your PC to a development tool for rapid control prototyping and is ideal for developing smaller control applications or for education purposes. Real-Time Interface (RTI, p. 62) provides Simulink® blocks for graphical I/O configuration. The board can be installed in virtually any PC with a free PCI or PCIe slot.

Using Real-Time Interface

With Real-Time Interface (RTI), you can easily run your function models on the DS1104 R&D Controller Board. You can configure all I/O graphically, insert the blocks into a Simulink block diagram, and generate the model code via Simulink® Coder™. The real-time model is compiled, downloaded, and started automatically. This reduces the implementation time to a minimum.



dSPACE GmbH • Rathenaustraße 26 • 33102 Paderborn • Germany • info@dspace.de • www.dspace.com