SIMULATION AND PERFORMANCE COMPARISON OF DOUBLE GATE TUNNEL FIELD EFFECT TRANSISTOR.

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by

Ajit Jakhar

(2017PEV5219)

Under the supervision of

Dr. Chitrakant Sahu

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY, JAIPUR

July 2019

Certificate

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology, Jaipur

This is to certify that the Dissertation Report on " **SIMULATION AND PERFORMANCE COMPARISON OF DOUBLE GATE TUNNEL FIELD EFFECT TRANSISTOR.**" by **Ajit Jakhar** is bonafide work completed under my supervision, hence approved for submission in partial fulfillment for the Master of Technology in VLSI, Malaviya National Institute of Technology, Jaipur during academic session 2018-2019 for the full time post graduation program of session 2017-2019. The work has been approved after plagiarism check as per institute rule.

Dr.Chitrakant Sahu

Assistant Professor

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology, Jaipur

July 2019

Abstract

Nowadays, technology to develop numerous features on a specific die we can use system-on-chip (Soc). These features are like converters, virtual, analog R/F applications, etc. To achieve this, the number of transistors is increased tremendously, so scaling is necessary. Due to this packaging density is also increases in the Nano electronics and micro electronics. According to ITRS guidelines, in contrast to conventional MOSFET we should use TFET, Schottky FET etc. As we are transferring closer to sub-20 nm scale, the Tunnel Field Effect Transistor (TFET) are terrific interest because of their low power applications. By using above devices the ON current is improved and OFF current decreased almost in the range of fA. Also better sub-threshold swing(SS) and short channel effects (SCE) are also eliminated. switching speed is good in TFET due to the transport mechanism, in contrast to conventional MOSFET, TFET use the band to band tunneling process instead of thermionic emission. Also gate control ability is way better than the conventional MOSFET.

Declaration

I declare that,

1. The work contained in this dissertation is original and has been done by me under the guidance of my supervisor.
2. The work has not been submitted to any other Institute for any degree or diploma.
3. I have followed the guidelines provided by the Institute in preparing the dissertation.
4. I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.
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(2017PEV5219)

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Abbreviations

BTBT	**B**and **T**o **B**and **T**unnling
CB	**C**onduction Band **B**and
CG	**C**ontrol **G**ate
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
D	**D**rain
ED-TFET	**E**lectrically **D**oped **T**unnel **F**ield **E**ffect **T**ransistor
JLT	**J**unctionless **T**ransistor
PG-1	**P**olarity **G**ate **1** **E**ffect
PG-2	**P**olarity **G**ate **2** **E**ffect
PVT	**P**rocess **V**oltage **T**emperature
RDF	**R**andom **D**opant **F**luctuation
S	**S**ource
SCE	**S**hort **C**hannel **E**ffect
SS	**S**ubthreshold **S**wing
TFET	**T**unnel **F**ield **E**ffect **T**ransistor
VB	**V**alence **B**and
V_{TH}	**T**hreshold **V**oltage
V_{DD}	**S**upply **V**oltage
I_{ON}	**O**n **S**tate **C**urrent
I_{OFF}	**O**FF **S**tate **C**urrent
C_G	**G**ate **C**apacitance
k	**B**oltzman **C**onstant
T	**T**emperature

q	**C**arrier **C**harge
m	**B**ody **C**oefficient
C_{DM}	**B**ulk **D**epletion **C**apacitance
C_{OX}	**O**xide **C**apacitance
I_{DS}	**D**rain **T**o **S**ource **C**urrent
V_{GS}	**G**ate **T**o **S**ource **V**oltage
C_L	**T**otal **S**witched **C**apacitive **L**oad
I_{leak}	**L**eakage **C**current
T_{SI}	**T**hickness **O**f **S**ilicon **F**lim
T_{OX}	**T**hickness **O**f **O**xide **F**lim
L_{CG}	**C**ontrol **G**ate **L**ength
$S_{GAP,S}$	**S**ource **S**ide **S**pacer **T**hickness
$S_{GAP,D}$	**D**rain **S**ide **S**pacer **T**hickness
V_{cg}	**C**ontrol **G**ate **V**oltage
V_{PG-1}	**P**olarity **G**ate-1 **V**oltage
V_{PG-2}	**P**olarity **G**ate-2 **V**oltage

Chapter 1

Introduction

As we are transferring closer to sub-20 nm scale, the Tunnel Field Effect Transistor (TFET) are terrific interest because of their low power applications. To understand why TFET can be used as semiconductor switches, first of all we must know that why conventional MOSFET's output is not satisfactory. So with a purpose to take into account that, we are going to figure out the merits and demerits of scaling of conventional MOSFET. According to Dennard's scaling guidelines,we have to do the source(s) drain(D)doping with the help of aspect of S. By maintaining electric field constant in the device [1]. Remaining dimensions of the device and voltages can be scaled by $\frac{1}{S}$. Now a days Dennard's scaling guidelines are not usedbecause of threshold voltage of conventional MOSFET, which is not follow these scaling guidelines. In modern era, Scaling is performed according to fig 1.1, According to this figure scaling is done from 1.4m to 65 nm node and supply voltage (VDD) is reduced to 78 value.and threshold- voltage is reduced to $\frac{1}{2}$. So we can say that overdrive voltage of the gate should be cut down[2]. decreasing of ON-current should be the of the overdrive voltage of the device and ON-current reduction directly affects the performance of conventional MOSFET. Basically performance depends on the $\frac{ION}{IOFF}$ ratio and dynamic speed.High gate overdrive voltage can be achieved by following two methods that are given below. (a)We need to do the proper threshold scaling. (b)We need to do the slow supply voltage(VDD) scaling.

1.1 Proper reduction of Threshold Voltage(V_{TH})

According to conventional MOSFET, We know that the carriers are flows from source to drain by means of thermionic emissions procedure. that's why its sub-threshold swing(SS)

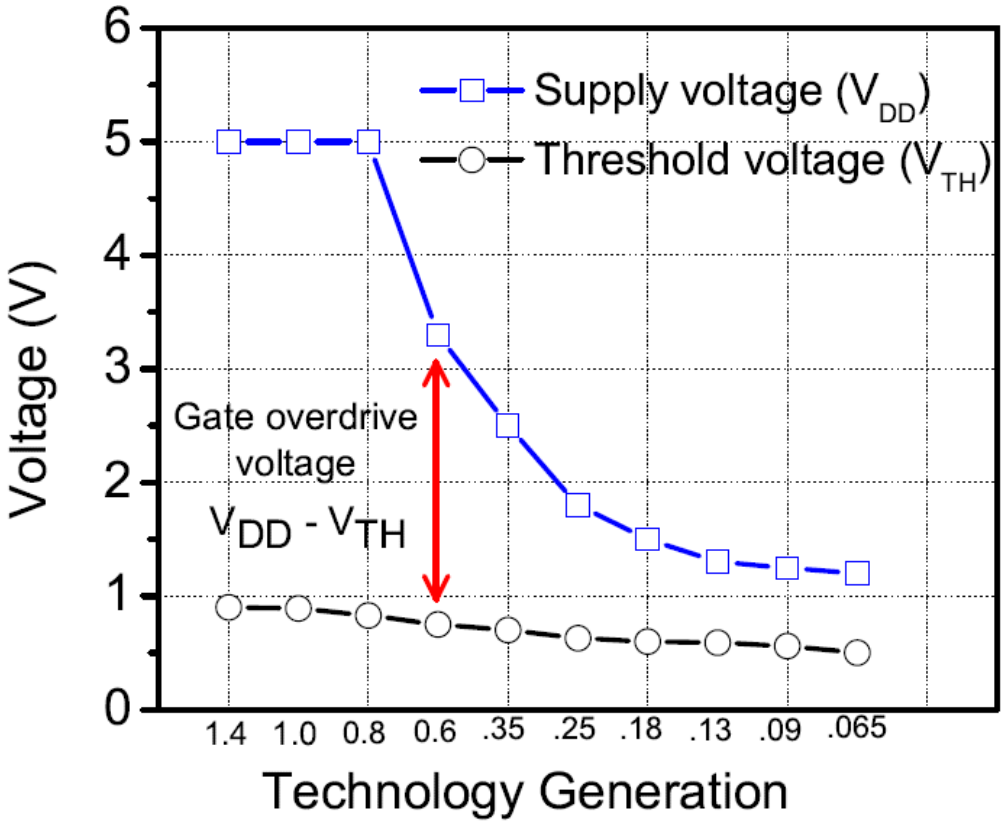

FIGURE 1.1: variation of supply and threshold voltage with respect to technology generations

will be restricted by thermal process i.e.$\frac{kT}{q}$. Here k represents the Boltzman's constant, T is temperature in kelvin and q is charge carriers. At room temperature SS should be less than $60\frac{mv}{dec}$ for conventional MOSFET[3]

$$SS = \frac{dVG}{dlogID} = \log_{10}\frac{mkT}{q} \tag{1.1}$$

Where m is the body-effect coefficient.The value of m should be near 1 to achieve optimized device.

1.2 Requirement Of Slow Supply Voltage(VDD)Scaling

By fig. 1.3(a) we can see theI_D-V_{GS} curve of conventional MOSFET, so to analysis the overall characteristics of MOSFET, the $\frac{ION}{IOFF}$ ratio is slow down. to achieve better performance we need to slow down the supply voltage. According to fig. 1.3(b) active and passive

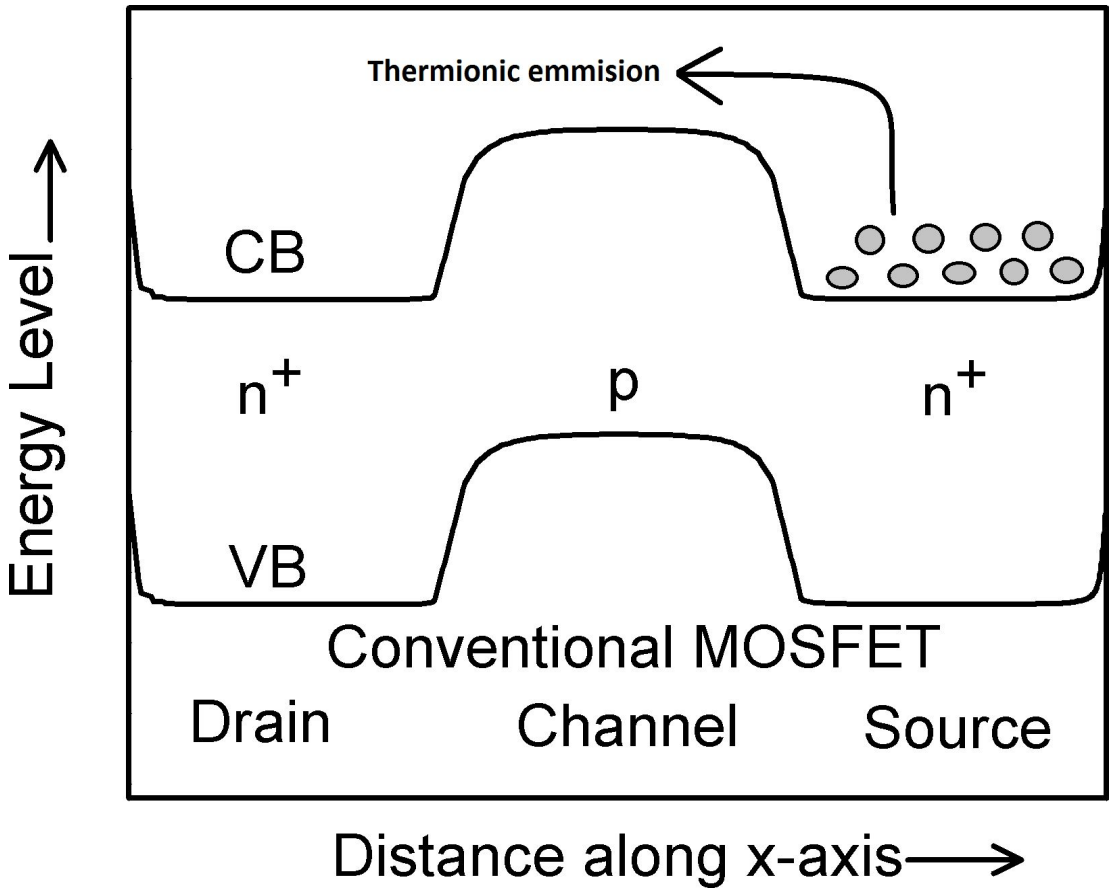

FIGURE 1.2: Process of thermionic emissions in conventional MOSFET.

power densities dissipation is mainly depends on total switch capacitance and supply voltage. So slow supply voltage is necessary to reduce this power dissipation. Frequency is also a parameter on which active power depends.whereas passive power is mainly depends on leakage current in conventional MOSFET. we know that leakage current is more in MOSFET in comparison to TFET so passive power is also more.

$$P_{Active} = fC_L VDD^2 \tag{1.2}$$

here f and CD will be the frequency and capacitance of the load.

$$P_{passive} = I_{leak} VDD \tag{1.3}$$

Leakage current is, current flow in the device should be work as OFF- state conditions. You could understand the shape in the Fig. 1.3(b), both the active passive current is

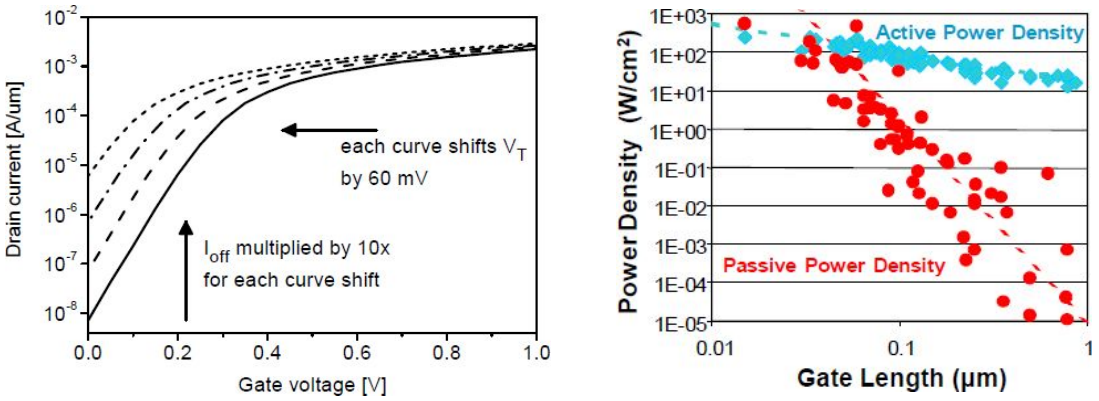

FIGURE 1.3: (a)input Characteristics Of The Conventional MOSFET[4],and(b)Active Passive Power dissipation plot with respect to different Gate Lengths[5].

exponentially increases with gate length.

1.3 Why TFET

Main reason of using TFET is, when devices are built on chip than power dissipation is increases in conventional MOSFET. But in TFET power dissipation is significantly low in TFET. Switching speed is also very high in TFET's in comparison to conventional MOSFET.

1.3.1 limitations of conventional MOSFET

(a)Leakage current : when$V_{GS} < V_{TH}$, the drain current should be zero but drain current reduces exponentially and this leakage current is main reason to power dissipation.

(b)Short channel effects (SCE)

When we scale down the conventional MOSFET, the size is reduces ,that's why electric field is increases and velocity of charge carrier will be saturates.

Drain induced barrier lowering (DIBL): When scaling is performed, the threshold-voltage is now depends on the drain voltage. this because carrier start flowing below the voltage less than the threshold voltage.

By reducing the channel length, holes and electrons start flowing through the dielectric.this phenomenon changes the total capacitance of the device.

1.4 Motivation

Main motivation towards TFET instead of conventional MOSFET is low leakage current and low power performance. also in conventional MOSFET short channel effect are more significant than the tunnel FET. we have already discussed the merits and demerits of scaling of conventional MOSFET. and main concern with convention MOSFET is their low ION/IOFF and sub-threshold swing (SS).

Chapter 2

Literature Review

2.1 Evolution of TFET

Initially in 1978, TFET was introduced at brown university for first time[9]. Furthermore the main characteristics of surface TFET was published at cambridge university in 1995. Forward biased TFET, Which was the same as above structure was proposed by koga [12] toriumi. Later in the year of 2004, band to band tunneling process is used to fabricate the TFET. Which is later used for making of carbon nano tube by the means of top gate and back gate methodology. Furthermore in the year of 2006, Theoretically noticed that the subthreshold swing (SS)should be less than the $60\frac{mv}{dec}$ [17]. Later on 2007, The simulation of double gate was completed and explore the tremendous possibility of TFET in various fields. By scaling of TFET there will be a lot of adverse effect is introduced which is analyzed further like low supply issue, Low threshold voltage problem , Short channel effect , drain induced barrier lowering issue and SS issue. Recently simulation of TFET and sensitivity analysis is performed and study about random dopant fluctuations of si TFET is performed[22]. Also nowadays TFET does not need the "ion implantation" techniques for the fabrication.

2.2 Advantages and Disadvantages of TFET

Advantage of tunnel FET over the conventional metal oxide semiconductor FET is the low off state current , Better subthreshold swing (SS) and negligible short channel effects . Because in tunnel FET current is flow through band to band tunneling off VB of source

to CB of channel instead of thermionic emission of MOSFET. Due to scaling conventional MOSFET has a major issue of power consumption and it could be reduced in TFET. Main disadvantage of TFET is the effectiveness of BTBT process is reduced in Si TFET. In TFET, ambipolar behavior is seen , In which p type shows majority of holes and n type shows majority of electrons.

2.3 Theory of tunnel FET

TFET is a better alternate of conventional MOSFET due to their low power applications and fast switching speed. Static power is also reduced by means of leakage current. Basically TFET usages the tunneling process for carrier flow. To increase the tunneling current, Source drain are heavily doped. Due to alignment of VB and CB , This phenomenon called non local BTBT tunneling.

2.3.1 Tunnel FET basic structure its working

Basically TFET is P^+-I-N^+ tppe diode with controlled with appropriate gate supply. In fig.2.1 a typical N type TFET structure is shown, In which drain is N^+ and source is p^+ type doped.Similarly for P type tunnel FET drain have P^+ type doping source have N^+ type doping profiles. Furthermore, To make device ON a reverse bias PN junction is formed in between intrinsic and source side structure, When appropriate gate bias is applied. The working operation can be understand by the help, the ON and OFF state conditions which could be understand by the Energy band diagrams(EBD). In fig.2.2(a),(b),(c)the OFF,ON- condition of N-type TFET ON condition of P-type TFET's are explained. Fig.2.2(a) shows that there is no alignment of cb and VB.That's why there is no current flow in this condition. According to fig.2.2(b),When a positive supply is applied the CB and VB are aligned and a current is start flow with mechanism called "Band To Band Tunneling". In this process the VB and CB of source and intrinsic region are aligned and current start flowing.Fig.2.2(c), Shows the tunneling process is get reversed because of change of polarity of gate terminal.To increase the tunneling current drain and source are heavily doped.

BTBT betwixt VB (valancy band) of P+ to CB(conduction band) of Intrinsic region (i), due to small tunneling power barrier height. Similarly,Fig. 2.2(c) indicates ON-nation band diagram of p-type TFET, while negative gate voltage is implemented on the gate.

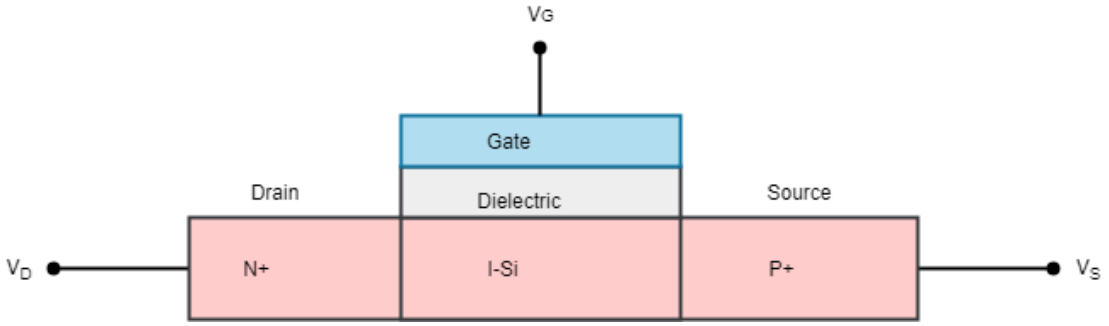

FIGURE 2.1: cross section of n type TFET

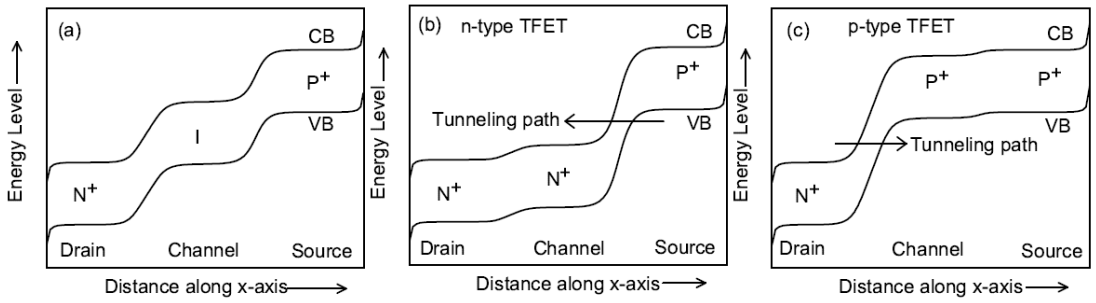

FIGURE 2.2: EBD of (a)off state (b) tunneling process in n type TFET, and (c) tunneling process in p type TFET)

You could analyze that underneath ON-state circumstance CB, and VB of I Getting aligned with CB(conduction band) and VB(valance band) of P+ area.

2.4 Potential Advantages Of The Tunnel FET Contrasted With The Conventional MOSFET

Potential advantage of TFET over the conventional MOSFET is understand with the help of these points as follows.

• At room temperature, Sub-threshold swing (SS)should be less than $60\frac{mv}{dec}$ which is achieved by TFET in comparison to MOSFET.

• With contrast to conventional MOSFET, TFET can be operated with low power supply. Hence they are low power devices.

Chapter 3

Ge ED-TFET

3.1 Introduction

In Tunnel FET, We know that the behavior of the transition slope is steepness when device change hid transition from off state to on state. that's why they have fundamental advantages over conventional MOSFET.To moderate overall requirements,TFET structure is complicated but they gives high $\frac{ION}{IOFF}$ ratio, however also saves the power at the same voltages for conventional MOSFET[2,3,4].to gain computationally efficient FET's, both the MOSFET and TFET has to be integrated into the chip's.that might increases the boolean functionality of that devices.Random dopant fluctuations (RDF)are decrease by the lightly doped TFET and MOSFET.due to dopingless structure,Which has no abrupt doping at source and drain junctions. therefore the effect of sensitivity towards many functions are increased. According to that explanations, we have to recommend a " Dynamically Configurable Double Gate FET" Which could be dynamically configured via constructing use regarding the appropriate Polarity bias. In different manners, the corresponding tool can be performed both similarly a TFET and MOSFET, accordingly getting the advantage of each device the privilege to high-performance low-energy (power saving) packages. Different switching among TFET and MOSFET, the polarity (n type ptype) to the suggested tool also can be handled dynamically. The idea of dynamic reconfigurability is depend upon an ED(electrically doped) Drain Source areas, in inclination to depends on external doping . The Ge- TFET device rented the identical scheme for experience to TFET and MOSFET, and others may processed to a n type-TFET and p type-TFET . Those days, logic- gates with property of configurability the regulation of gate controlled silicon nano-wire (SiNW) FETs had been exhibited beside adjustable n

Type	Ge ED-TFET	
	n-type	p-type
PG-1	+1.2	-1.2
PG-2	-1.2	+1.2

TABLE 3.1: Suitable Bias Resembled To PG-1 PG-2 For Configuring the Ge ED-TFET

and p type MOSFET usage greater gates with electrically doped conferred the remarkable capacity for more eminent cost compatibility with CMOS procedure [5, 6, 7,8]. In this Ge ED-TFET , introduced double gate are lightly doped which gives good performance against short channel effects(SCE) [8,9]. In the given device, Gate is divided into two partd which is authorized as PG-1 and PG-2 (a)In conventional TFET single gate is used but in this device CG is used to make device on state and off state, and (b)The gates are manufactured between the source (s)and drain(d),conduction mechanism control of switching of drain(d)and source(s) , i.e., nature of the device, for this reason, electrically transfer to n- type TFET p-type TFET. Also, It can specify the polarity and suggested adjustable TFET gives exactly same IDSVGS traits, That is necessary for given common gates. but, the explained tool additionally have a downside to expected another gates with electrically doped, As a result, extra metallic deposited isolation is needed might intend greater parasitic consequences. From the SILVACO simulation outputs display utilized the ED-TFET device (both n,p type-TFETs and n,p type-MOSFETs) has a proper compliance to traditional static contrivances having considered essential traits to low-energy high-performance application.

3.2 Structure and Analysis of Ge ED-TFET

Fig. 3.1, exhibits the cross sectional scenario of the recommended polarity primarily depend device shape, section 3.1 indicates external bias expected to dynamically configure alike ntype or p type TFET(tunnel field effect transistor) or MOSFET. drain and source are made of very thin film on silicon wafer by electrically doping. polarity gates (PG-1,PG-2) are made of equal metallic material like TiN. also drain and source contacts are manufactured by Nickle Silicide (NiSi).the barrier gap needed is approximately around 4.5ev which is fullfilled by NiSi. The operating mechanism and characteristics of proposed Ge ED-TFET is utilized with the help of TCAD simulator[9,11]. For MOSFET, the process mechanism is transmission through hydrodynamic procedure[1,7]. while, for TFET the method is used, called non local band to band tunneling (BTBT) version in which tunneling procedure is processed directly through valance band to conduction band [6,11].

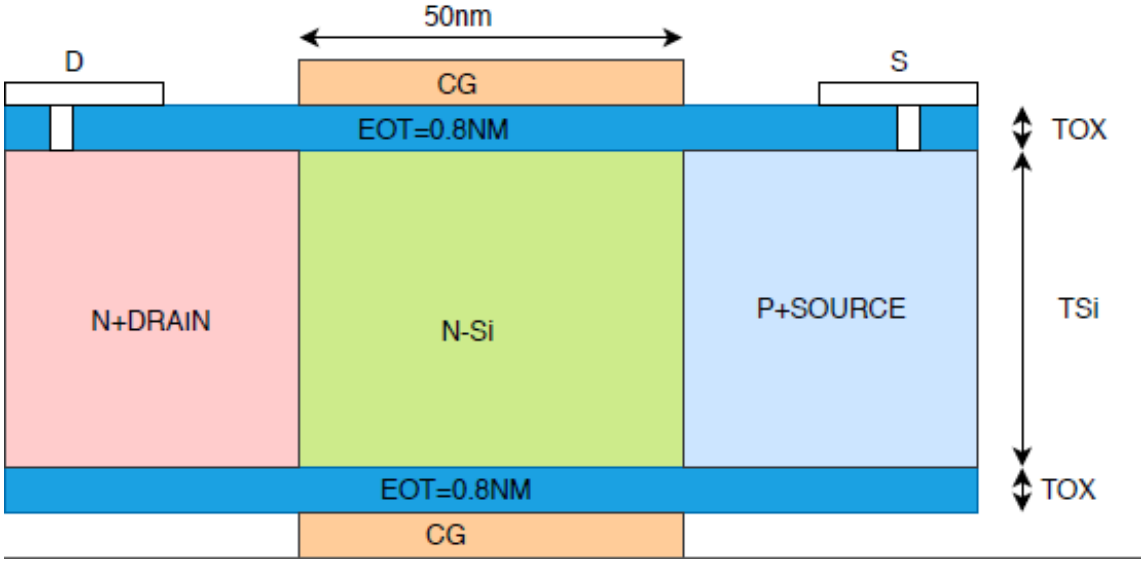

FIGURE 3.1: Cross Sectional View Conventional TFET.

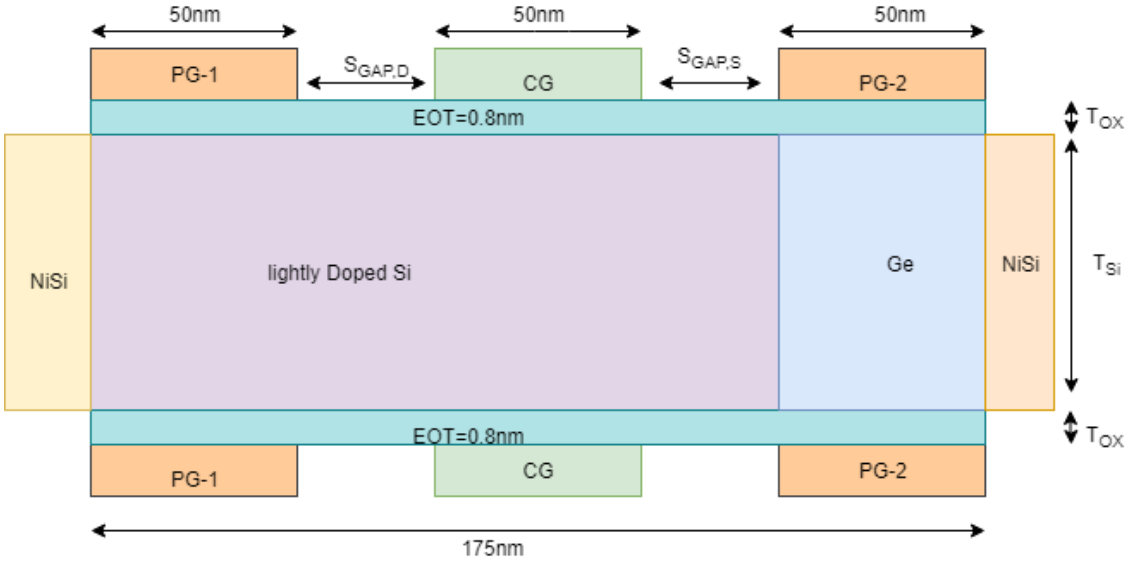

FIGURE 3.2: Cross Sectional View Of Proposed Ge ED-TFET Device.

3.3 Simulation Parameter And Models

Fig. 3.1 exhibits the cross sectional aspect of a conventional TFET simulation Parameters which will defind as follows [3,4]: thickness of silicon (T_{SI}) = 10 nm, gate oxide thickness (T_{OX}) = 0.8 nm, manipulated gate duration (L_{CG}) = 50 nm, channel is doped with = 1x1017cm^{-3} ,P_+ source doping$N_A = 1 * 10^{20}$ cm^{-3} , N^+ drain doping ND = $5 * 10^{18}$ cm^{-3}, and common gate work function is -gate (CG = 4.5 eV. According to Fig. 3.2 the cross sectional view of the given ED (electrically doped) Ge TFET (EDTFET) shape

and parameters of simulation are carried into the same way as conventional TFET are as follows. In the Ge ED-TFET, Shape is almost same as the conventional TFET besides of variation in doping concentration .In the Ge TFET ,The source (P^+) and drain (N^+)are made of polarity gate (PG) phenomenon[13,14,15]. To built the drain as N^+ region,The doping of electrons are increased similar to drain regions are formed. And to make the source (S),The concentration of holes are inhanced similar to P^+ supply as the lightly doped Ptype silicon wafer. So said that the biasing is poor at the source side or PG-2 side. And length of both polarity gate (PG-1,PG-2)is 50nm. Also metal workfunction of both the gates should be 0.45 ev which is same asin conventional TFET. To construct the drain (D and source region (S) Nickel Silicide (NiSi)is used whose barrier potential or width is near to 0.45ev.Spacing between source side($S_{GAP,S}$)is made 5nm between the PG-2 and common gate (CG) and spacing between drain side($S_{GAP,S}$)is made 20nm between PG-1 and common gate (CG).

All the simulation parameters are tabulated as follows for both the conventional TFET Ge ED-TFET.

Parameters	**Values**
N_D	$5X10^{18}\ cm^{-3}$
N_A	$1X10^{20}\ cm^{-3}$
Channel doping	$1X10^{17}\ cm^{-3}$
G_e	$1X10^{19}\ cm^{-3}$
W.F of CG, PG-1,PG-2	0.45 eV
T_{SI}	10nm
T_{OX}	0.8nm
L_{CG},L_{PG-1},L_{PG-2}	50nm
$S_{GAP,S}$	8nm
$S_{GAP,D}$	20nm

TABLE 3.2: Simulation parameters of Ge ED-TFET

3.4 Benefits of polarity gates

• By the usage of polarity gates dynamic switching between the N and P type gate can be easily done. In different words, The polarity throughout the operation is same and distinct functionality is also achieve with identical circuit.

• With the help of polarity gates the dependency of short channel effects (SCE) is tremendously reduced in comparison to conventional TFET. And by using this the device doesn't demand any exceptional methods inclusive of strain technology and various others.

• Large scale integration could be very easy with the help of polarity gates method because no need of " Thermionic Annealing" and "Ion-implantation" techniques.

3.5 Atlas Silvaco simulator

Atlas software provides simulation based general solutions for based on physical simulation may it be two or three-dimensional (2D,3D) simulation. Atlas tool is made in such a way such that tool may be used along with the VWF based Interactive Tools. These VWF tools are also known as Virtual Wafer based Fabrication Interactive Tools. These are made of the following: Tony Plot, Optimizer, MaskViews, Deck Build and also DevEdit[15].

Function can be explained as below:

• Deck Build is a window which is used for all command instructions.

• Devedit makes it possible to craft structure of device and also helps in designing the meshes which is used in a very cooperative surrounding.

• Optimizer can be used across various simulators to provide Optimization.

• MaskViews help in providing IC layout correction.

• TonyPlot is like the output window which is used to actually display the various electrical characteristics such as drain current for the device as well as also display the generated structure files. These files can be reopened with the help of TonyPlot.

Since the results of VWF Tools simulation based results are closely similar with new advancement in technology and hence results obtained are very similar to experimentation done. These tools can be very useful since they are very similar to approaching technology. It has also proved to be helpful in prediction of nearly all the current and voltage related characteristics and options related to the all new devices and also processes of technology.

Similar to Atlas, one other process simulator, is named as Athena. This can also produce prepared structures through many process based steps. It is mainly used in fabrication related devices. The same structure can be used by Atlas in form of inputs. Later various electrical characteristics can be predicted about the designed device with the help of Atlas. Next stage include providing the output of the Atlas to the SPICE modelling code and produce device based characterization at last.

Atlas can also be considered as simulation machine based on physical simulations for devices because this is capable of finding characteristics like drain current, frequency analysis etc. related to a specific device with selected structure and also the voltage outputs present at the electrodes. Simulators make the complete device space with grid like structure known as meshes and end known as nodes. Differential equations based Maxwell's laws and current conduction are applied at every location throughout the structure which helps in determining the electrical parameters. Being physically based device simulator has several advantages because without fabricating the device directly, a deep understanding can be brought about the device. Calculation of many complex parameters becomes easy and quick. It also helps in approximation of the output ,also the input can be varied in stepwise manner to get very close discrete output.

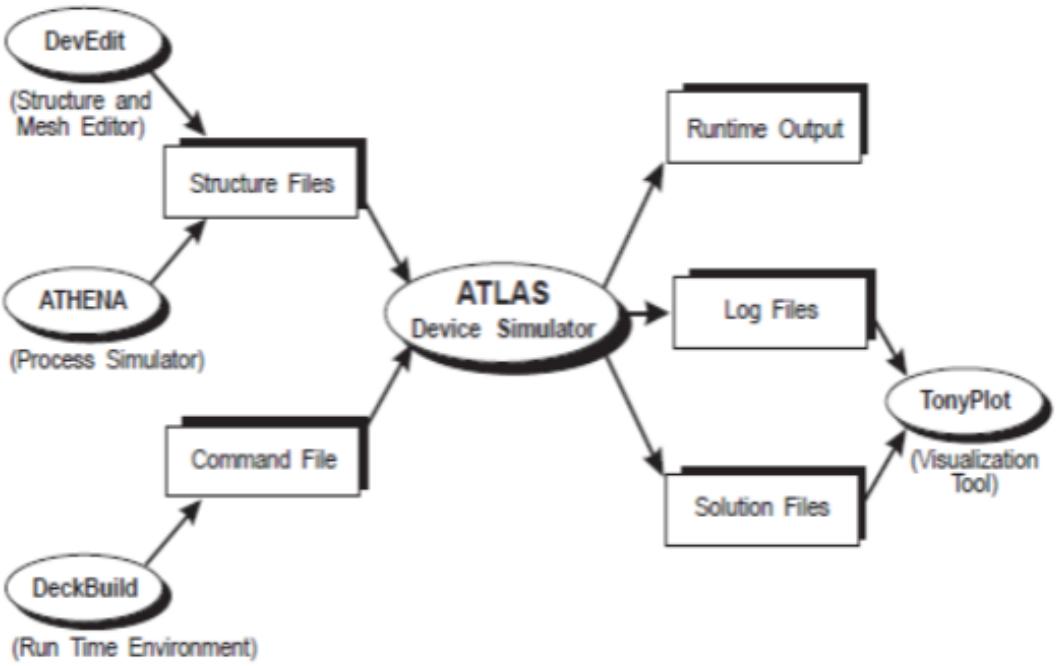

FIGURE 3.3: Atlas device simulator.

Above diagram explains how the information flow through Atlas device simulation (Figure3.1).Code is written on the text file which is run through the atlas simulator which in result is saved into a structure and log file.

Atlas mainly has three types of output files:

• Runtime output provides necessary data to be processed at every execution of atlas commands. It also shows errors and warnings at the same time.

•Log file data can be run later through tonyplot tool to plot required graphs.

Log files also provide all necessary electrical characteristics like drain current, trans conductance etc. 3.1: Introduction Atlas software provides simulation based general solutions for based on physical simulation may it be two or three-dimensional (2D,3D) simulation. Atlas tool is made in such a way such that tool may be used along with the VWF based Interactive Tools. These VWF tools are also known as Virtual Wafer based Fabrication Interactive Tools. These are made of the following: Tony Plot, Optimizer, MaskViews, Deck Build and also DevEdit[15].

Function can be explained as below:

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Chapter 4

Simulation results and analysis of Ge ED-TFET

4.1 DC analysis of Ge ED-TFET

According to this section, Analysis and comparison of carrier concentration of the holes and electron, energy band diagrams (EBD),input and output characteristics of both conventional Ge ED-TFET has completed.

4.1.1 Carrier concentration plot of Ge ED-TFET device

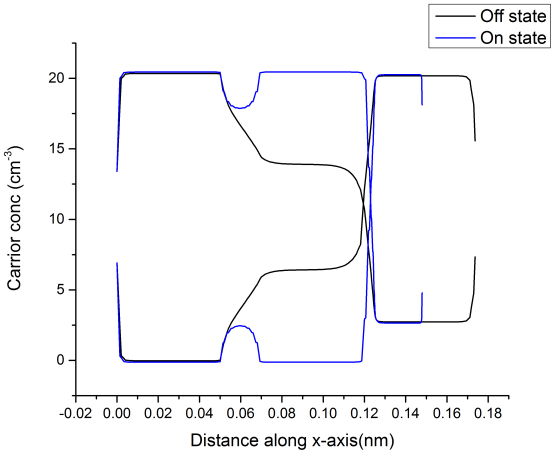

FIGURE 4.1: Electron and hole conc. of Ge ED-TFET for ($V_{DS} = 1V$, $V_{PG-1} = 1.2V$, $V_{PG-2} = -1.2V$) in OFF - state($V_{CG} = 0V$) and ON- state ($V_{CG} = 0V$)

As we can see in fig. 4.1 we can achieve carrier concentration for distinct regions conditions.in the ED-TFET a horizontal cut line is made near to the control gate side of the silicon (Si) material is almost alike the conventional TFET. And it should decreased down near the source(S) drain region(D) due the presence of NiSi.by applying the $V_{CG} = 0V$,the electron concentration become the order of $10^{19}cm^{-3}$. That is same as we could see at the n+ region. so in advised device abrupt pn junction is formed and tunneling process is happen from the VB of p^+ and flow towards the CB of Drain(D) region.

4.1.2 Energy band diagrams of Ge ED-TFET device

further tunneling process we can understand by the help of fig. 4.2, in off state the probability of passing the electron from CB to VB is extremely low due to very high barrier gap. Two distinct PG will be applied to separate the energy gap(Eg) near the source(s) drain(d). also the charge carriers started deposit near the junction of Drain(D) Source(S) when a with the help of proper biasing both the CB and VB are aligned together and tunneling process is happened.

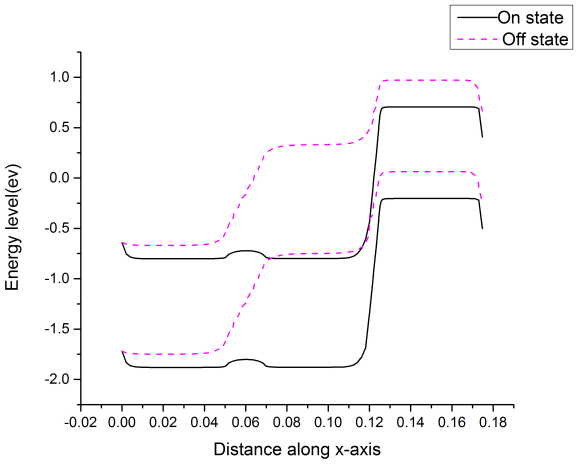

FIGURE 4.2: Energy band diagram of Ge ED-TFET for ($V_{DS} = 1V$, $V_{PG-1} = 1.2V$, $V_{PG-2} = -1.2V$) in OFF- state($V_{CG} = 0V$)and ON-state ($V_{CG} = 0V$)

.

4.1.3 I_D-V_G characteristics analysis of conventional TFET and Ge ED-TFET

Fig 4.3 exhibits the characteristics of conventional given device , we can see from the figures that the both follows the same trend. and also the Ge ED-TFET will have one

order less than the comparison with the conventional TFET. It is the effect of the high on- state resistance given from the doping -less structure of proposed device.but off state current is very low in comparison with the conventional TFET. This is due to Si which is lightly doped absence of pn junctions.

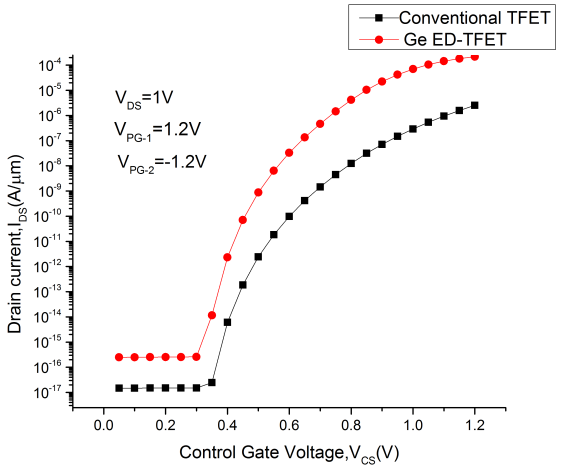

FIGURE 4.3: I_D-V_G plot of conventional TFET and Ge ED-TFET

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4.1.4 Comparison of output characteristics of conventional TFET and Ge ED-TFET

Fig 4.4 and 4.5 exhibits the analysis and comparison of output characteristics for different values of VCG, in which as we increase the VDS the carrier through the tunneling is also increases.and the exponential relationship is hold between the drain current and VDS.this relationship due to the SS swing. at room temperature higher ION and step SS is must required for better device.

4.2 AC analysis of Ge ED-TFET

In this section study and analysis of capacitances, Transconductance and operating frequency has been done. for any device, Analog/RF performance is based on these parameters which are as follows.

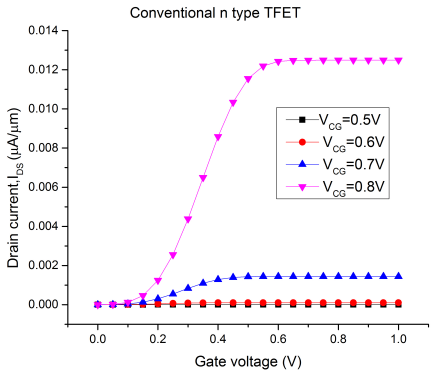

FIGURE 4.4: output characteristics of conventional TFET

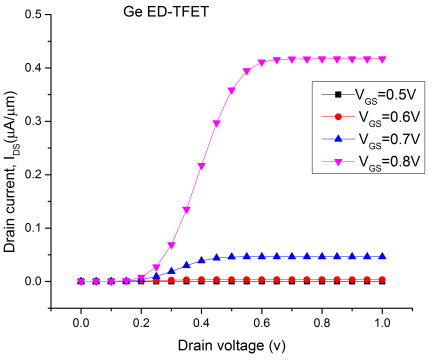

FIGURE 4.5: output characteristics of Ge ED-TFET

4.2.1 Analysis of gate to source(C_{gs}) and gate to drain(C_{ds}) capacitances

Due to parasitic capacitances, The performance is affected at higher frequencies. At lower frequencies, The electrical performance of the device at circuit level is negligibly affected by parasitic capacitances. Signal is distorted by the parasitic capacitances at higher frequencies due to oscillation.so we need to suppress these capacitances to make fine performance at high frequencies. the effect of C_{gs} is negligible as comparison to C_{ds}, So to avoid the degradation of device performances,C_{ds} must be as low as possible.

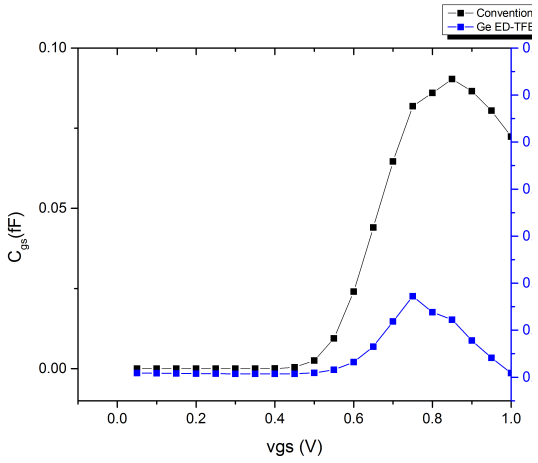

FIGURE 4.6: Comparison of C_{gs} of conventional TFET Ge ED-TFET

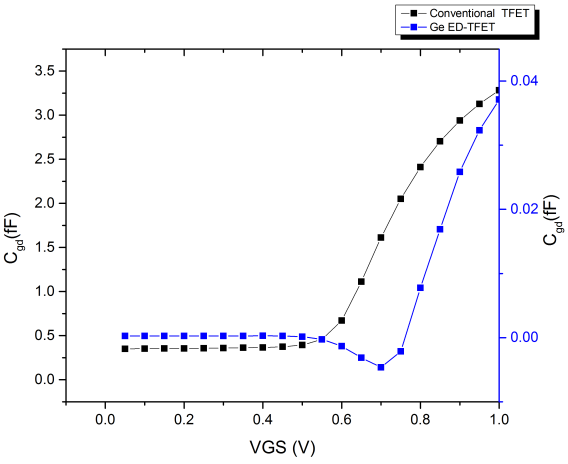

FIGURE 4.7: Comparison of C_{ds} of conventional TFET Ge ED-TFET

4.2.2 Analysis and comparison of transconductance of conventional TFET and Ge ED-TFET

In this section, The comparison of transcondutance (both input and output)is completed. the ability of performance of device is based on the transcondutance(g_m). transcondutance(g_m)of the device is ability to convert input voltage into the drain current.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

In the above equation, g_m shows the sensitivity of converting gate voltage into drain current. similarly with respect to drain voltage, known as output transconductance (g_{ds})is defined.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$$

From above equation we can say that the g_{ds} is inverse of output resistance. so for better performances output transcondutance(g_{ds})must be as low as possible.

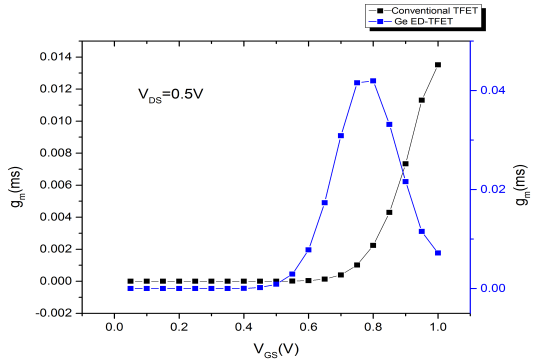

FIGURE 4.8: Comparison of g_m of conventional TFET Ge ED-TFET

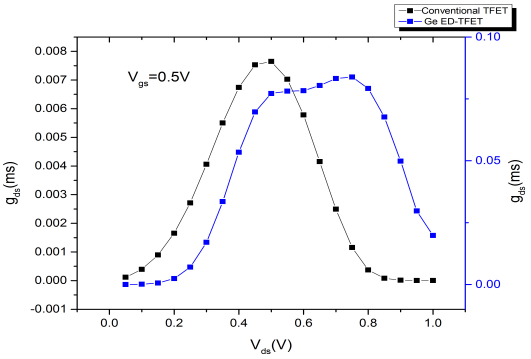

FIGURE 4.9: Comparison of g_{ds} of conventional TFET Ge ED-TFET

4.2.3 Analysis of operating frequency(f_T,f_{Tmax}) of conventional TFET and Ge ED-TFET

$$f_T = \frac{g_m}{2Pi(C_{gs} + C_{gd})}$$

$$f_{Tmax} = \sqrt{\frac{g_m}{2Pi(C_{gs} + C_{gd})R_{gd}}}$$

Dependency of the capacitances with input and output voltage is seen from above equations gives the operating frequency is mainly depends on the g_m and the capacitances. As g_m increases, Operating frequency is increases and due to mutual increment of capacitances, f_T should be decreases. so both parameter (g_m and capacitances) is improved in proposed Ge ED-TFET than operating frequency and maximum operating frequency both improves. From above graphs we can see the improvement in the operating frequency of Ge ED-

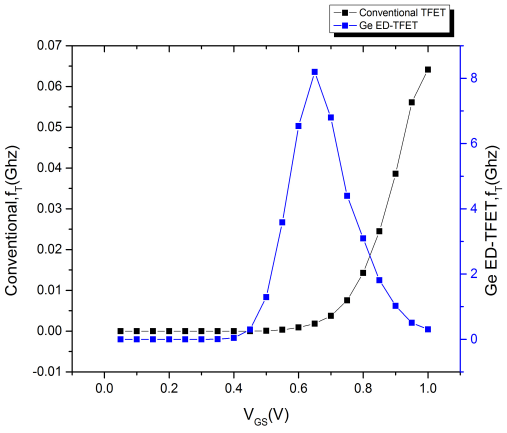

FIGURE 4.10: Comparison of f_T of conventional TFET and Ge ED-TFET

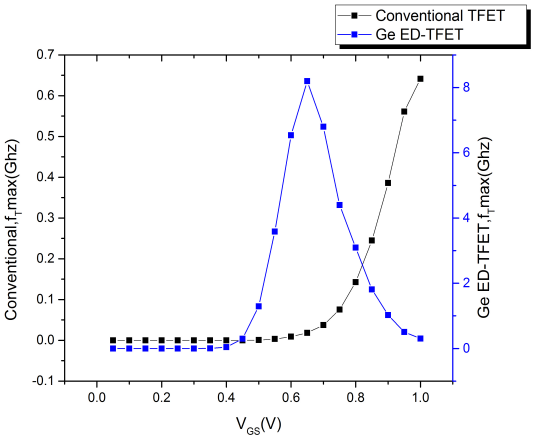

FIGURE 4.11: Comparison of f_{Tmax} of conventional TFET and Ge ED-TFET

TFET in comparison to conventional TFET. All the simulation results of Ge ED-TFET is as follows.

Parameters	Units	Conventional TFET	Ge ED-TFET
I_{ON}	A/μm	$2.5X10^{-6}$	$2.16X10^{-4}$
I_{OFF}	A/μm	$2X10{-}16$	$2X10^{-18}$
g_m	mS	0.014	0.05
f_T	GHz	0.08	8

TABLE 4.1: Comparison of simulation results of conventional TFET and Ge ED-TFET.

Chapter 5

Conclusion

5.1 Conclusion

In this thesis, We designed the Ge ED-TFET where Ge is doped on the source side of electrically doped TFET. The ON current is improved by 2 decade in comparison with conventional TFET and OFF current is in the range of 10^{-16} $A/\mu m$.

Secondly, We done the DC and AC analysis of both Ge ED-TFET and conventional TFET. In DC analysis, The input characteristics shows the better $\frac{ION}{IOFF}$ ratio and output characteristics shows the better exponentially increment in drain current with respect to drain voltages. Further, Input and output capacitances (C_{gs} and C_{gd})is also reduced in comparison with conventional TFET. The response of transconductance(g_m) is also better, That means drain current is increased with less supply voltage. The disadvantage of this device is that the OFF current is more as compared to conventional TFET.

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