Self Biased Cascode Op Amp

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by

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CANDIDATE'S DECLARATION

I hereby declare that the work that is presented in this dissertation entitled, Self Biased Cascode Op Amp in Electronics and Communication Engineering with specialization in Embedded System submitted to Department of Electronics and Communication Engineering, Malaviya National Institute of Technology Jaipur is a record of my own investigation carried under the supervision of Shri. Sanjeev Agrawal, Associate Professor, Department of Electronis and Communication Engineering, Malaviya National Institute of Technology Jaipur. I have not submitted the matter presented in this dissertation anywhere else for the award of any other degree.

Date: G.Vinay Kumar

Place: MNIT Jaipur 2017PEB5214

CERTIFICATE

This is to certify that the project report titled **"Self Biased Cascode Op Amp"** done by Golkonda Vinay Kumar, Enrollment Id. 2017PEB5214 is a work carried out by him at Malaviya National Institute of Technology, Jaipur under my guidance. The matter embodied in this work has not been submitted earlier for the award of any degree to the best of my knowledge and belief.

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Abstract

It describes a technique of interpreting MOSFET behaviour that is more consistent with contemporary analog CMOS circuit design. This technique surpasses the use in design of easy but antiquated equations and replaces them with an strategy based on the individual transistor's inversion coefficient in design. Measurements and modeling confirm that this technique can be used effectively to arbitrate challenging analog models between the multiple countervailing demands.

This report presents the reader to the g_m/I_D methodology -based design, which is a way to assist CMOS analog circuit developers connect physical transistor parameters to small models of signal.

Contents

List of Figures

Chapter 1

Introduction

1.1 Aim

Designing a High Gain Cascode Operational Amplifier using g_m/I_D Method.

1.2 Overview

As technology has progressed, the MOSFET's behaviour has become more complex owing to lower geometries, greater electrical fields and (lately) a continuous decline in the voltage of the power supply. Despite these modifications, approaches to analog design have basically continued to use techniques based on much older and simpler MOSFET behavior interpretations. This has resulted in an analog "design gap" in which designers attempt to create previous techniques function on fresh technology; this prevents designers from realizing the complete potential of contemporary deep submicron CMOS technology.

1.3 Motivation

CMOS has become an exceptional analog circuit designing platform. It is not only unrivaled in the processing of switching and charging mode,

but it also benefits from constant process changes driven by the digital consumer market. Unfortunately, it may be very difficult for developers to take advantage of these strengths.The main reason for this is that CMOS behaviour is difficult to estimate without the use of very complicated models, and with technology scaling this complexity only worsens. Designers are expected to integrate complicated models into their hand calculations or spiral into a spice-intensive design loop, incidentally under pressure to fulfill deadlines. None of these are as effective or pleasant as we would like.

1.4 Objective

My objective is to introduce you to the g_m/I_D based design methodology that demonstrates the predictability of CMOS small-signal behavior without the need for complex equations. We will define the ratio g_m/I_D as a design variable that encapsulates a MOS transistor's biased conditions.At quantitave level we shall rehash the whole discussion. This involves a review of the operation of the transistors and a chronological development of the tools available.

1.5 Organisation of Thesis

This thesis is organised as follows.First chapter outlines the introduction of the thesis.Chapter two reviews the literature work.Chapter three describes the cascode operational amplifier which uses transconductance over drain current methodology.Chapter four consists of simulation results and chapter five concludes the report with conclusion and future works.

Chapter 2

Literature Review

2.1 How better g_m/I_D than V_{ov}?

When CMOS designers decide to seek a V_{ov} design approach, the validity of the long-channel model is implicitly accepted. I am sure you know the long channel model. When we first studied MOSFET analysis, we showed that it was derived using the fundamental calculus. Unfortunately for the small geometries in today most of the assumptions that hold the derivation base untrue. As a result the methodology of the V_{ov} no longer yields as expected circuits. To safeguard the design, developers have attempted to adjust it with short-channel effects (and sometimes just desirable) based on different physical arguments. But V_{ov} design ultimately only gets tougher and less effective.

The validity of the long-channel model does not depend on our current strategy, g_m/I_D based. It doesn't actually depend on anything except simulation to be valid. This is a lookup table-based methodology.The philosophy underlying this is that the equations of MOSFETs are so difficult that a few tables or charts need to be in favour. And as the graphs are generated using Spice device simulations, they are much more consistent than the long channel model would ever expect.

For $V_{ov} = 0, I_D = 0$, it is possibly predicted by the long channel model that we must never bias a MOSFET close to V_T as it may turn it off. However, the g_m/I_D value continues to ascend as we enter the sub threshold region, which is a helpful point of bias.

Subthreshold transistors are slow, but consider the fact they are not slow in modern techniques. In reality, the sub threshold and weak inversion regions are particularly essential in low-power design. Indeed, they can often be much quicker than usual to allow designers to trade some of this speed for low power. For many power constraints in today's models, the operation of a sub threshold is essential.

Even though the design variable V_{ov} is very good in theory, in reality it does not work. When the long channel model was perfect, V_{ov}'s design was brilliant and there is no cause to look elsewhere. However, the model on a long channel does not operate and so we need a unique variable something in the V_{ov} spirit but better convergence between hand calculations and simulation.

Mallya, S., & Nevin, J. H. (1989). Design procedures for a fully differential folded-cascode CMOS operational amplifier. IEEE Journal of Solid-State Circuits

The analysis of a differential cascode operational amplifier is discussed and the results are executed in the form of design equations and processes.Trade-offs are made between specifications like bandwidth, gain, phase margin, bias currents, signal swing, slew rate and power. Expressions in a closed form are created and a process of design steps is set. A graphic repre-

sentation of the characteristics between gain, power and phase margin is obtained for various capacitive loads to demonstrate one way of optimizing design. The findings of SPICE simulations are very much in line with the use of our design equations.

This article discusses the need for comparatively unexperienced analog integrated circuit engineers to be able to design complicated analog building blocks in reasonable efficiency. An attempt has been created to formalize by designing design equations and procedure to help in this process for a fully differential folded-cascode amplifier for switched-capacitor applications. The Op amp has to meet op amp properties or specifications. These properties often conflict and are highly susceptible to differences in processes. The procedures described in this report indicate how these performance requirements can be effectively fulfilled and at the same moment maintain adequate protection.

Hadri, S., & Leung, B. (1993). Impedance boosting techniques based on BiCMOS technology. IEEE Journal of Solid-State Circuits

A method of impedance improvement is provided, based on a combination of bipolar and MOS. The method utilizes negative feedback to increase a Cascode Circuit's impedance level. By the loop gain of the feedback loop, this method increases the gain of the conventional BiCMOS folded cascode amplifier. The BiCMOS impedance enhancement circuit provides a greater bandwidth and a greater output current range compared with the CMOS version.

The rate and efficiency of mixed analog-digital devices such as switched

capacitator filters and AD converters with high performance are primarily determined by the setting time and dc gain respectively of the operational amplifiers. The design should combine high dc gain and high unitygain bandwidth together with a single pole system performance to optimize the op amp design for high speed and accuracy. The folded casecode is appropriate for applications with a high frequency where the op amp drives small capacitive loads.

However, in order to achieve high dc gains it is required to use large input units or triple cascode stages that brings additional poles which degrades the phase margin. This reduces the gain bandwidth product. By shifting the non-dominant pole to higher frequencies by reducing parasite capacitances and increasing transconductance g_m in the BJT than MOS devices, bipolar cascode enhances the unitygain bandwidth. Negative feedback has been used to enhance output resistance.

N-folded cascode technique for high frequency operation of low voltage op amps S. Setty ; C. Toumazou Electronics LettersYear: 1996 Volume: 32, Issue: 11 Journal Article Publisher: IET

A method to improve the high frequency operation of a low-voltage folded cascode structure with a zero at the nondominant pole position and phase compensation is provided. The method can be used to create low voltage op amp bandwidth and no overhead amplifiers for power consumption.The results are achieved for two folded cascode operational amplifiers simulated with and without the cascode transistor feed forward connection. The Opamp architectures are based on the single stage and differential amplifier.

Gulati, K., & Hae-Seung Lee. (1998). A high-swing CMOS telescopic operational amplifier. IEEE Journal of Solid-State Circuits

By utilizing tail and current source transistors in the deep linear region, the improvement in the swing of the op-amp is accomplished. By applying a differential gain improvement and a replica-tail feedback method compensates for the resulting degradation of differential gain, common-mode rejection ratios (CMRR) and other amplifier characteristics. Increasing the op-amp swing contributes to an overall enhancement in performance that can be used to achieve lower power or greater SNR or speed.

The op-amp output swing becomes an highly critical parameter with supply voltages increasingly restricted. Although the telescopic architecture has a very low output swing, achieving high rate and power consumption, this design associates the telescopic architecture's high-speed, low-power aspect with the highly swinging capacity of the folded cascode with a two stage configuration, with high common mode and supply rejection and steady efficiency parameters.These methods may also be used to enhance the performance of certain other topologies. An amplifier with an output swing of 2.45 V at 3.3 V, an unitygain frequency of 90 MHz and power consumption of 4.8 mW at a capacitive load of 3.6 pF and 50 dB of CMRR, have been experimentally proved. We showed that the amplifier retains its high CMRR even at high speeds, qualitatively and by simulation. This op-amp provides an alternative to standard topologies given the declining supply voltages.

Roewer, F., & Kleine, U. (2002). A novel class of complementary folded-cascode opamps for low voltage. IEEE Journal of Solid-State Circuits

Many analog signal processing algorithms with signals that has megahertz range. VLSI chips are mostly equipped with one-stage OTAs, which can be easily adjusted to the particular implementation. The high bandwidth of these opamps is due to minimum internal nodes. By changing the output cascode transistor gate voltages near to the power supply voltages, the output swing is increased

Harrison, R. R., & Charles, C. (2003). A low-power low-noise cmos for amplifier neural recording applications. IEEE Journal of Solid-State Circuits

Researchers and clinicians need low-noise biosignal amplifiers to amplify signals in the millihertz to kilohertz range, while rejecting large dc offsets produced at the electrode-tissue interface. A new bio-amplifier that utilizes a MOS-bipolar pseudoresistor element in which low-frequency signaling is amplified to the millihertz range and large dc offsets are refused. DC offsets with 1-2 V are prevalent across differential recording electrodes due to electro-chemical influences at the electrode-tissue interface. When recorded, typical potentials or spikes of neural action have amplitudes of up to 500 V with 100-Hz to 7 KHz band, while local field potentials with amplitudes as high as 5 mV can contain signal energy below 1 Hz. amplitudes are available. Some recent VLSI bioamplifier concepts are using nanofarad off-chip capacitors to achieve a low-frequency cutoff, which passes the LFP signals and rejects big dc offsets.

Johnson, B., & Molnar, A. (2013). An Orthogonal Current-Reuse Amplifier for MultiChannel Sensing. IEEE Journal of Solid-State Circuits

By stacking the differential input pairs of four amplifiers, the submitted circuit uses current reuse. For the differential pairs of the following channel, the output drain current of each channel's differentiation pair is used as the tail currents. Orthogonal current reuse improves tradeoff between noise and power by using bias devices for headroom conservation. There are 16 single output currents (2n) with (n = 4) four channels , which is a linear combination of four inputs. Reconstruction of enlarged versions of the initial input signals involves adequately combining the small output currents in the output steps with much reduced biasing currents.

Using a combination of subthreshold design for maximum g_m ratio, folded cascodes for small current folds or g_m boosting with current splitting, state-of - the-art energy effective amplifiers try to minimize the power and thermal noise. Additional methods for formula boost include additional device inputs. Neural signals have a comparatively low frequency spectral energy limit varying from 300 Hz to 6 kHz with action potentials, and under 300 Hz with regard to LFP. For 1/f noise, energy-efficient amplifiers must also be optimized with large input or chopping equipment.

The primary objective of efficient design was to maximize the transconductance of the amplifier for a particular bias current. The observation that the noise quality is influenced by the differtial input pair of the amplifier. Therefore, the input pair should consume the more of bias current while subsequent circuits are biased at a much reduced current.Given that

the voltage headroom needed for an input pair with subthreshold bias is limited, amplifiers with self-stacked subthreshold input can function without affecting noise with low voltage supplies.

Orthogonal current-reuse uses a input stacking to raise differential amplifier g_m proportional to the total of stacked differential input pairs. As only one $V_{DS}$of voltage Headroom is necessary for each differential pair, g_m growth takes place at a low voltage price. Orthogonal reuse of the current in two channel design for the input of the second channel to be divided into two equal sized differential pairs using the first channel drain currents as tail currents.Channel two differential pairs are independent but efficiently parallel because they have same inputs. In addition, the DC current is divided equally ($I_{bias}/2$), meaning that the g_m of the two pairs are equivalent. Since the current by channel one is the sum of the current through the two channel pairs, the g_m of the both channels is identical.In order to achieve same operating points and noise perforance, the efficient widths of both channels are identical. The active loads at the bottom of the stack are intended to sink one fourth of total current. By placing more differential pairs, orthogonal current reuse can accomodate various signal channels with the same g_m amplifier, improving the performance of the amplifiers further.

Song, S., Rooijakkers, M., Harpe, P., Rabotti, C., Mischi, M., van Roermund, A. H. M., & Cantatore, E. (2015). A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring With a 1.41 Power Efficiency Factor. IEEE Transactions on Biomedical Circuits and Systems

The frontend amplifier describes biomedical acquisition system's noise

level. It usually uses capacitive feedback to define the accurate gain of the feedback components without introducing noise. The present domain's power optimization of the front amplifier for improved effectiveness is becoming more and more hard, while voltage optimization can still attain substantial savings. This is because there are small signal swings the input and output signal of the front amplifier, thereby reducing the supply voltage aggressively. This allows more than one amp between the rails, which allows the reuse of the current between various channels.

The low voltage amplifier enables the individual noise level in each channel to be tuned.Thus, in fetal ECG system, it reduces power consumption compared to the stacked multichannel amplifier. The suggested cascode topology for a low-voltage current-reuse allows for an input voltage of 0.3V in the input and 0.6V in the output section, which reduces power usage significantly.The aggressive scaled input supply in the input stage is achieved using appropriate biases for the input devices and the bulk bias of PMOS systems The power management circuit is developed and optimized for high performance voltage conversion.

Shen, L., Lu, N., & Sun, N. (2018). A 1V 0.25μW Inverter Stacking Amplifier With 1.07 Noise Efficiency Factor. IEEE Journal of Solid-State Circuits

A fundamental noise-power tradeoff exists. Therefore, in order to remove noise below a certain target, a sufficient amount of power must be consumed. Furthermore, technology scaling does not decline the amplifier power , as it is not technology limited but noise limited. As a consequence, the front-end amplifier generally occupies a substantial part of the system power budget for low-noise sensor applications. Thus, the

development of conception techniques that can relax that close noise and power compromise is highly desirable.For a broad range of power-and energy-controlled applications, reducing amplifier power while maintaining the same amount of noise is crucial.The objective is to decrease the amplifier's power noise product. The amplifier power can therefore be reduced at the same noise or the amplifier noise can be kept to a minimum with the same power. These two scenarios can be changed.

The basic idea is to improve the overall transconductance g_m of the amplifier, without increasing the current I_D. Input transistors in a weak inversion are biased to maximize their g_m/I_D by classic design techniques. A pair of PMOS inputs could be stacked on top of an input pair of NMOS in order to build an inverter-based input stage, which doubles the total amplifier g_m without any further current.It achieves a 2N time current reuse for a single channel input by stacking N inverters vertically. It only combines output branches of N, so that the exponential dependence becomes a moderate linear dependence.This reduces circuit power and increases the overall power efficiency of the amplifier.

Chapter 3

Working Model

Depending on the type of application, the design of an operational amplifier must specify its specifications. The designer selects the appropriate opamp architecture to meet these requirements. In this chapter, we talk about some of the specifications of operating amplifiers that are important for amplifier design.

3.1 Op Amp Characteristics

An opamp's performance is characterized by the specifications and takes the non-ideal impacts into consideration that restrict the performance. Although an opamp can most often be characterized by many specifications, some of these specifications are only required for the design of an opamp.The opamp design specifications of Amplifier may be specified as follows:

1. Gain
2. ICMR
3. Output Swing
4. Unity Gain Bandwidth

5. Phase Margin

6. PSRR

7. Equivalent Input Noise

These specification allows the designer to determine which type of opamp architecture is appropriate and will be briefly discussed in the following sections.

3.1.1 Gain

The gain in any CMOS topology is described as the product of input stage transconductance g_m and output stage resistance R_{out} which is expressed as

$$A_v = g_m * R_{out}$$

Opamp gain is based on the frequency of the input signal and rolls out quickly at greater frequencies because of poles created by parasite capacitances. The closed loop gain of the amplifier becomes insensitive to the gain of the opamp when a negative feedback is used in opamp. The feedback usually made from passive components then describes the amplifier's closed loop gain

3.1.2 Input Common Mode Range

The ICMR defines the input voltage range over which the amplifier reacts properly to small input differential signals. The ICMR depends on the input stage type, i.e. a differential N channel pair with a differential P channel input pair. ICMR of the input stage, as shown in fig. 3.1, with

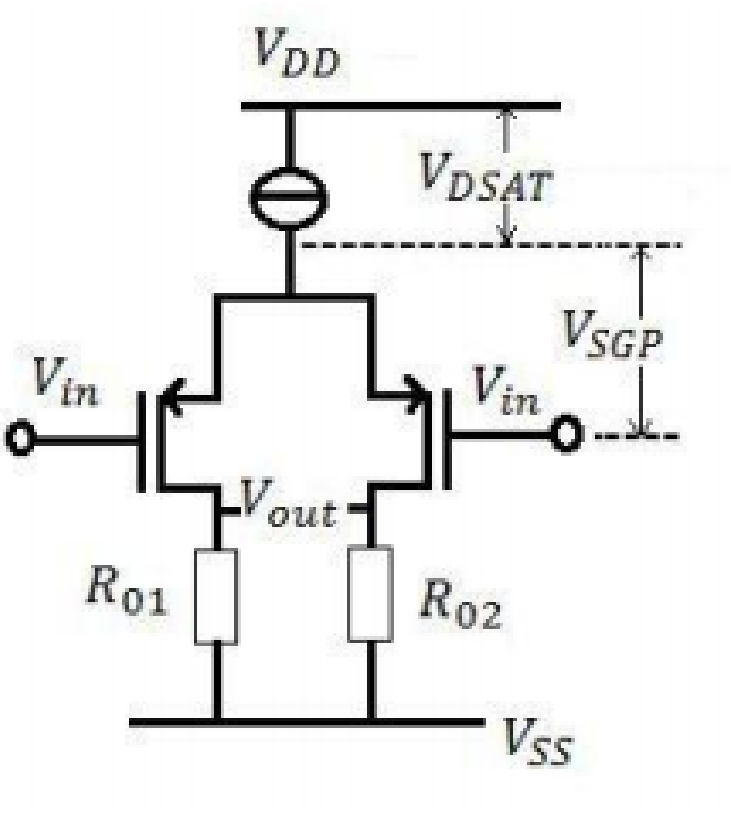

Figure 3.1: P channel Differential Input Stage

P channel differential input transistors may be expressed as

$$V_{SS} < V_{common} < V_{DD} - V_{DSAT} - V_{SGP}$$

where V_{common} is the common-mode input voltage, V_{DSAT} is the voltage across the current mirror, V_{SGP} is the source-gate voltage of an input transistor and V_{SS} and V_{DD} are the negative and positive supplies respectively.

3.1.3 Output Voltage Swing

The output stage type in an amplifier specifies the voltage swing of the output. The larger the transistor stacks in the output stage, the lower the output swing. The output swing of an opamp is generally the sum

of stacked transistors V_{DSAT} minus V_{DD} and expressed as

$$V_{DD} - \sum V_{DSAT}$$

3.1.4 Unity Gain Bandwidth and Phase Margin

The frequency response in an opamp are related to these two parameters.The Unity Gain Bandwidth,f_u, also known as Gain Bandwidth Product, specifies the unity or 0dB frequency for an opamp's open-loop gain. The phase margin specifies the stability of an opamp and is the difference between the phase shift in an operating signal through opamp's unity gain. The phase margin may be expressed as;

$$PM = 180 - phase@f_u$$

3.1.5 Power Supply Rejection Ratio

Power supply rejection ratio, PSRR, is defined as the ratio of changes in power supply voltage to the changes in the output voltage

3.1.6 Equivalent Input Noise

Due to multiple sources, noise may be present in an opamp. Noise is normally referred to input by dividing the output noise to the amplifier gain and thus called the equivalent noise input. Noise is generally indicated between 100 Hz to 10 KHz bandwidth.

3.2 Opamp Topologies

The choice of the correct opamp topology depends primarily on the opamp specifications. Some of the merits and demerits of those topologies leading to the decision on the appropriate opamp topology are briefly outlined here.

3.2.1 Telescopic opamp Topology

The opamp architecture shown in figure 3.2 severely restricts the prevalent ICMR with stacked transistor(M5-M8) positioned at the top of the input differential pair.It provides high PSRR and has internal compensation.

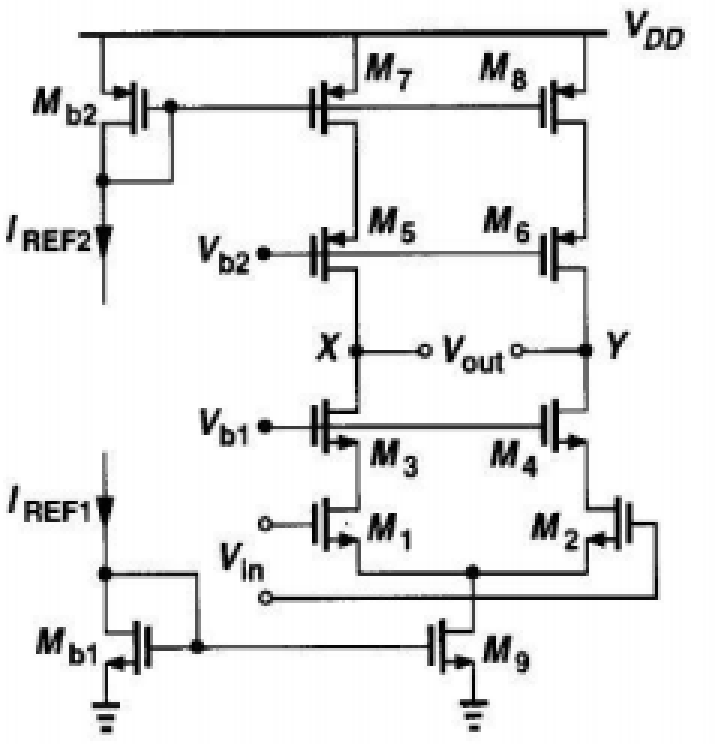

Figure 3.2: Fully Differential Telescopic Operational Amplifier

3.2.2 Folded cascode opamp topology

The stacked transistors (M3-M6 and M7-M10) limits the output voltage swing in the folded cascode stage.Opamp architecture, as shown in the fig 3.3 provides high PSRR and has internal compensation.

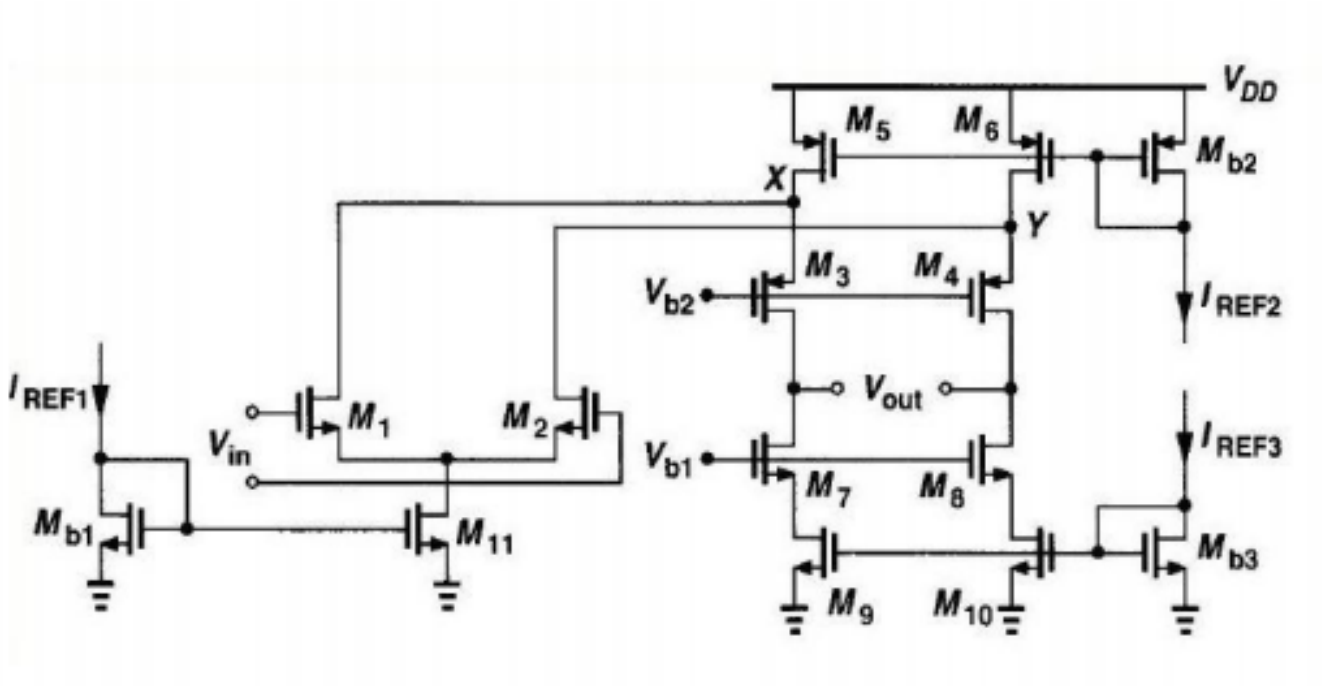

Figure 3.3: Fully Differential Folded Cascode Operational Amplifier

3.2.3 Two Stage Topology

As in figure 3.4, the two-stage opamp architecture is quite compact and offers a reasonable gain and has large swing in input and output voltages with less power consumption. There is no inner compensation, however, and poor PSRR is provided.

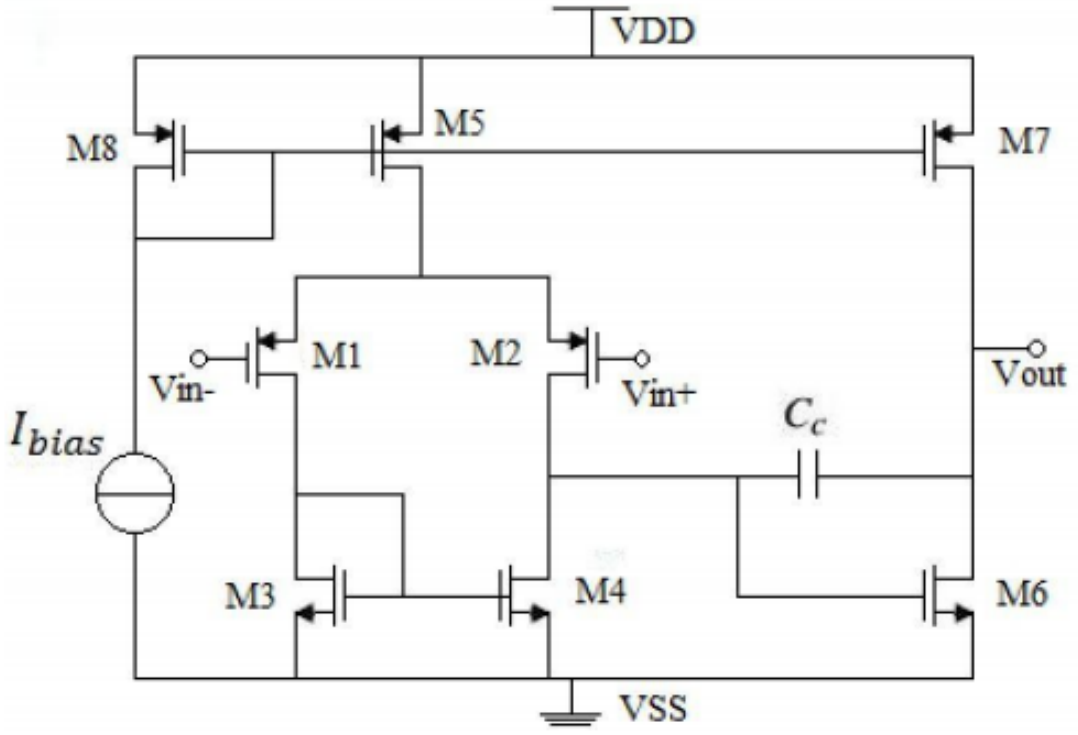

Figure 3.4: Two Stage Operational Amplifier

3.3 Technology characterization using g_m/I_D method

The standard analog design approach is based on long length channel equations and is a main design parameter for V_{ov}(over drive voltage).The V_{ov} describes the MOS transistor operating regions. In order to compromise a common source amplifier's bandwidth and power usage, V_{ov} has to be decreased, resulting in increased transistor sizes. The following equation shows how transistor size is related to V_{ov}.

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{ov}}$$

The above equation shows that lower V_{ov} values lead to a bigger device and thus a larger C_{gs} for fixed values of g_m and L. From this situation, it can be concluded that V_ov is not a good design parameter.

3.4 Performance Metric of Interests

1. Transit Frequency, $f_t = \frac{g_m}{2\pi C_{gs}}$
2. Trans-conductance Efficiency, $\frac{g_m}{I_D} = \frac{3\mu V_{ov}}{2L^2}$
3. Intrinsic Gain, $\frac{g_m}{g_{ds}} = \frac{2}{\lambda V_{ov}}$

3.5 Technology Characterization

The g_m/I_D approach produces the corresponding characteristic curves for each of the above described performance parameters. The following curves can therefore be categorized as:
Intrinsic Gain $\rightarrow \mathrm{g}_m/\mathrm{g}_{ds} versus \mathrm{g}_m/I_D$
Transconductance Efficiency $\rightarrow g_m/\ I_D$ versus $I_D/$ (W/L)
Transit Frequency $\rightarrow f_t$ versus $g_m/\ I_D$
These curves provide for a number of ways to determine the size of a transistor with regard to performance parameters. For all transistors of the same kind (e.g. PMOS or NMOS) in a certain technology, the g_m/i_d and $I_D/$(W L) relation is a unique characteristic. During the design stage to determine the transistor size, this unique characteristic can be used. The ratio W/L is determined by indicating a drain current from current usage and the g_m/I_D ratio is determined on the basis of the transistor operating region or by the specifications.

The 2 stage opamp design normally provides a g_m/I_D ratio from the specifications for gain bandwidth, whereas a transistor drain current can be determined based on current consumption requirements.

3.6 g_m/I_D vs I_D/(W/L) Curve Generation

Figure 3.5 demonstrates a typical g_m/I_D vs $I_D/(W/L)$ curve, in which three operating regions can be recognized: weak inversion, moderate inversion, and strong inversion.

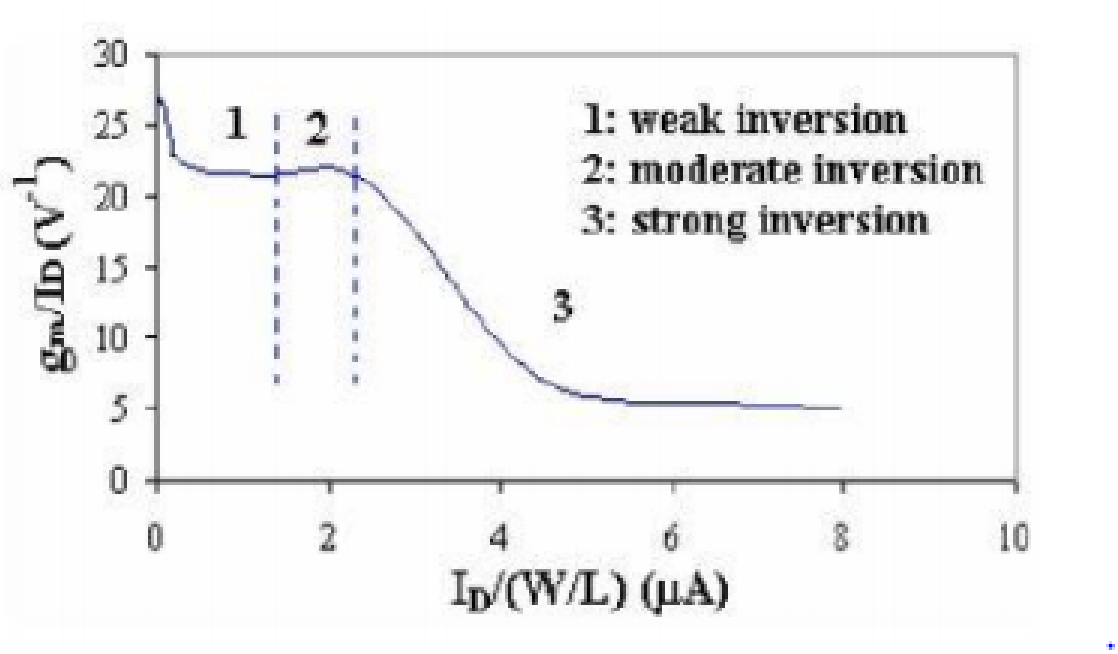

Figure 3.5: g_m/I_D vs I_D/(W/L) Curve

But g_m/I_D vs V_{GS} and I_D/(W/L) vs. V_{GS} curves can be plotted to select the operating areas. The V_{GS} values define the operating region and the values of both g_m/I_D and I_D/(W/L) can be established for the selected values of V_{GS}, which can then be used to detect the size of the transistor.To generate these curves, two distinct schematics have been set up for an NMOS and a PMOS technology transistor, in which a varying voltage source is connected between the gate and source as shown.

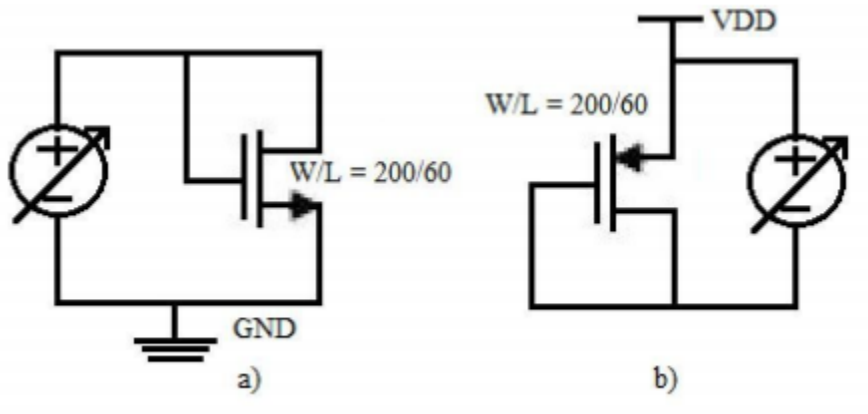

Figure 3.6: a) NMOS transistor b) PMOS transistor

The schematic is then set up through DC analysis, where the value of V_{GS} voltage for both transistors is swung from 0 to 1V. Following the DC analysis, the op calculator function lists transistor's operating point parameters, by choosing the corresponding transistor from the diagram.These parameters include intrinsic capacitances, transconductance, DC currents and voltages, and so forth. Op parameter selection imports their values into the calculator's workspace through the entire DC sweep where the expressions can be formed which can be plotted.The results of these DC simulations are shown in the following figures and are manipulated in the form of necessary characteristic curves.

3.7 Important Features of g_m/I_D Method

- It allows the designer to choose any operating region as the curves are continuous and there is no transition from region to region. This technique is also accurate, as the curves are unique and independent of transistor size for a specific technology.

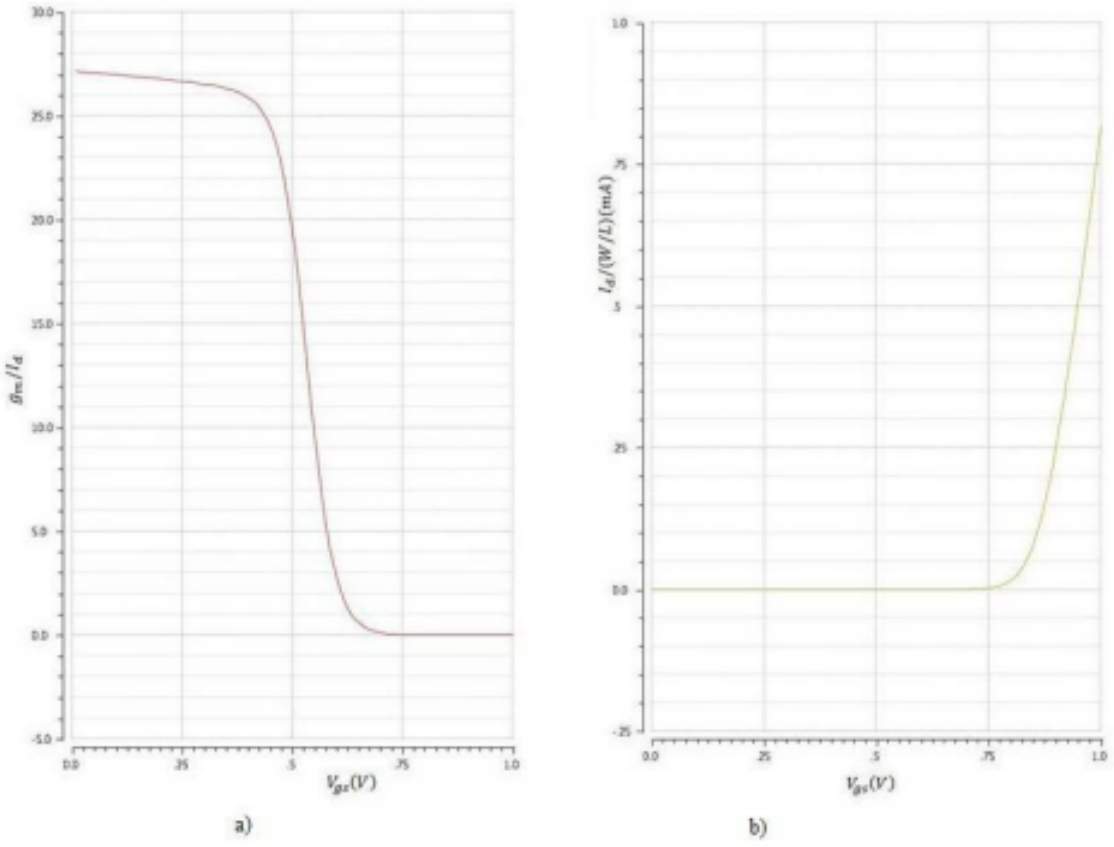

Figure 3.7: g_m/I_D curves for PMOS a)g_m/I_D versus V_{GS} b) g_m/I_D versus I_D/(W/L)

- This approach enables the designer to conclude significant design tradeoff between bandwidth, gain and power usages, etc. The level of the transistor inversion can also be selected.
- A family of characteristic curves for a particular technology of analog circuit like a two stage opamp can be split into smaller parts. Then, depending on large signals and small signal requirements the transistor size of these components can be found comfortably.
- The iterative design process needed by a complicated analog circuit can be decreased considerably once the technique is thoroughly characterized.

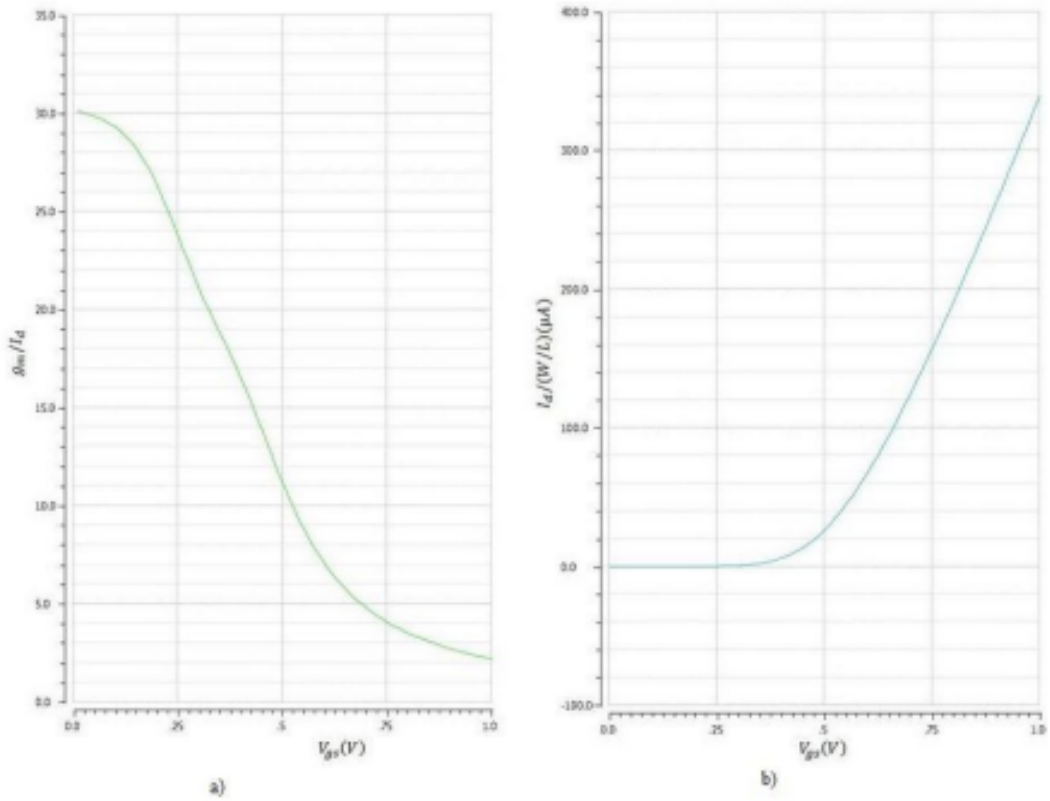

Figure 3.8: g_m/I_D curves for NMOS a)g_m/I_D versus V_{GS} b) g_m/I_D versus I_D/(W/L)

Chapter 4

Simulation Results

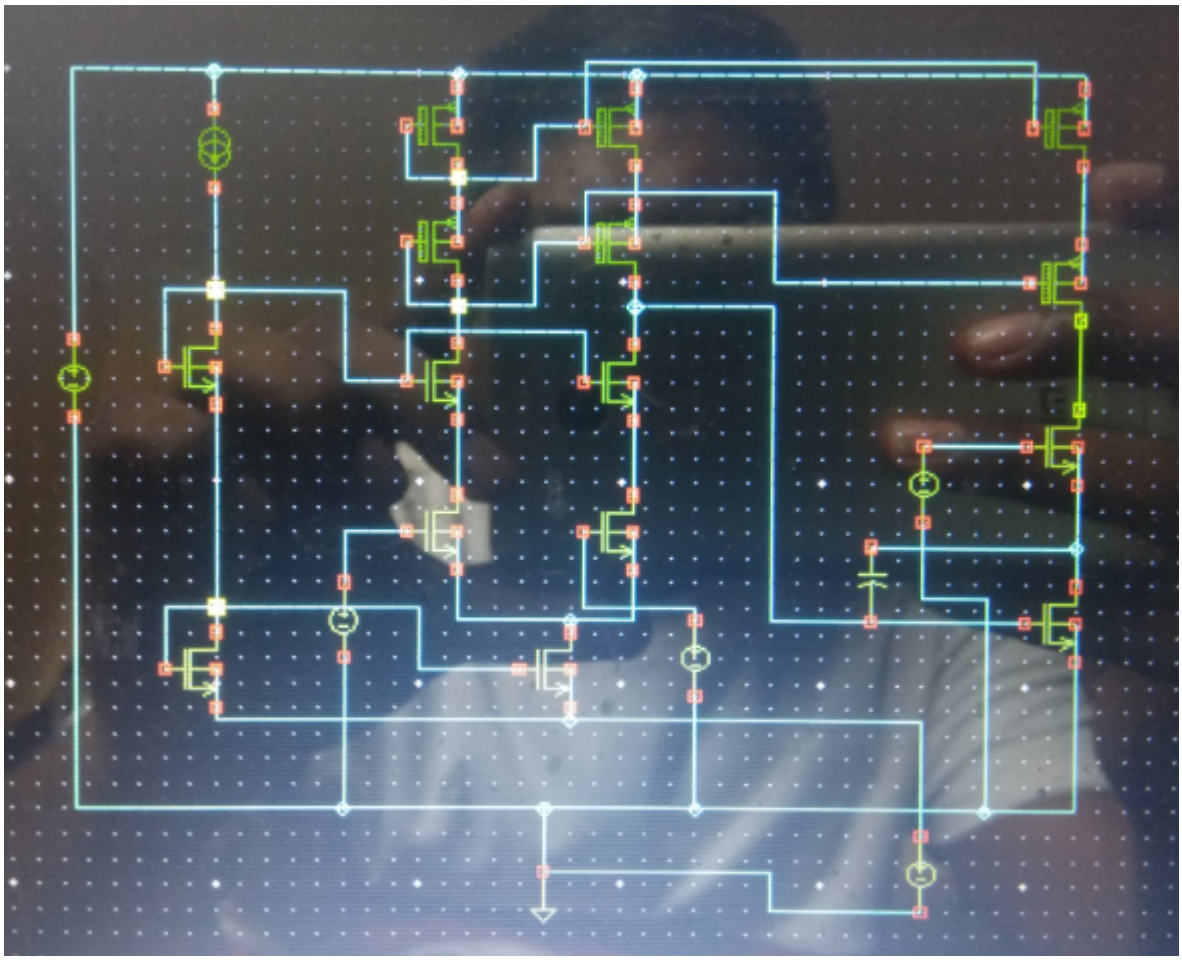

Figure 4.1: Self Biased Cascode OPAMP

The above Op Amp is expected to have large DC gain with large

bandwidth by using g_m/I_D methodology. The input resistance of the circuit will be very high and the input capacitance will be very low when compared with the other opamps. The opamp consists of two stages. The above circuit has self biased current mirrors which acts as current sources in the first stage of the opamp which is a cascode differential amplifier. And the second stage is the cascode amplifier. In this circuit,a compensation capacitor is also been used to compensate the poles properly .It contains two zeros and four poles. The poles are well adjusted in such a way that the opamp is also suitable for closed loop configuration. The opamp has been checked under different processes at different temperatures. As the output resistance of the opamp is same as the cascode amplifier output resistance, a buffer should be used if the opamp has to deal with heavy load.

- 180nm SCL technology is used
- VDD=1.8
- VSS=-1.8
- Gain=71dB
- Power Dissipiation=7.2 μW
- Bandwidth=5KHz
- UnityGain Bandwidth=8MHz

The following figures shows the frequency response of different processes at different temperatures.

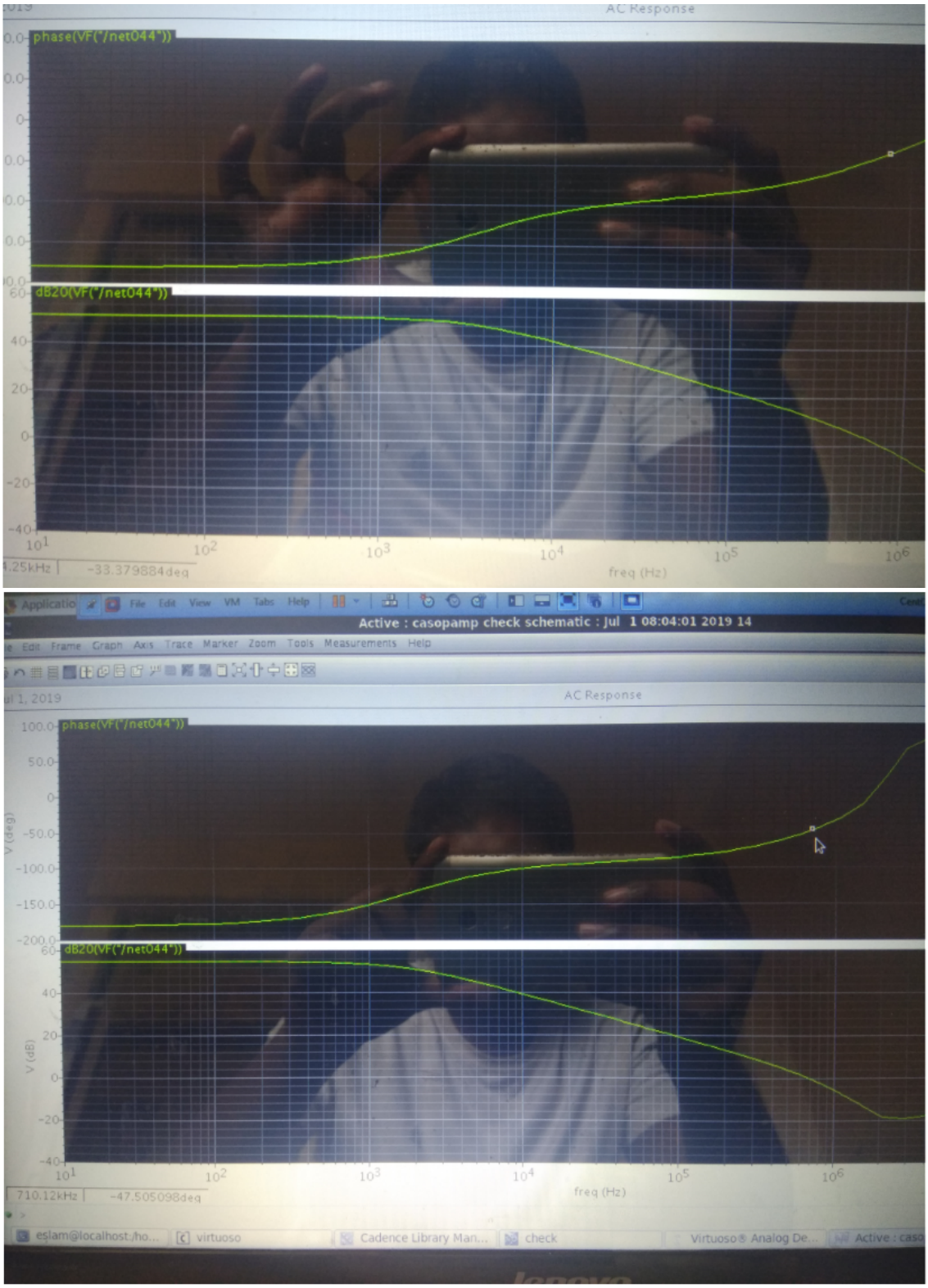

Figure 4.2: tt process at -20 & 0 degree celcius

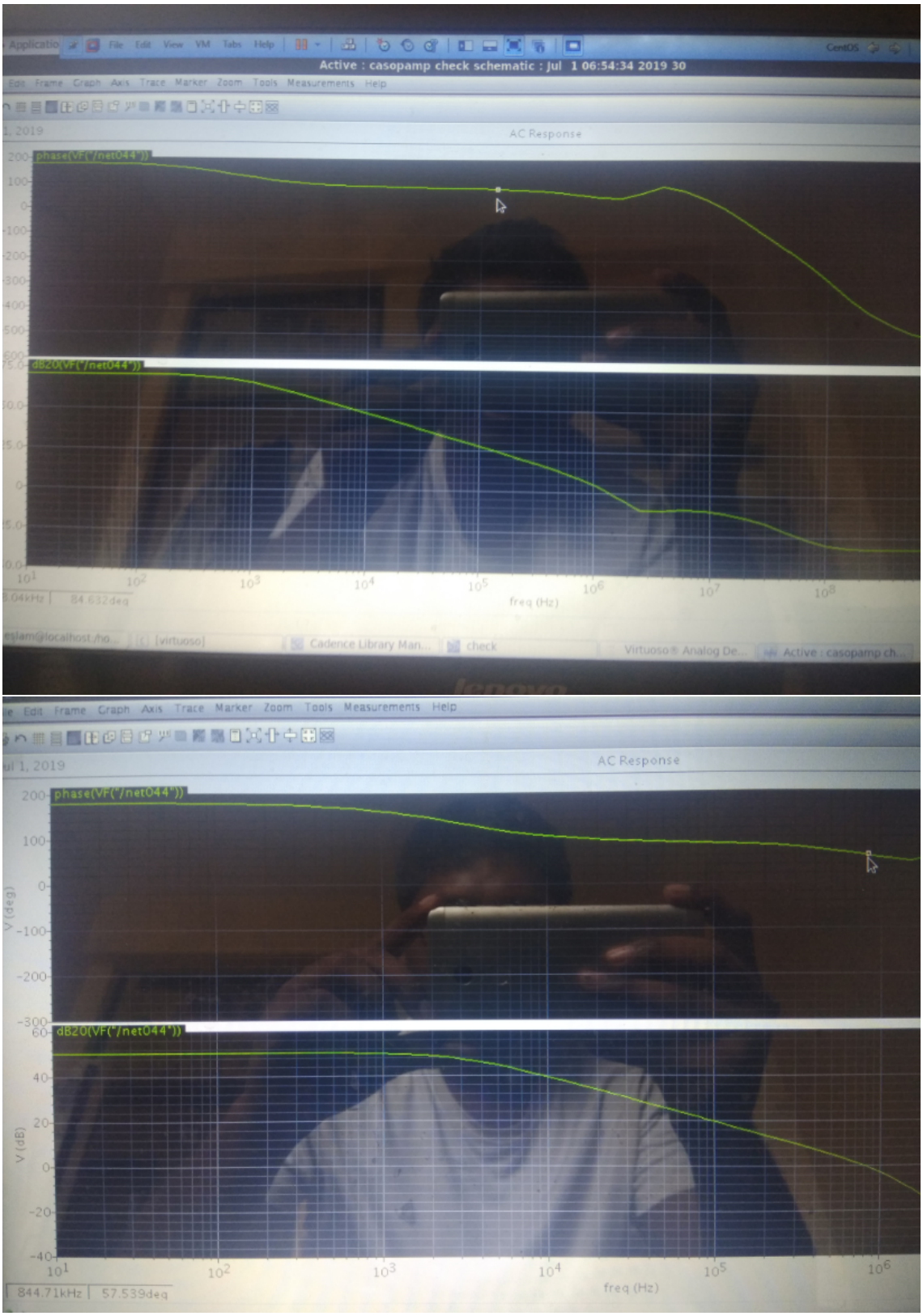

Figure 4.3: tt process at 27 & 50 degree celcius

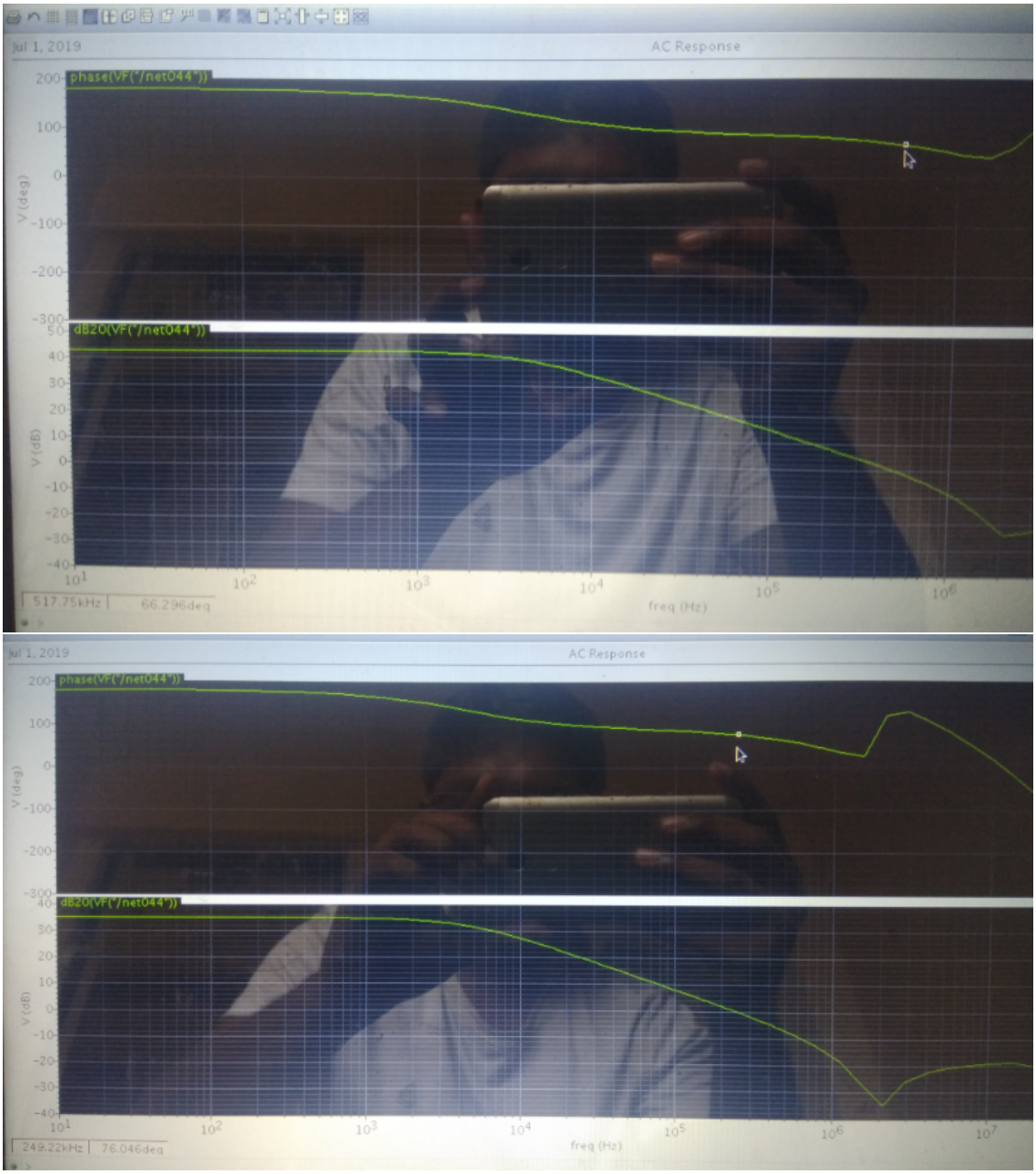

Figure 4.4: tt process at 80 & 150 degree celcius

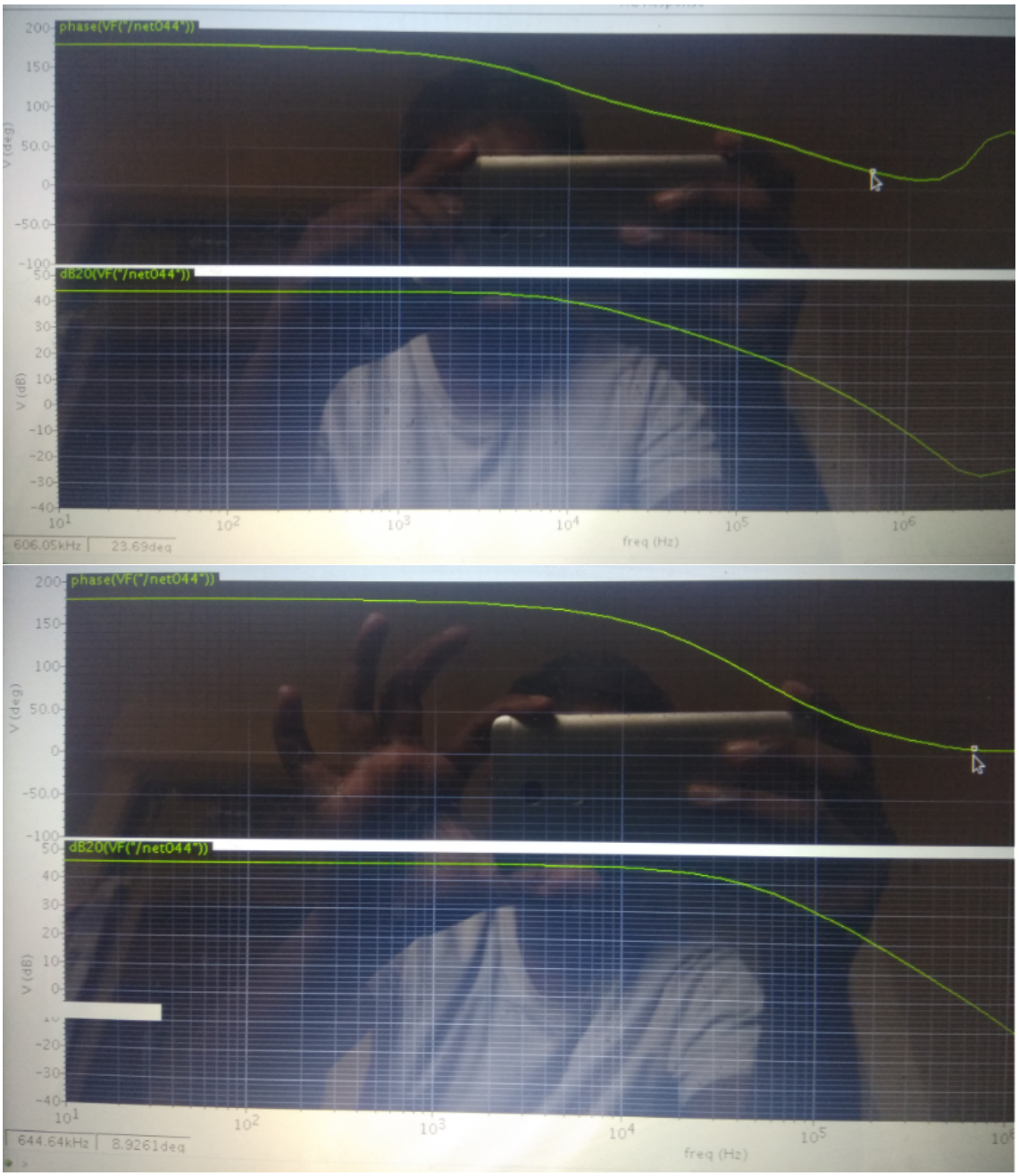

Figure 4.5: ss process at -20 & 0 degree celcius

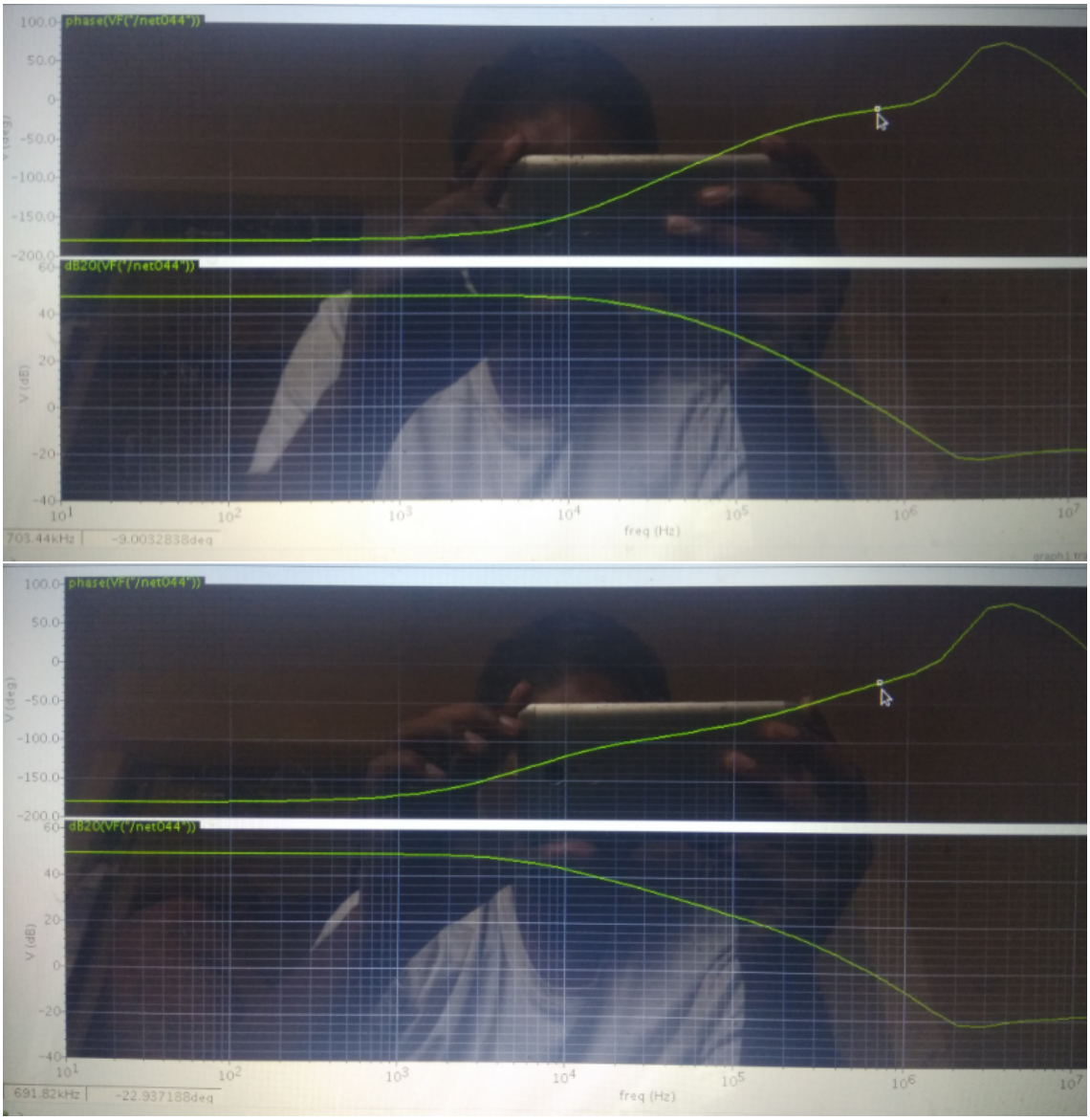

Figure 4.6: ss process at 27 & 50 degree celcius

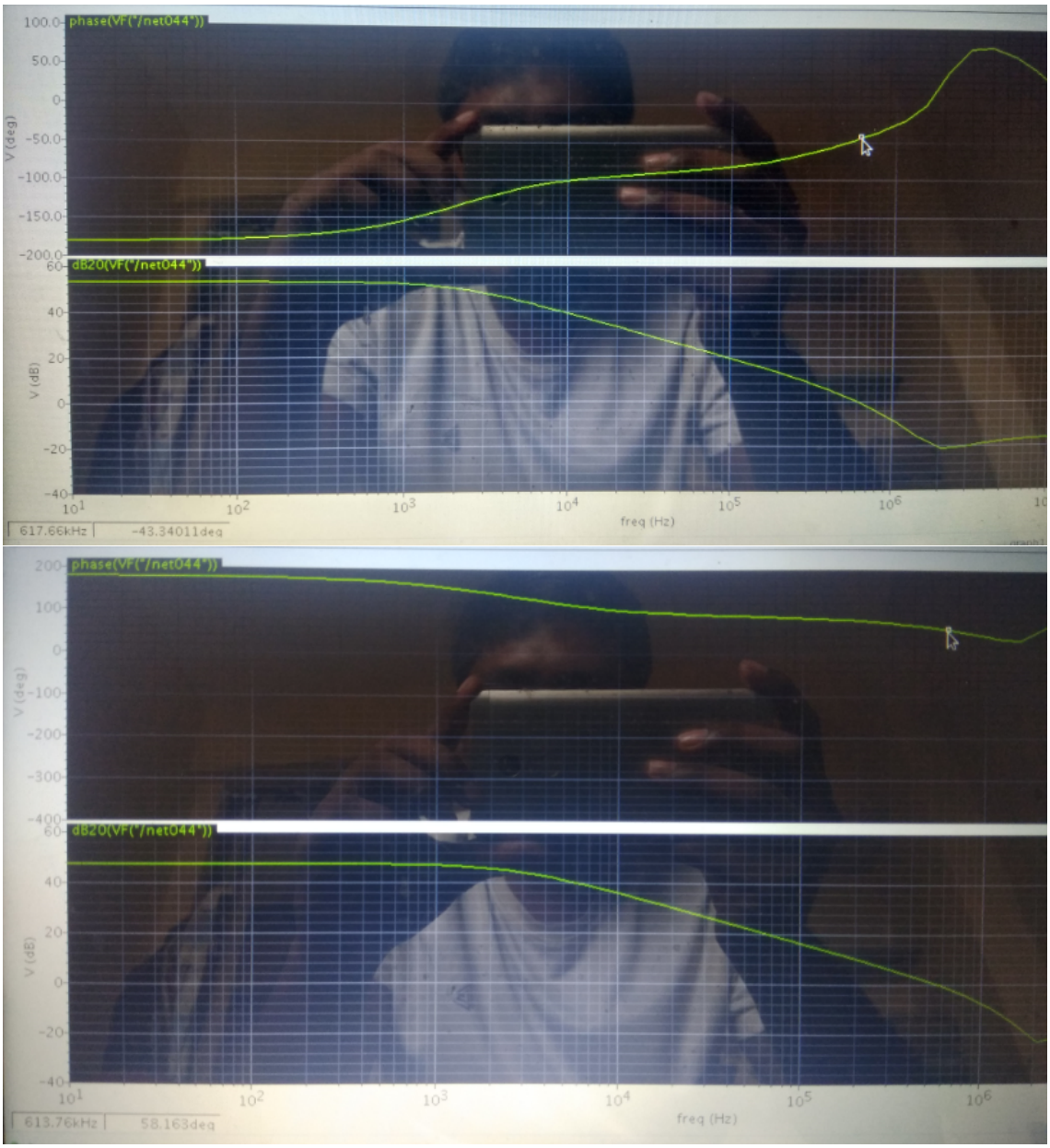

Figure 4.7: ss process at 80 & 150 degree celcius

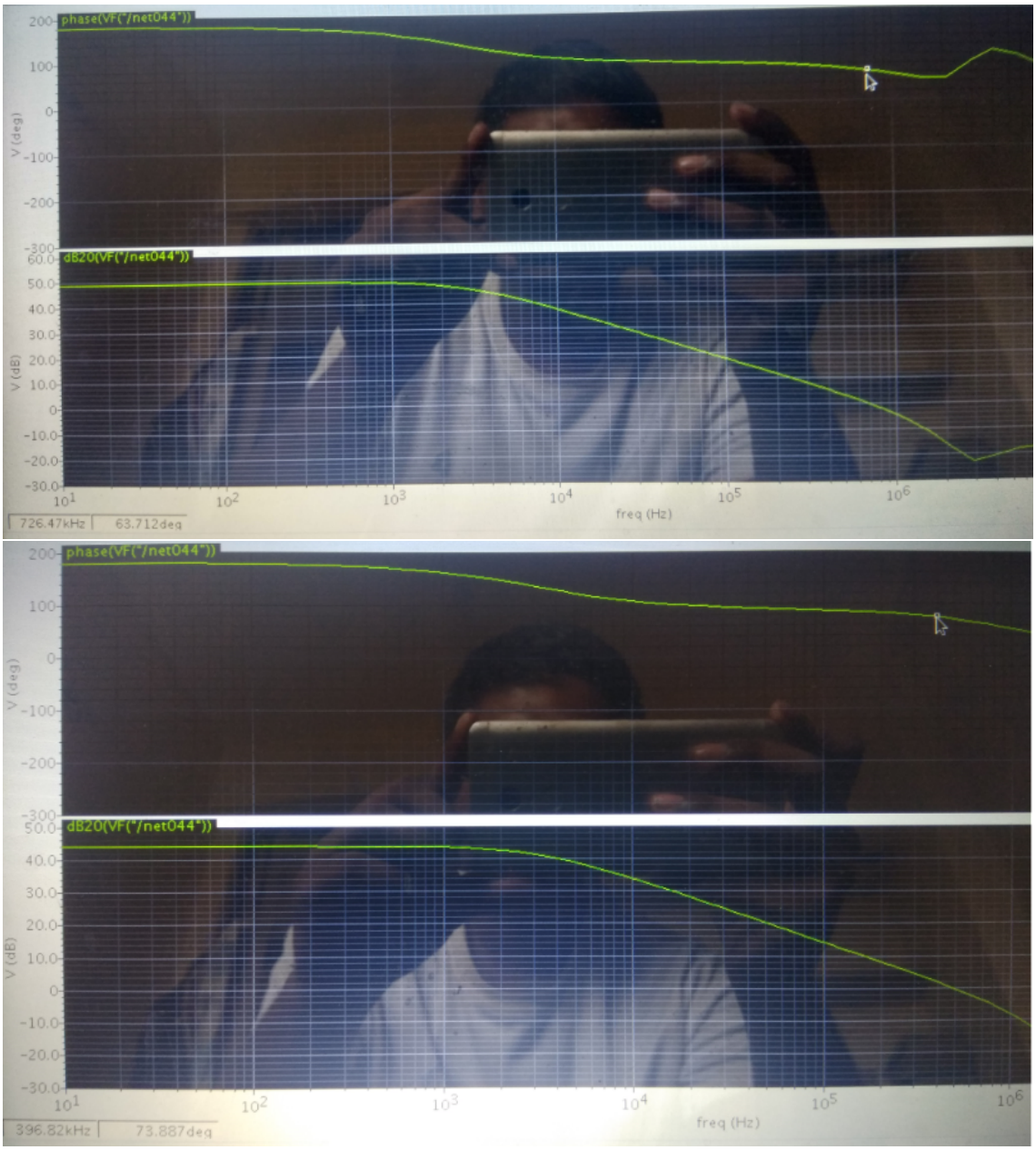

Figure 4.8: ff process at -20 & 0 degree celcius

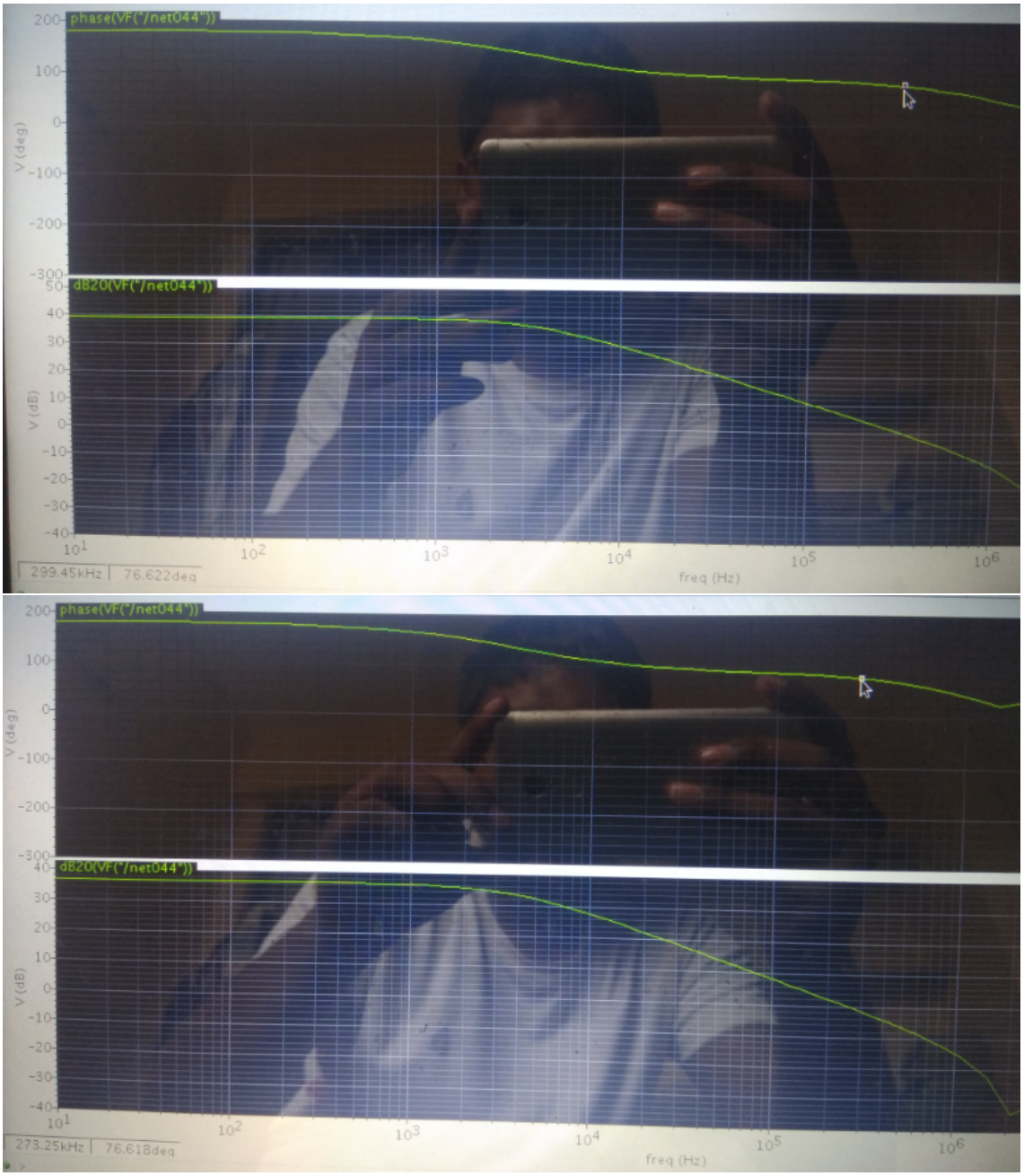

Figure 4.9: ff process at 27 & 50 degree celcius

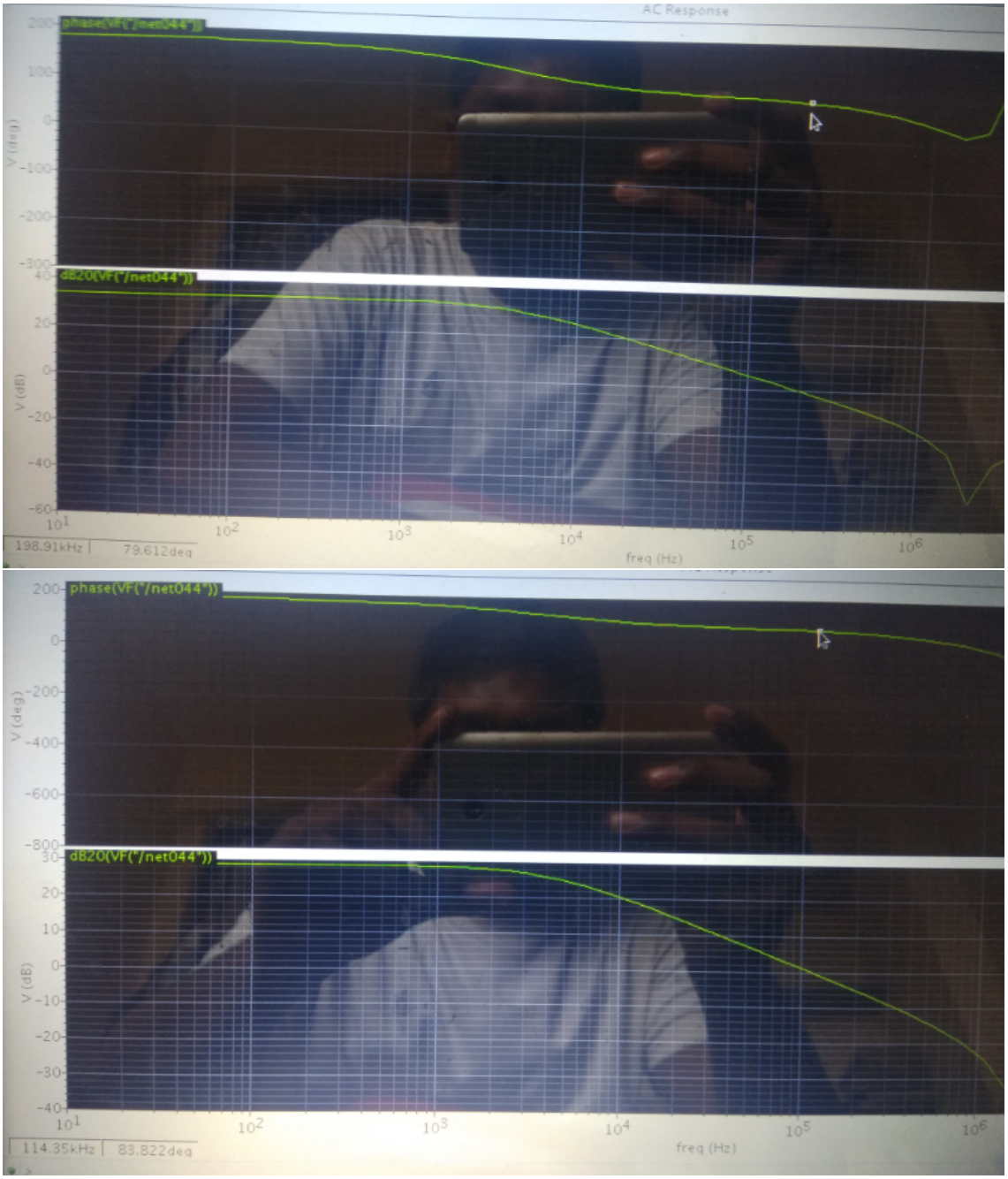

Figure 4.10: ff process at 27 & 50 degree celcius

Chapter 5

Conclusions and Future Work

5.1 Conclusions

- The thesis work primarily focuses on the design of high gain cascode operational amplifier using g_m/I_D method.
- The comprehensive simulations assist us to achieve the amplifier requirements. To fulfill these specifications, a well designed transistor level amplifier is must.
- Design illustration of the short channel design technique using the g_m/I_D method for analog transistor design.
- For various opamp configurations, a structured design approach is introduced to design complicated analog structures by dividing them into its small components and designing each component using the g_m/I_D procedure.
- A two-stage amplifier with frequency compensation techniques like the Miller capacitor is designed to achieve high-bandwidth specifications.

5.2 Future Works

- In the design of the amplifiers for the proposed on-chip implementation, the g_m/I_D techniques can be increased.
- A procedure for using a device operating in the linear region in the g_m/I_D technique requires to be investigated for implementing the null resistor.
- It requires designing a bias circuit, regardless of temperature changes and other aspects.
- The effects of slewing of the pulse input to the analog front-end amplifiers also need to be studied.

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