A

DISSERTATION REPORT

ON

System Monitoring Tool for Remote Debugging, Monitoring and Validation

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MASTER OF TECHNOLOGY IN WIRELESS AND OPTICAL COMMUNICATION

BY

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Certificate

This is to certify that the dissertation report entitled **System Monitoring Tool for Remote Debugging, Monitoring and Validation** submitted by **Monika Upadhyay (2017PWC5435)**, in the partial fulfilment of the Degree Master of Technology in **Wireless and Optical Communication** of Malaviya National Institute of Technology, is the work completed by her under our supervision, and approved for submission during academic session 2018-2019.

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Declaration

I, Monika Upadhyay, declare that this Dissertation titled as "**System Monitoring Tool for Remote Debugging, Monitoring and Validation**" and the work presented in it is my own and that, to the best of my knowledge and belief.

I confirm that the major portion of the report except the refereed works, contains no material previously published nor present a material which to be substantial extent has been accepted or the award of any other degree by university or other institute of higher learning. Wherever I used data (Theories, results) from other sources, credit has been made to that source by citing them (to the best of my knowledge). Due care has been taken in writing this thesis, errors and omissions are regretted.

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Abstract

To validate a platform developed for computers, laptops or any other electronic device from the remote location requires heavy infrastructures and ultimately cost of such infrastructure. There is always a problem of remotely flashing BIOS chip, monitoring health of the platform and controlling it through remote end. There is always a constraint for debugging the issue from a remote location and also, remote debugging capabilities are limited. So, debuggers face many limitations to debug failure if they can't physically reach the platforms. Typically, there is a critical requirement that debuggers should continuously test their codes in order to debug an issue during development process itself. But, this is unfortunate that all the developers don't sit next to platforms all the time.

In this dissertation work, we propose an architecture of remote debugging tool which helps in monitoring as well as debugging the platform from the remote end. This remote debugging tool acts as an interface between targeted platform and host machine. In our proposed tool, we are trying to develop a small add-in card which could be connected to the platform to be validated or monitored. Then, this add-in card is responsible for collection of the data from platform first and then it could send the data to remote location through servers.

In this dissertation work, we have developed the System Monitoring Tool hardware which is designed to address above mentioned problems. It gets connected to the platform on one side and to the host on the other side and is capable of collecting data from the platform and send it to host machine.

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List of Abbreviations

API	-	Application Programming Interface
BCR	-	Bar Code Reader
BOM	-	Bill of Materials
DDR	-	Double Data Rate
EMC	-	Electro Magnetic Compatibility
FTDI	-	Future Technology Devices International
GPIO	-	General Purpose Input Output
HDL	-	Hardware Descriptive Language
HSE	-	High Speed External
ICH	-	Input/Output Controller Hub
ICT	-	In-Circuit Testing
IoT	-	Internet of Things
IP	-	Internet Protocol
MCH	-	Memory Controller Hub
MCU	-	Micro Controller Unit
MISO	-	Master In Slave Out
MOSI	-	Master Out Slave In
OSE	-	Operating System Environment
PCB	-	Printed Circuit Board
PCH	-	Platform Controller Hub
PM	-	Platform
RAM	-	Random Access Memory
RFID	-	Radio Frequency Identification

RTC	-	Real Time Clock
RVP	-	Reference Validation Platform
SCLK	-	Serial Clock
SDRAM	-	Synchronous Dynamic Random Access Memory
SI	-	Signal Integrity
SMT	-	System Monitoring Tool
SoC	-	System-on-Chip
SPI	-	Serial Peripheral Interface
SS	-	Slave Select
SWD	-	Serial Wire Debug
TCP	-	Transmission Control Protocol
TPM	-	Trusted Platform Module
UART	-	Universal Asynchronous Receiver Transmitter
USB	-	Universal Serial Bus

List of Symbols

°	-	Degree
A	-	Ampere
V	-	Voltage
Oz	-	Ounce

CHAPTER 1

INTRODUCTION

1.1 Motivation

IoT is a concept introduced to connect objects in physical world to the internet. These objects can communicate with each other without or minimal human intervention. A network of such smart objects reduces human effort to do tasks and helps them to make their lives easier. The objects connected to internet have a capability to interchange information among them. Each object is associated with a unique identity such as RFID, BCR, IP address, etc. These smart objects can be mobile phones, mini-computers, etc.

By 2025, it is anticipated that the worldwide industrial IoT market will reach $933.62 billion. The range and scalability of cloud applications are two of the variables that will drive the extra development within it across all sectors. Healthcare, manufacturing, power and energy generation, transportation and logistics, gas and oil, and agriculture are the industries that are benefitted the most currently from industrial IoT solutions. It is anticipated that manufacturing sector is going to dominate in the upcoming few years [1]. The solution of IoT will help in accomplishment of following things:

1. *Management of Inventory :* In order to decrease the risk of errors in inventory management, the solutions provided by IoT prove to be very beneficial. Events will be easy to monitor throughout the supply chain, providing businesses with an extensive inventory perspective. Estimates of supplies and materials available are precise, preventing slowdowns.
2. *Management of Facility* : Condition-based maintenance is an effortless task and so sensors can be used to increase the effectiveness of facility management. Manufacturing equipment is prone to wear and tear. It's also susceptible to specific conditions. Sensors can monitor temperature, vibrations and other factors that could be leading to less than optimal operational conditions.
3. *Improved Industrial Safety :* The Internet of Things combines effectively with the analysis of big data. Key performance indicators of health and safety can thus be

monitored constantly to ensure better workplace conditions. Lagging indicators like the number of accidents can be addressed immediately.

4. *The supply chain and logistics optimization* : Real-time supply chain information will also become available through the reliance on an IoT solution. Products and supplies will be much easier to track, identifying slowdowns and inefficiencies. In a sense, plants will be connected to suppliers via the cloud. All concerned parties can trace the required information to predict issues and address inventory reductions as quickly as possible.
5. *Smart Metering* : Smart meters can monitor the consumption of resources like electricity, water, fuels, etc. Through the use of IoT sensors, manufacturers will know how much is consumed and what for. Through effective management, operational expenditure can be reduced significantly.

While a zero downtime solution is yet to be developed, industrial IoT makes it much easier to identify problems and conditions before these could contribute to massive halts in the industrial process [1].

This master thesis is related to one of the solutions provided by IoT, called as System Monitoring Tool. This tool helps in collection of data from remote location and the data collected can be helpful in some system monitoring and debugging errors as well.

1.2 Challenges

In order to validate or debug any issue on board, one needs to check every connection manually or probing signals and has to be present at the physical site. There is always a constraint for debugging the issue from a remote location. But, remote debugging capabilities are limited. So, debuggers face many limitations to debug failure if they can't physically reach the platforms. Typically, there is a critical requirement that debuggers should continuously test their codes in order to debug an issue during development process itself. But, this is unfortunate that all the developers don't sit next to platforms all the time. So, there is a requirement of such a tool which could help in debugging or validating or fixing an issue or make any changes as per requirement in platform from a remote location.

There are various challenges for platforms testing mentioned as under:

1. *Debug Limitations*: Debugging capabilities from remote location are limited. Controlling the platform, monitoring various voltage rails from remote location becomes tedious task as it is difficult to collect logs from the platforms. Few costly solutions are available for remote debugging which are used by certain industries. So, it can be said that capabilities to debug a platform or motherboard from remote end are limited. There is a requirement of cost effective solution of IoT which could help in controlling, monitoring and validation of the platform from the remote site.
2. *Constrained Platforms*: Debuggers face many limitations to debug failure if they can't physically reach the platforms. Improvement of platform utilization through Timeshare Model is crucial. Also, it is not necessary that debuggers or design engineers are present at remote location all the time. Since, they do not sit next to the platform always, so it is a crucial requirement that debuggers or developers should test their codes during the development process itself. Also, developers do not get the logs out of the platform all the time. So, developers want to test their codes from remote end is limited.
3. *Extract Power Information*: There is a need to extract power information from system with simple solution. Getting the information from the platform regarding voltage, current, energy and power is a crucial requirement for controlling the platform or motherboard from remote end. So, a solution is required through which details regarding voltage rails can be fetched.

The hardware design is regarded as a critical element for the achievement of the IoT product when it comes to creating embedded IoT systems. During the hardware design stage of these systems, many difficulties are confronted by the embedded IoT device suppliers to guarantee that the embedded IoT product meets the necessary feature, consumes low energy and is safe and reliable. There are following few challenges for designing of IoT based embedded system:

1. *Unavailability of necessary flexibility for operating applications over embedded systems:* Embedded systems have to operate with different devices and make itself adjustable to different architectures to cope up with new functions and performances in the real time. This happens just because of the increasing demand for connected devices.

As a result of adapting the latest technology, new applications have been set up. And embedded system designers have to face the following problems such as:

1. Smooth combination of new services with the old ones.
2. Non adapting environment.
3. Changes in software and hardware facilities has been frequent.
4. Small size chip faces which are having low weight and lower power demand face issues in packaging and their integration, etc.

2. Security danger in designing of embedded systems: IoT hardware products must be safe to operate in an integrated setting in real time. Because all integrated parts function in extremely resource-constrained and physically insecure circumstances, technicians often face challenges in ensuring the safety of these integrated parts. To be robust and safe, these systems must be intended and implemented and safe with cryptographic algorithms and safety processes [2].

1.3 Objective

To validate or debug an issue on board, one needs to check every connection manually or probing signals and has to be present at the physical site. There is always a constraint for debugging the issue from a remote location. But, remote debugging capabilities are limited. So, debuggers face many limitations to debug failure if they can't physically reach the platforms. Typically, there is a critical requirement that debuggers should continuously test their codes to debug an issue during the development process itself. But, this is unfortunate that all the developers don't sit next to platforms all the time. So, debug limitations, constrained platforms, extract power information are among the few challenges that design engineers face during platform monitoring and its validation.

So, simple hardware or software is missing for debuggers/developers when they want to test their codes for power measurement, inability for flash BIOS chip through the remote end and also, when they want to collect Postcodes and UART logs from the platform.

A device or an Integrated Circuit or a Board needs to be validated before it is launched into the market. In order to validate or debug platform from a remote location, there is a need of such tool which can do this. Such a tool that provides a solution for mentioned

challenges is System Monitoring Tool (SMT). The purpose of this project work is to design System Monitoring Tool.

Along with the designing of such tool, following are the objectives which are considered for this master thesis to be achieved:

1. Monitoring various sleep signals.
2. Flashing the bios into flash chip.
3. Monitoring various voltage rails used for supplying power to the platform.
4. Collection of data from platform for debugging.
5. Controlling the platform that is make it switched on/off.

1.4 Thesis Orgranisation

In this thesis, we are trying to tackle the above-mentioned problems and explain the main idea behind the tool development which is described in Chapter 1. The study related to existing solutions of remote debugging and study about Intel System-on-Chip architecture is discussed in Chapter 2. This chapter basically deals with the literature survey done required for completion of this master thesis. The tool development approach, project proposal, various protocols required for SMT development and information related to software used for schematics and layout designing is explained in Chapter 3. The next chapter 4 deals with the architecture, schematics design capture, bill of materials required and layout designing of System Monitoring Tool. Chapter 5 deals with the stack-up significance, requirements, guidelines for PCB designing, stack-up chosen for SMT and layout capture of SMT. PCB testing and validation is discussed in chapter 6. Finally, this master thesis is concluded along with results and discussion of future scopes in Chapter 7.

CHAPTER 2

LITERATURE SURVEY

2.1 Literature Review

This section covers the research which has already been carried out in the field of remote debugging of a platform. It shows the different kind of techniques used in debugging and validation of the embedded systems or platforms.

(2013) Xiaoxi (Jessie) Zhao, "**Remote Debugging of Embedded System**", Graduate Dissertation, Dept. of Electrical and Computer Engineering, The Ohio State University [3]. In this research, a remote debugging framework is designed and implemented using WiFi technology and the drawbacks of wired programming are addressed along with the comprehensive study of the microcontroller debugging. This framework helps to remotely manage, monitor and debug the embedded system from remote ends. In this project, MSP430FR5739 microcontroller with a wireless module and a GUI. The GUI is programmed using C# programming language. The communications at the register level between GUI and microcontroller is successfully executed. To facilitate machine level programming a method is devised to modify memory locations within the microcontroller unit.

WiFi technology is used for establishing a connection between the microcontroller and a web server. Embedded C code is run by the microcontroller. In C# programming language the code on the client and the server is developed.

In the server database the memory states of the microcontroller is stored. On the web server SOAP web services are run through which the data stored in the database becomes accessible to the cloud. The programming on the client end is developed using C#. The GUI is developed using Windows presentation foundation. The connectivity between the client and the cloud is achieved using WiFi or there could be a hardwired connection.

Remote debugging is achieved by connecting the unified memory FRAM microcontroller to a web server via Wi-Fi protocol. Using a graphical user interface

(GUI) on the client's end, a user can directly interact with the registers and memory spaces of the microcontroller and perform debugging of programs remotely.

2.2 Intel Architecture of System on Chip

The requirements for hardware for various customers are different. So, hardware designs for them will also be different. But, basics applied to all hardware designs will be same. For example, processor used in designing a hardware. There would be very less exceptions in a case where processors are made to work along with some other compatible small chips in support.

In general, architecture of Intel's hardware platform consists of two main components. One is the main chip known as Microprocessor chip and other chip along with main chip known as PCH. Previously, Intel processor consists of North Bridge and South Bridge. North Bridge, also known as MCH and South Bridge, also known as ICH. Now-a-days, North Bridge is replaced with processor chip and South Bridge with additional features is now replaced by PCH. In a one-chip configurations, PCH is not there, rather its functions and features are incorporated in the processor chip itself.

The two components, processor chip and PCH chip are present in a dye and it will be connected with several other components supplied to customer such as a power supply, Dynamic RAM, ROM for boot configuration and certain interfaces required by the system at its peripheral. At peripherals, there may be sensor, audio devices, or network connections. System also has a non-volatile storage such as flash memory or EEPROM [4].

The Intel System on chip architecture may be based upon one chip set or two chip set. The architecture having two chip sets is designed in such a way that it has better performance than architecture with single chip set. Also, the expansion capability of architecture having two chip sets is high, whereas architectures with single chip sets are designed for lower costs and optimum smaller size.

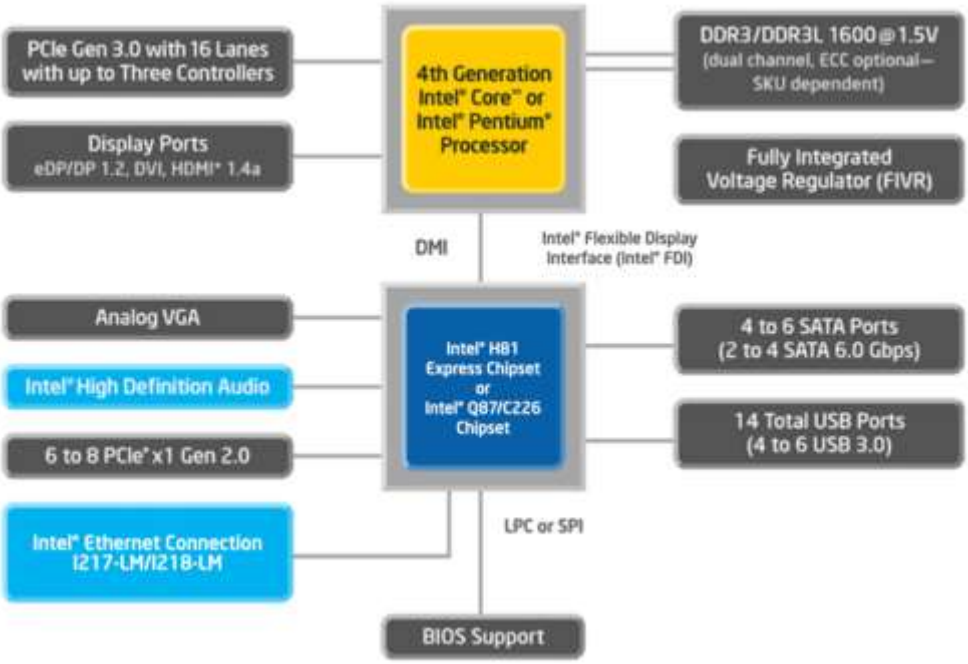

Figure 2.1 Typical System Based on Intel Processor [4]

2.2.1 Core Processor

The heart of the system design is Core processor with following features:

1. Independent CPU cores
2. Multithreading options available per CPU core
3. A built-in two channel DDR3 DRAM controller
4. Integrated Caches
5. Direct Media Interface (DMI) connection between the processor and the PCH

2.2.2 Direct Media Interface (DMI)

DMI is a special name which is given by Intel to interface that exists between supportive chip, PCH and core processor. Specifically, Intel® DH82Q87 PCH and i7 core processors are the chips for which DMI name is used. Additionally, same DMI link is used for other core processor and PCH chips. Also, it is the point to point and high speed interface used between processor and PCH chips. There are four serial links in DMI with dedicated pins for transmission and reception. The serial links present in DMI are called as lanes and all lanes use differential signals. Therefore, number of pins for DMI interface is calculated as follows:

No. of pins (DMI) = No. of Lanes * Transmit and Receive pins * Differential signals

= 4 * 2 * 2

= 16 pins

DMI has additional features such as it allows concurrent traffic, prioritizing services. Also, DMI makes sure that bandwidth requirement by I/O subsystems for their peak performance is met [4].

2.2.3 Platform Controller Hub (PCH)

The Platform Controller Hub (PCH) chip is a family of highly integrated chipset designed to provide high-value features and interfaces needed for the operation of midrange and high-end systems. The components present in a PCH chip differ from model to model, it may comprise a controller catering for multiple DRAM banks, multiple graphics display controller (the accelerator for which is present on the processor), various Universal Serial Bus (USB) interfaces, a Serial ATA (SATA) controller for interfacing hard disk drives and storage media, an Ethernet LAN port, Intel® High Definition Audio etc. There is a direct connection between PCH and Direct Media Interface (DMI) interface, without the requirement of additional engineering from the developer. There is a simple connection between the appropriate pins and the process begins. The design of PCH is very complex and it is a programmable component providing various features for augmenting the performance and reliability of the system.

2.2 Modern Input/Output Interfaces

The PCH bridges the gap between varieties of industry-standard interfaces thus allowing the system designer to pick from a vast range of peripherals, including [4]:

1. Peripheral Component Interface (PCI) operating at 33 MHz and provides for many external bus masters. The role of the central arbiter is performed by PCH and it also acts as the core of the PCI bus.
2. Root Port Controllers for PCI Express. The variation in number of ports is in accordance with the specific PCH chip but it generally varies from 1 to 4. At 2.5 GT/s speed, link widths of ×1 ×4 are supported.
3. SATA controllers that support the two legacy operations using I/O space and the Advanced Host Controller Interface (AHCI) using memory-mapped I/O. SATA

controllers also allow for enhanced features such as hot-plug and native command queuing. Data rates of 1.5 Gb/s and 3 Gb/s are well supported by SATA II.

4. Universal Serial Bus supporting high speed USB 2.0 (480 Mb/s) operation as well as full-speed operation (12 Mb/s) and also signaling at low speeds.
5. General Purpose Input/output (GPIO) pins for system customization. To begin interrupts and wake events some pins can be configured for this purpose.
6. System Management Bus (SMBus 2.0). The processor communicates with the SMBus slaves via SMBus host interface. This interface provides high compatibility with most of the Inter-IC (I2C) devices. Slave functionality, including the Host Notify protocol is realized.
7. Serial Peripheral Interface (SPI) is used for interfacing BIOS flash devices that are comprised of boot firmware and initialization code. At maximum two SPI flash devices operating at 33 MHz can be connected. It is to be noted that the flash devices connected to the Low Pin Count Interface (LPC) interface are now outmoded and eventually SPI will emerge as a standard interface for BIOS flash. On the SPI interface, the PCH is a master.
8. Low Pin Count Interface (LPC). The Industry Standard Architecture (ISA) bus made by IBM in the early 1980s, is replaced by LPC but it works with only 7 signals along with a clock signal. This interface is used for establishing the connection to low speed devices that do not need PCI Express or PCI bandwidth. It is also used for interfacing Super I/O devices consisting of several interfaces such as floppy driver controller, PS2 keyboard/mouse controls and serial ports.
9. Joint Test Action Group (JTAG) boundary scan allows the testing of PCB board after assembly.

CHAPTER 3

PROPOSAL AND PRE-REQUISITES

3.1 Project Proposal

The idea of the project is to design a system which could able to control, monitor, debug and validate a platform from remote location. The name of such a tool is System Monitoring Tool (SMT). SMT is a hardware and software solution which provides remote debug capabilities. The tool's remote capabilities include BIOS SPI programming, switching ON/OFF platform, remotely handling power cycles and power state delays. It uses a common/generic software interface and a customizable hardware layer for extensibility. The tool helps in getting meta data from system to remote user. The tool helps in rework for deployed system. The advantages of such a tool is mentioned below:

1. Controlling the platform remotely. Controlling includes Remote Platform Access, control and programming capabilities with the help of SMT through remote location.
2. Remote access is the capability to control, monitor, and program a target platform or hardware remotely.
3. It let the user to track system.
4. Power Checks on Software Updates.

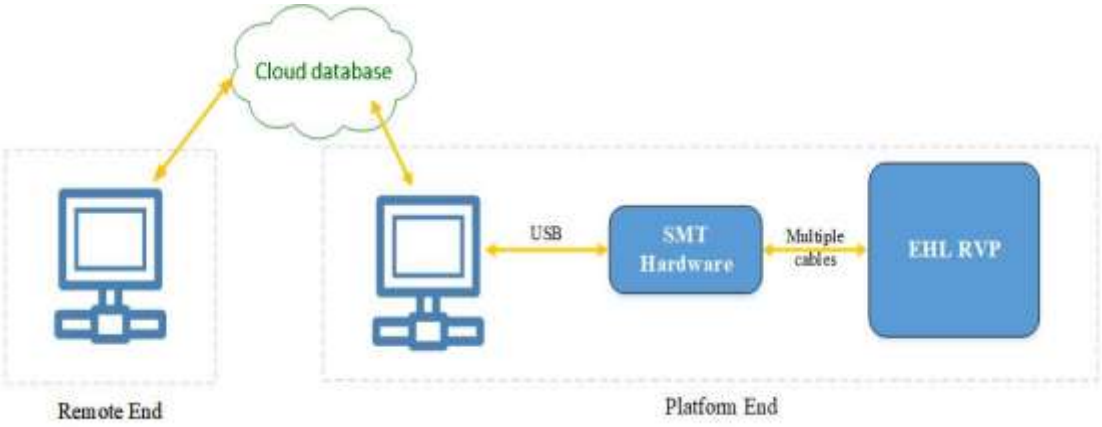

Figure 3.1 Block Diagram of SMT Implementation

3.2 Reference Validation Platform

Reference Validation Platform, also called as RVP, is a platform used prior to boards meant for customer needs. The board meant for customers are called as Customer

Reference Boards. In other words, it can be said that the RVP are those boards which are provided to customers as CRB. RVP consists of all the basic features, interfaces, buses, memory, display and the Intel processor. Generic architecture of Intel Reference Validation Platform is shown below in Figure 3.2.

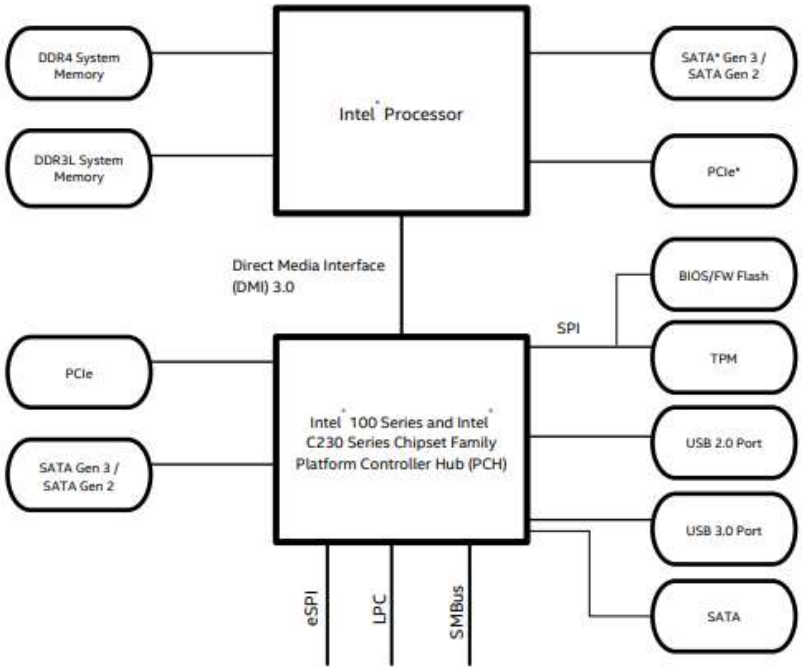

Figure 3.2 Generic Architecture of Intel RVP [5]

The processor placed at the center of the generic architecture shown in Figure 3.2 is based upon the 14 nm technology of Intel that enhances performance of CPU. DDR3 is a low voltage RAM and DDR4 is a fourth generation SDRAM. PCH is a chipset with centralized platform functionalities including the display connectivity, primary I/O interfaces, power handling and management, security, storage and audio features. The core Silicon die is the Intel processor that contains multiple cores. Each core has a data cache, instruction cache and L2 cache with capacity 256 kB. The SMT add-in card discussed in this master thesis gets connected to the RVP and will debug, monitor and validates RVP. SMT will collect logs from RVP and process it for further use.

3.3 Protocols

3.3.1 I2C

The I2C protocol is very famous and extremely powerful serial protocol used these days. Using this protocol, one master can talk to one or more than one slave devices. This protocol allows one master to communicate with slave devices by using only two-wired bus. All the peripherals or slave devices share the same two-wired bus. This is one of the biggest advantages offered by I2C protocol over other protocols. Figure 3.2 shows how multiple peripherals are connected to a processor by sharing same two-wired bus.

This protocol allows the bidirectional flow of data on single line i.e. data bus. This interface, using which master communicates with slave devices, is a standard protocol that allows bidirectional flow of data. I2C protocol uses an open collector or open drain configuration along with an input buffer. This is responsible for bidirectional flow of data. Data cannot be transmitted by a slave unless master addresses it. Each devices is assigned a particular address that uses same channel so that devices could be differentiated. There are multiple slave devices that need to be configured first in order to set their behavior. Such a device configuration is done when master has to access the internal registers with unique addresses inside slave. A device has one or more than one registers where data is read, written or stored [6].

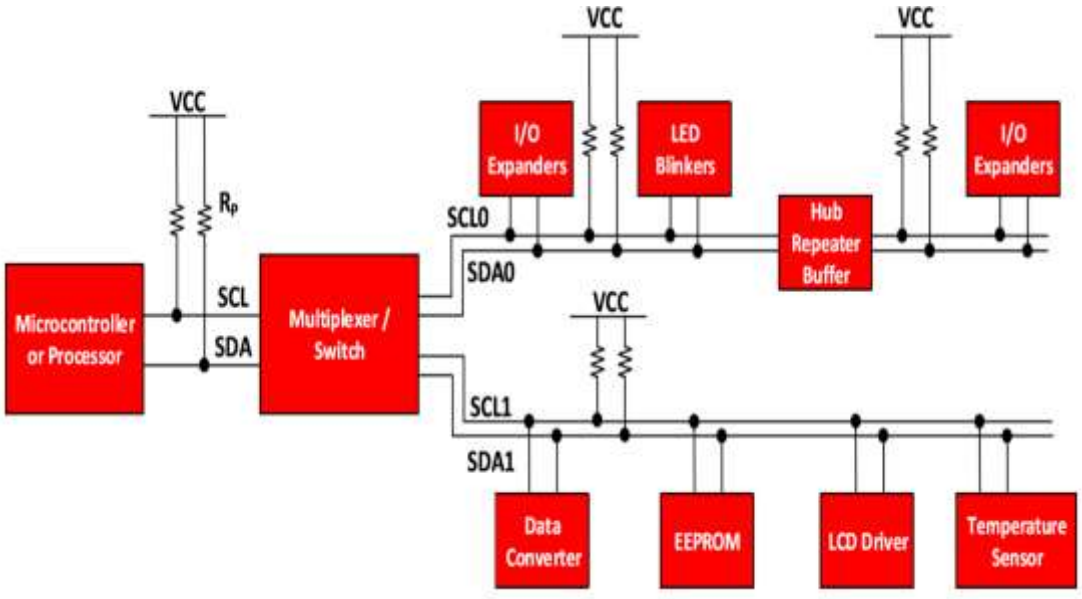

Figure 3.3 I2C Bus Example [6]

The generic steps involved for a master in order to access a slave device is given as follows:

1. Let us assume that a master is supposed to send data to a slave device:
    a. The transmitter of master sends a START condition and then sends the slave address to slave-receiver.
    b. The transmitter of master sends data to the receiver of slave.
    c. The transmitter of master halts the transfer by sending a STOP condition.

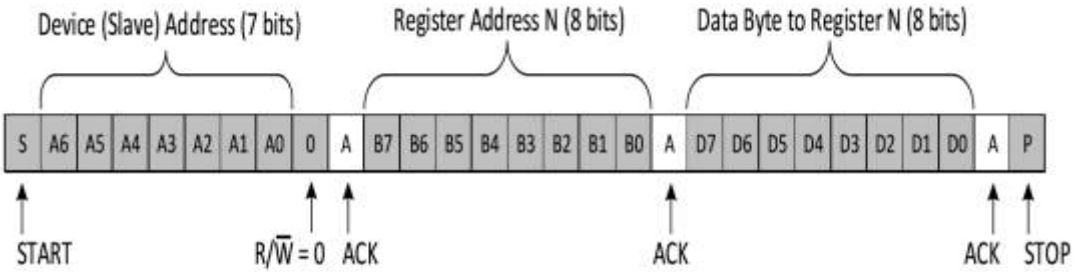

Figure 3.4 I2C Write to Slave's Device Register [6]

2. Steps involved if a master read/receive data from a slave device:
    a. Receiver of master sends a START condition to the transmitter of slave.
    b. Receiver of master first sends the requested register from which it wants to read to transmitter of slave.
    c. Receiver of master receives data sent from the transmitter of slave.
    d. Receiver of master halts the transfer by sending a STOP condition.

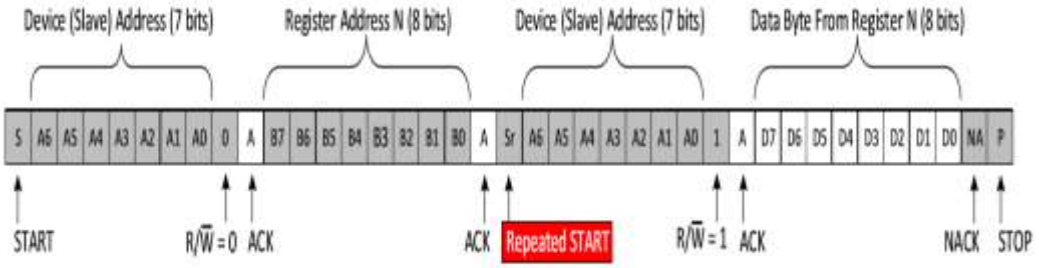

Figure 3.5 I2C Read from Slave's device Register [6]

3.3.2 SPI

SPI stands for Serial peripheral Interface. This is a synchronous standard used for short distance communication. This protocol was developed by Motorola in mid-1980s [7]. This protocol operates in full duplex mode having master-slave architecture with multiple slave devices and only one master. Master device always initiates communication by sending frames for writing and reading purpose. SPI is four wire serial protocol. The four serial buses of SPI are SCLK, MOSI, MISO and SS. In case of multiple slaves, selection of slave device by master is done using SS line.

In case of master to single slave communication, the SS pin can be used and kept at a fixed logic as per slave requirement. In case of master to multiple slave communication, individual SS line is required for each slave in order to select the desired slave device.

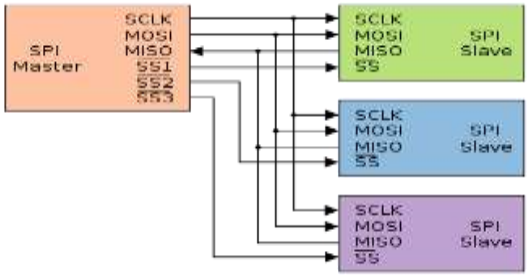

Figure 3.6 Communication between master and multiple slaves through SPI protocol

In order to begin a communication by master, firstly master has to configure a clock supported by slave device. This protocol supports clock frequency typically upto few MHz. The, a slave device is selected by a master by sending a low logic on slave select line. For any task such as analog to digital conversion, if there is need for waiting period, then master waits for minimum that much period before it issues new clock cycles.

3.3.3 UART

UART stands for Universal Asynchronous Receiver Transmitter. It is protocol which follows serial communication. Most of the microcontrollers supports UART. UART receives data bytes and always transmits these bytes in form of bits in sequential fashion. At the destination side, there is another UART which receives these sequential bits and reconverts them into bytes [8]. The full duplex communication in UART protocol can be done using only two wires as shown in Figure 3.6.

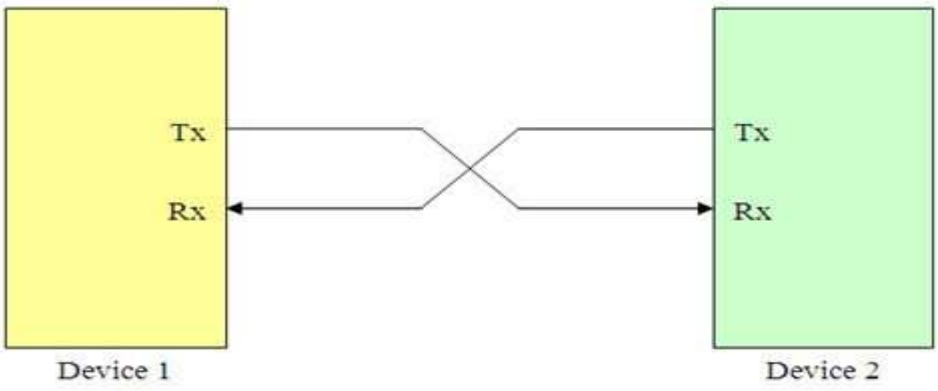

Figure 3.7 Communication through UART between two devices

In asynchronous communication, sender need not to send a clock signal to the receiver for sending data from sender to receiver. In order to synchronize on sending and receiving data units, addition of certain bits at the end of each word is done and also, both receiver and sender must agree on timing parameters i.e Baud rate prior transmission. In asynchronous kind of transmission, sender initially sends a START bit, followed by five to eight data bits, then followed by parity bits which are optional and at last, 1, 1.5 or 2 STOP bits. The START bit sent by sender indicates receiver that certain data bits are about to come, so it receiver's clock should get forcibly in sync with the transmitter's clock. The parity bit is sent to perform checking of errors by receiver. The STOP bit indicates transmission halt by sender. The drift in frequencies of transmitter and receiver is allowed upto 10% for communication through UART. Basic UART packet format is shown in figure.

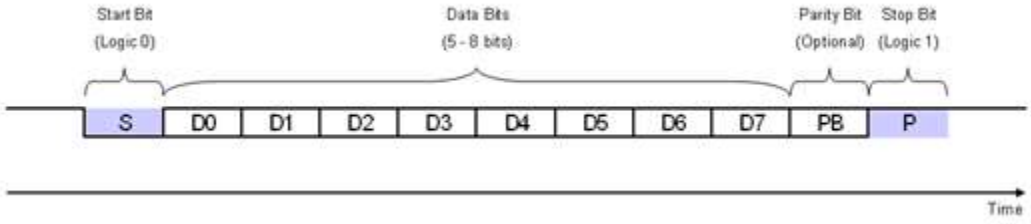

Figure 3.8 Basic UART packet format: 1 START bit, 8 data bits, 1 Parity bit and 1 STOP bit [8]

3.3.4 USB

USB is an interface through which communication can be done among peripheral device and host device. Peripheral device could be printer, keyboard, flash drives, externally connected hard drives, digital cameras, mice etc. This interface is intended for higher

quality cabling, higher transfer rates, hot swapping and simple installation. Hot swapping is one of the greatest advantage of USB interface which enables detection of peripheral device by host device without requirement of interrupting and rebooting the system in host device. Hot swapping means capability to tolerate fault which means it can proceed to operate despite a failure of the hardware [9].

Devices in the networks should be as simple for customers to connect as setting up a stereo equipment which means it operates as it is plugged in and switched on. This is possible using Plug-and-Play technology. Recent standards like USB and Plug-and-Play have enhanced the condition to automatically detect the devices and install device drivers [10].

S.No.	Usb type	Width (mm)	Height (mm)
1	Type A	12	4.5
2	Type B	8.45	7.26
3	Mini/Micro	6.8	1.8-3
4	Type C	8.25	2.4

Table 3.1 USB Specifications

There are generally 5 pins in USB connector. Its pinout is mentioned below [11] :

Pin 1 : VBUS

Pin 2 : Data Minus

Pin 3 : Data Plus

Pin 4 : Identity

Pin 5 : Ground

3.4 Tool Requirements

3.4.1 Cadence Concept HDL

Concept HDL is a tool which provides environment for designing schematics. The schematics consists of structural and behavioural designs blocks in form of graphics and texts. The tool is developed by Cadence. It allows creation of project, placing parts or components, naming signals, addition of ports and then saving designs. When the design is saved, the tool first inspects for error and then helps the user by locating the places

where connectivity errors are present in schematics. The tool is also called as by-reference editor as it assigns references to all the components used in designing the schematics. The references are created with respect to the libraries created in local or global domain. The libraries includes various cells, symbols, attributes, properties etc. The libraries are mapped to the schematics design in Concept HDL. The schematics is basically the circuit design in which all the connections to the components and routing of the signals to different pages are shown. This helps the user to understand the design flow of the circuit [12] .

There are following two models supported by Concept HDL:

1. Post Select
2. Pre Select

In Post Select model, command is selected first and then selection of component in schematics is done. But, in Pre Select model, selection of component in schematics is done first and then command selection is done.

In order to understand these models, let us consider an example in which a component in schematics is to be deleted. In Post Select Model, select "Edit" in menu bar, then select "Delete" option from the drop down list. Then, selection of the component is done to be deleted. Where as in Pre Select Model, selection of the component is done to be deleted and then select "delete" option from the drop down list under "Edit" menu.

Various features of Concept HDL tool are as follows:

1. Top-down approach in hierarchical manner that allows user to draw blocks quickly and connect them using wires.
2. Provides customizable user interface in which user can customize toolbars and menus, key mapping to functions could be done and also, creation of new commands.
3. The structure of design could be viewed in Hierarchy Viewer.
4. In order to drive the actual layout, one can add properties in the design using attribute editor feature.
5. Cross probing between various Cadence tools and Concept HDL.
6. It provides support for reusing design. Logical components can be associated with layout section in order to create components that could be reused.

7. Additional feature of Check Plus for development of rule and an advanced rules check.

Hierarchical Designs are created in Concept HDL. This technique helps in developing the complex designs which consists of multiple modules.

3.4.2 Allergo PCB Designer

The Cadence® Allegro® PCB Designer serves the purpose for ensuring functionality and manufacturability by taking simple as well as complex designs from concept to production in a constraint-driven design system. The designers avail the benefits of scalable technology by matching current and future technological and methodological requirements for organizations and highly complex projects [14].

Key benefits of Allergo PCB Designer are as follows:

1. Enhances design pace from routing of traces and components placement to manufacturing.
2. Incorporates powerful features such as partitioning of design, RF designing and interconnects design planning.
3. Production proven to boost productivity and assist technicians rapidly increase production volumes.
4. TÜV SÜD "Fit for Purpose – TCL1" certified to fulfill the automotive functional security criteria of ISO 26262.

Features of Cadence tool Allergo PCB Designer are as follows:

1. Provides a solution for PCB design which is scalable and fully featured.
2. Design iterations are reduced by enabling a constraint-driven design flow.
3. Integrated Design True DFM technology providing real-time DFM checks
4. Provides a constraint management environment which is consistent
5. Using advanced rigid-flex design features, the design iterations are minimized and overall cost for flex and rigid-flex designs is also reduced.
6. Shortens design cycle by reducing the time spent on routing, tuning and signal optimization by enabling dynamic concurrent team design capability.
7. An integrated RF/analog design and mixed-signal design environment is provided.
8. Provides interactive planning of floor and positioning of components
9. For large and dispersed development teams design partitioning is provided

10. Allows an interactive shove editing of etch in real time.
11. Capability to manage net timing, scheduling, layer set routing, crosstalk and geometric limitations.
12. For auto routing of random signals, PCB router technology is provided
13. The process of design completion is accelerated by enabling hierarchical route planning
14. With high-speed interfaces the routing time and interconnect planning for highly dense designs is shortened
15. Provides a user friendly, powerful and comprehensive tools suite to help designers with an effective and successful transfer to production.

CHAPTER 4

CONTRIBUTION

4.1 SMT Architecture

The idea behind SMT id remote monitoring, controlling and debugging of one of the platforms developed by Intel Corporation. This is basically a small add-in card that gets connected to Intel platform. Add-in card is a small PCB with dimensions 68mm X 53mm having four layer stack-up consists of various components such as headers, microcontroller, low dropout voltage regulator etc. In this section, architecture of the add-in card, its design, block diagram, schematics is discussed.

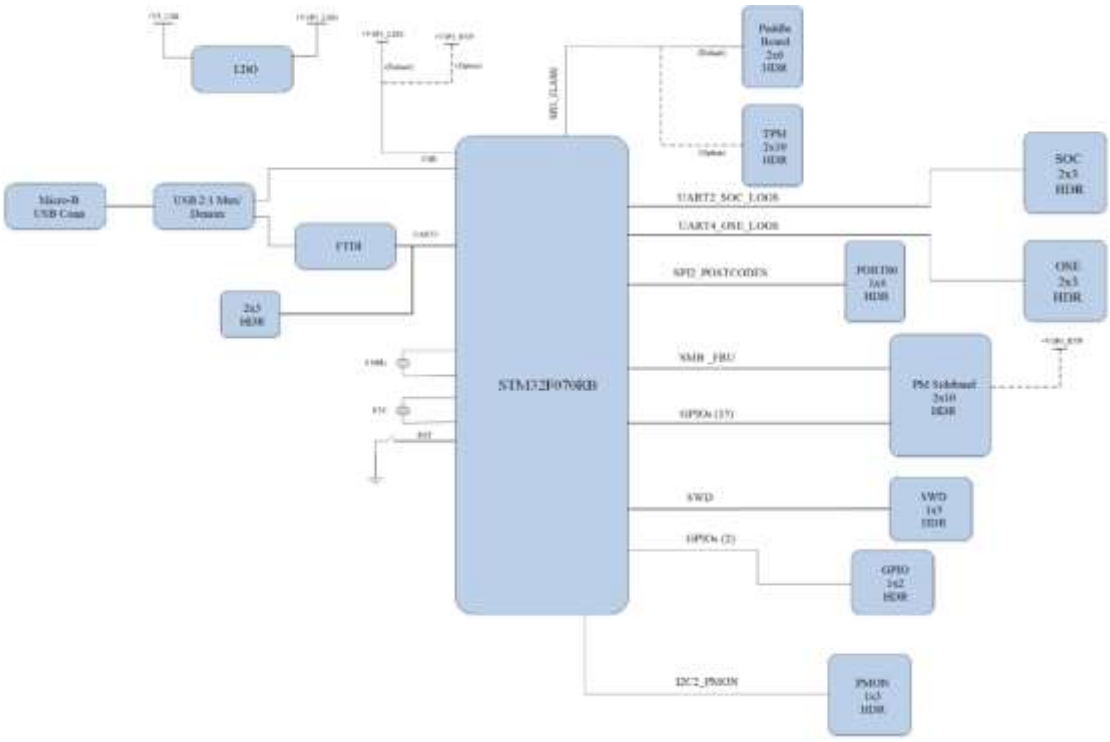

Figure 4.1 SMT Architecture

Figure 4.1 shows the detailed block diagram of System Monitoring Tool for remote debugging. SMT is designed in such a way that it has the capability to connect to some standard called as RVP, fetches the data from RVP and then it is responsible to send the collected data to remote location through servers. The tool consists of microcontroller which is the master of this add-in card. There are few headers such as Paddle Board

header, TPM header, header for SOC and OSE logs from RVP, Port80 header, PM sideband header, SWD header, header for power monitoring and UART header present in this board. Other than these headers, FDTI chip and crystal oscillators are used in this add-in card. Also, one reset switch, USB connector and 2:1 mux/demux are used. This board gets connected to the host device from one side with the help of micro-B USB connector shown in left side of block diagram. On the other side, it gets connected to the RVP (to be validated/monitored/debugged) through various headers present on this board with the help of different cables. The components used to design SMT add-in card and their utilities are discussed in next section.

Following are the components used in SMT add-in card design:

1. Microcontroller: The selection of the microcontroller is done based upon the requirements of end user. End user wants to select such a device which is capable of collecting certain signals, should be able to support certain interfaces, should have sufficient amount of memory for code storage and also capable of sending data to a wireless link. Special interfaces such as I2C, SPI, USART and GPIO signals should be supported by the device chosen by end user. 32-bit ST Microelectronics MCU is chosen for this board. It consists of 128kB programmable memory, RAM size is 16 kB. SPI, I2C, USART interfaces are also supported by the chosen MCU. Its operating voltage range is 2V-3.6V and consist of 51 GPIO pins.
2. Crystal Oscillators: There are two crystal oscillators used in the board design. These are Low speed external crystal oscillator and High speed external crystal oscillator. LSE crystal is used for providing 32.768 KHz clock frequency for RTC clock. HSE crystal is used for providing 8 MHz clock frequency required by microcontroller.
3. Multiple Headers: Various headers are selected in platform developed by Intel for collection of multiple data signals based on different interfaces. One fine pitch header with 2x20 pins is used as TPM header for flashing a BIOS. Other are normal pitch headers. TPM header has a pitch 1.57mm and other normal pitch headers have a 2.54mm pitch.

4. USB Connector: Micro-B USB2.0 connector is used in SMT design for establishing communication between SMT board and host machine.
5. USB Multiplexer/Demultiplexer: This is used for selection of either of the two USB interfaces available on SMT board.

4.2 Bill Of Materials

A BOM refers to an extensive inventory of the components, parts, sub-assemblies, assemblies and raw materials with their respective quantities needed to produce a product. The BOM used for SMT board designing is shown in Table 4.1. BOM represents the brief description of the components used in designing of SMT PCB board along with their quantities. Few of the components given in Table 4.1 are unstuffed in SMT PCB design, but they are included in SMT BOM representation.

S.No.	Description	Qty
1	IC,DS,DIO,SMT,CM123002CP,ZENER	1.000
2	IC,HI SPEED USB 2.0,QFN,10P,TS3USB30ERS>	1.000
3	IC,LIN,ANALOGSWITCH,STDFN,SLG5NT17	1.000
4	IC,MCU 32BIT,128KB FLASH,64LQFP	1.000
5	IC,VLSI,OTHER,FT234XD,DFN,12	1.000
6	IC,ADJ,500MA,LDO,WSON-6,	1.000
7	IC,DS,FET N,SOT723,SSM3K15AMFV	1.000
8	IC,DS,FET N,SOT723,SSM3K35AMFV	2.000
9	DIODE,SCHOTTKY 20V 2A SMA,	1.000
10	IC,DS,DIO,SOD-882,AOZ8131DI,ZENER,	1.000
11	IC,DS,DIO,DFN,ESD9N5BM-2,TVS,	3.000
12	LED,BRIGHT GREEN,0603,VF=2V,,IF=0.03A	1.000
13	CHOKE,90.0 OHM 330.0MA,0805,2 LINE	1.000
14	FER-BEAD,0603,600.0 OHM,500MA,+/-25%	1.000
15	FER-BEAD,0805,100.0OHM,2.5A,+/-25%	1.000
16	XTAL,CER3.2X1.5,32.768,KHZ,12.5,PF,0.002%,SM	1.000
17	XTAL,5.00MM X 3.20MM,8MHZ,18PF,30PPM,SMD	1.000
18	CAPC,C0G,0402,18.000PF,50.000V,+/- 5%	2.000
19	CAPC,C0G,0402,20.000PF,50.000V,+/- 5%	2.000
20	CAPC,X7R,0402,2200.00PF,50.00V,+/- 10%	1.000
21	CAPC,X7R,0603,0.010 UF,16.000V,+/- 10%	1.000
22	CAPC,X7R,0402,0.010UF,25.000V,+/- 10%	1.000
23	CAPC,X7R,0603,0.100UF,25.000V,+/- 10%	4.000
24	CAPC,X5R,0402,0.100UF,10.000V,+/- 10%	8.000

25	CAPC,X5R,0603,1.000UF,25.000V,+/- 10%	1.000
26	CAPC,X5R,0402,1.0UF,10.00V,+/- 10%	2.000
27	CAPC,X7R,0603,1.00UF,25.00V,+/- 10%	3.000
28	CAPC,X5R,0603,2.200UF,6.300V,+/- 10%	2.000
29	CAPC,X5R,0402,4.700UF,6.300V,+/- 20%	1.000
30	CAPC,X5R,0402,4.7UF,10.00V,+/- 20%	1.000
31	CAPC,X5R,0402,10.00UF,10.00V,+/- 20%	1.000
32	RES D,0402,0.00 OHM,5.00%,1/16W	24.000
33	RES D,0402,100.00 OHM,5.00%,1/16W	2.000
34	RES D,0402,330.00 OHM,5.00%,1/16W,YES	1.000
35	RES D,0603,0.00 OHM,5.00%,1/10W,YES	2.000
36	RES D,0402,49.90 OHM,1.00%,1/16W	1.000
37	RES D,0402,1.00 kOHM,5.00%,1/16W	3.000
38	RES D,0402,4.70 kOHM,5.00%,1/16W	1.000
39	RES_D,0402,5.1kOHM,5.00%,1/16W,	1.000
40	RES_D,0402,10.00kOHM,1.00%,1/16W,	2.000
41	RES D,0402,10.00 kOHM,5.00%,1/16W	4.000
42	RES D,0603,10.00 kOHM,5.00%,1/10W,YES	1.000
43	RES D,0402,100.00 kOHM,1.00%,1/16W	3.000
44	CONN,HDR,PIN 2X3,2.54MM PITCH,SMT	3.000
45	MWG,CONN,CONN, HDR, 3P, 0.25	1.000
46	CONN,MISC,5P,MICRO USB,TYPE B	1.000
47	CONN,HDR,PIN 1X3,2.54MM PITCH	1.000
48	CONN,HDR,PIN 1X2,2.54MM PITCH	3.000
49	CONN,HDR,PIN 1X4,2.54MM PITCH	1.000
50	CONN,HDR,PIN 1X5,2.54MM PITCH	1.000
51	CONN,HDR,PIN 2X6,2.54MM PITCH,SMT	1.000
52	CONN,B2B,FEMALE,2X20,2.54MM PITCH	1.000
53	CONN,SWITCH,TACTILE,VT,SPST,1,15.0V,SMT	1.000

Table 4.1 SMT Bill of Materials

4.3 Schematics Capture

Schematics refers to the designing of circuit. Circuit design is created in Cadence tool Concept HDL. Schematics drawing involves selection of components first, then these components are used to draw circuits. Concept HDL provides designing user friendly environment to the user. Designing schematics is the first step involved in PCB designing process. The circuit designing of SMT is shown as follows:

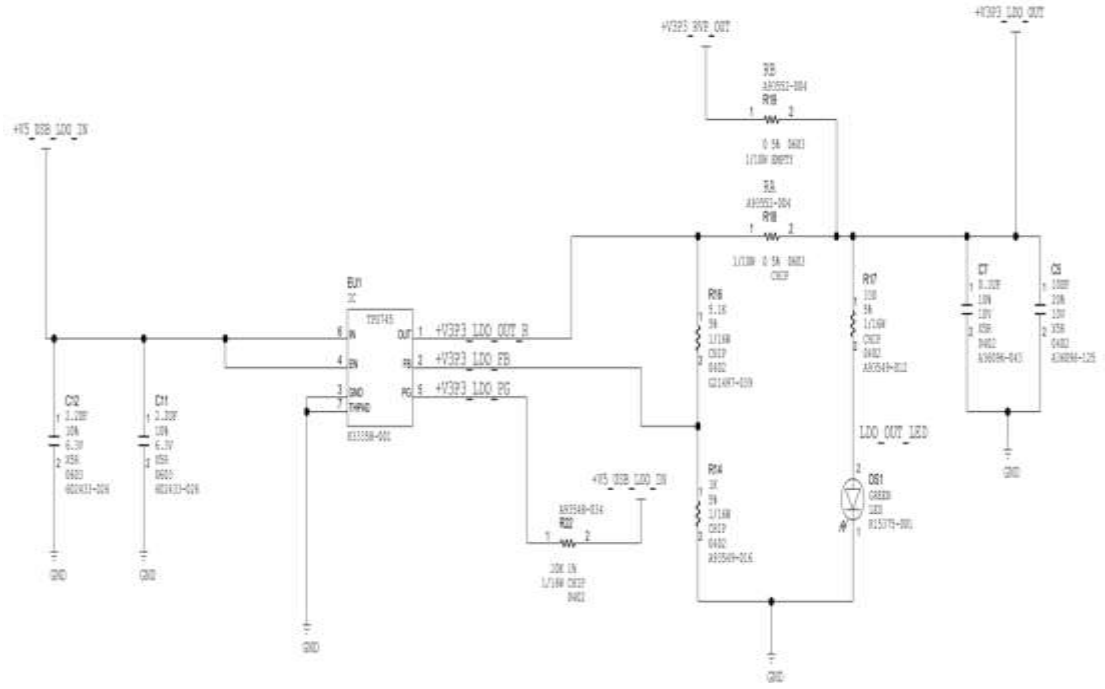

Figure 4.2 Voltage Regulator

Figure 4.2 shows the snapshot of power delivery section taken from the schematics design. In this section, a low dropout voltage regulator is used which is capable of taking 5V as input and giving 3.3V as output. Low dropout Voltage Regulator is selected based upon the current, voltage and thermal requirements of this tool. Output of this regulator is fed to various components such as microcontroller, USB 2:1 Multiplexer/Demultiplexer and load switch used for BIOS flash involved in SMT.

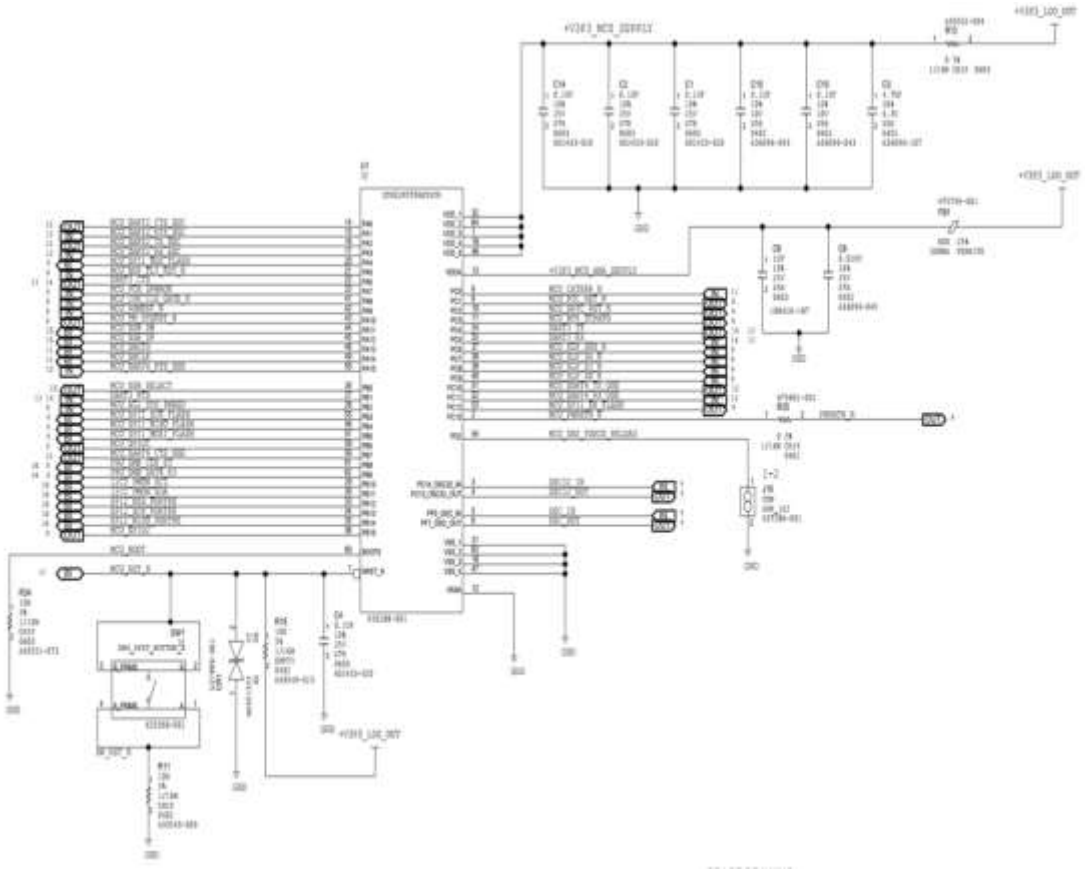

Figure 4.3 MCU STM32F070RB

Figure 4.3 shows the way microcontroller is connected to other components. It also shows multiple decoupling capacitors connected in both analog as well as digital supply paths. In order to decouple on electrical network from the other, decoupling capacitors are used. Decoupling capacitors are responsible for reducing impact of noise or voltage spikes caused by other circuit [14]. A ferrite bead is also used for isolation of analog and digital voltage supplies.

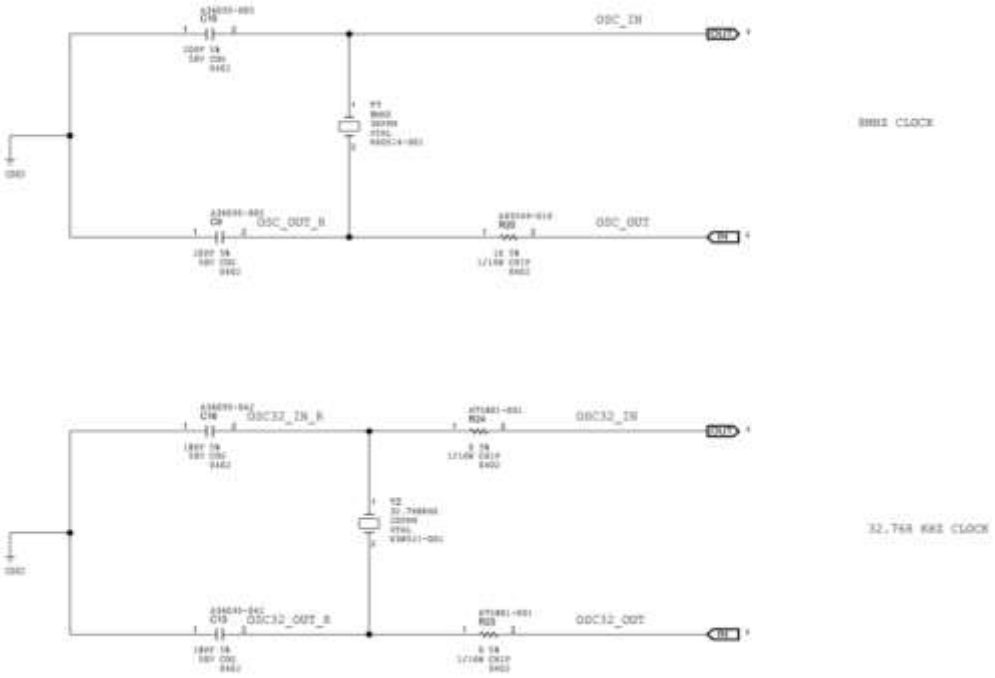

Figure 4.4 Clock crystal for MCU

Figure 4.4 shows the two crystals used to provide two different clocks to the microcontroller. These are Low speed external crystal oscillator and High speed external crystal oscillator. LSE crystal is used for providing 32.768 KHz clock frequency for RTC clock. HSE crystal is used for providing 8 MHz clock frequency required by microcontroller.

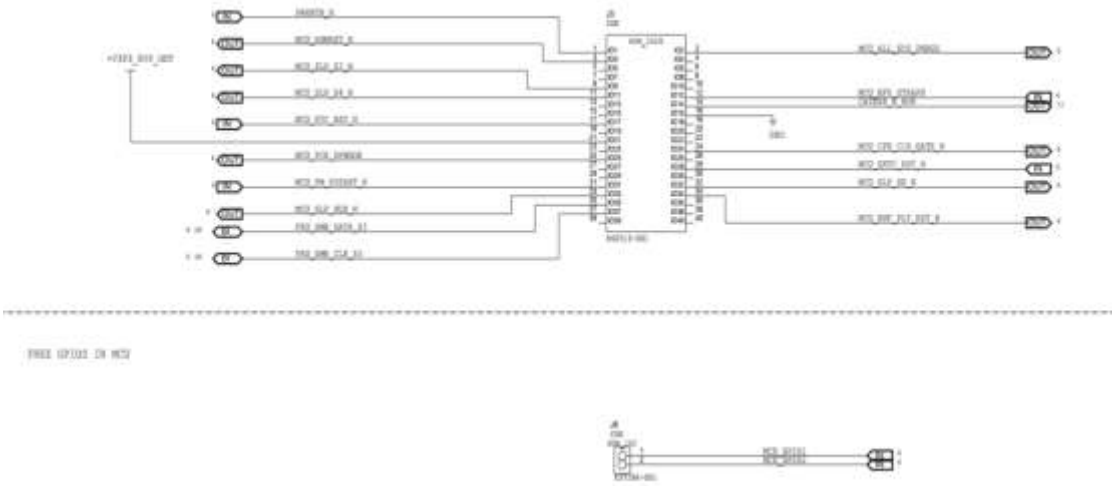

Figure 4.5 GPIO and Free GPIO header in MCU

Figure 4.5 shows the 2x20 and 1x2 pins headers used in board design of SMT. 2x20 pin header is 2.54 mm pitch header which is capable of collecting maximum signals from the Intel platform. Also, a small header with 2 pin is shown in this figure which gives access to use the free GPIO pins available in microcontroller.

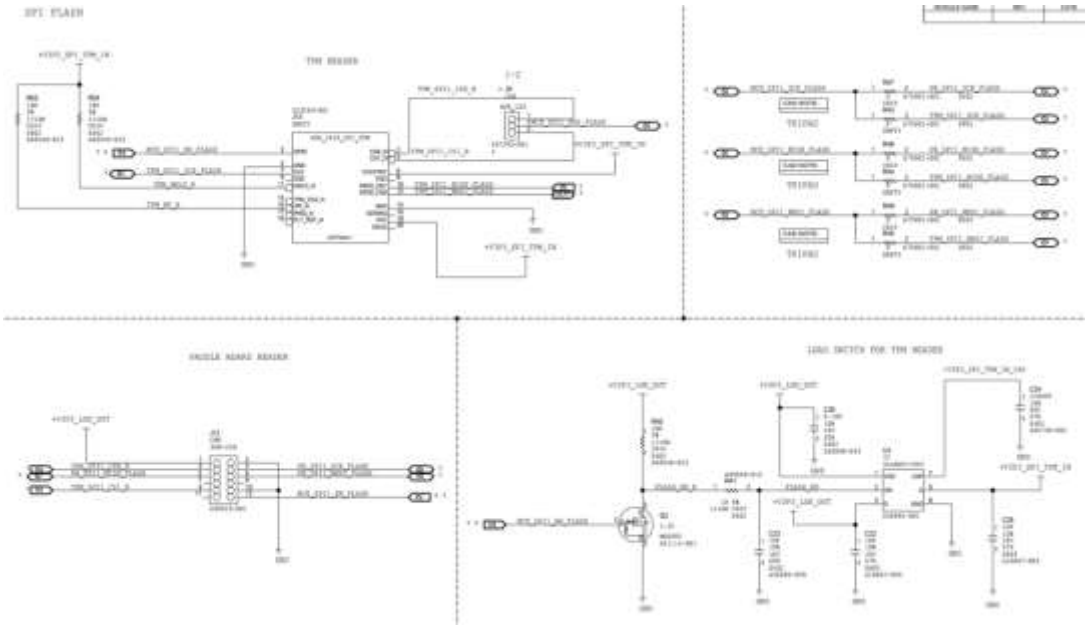

Figure 4.6 BIOS Flashing circuit

Figure 4.6 shows the circuitry required for flashing the BIOS in the platform. There are two headers given as options for user to flash the BIOS chip. User can choose either of the two headers depending upon the environment he exists.

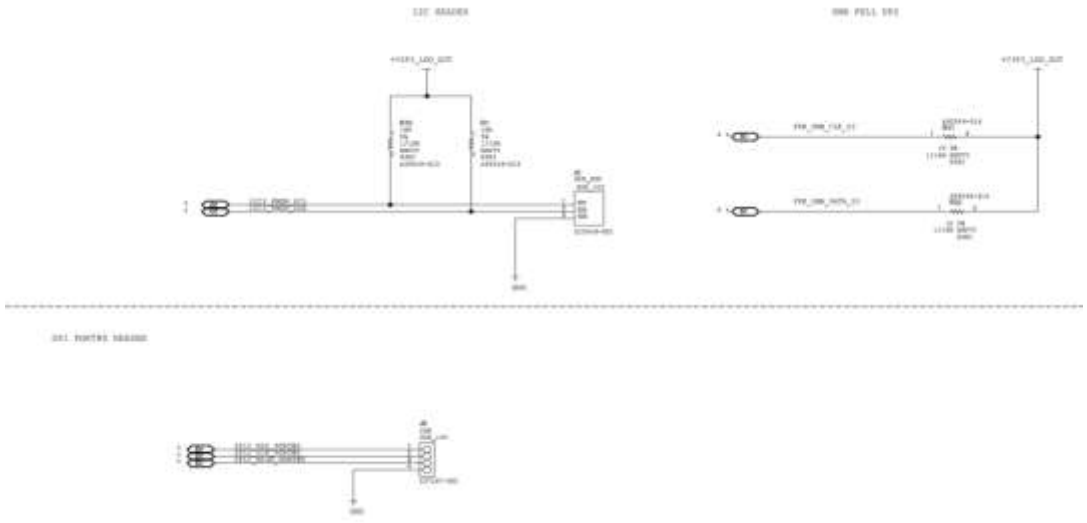

Figure 4.7 Power Monitoring, FRU EEPROM Read and Post Codes Read Headers

Figure 4.7 shows the pull-ups required to follow I2C and SMB protocols. I2C protocol is used for power monitoring from remote end and SMB is used for FRU-EEPROM chip. There is additional 1x4 pin header. This header is for reading postcodes from Intel platform.

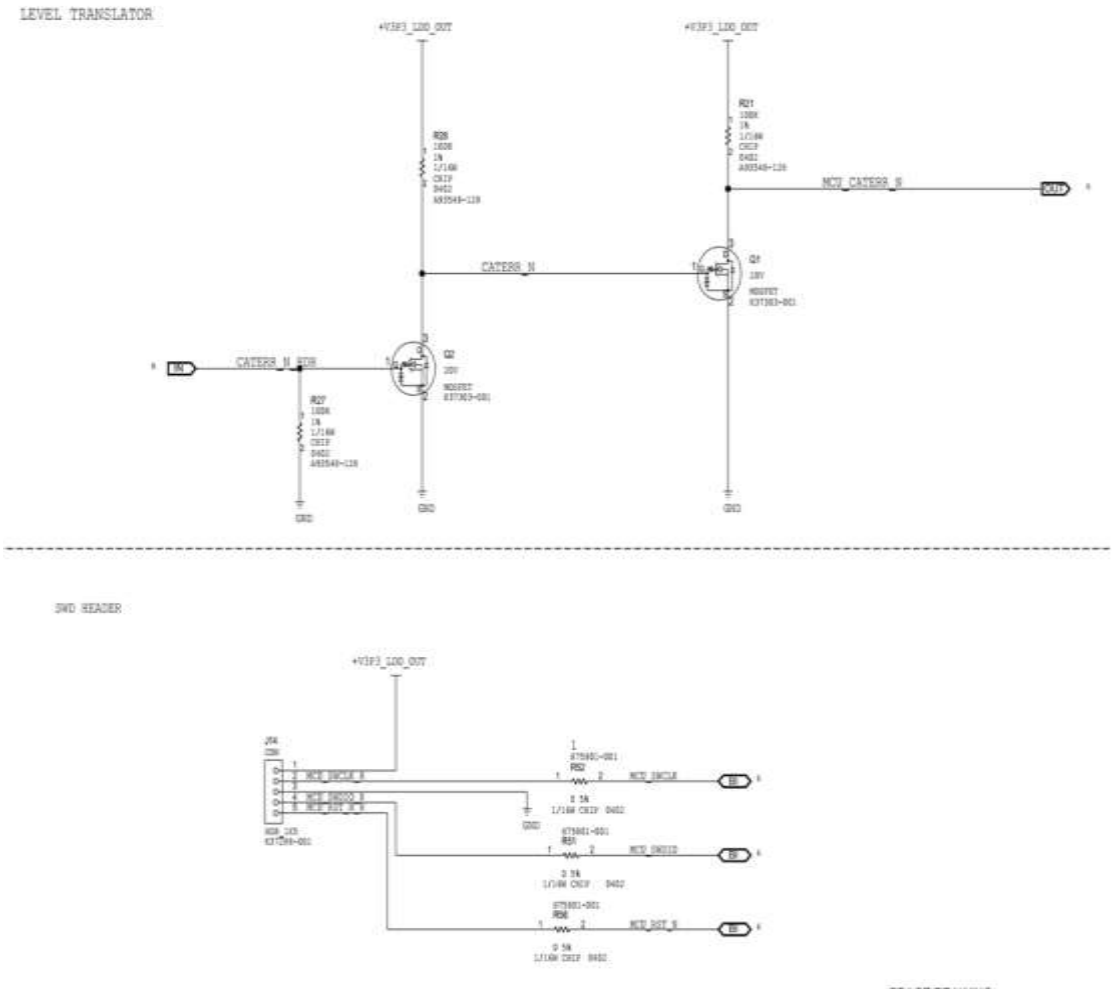

Figure 4.8 Level Translator and Programming header

In SMT board design, there is one signal which has voltage level of 1.05 V. In order to convert this signals to 3.3V, a voltage translator circuitry is required. This circuitry is shown in above Figure 4.8. Also, there is one 5 pin header which will be used for programming and debugging the microcontroller used in SMT board.

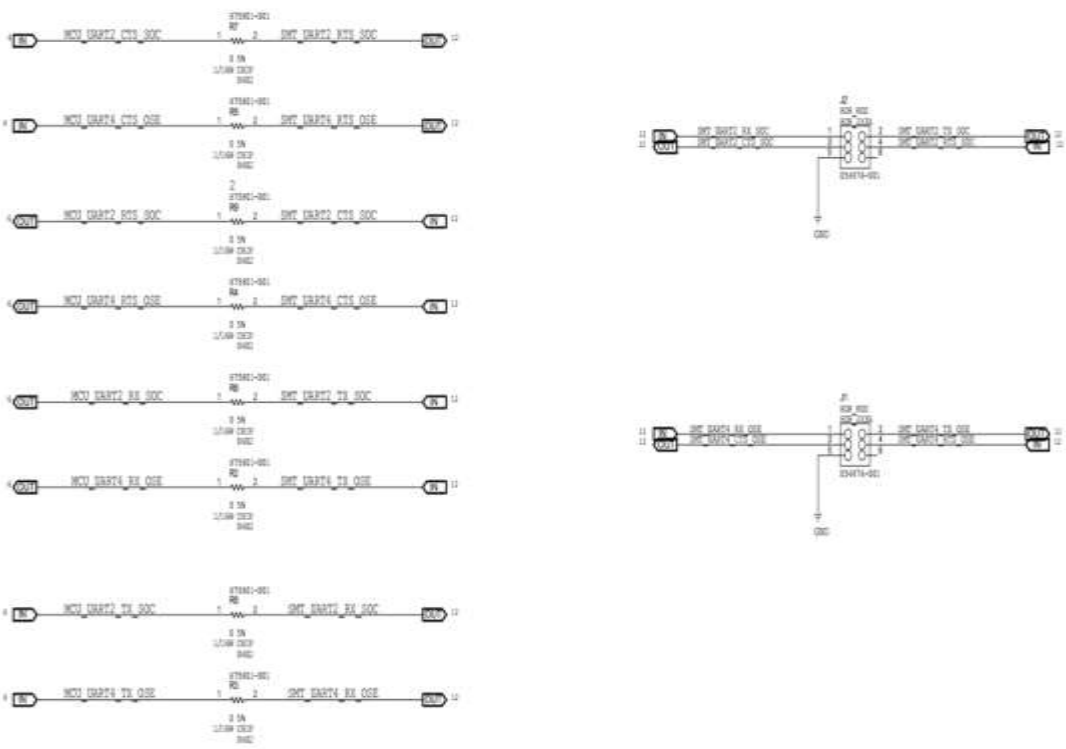

Figure 4.9 UART Header for SoC logs

Two 6 pins headers are used for collection of logs from System-on-Chip by SMT. These are UART headers shown in figure 4.9. The pinouts of UART header includes UART-Transmitter, UART-Receiver, UART-Request to Send, UART-Clear to Send and Ground. One extra pin is available for Synchronous UART communication (USART).

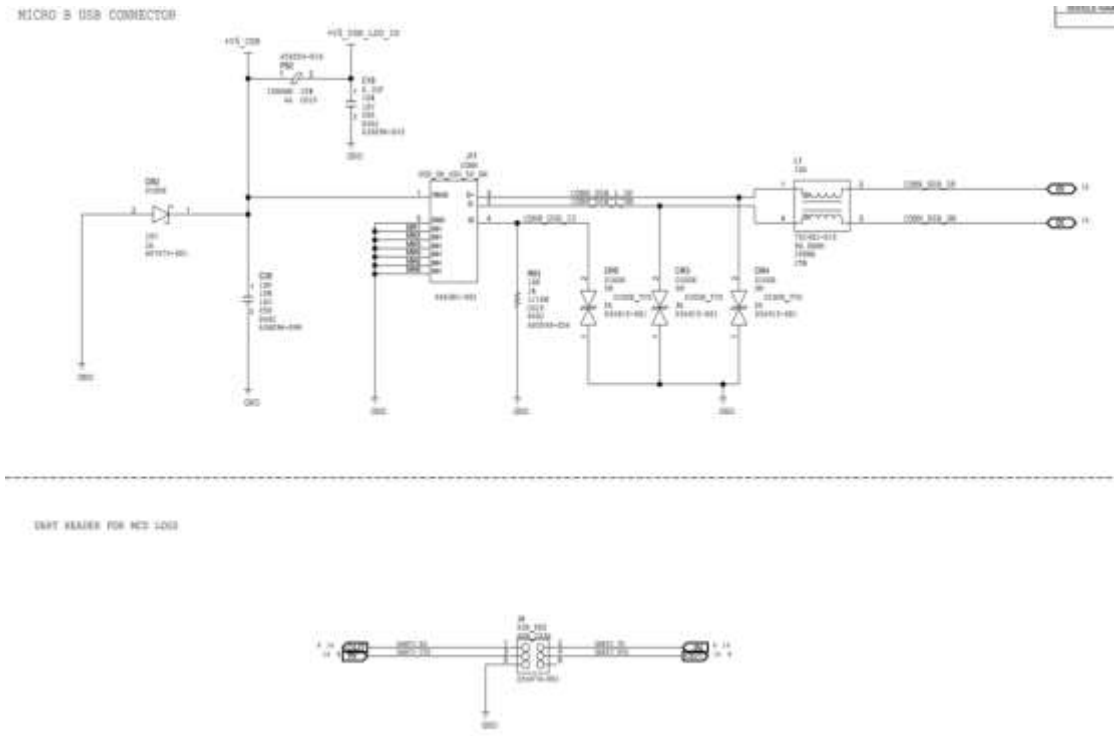

Figure 4.10 USB Connector and UART Header for MCU Logs

Figure 4.10 shows the USB connector used for establishing connection between host device and SMT hardware. Also, there is one more 6 pin header used for sending UART logs from SMT board to the host machine.

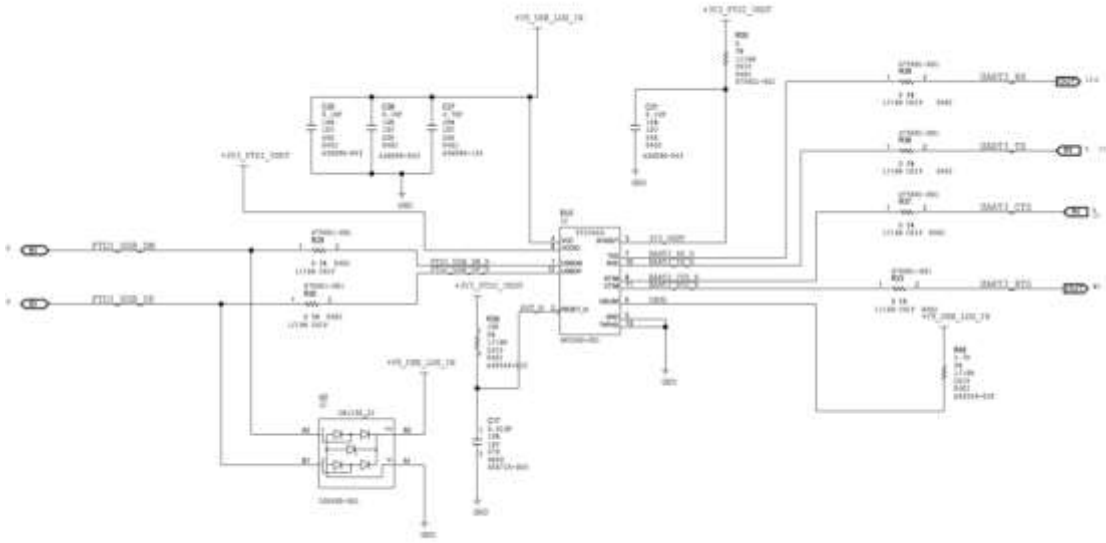

Figure 4.11 FTDI Serial Port

In order to send logs from SMT board to host machine, UART interface is used. To convert these UART signals to USB signals, FTDI chip is used. Its interfacing with components, decoupling capacitor and various connections are shown in Figure 4.11.

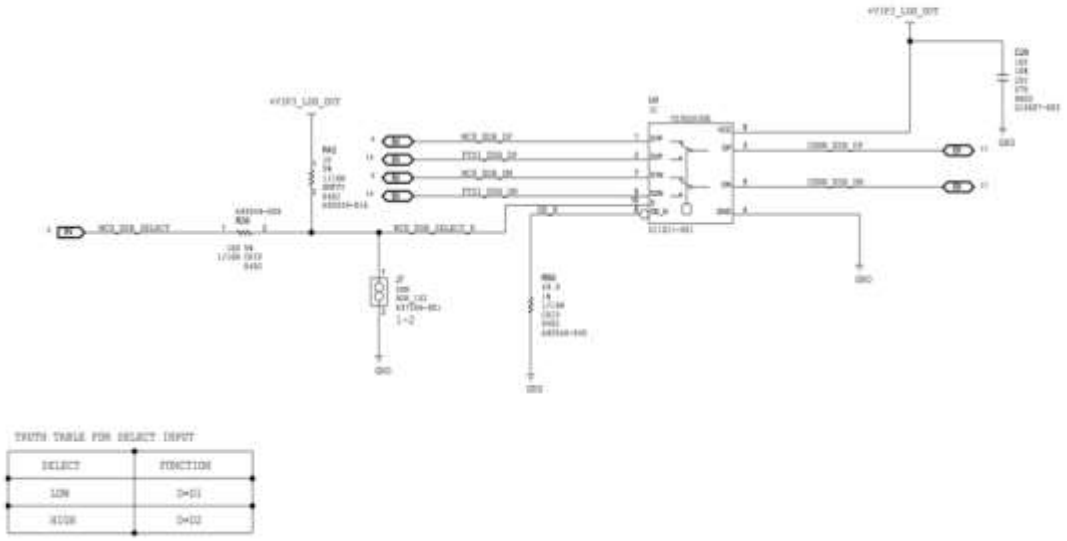

Figure 4.12 USB 2:1 Mux/Demux

There are basically two different USB signals routed in SMT board. One pair of these signals is directly going to the microcontroller and other pair of signals coming out of the FTDI chip. So, for selection of one pair of USB signals out of two different USB signals, USB 2:1 multiplexer/demultiplexer is used. This is shown in Figure 4.12.

4.4 Remote Debugging

Remote debugging, is debugging a piece of code by connecting the application running remotely with your environment of development.

When a hardware component is connected to a device it receives digital data and processes it. The in-built drivers and layers convert the digital data (binary data) into user understandable form.

In this infrastructure the microcontroller (MCU) is connected to a host via USB port. The host accepts the data from the MCU and the data is send to a web server through windows socket interface. An application programming interface (API), windows socket provides

an interface for communication between windows network software and TCP/IP services. The web server stores the state of the memories of the MCU in its database.

On the remote end the user logs into the GUI (Graphical User Interface), an application developed in programming language C++ or Java which retrieves the data of the MCU registers from the web server and displays it graphically. The user can easily accomplish remote debugging, monitoring and controlling by maneuvering the various options on GUI at the client's end.

Figure 3.1 shows the implementation of System Monitoring Tool. The gateway which is used to establish a connection between clients and server is called as Windows Socket and we are using Windows Socket for establishing a connection between platform end and remote end. Platform end is the site where the platform to be monitored, controlled and debugged is connected with System Monitoring Tool and the ultimately to a host machine through a USB. Remote end is the site where engineer sits to debug, monitor or validate a platform through servers.

Windows Sockets are used for connecting servers and clients. Winsock or Windows Sockets 2 allows the programmers to develop advanced Intranet, internet and several other network-capable applications for sending application data across the wire, irrespective of the network standard/protocol being followed. The Windows Open System Architecture (WOSA) model is followed by Winsock. WOSA Service Provider Interface (SPI) standard that defines a model which acts as an interface between different APIs, along with stacks of protocol and exported functions.

The most influential network protocol used across the Internet and corporate networks is IP. The wide range of layered network protocols is represented by Internet Protocol. TCP / IP is often referred to as the Internet Protocol Suite based on two of the most significant protocols that are included in the suite: TCP and IP.

CHAPTER 5

PCB DESIGN

5.1 Stack-up

PCB Stack-up planning is one of the most important steps involved to achieve the best possible performance of a product. The arrangement of insulating and copper layers which makes up a printed circuit board prior to board layout design is called as Stack-up. For SMT board, four-layered stack-up is chosen [15].

5.1.1 Stack-up Requirement

Before proceeding with the details of stack-up, one should understand why stack-up is needed. There are several reasons for stack-up requirement. These are discussed as under:

1. Stack-up is responsible for determination of EMC of a product.
2. It is required in order to meet the SI requirements against reliability and manufacturability of a PCB.
3. It helps in emission of crosstalk, radiations and all different kind of disturbances involved in high speed circuits.
4. Stack-up designs are used to meet the mechanical as well as the electrical performance requirements of a particular design.

There are two kinds of radiations emitted by PCBs. One is Differential-Mode Emission, which means the radiations emitted from the loops present on PCB. The other one is Common-Mode Emission, which means the radiations from the cables connected to the PCBs. In order to reduce these radiations, good stack-up planning is required.

5.1.2 Merits of Stack-up

Stack up helps in improving the performance of PCB. Stack-up has following advantages in PCB creation:

1. More circuity can be created on a single board due to availability of multiple board layers of PCB.
2. A PCB layer stack helps in minimizing the proneness of the circuit towards external noise, interference from other signals and radiations.

3. For high speed layouts, PCB layer stack up also helps in reduction of crosstalk and impedance concerns.
4. Impedance and crosstalk goals are achieved by controlling trace widths, spacing between board layers and thickness of the dielectric medium used between layers.
5. Ease of availability of materials and adhere to assembly necessities.
6. Due to availability of enough space between power and ground layer, there is resultant adequate amount of capacitance which complies with rules of voltage breakdown.

5.1.3 Factors considered for Stack-up

There are multiple factors considered while deciding stack-up for a PCB design. Such factors are the number of layers present in stack-up, the amount spacing between stack-up layers, the arrangement of the stack-up layers, the types and number of power and ground planes used in stack-up. One of the critical factor in deciding stack-up is the numbers of layers. While deciding number of layers for stack-up, one should think of number of signals to be routed in PCB. The frequency of signals, their speed, emission needs, housing needs, EMC should also be considered while deciding layer count for PCB.

Based upon number of layers used for PCB design, there are following two varieties of PCB:

1. Single and two layer PCB
2. Multiple Layer PCB

Multiple layers PCBs are preferred over Single layered PCB due to 15db less radiation produced by multiple layered PCB. For higher frequencies also, multiple layered stack-up is preferred.

5.1.4 Stack-up for SMT

Stack-up chosen for the SMT board consists of four layers. The number of layers are chosen based upon the number of signals, high speed and low speed interface used. The 4 layer stack-up is chosen for SMT PCB fabrication with a thickness of 0.8mm ± 10%. There are two layer impedance 50 ohm and 85 ohm. In PCB design, the trace impedance for single ended signals is considered to be 50 ohm. The impedance seen by differential pair of signals is called as Differential Impedance and the trace impedance for differential

signal for this PCB design is considered to be 85 ohm. Pair of USB signals are differential signals in this design. The size of the PCB is 68 X 53 mm^2. In this PCB stack-up, first layer is mainly used for component placement and silkscreen is placed over this layer. Second layer is ground layer. Layer 2 is chosen to be ground so that shortest path is available for every signal and component placed in layer 1. Layer 3 is mainly designed for power flow and ground. Layer 4 is used for one header placement and few signals routing. The stack-up chosen for SMT is given in Figure 5.1 shown below.

Material: NPG-150								
Layer	Type	Stackup	Thickness		Single End			Differential
					50±10%	50±10% (Coplanar)	50±10% (Coplanar)	85±10%
		Mask	0.6					
L1	Signal	Cu +Plating	1.6	W / S	5 → 4.8	4.8/7.2 → 4.6/7.3	20/7 → 21/6.5	5/5 → 4.8/5.2
				Ω	49.5	49.4 (Ref.L2)	50.2 (Ref.L3)	84.3
		Prepreg	3.2					
L2	Plane	Cu	1.2					
		Core	18					
L3	Plane	Cu	1.2					
		Prepreg	3.2					
L4	Signal	Cu +Plating	1.6	W/S	5 → 4.8			
				Ω	49.5			
		Mask	0.6					
Total Thickness			0.8 mm ± 10%					

Figure 5.1 Stack-Up for System Monitoring Tool

5.2 PCB Design Guidelines

It is possible to draw up multiple ideas and guidelines for the PCB design and layout [16]. Out of those multiple guidelines, few are mentioned under as follows:

5.2.1 Board Constraint Design Guidelines

These are among those basic guidelines to be followed during PCB design that are based on limitations due to board size, appearance, shape and various factor which affect the overall PCB concept. So, these are few factors which need to consider first for any PCB design.

1. Selection of reference points suitable for process of manufacturing: Normally, there are certain reference points or holes that need to be present on the board. These reference points and holes are used for machine placement and fixtures testing. These must not be obscured by any component.

2. Allowance of sufficient area for the board: In order to accommodate all the components that need to be assembled on board, a rough approximation should be made prior to PCB design.
3. Determination of number of layers needed: It is always worthy to determine number of layers to be decided prior to PCB design in order to have cost effective design. However, number of layers can be increased later based upon the requirements.
4. Consideration of mounting technique of Board: It is always necessary and wise to decide the way PCB will be mounted in the beginning stage of the design, otherwise it may lead to lot of rework and manual efforts to redesign the PCB.

5.2.2 Overall Layout PCB Design Guidelines

While deciding PCB layout design, one should start by considering major components placement in the board. Placement of main or larger components is one of the critical steps involved in PCB design. This will lead to smooth designing and judging of PCB layout.

5.2.3 Guidelines associated with Layers

For earth or power rails, a complete layer or plane is commonly used. The effective methods must be carried out early in the PCB design.

1. ***Considering complete planes for power, earth, etc.*** Generally, a complete plane is used for earth and some power rails. It is beneficial in terms of noise removal and current capability.
2. ***Avoiding of partial planes*** Large gaps must not be left in earth planes or power planes, or partial planes in a certain board area. These gaps can build up stresses in the board which may lead to warping during bare board manufacturing, or even later during the soldering process. If warping occurs after the addition of surface mount components, it may result in component fractures which eventually leads to a great rate of functional failures.

5.2.4 Track Design Guidelines

Consideration about the aspects of the tracks on the printed circuit board themselves needs to be given at an early stage as there are trade-offs that may need to be made.

1. ***Determining the width of standard track to be used*** The balancing of the standard track size is quite vital for proper functioning. Excessive thin tracks that are too close may lead to short occurring. On the contrary if the tracks are too wide and fairly apart then in a given area it can certainly limit the number of tracks. As a result of which additional planes are used in the boards for ensuring the routing of PCB design.
2. ***Considering track size for current carrying lines*** Presently the PCBs comprise narrow tracks which can only carry a limited current. The tracks carrying power rails should be considered than the tracks carrying low level signals. The Table 5.1 below gives some track widths or a 10degree C temperature rise for different thickness copper boards.
3. ***Fixing the PCB pad to hole ratio and size*** The pad and hole dimensions are decided at the beginning of PCB design. Typical value of the pad to the hole ratio is about 1.8: 1. Sometimes a pad 0.5 mm larger than the hole is used which allows for hole drilling tolerances, etc. The bare PCB manufacturer is able to direct on the standards required. The ratio plays a key role when the pad size and hole size reduces.
4. ***Determining the shapes of PCB pads*** PCB CAD systems have component libraries for the schematic and PCB footprints for the various components. As per the manufacturing process pad shapes may vary. The pad size for wave soldering is larger than infra-red reflow soldering. Thus it is necessary to determine the manufacturing process before the start of design in order to choose the optimal pad size so that it can be used on PCB CAD system and finally on PCB itself.

S.No.	Current (Amps)	WIDTH FOR 1 OZ BOARD (THOUS)	WIDTH FOR 2 OZ BOARD (THOUS)
1	1	10	5
2	2	20	15
3	3	50	25

Table 5.1 Recommended Maximum Currents for PCB Tracks [16]

5.2.5 Thermal Issues

Thermal issues are not a concern for many smaller PCBs but as the processing speeds are increased and components are closely packed in the case of modern PCBs, thermal issues present a serious threat.

Allowing adequate space for cooling around hot components Components dissipating huge amounts of heat do require sufficient space around them for cooling. In case if heatsinks are needed around, enough space should be provided.

5.2.6 Signal Integrity and RF Considerations

Many issues associated with PCB design are related to Signal integrity, RF and EMC considerations. Many problems can be avoided by intelligent routing of tracks [16].

Avoid running tracks in parallel Tracks of any length running in parallel have a greater level of crosstalk with signals flowing on one track appears on the other. The presence of crosstalk in the circuit gives rise to a wide range of problems and it becomes very difficult to eradicate crosstalk after the designing and manufacturing of PCB.

Crossing of tracks at right angles To minimize the crosstalk level generated in the circuit, the crossing of two signal lines should be made at right angles so that the capacitance level and mutual inductance between the signal lines get reduced.

The PCB design guidelines mentioned above give the insight on guidelines for general PCB designing.

Signal integrity has become a very important factor of circuit and PCB designing. As the frequency of operation in digital circuits increases, the short connections start acting as transmission lines, which has an adverse effect on the integrity of signals flowing in the circuit. The nature of purely digital signals is altered by effects that may be thought of as applying to the analog domain. These effects cause the circuit to be dysfunctional and hence signal integrity has become a key issue for circuit designing.

In the world of high speed processors, to maintain the signal integrity intact it is imperative to include design simulations and checks during the process of PCB designing. Circuit boards should undergo signal integrity engineering. If the checks are not carried out during the PCB design, not much can be done once the board has been developed. In this perspective the PCB design packages include signal integrity engineering and checking options which enable the circuit checks as the design develops. In this manner

the optimization of PCB layout is achieved and it is ensured that signal integrity is properly engineered so that the problems are minimized once the developed PCB undergoes testing.

5.3 Signal Integrity Issues

In order to maintain the signal integrity of a circuit following four major areas of circuit layout and design must be taken into account:

1. Transmission line effects
2. Impedance matching
3. Simultaneous switching effects
4. Crosstalk

For maintaining the signal integrity and ensuring that the signal is not corrupted the above mentioned issues are addresses in the below sections.

5.3.1 Transmission Line Effects

In the low frequency regime, the track length may be characterized by its DC characteristics.

With the increase in the frequency, the capacitance and inductance effects related to the track start impacting the line performance. The tracks should be considered as transmission lines and treated accordingly. The characteristic impedance of the line should be maintained same across the entire length otherwise discontinuities are introduced. These discontinuities are responsible for signal reflections which give rise to problem of ringing and hence poor signal integrity.

In order to carry out the proper treatment for transmission lines firstly there should be a ground plane underneath the lines. Impedance calculation is also necessary which is achieved from a combination of line thickness, the separation between the ground plane and the line, and the relative permittivity of the board. Sometimes the line is traversed between layers due to which the separation between line and the plane changes.

5.3.2 Impedance matching

Considering the fact that the PCB lines act like transmission lines when the frequencies are raised, for maintaining a good signal integrity the impedance matching should be done

successfully. The mismatch between the line impedance and load impedance results in reflection of some energy of the incident signal back along the line. The reflected signal may not again be absorbed if there exists a mismatch between source and line. This may result in ringing and overshoot leading to signal errors.

This problem can be alleviated by matching the transmission line to line drivers and receivers. By putting a resistor down to ground, the parallel combination of line receiver and resistor can equal the line impedance. Special line drivers are used since they exhibit higher driving capability and supply the current for the proper driving of lines. Clamping diodes are added in some applications to decrease the overshoot and undershoot levels and thus maintaining the signal integrity.

5.3.3 Simultaneous switching Effects

The simultaneous switching of many output lines can violate the signal integrity on a PCB. As the charge stored on the output lines discharge, high magnitudes of transient currents are generated. When a single output changes the level of transient is low but simultaneous switching of several lines in the same chip gives rise to larger transient currents which creates problems. Problems occur because of voltage generation between device and board grounds. The signal switching levels exceed if the rise in the chip ground is sufficient resulting in spurious switching.

One of the ways to uproot this problem is to avoid simultaneous switching but it is not always feasible especially when the operation of the circuit is carried out in a synchronous manner. There must be a ground plane for low resistance ground return. Sufficient decoupling across the chip may also help.

5.3.4 Crosstalk

This issue arises from the fact that signals flowing on a line appear on the neighboring lines. As a result of which clock pulses or erroneous data appear and in some situations it could be very difficult to track down. Mutual capacitance and mutual inductance are the two factors of crosstalk that hamper the signal integrity.

The effect of mutual inductance is utilized in transformers. The current flow in one track establishes a magnetic field and any change in this magnetic field induces a current in the adjacent track. The electric fields in two tracks when couple together they create mutual

capacitance. Voltage in one track generates an electric field which coupled to a nearby track. Fast edge voltages result in identical edges that appear on lines nearby.

There are many methods that can be employed to mitigate these effects. By reducing the mutual capacitance and inductance the signal integrity can be raised. The layout should be arranged by keeping these factors in mind. If possible parallel running lines should be avoided. In case if lines need to be crossed, the crossing should be made at right angles. Line spacing should be large and by using thin lines mutual capacitance can be curtailed. Finally, transmission lines should be kept very close to the ground plane to reduce coupling to lines present in the vicinity.

5.4 SMT PCB Layout Capture

PCB Layout refers to high level board design engineering tool featuring intelligent manual differential and high speed signal routing, complex verification, and extensive export or import capabilities. For PCB design of System Monitoring Tool, firstly schematic design is done using the Cadence Concept HDL designing tool. After drawing schematics, the layout is prepared in a production environment provided by the Allegro PCB designer. This takes complex and simple designs from Concept to production environment and also ensures the functionality, feasibility, and manufacturability of the PCB design. The stack-up chosen for System Monitoring Tool is four layered, having signals routing and components placement on the top and the bottom layers. Second layer is meant for providing ground. Second layer is chosen as ground layer so that shortest grounding path can be provided to multiple signals present in SMT PCB board. Third layer in SMT PCB stack-up is meant for providing power and ground to the board. Power available on SMT board are 5V and 3.3V. Also, above top layer, there is another layer made up of silksreen. Silkscreen consists of label names, components and connector reference designators used in schematics design to be printed in white color on SMT PCB. Also, multiple vias are used in the layout to establish connectivity between the signals going through different layers. The current carrying capacity of a copper trace in PCB is directly proportional to the cross sectional area of the trace. Under the temperature rise of 10°C, one ounce of copper with a trace width 10 mils is capable of carrying 1A of current. Various snapshots are taken for SMT PCB design developed on Allegro PCB Designer tool which are shown in below figures.

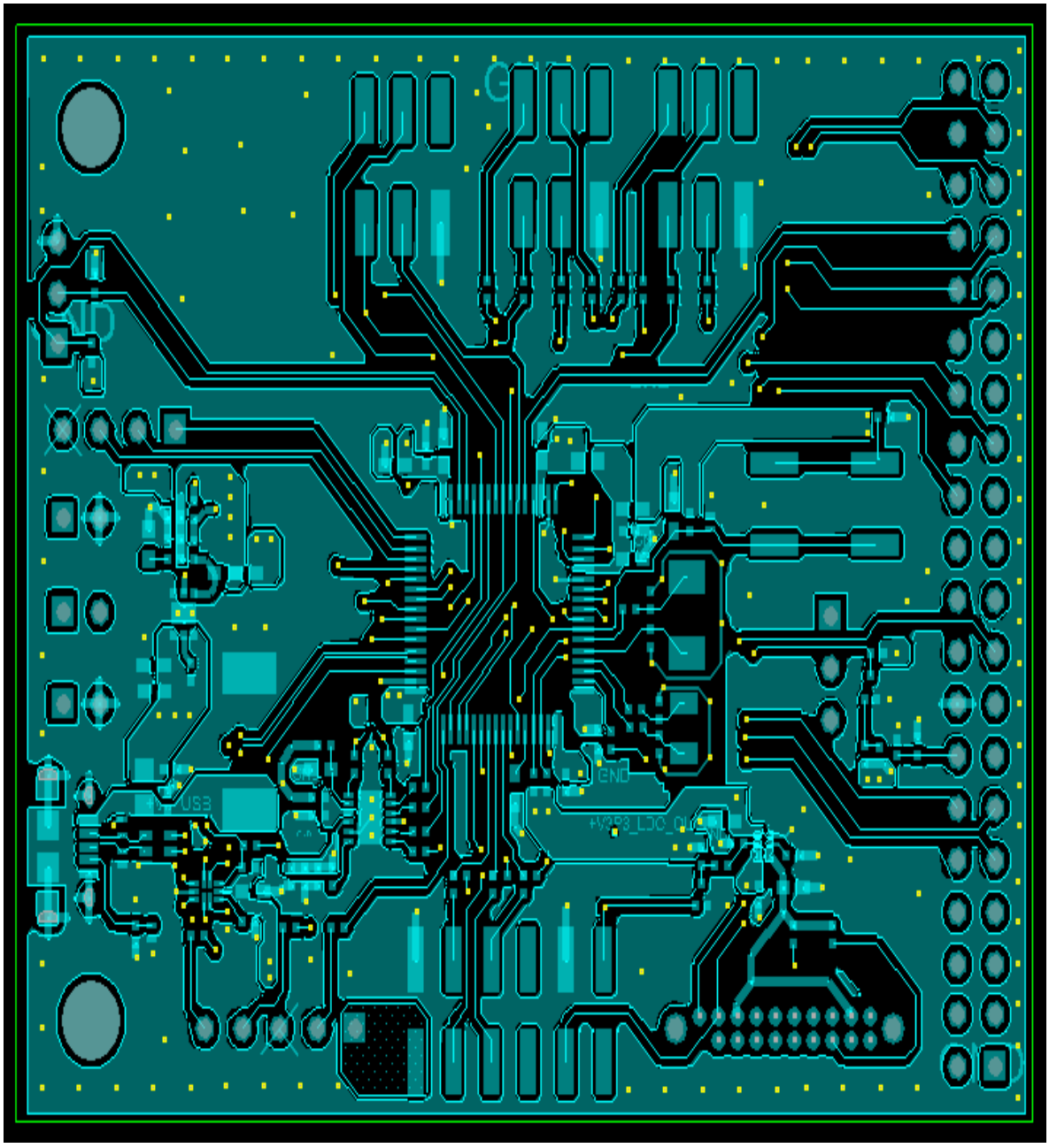

Figure 5.2 Layer1 in SMT Stack-up used for signal routing

The top layer in PCB stack-up of System Monitoring Tool is shown in Figure 5.2. This layer is actually used for multiple components placement and various signals routing in

SMT PCB. Majority of the signals are routed through this layer. Also, vias are used to provide connectivity among signals if they are going through different layers.

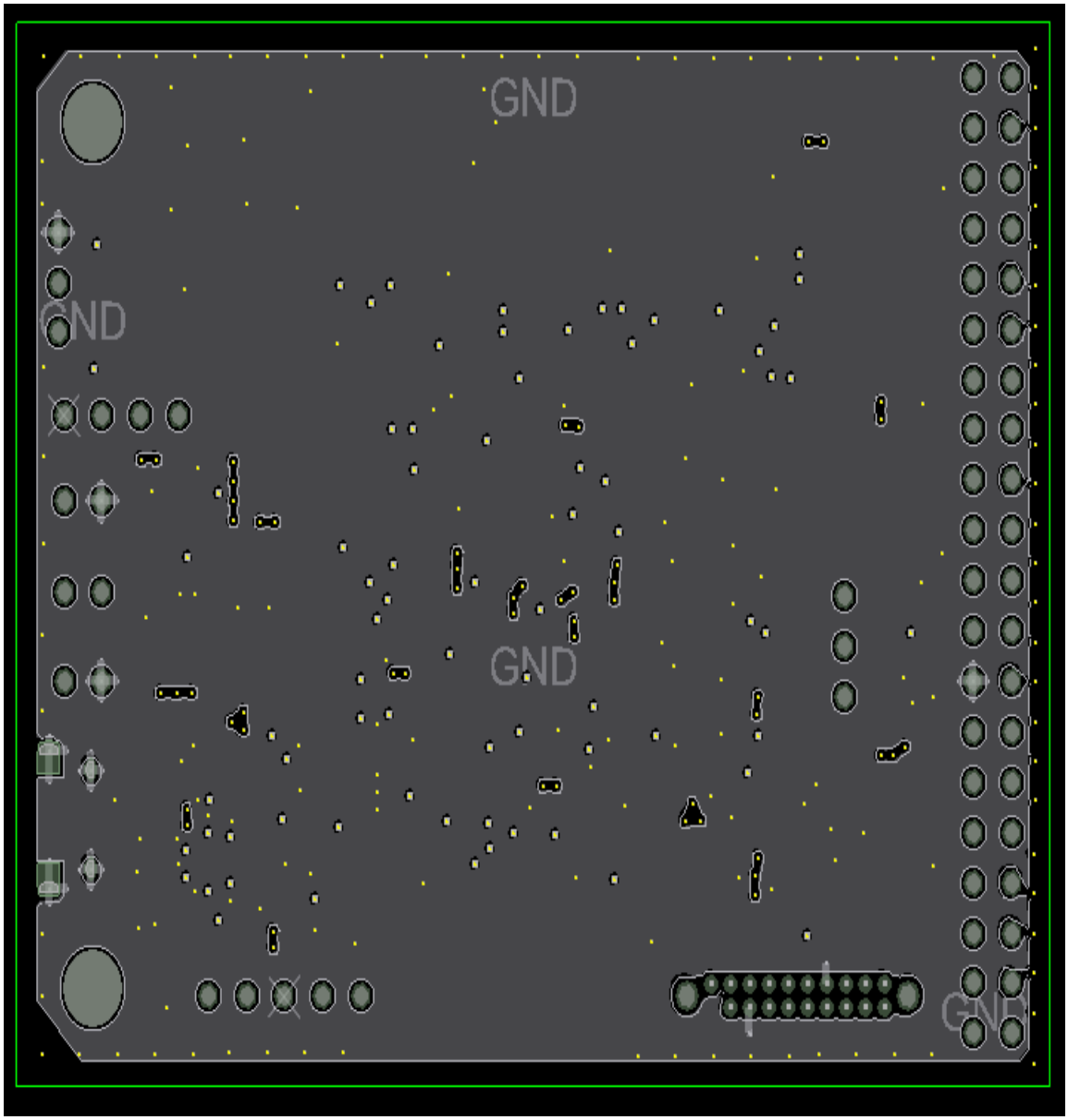

Figure 5.3 Layer2 in SMT Stack-up used for Grounding

The second layer lies exactly next to the top layer in PCB stack-up of System Monitoring Tool is shown in Figure 5.3. This layer is actually used for providing nearest ground to all signals present in top layer of SMT PCB. Signal path to the ground is always recommended to be the shortest path to avoid interference that could generate from multiple signals.

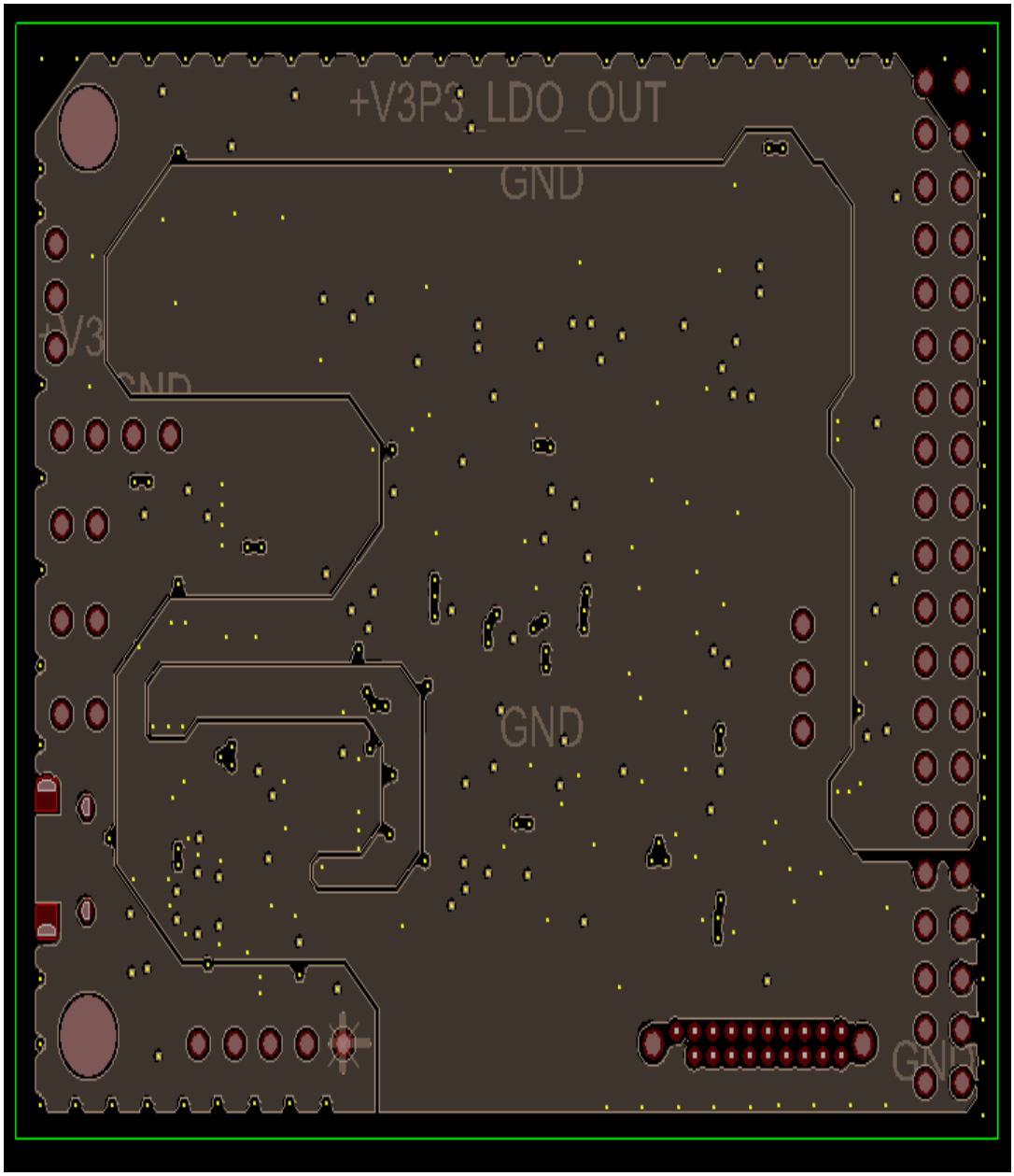

Figure 5.4 Layer3 in SMT Stack-up used for Power and Ground

The third layer lies exactly next to the second layer in PCB stack-up of System Monitoring Tool is shown in Figure 5.4. This layer is actually used for providing power to all power requiring components present in top layer of SMT PCB. There are two kind of power flowing in this layer. One is provided through 3.3V supply and other is provided through 5V supply. This layer also provides path to ground to various signals.

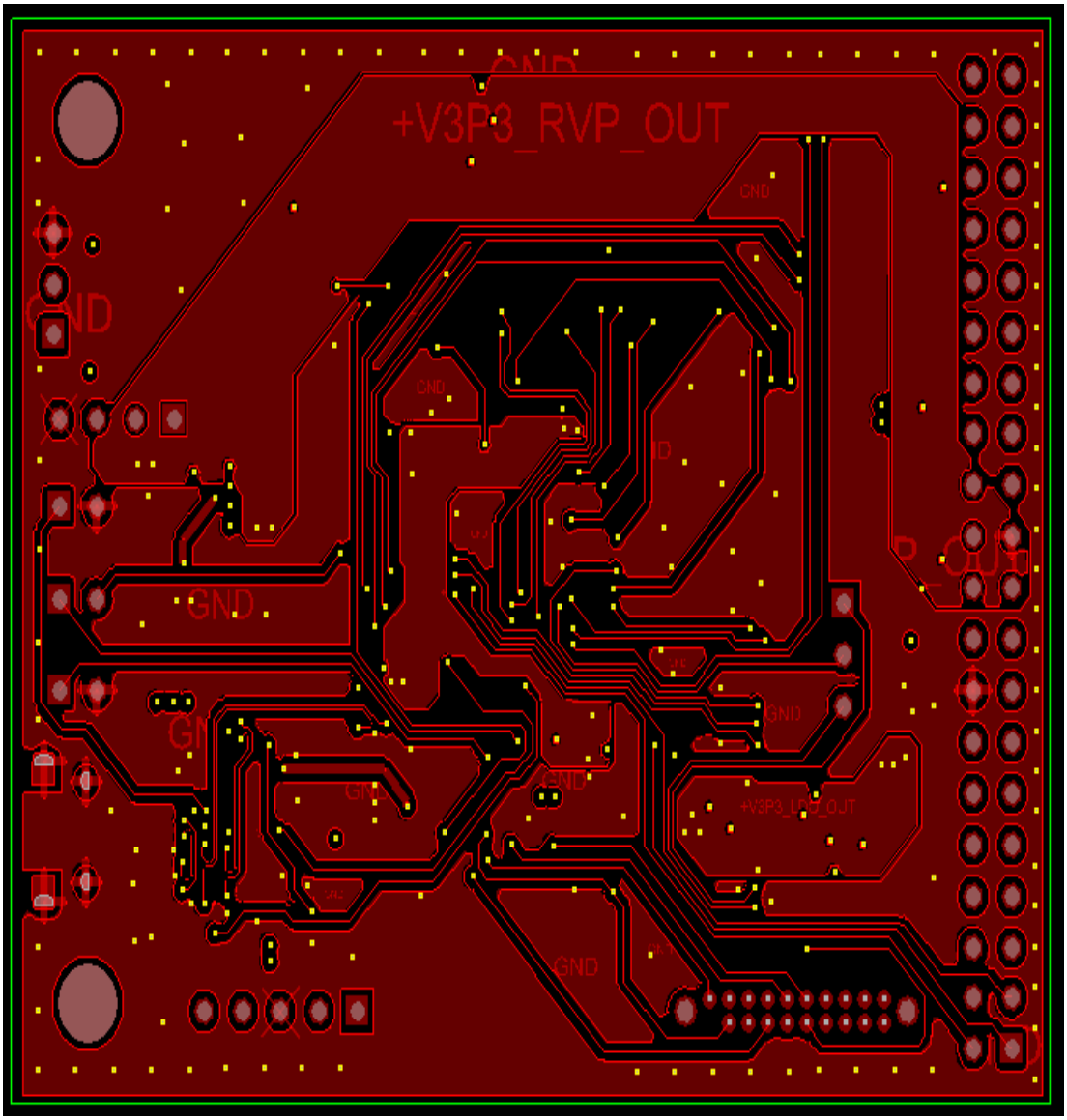

Figure 5.5 Layer4 in SMT Stack-up used for Signal Routing and Component Placement

The fourth and last layer lies exactly next to the third layer in PCB stack-up of System Monitoring Tool is shown in Figure 5.5. This layer is actually used for routing of multiple signals in SMT PCB. This layer is also used for placement of only one 40 pin header. Placement of this header is bottom-sided in SMT PCB.

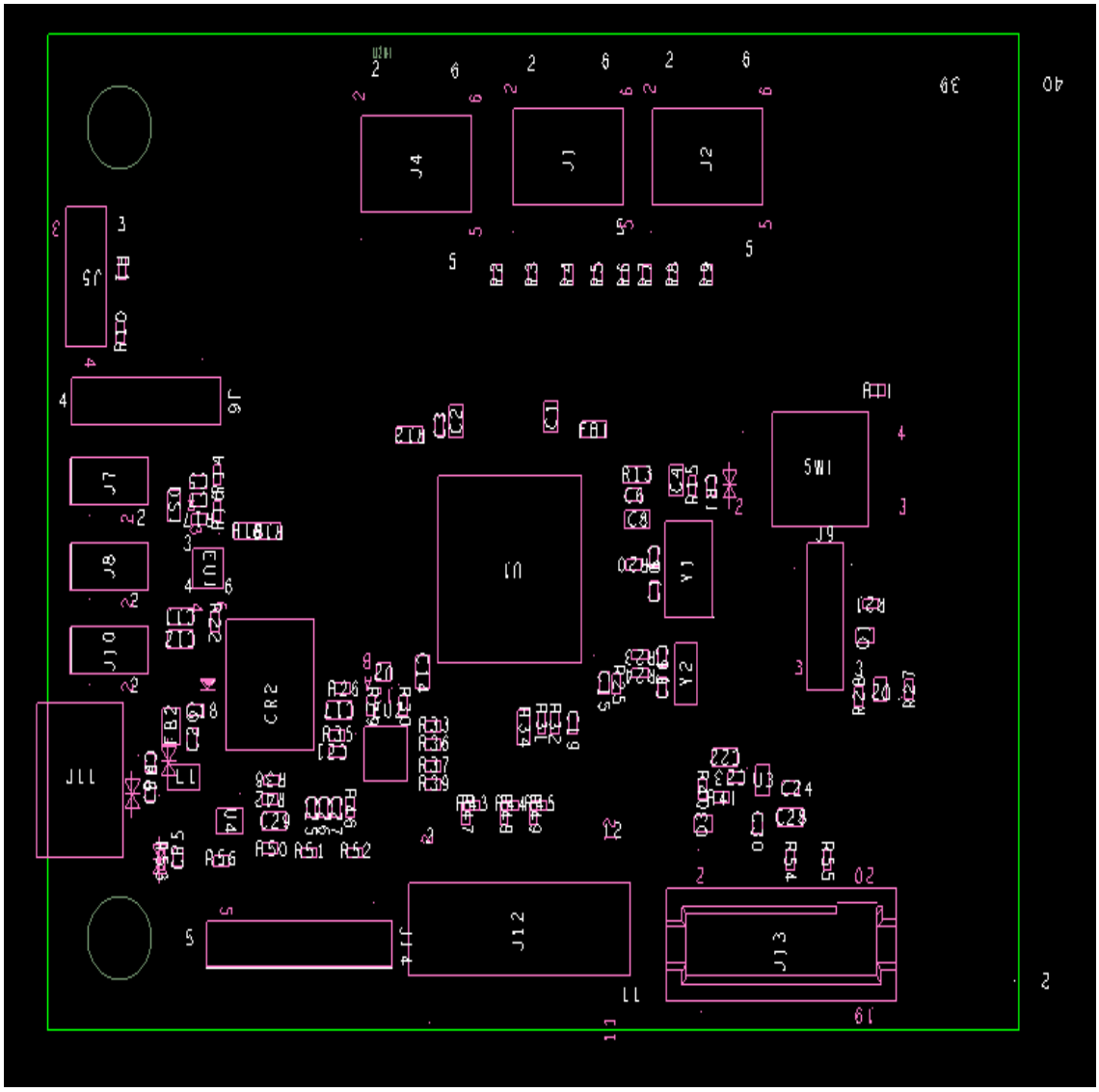

Figure 5.6 Silkscreen Layer in SMT

There is another layer lies exactly above to the top layer in PCB stack-up of System Monitoring Tool is shown in Figure 5.6. This layer consists of label names, components and connector reference designators used in schematics design to be printed in white color on SMT PCB.

In order to understand the trace width requirements for particular current carrying capacity as per temperature rise, Table 5.2 could be referred.

Temp rise	**10°C**			**20°C**			**30°C**		
Copper	**0.5oz**	**1.0oz**	**2.0oz**	**0.5oz**	**1.0oz**	**2.0oz**	**0.5oz**	**1.0oz**	**2.0oz**
Trace width (inch)	**Max. current amps**								
0.01	0.5	1	1.4	0.6	1.2	1.6	0.7	1.5	2.2
0.015	0.7	1.2	1.6	0.8	1.3	2.4	1	1.6	3
0.02	0.7	1.3	2.1	1	1.7	3	1.2	2.4	3.6
0.025	0.9	1.7	2.5	1.2	2.2	3.3	1.5	2.8	4
0.03	1.1	1.9	3	1.4	2.5	4	1.7	3.2	5
0.05	1.5	2.6	4	2	3.6	6	2.6	4.4	7.3
0.075	2	3.5	5.7	2.8	4.5	7.8	3.5	6	10
0.1	2.6	4.2	6.9	3.5	6	9.9	4.3	7.5	12.5
0.2	4.2	7	11.5	6	10	11	7.5	13	20.5
0.25	5	8.3	12.3	7.2	12.3	20	9	15	24

Table 5.2 Relation between Temperature rise, trace width of copper and Current Carrying Capacity [17]

The current carrying capacity of copper trace width is determined by the temperature rise and cross sectional area of the trace. Also, cross sectional area of the copper trace is directly proportional to width and thickness of the copper trace. Keeping in mind the current requirements of various signals in System Monitoring Tool, trace widths of copper are chosen for designing SMT PCB layout.

CHAPTER 6

PCB TESTING AND VALIDATION

ICT is an instance of white box testing in which an electrical probe checks a populated PCB, checking for opens, shorts, capacitance, resistance and other fundamental quantities to demonstrate whether the assembly has been properly manufactured.

The broad and diverse areas of PCB applications demand one thing – PCBs must work in accordance with their design parameters without any failures or errors. The working of PCBs must be flawless since they are employed in many high stake applications. The presence of hundreds of components and solder connections make the PCB very complex. The PCB manufacturers implement a wide range of inspection and testing methods to maintain the quality of their products. The device reliability and the yield is augmented by carrying out the testing and inspection of each PCB based on its design specifications.

Since every manufacturing environment is different so there is no single PCB testing system that works for every PCB. Hence to devise a PCB testing system many factors are taking into account and is product specific. If a product is well developed and fully functional then minimum debugging and testing is needed. While complex PCBs using surface mount technology (SMT) requires intricate details for testing.

There are two types of PCB testing: Functional test (FCT) and in-circuit test (ICT).

6.1 Functional Test:

Functional test is the last step in manufacturing of PCB. It approves the PCB before it gets shipped by tagging the PCB pass or fail. The purpose of the FCT in the manufacturing step is for the validation of the product hardware. To check it is not prone to defects which could hamper the functioning of the product in the system application. To be precise, the functionality and behaviour of a PCB is verified using FCT. It should be noted that requirements, development and procedures of the FCT vary from one PCB to other.

The functionality of the PCB is tested by interfacing a functional tester to the PCB through its edge connector or a test-probe point. After this the final environment of the PCB is reproduced. For example, if a PCB is positioned in a computer slot, then the slot

going to be occupied by the PCB is simulated by the functional tester (inputs, outputs, etc.).

The commonly used functional test form, called the hot mock-up simply validates the PCB functioning. The other types of functional tests involve PCB cycling through a huge number of operational tests. Functional testers are product specific and for testing different products different functional testers are needed. The testing manufacturers are trying to standardize for keeping the costs in control. The tester comprises a cabinet, a DUT interfacing, cabling for connecting the instruments, a CPU and monitors. Depending on DUT and the environment there is variation in hardware but the hardware typically comprises instrumentation and power supplies. Functional testing depends on DUT so the investment of money and time is imperative to achieve success.

FCT simulates the operational environment of the product to check its functionality. Several signals and power supplied are operated directly on PCB. Responses are observed at some specific points to check the functionality. The OEM test engineer defines the standards and procedures needed for carrying out the test successfully and under his guidance the test is executed. This test is highly convenient for the detection of the incorrect values of the components and different functional and parametric failures.

The functional line operators execute the functional test via a computer using a test software known as firmware. In doing this, the test software establishes communication with the external programmable instruments.

Advantages to the customers:

- This method reduces the cost for the customer because FCT reproduces the product operating environment. So the customer does not have to present the actual testing equipment.
- The functional defects within the PCB are identified and the power consumption of DUT during the operation is also measured.
- In some cases, the time and financial resources of the OEM are saved owing to the elimination of the high-priced system tests.

- It checks the product functionality anywhere in the range from 50% to 100%. Therefore, the OEM can save a lot of time and effort required for checking and debugging.
- FCT enhances the ICT and flying probe test, thus the product becomes less prone to errors and more robust.

6.2 In-circuit testing:

In-circuit equipment measures each component and checks that the component is in right place and is of correct value. The majority of the faults on the circuit board originate during the manufacturing and usually involve short and open circuits and incorrect components. ICT catches majority of the problems on PCB. One of the major reasons of the failure of the ICs is the static damage that appear in the areas close to the IC and these faults are easily detected using in-circuit test methods.

In-circuit test equipment comprises following elements:

- *In circuit tester:* For the purpose of setting up and performing the measurements the ICT system contains a matrix of sensors and drivers. The count of the driver sensor points may reach 1000 and even more. These points are taken to a big connector.
- *Fixture:* The ICT system connector interfaces with the fixture. The designing of the fixture varies from board to board and it plays the role of interfacing the board and the in circuit tester. It routes the driver sensor points directly to the concerned points on the board.
- *Software:* For different types of boards to be tested software is written. The software directs the test system on performing different tests between relevant points and the results of the pass/fail criterion.

ICT can be performed with a bed-of-nails test fixture or with a flying probe setup. A bed-of-nails tester consists of an array of spring loaded pogo pins. With a node in the circuit of the DUT each pogo pin makes a contact. When DUT is pressed against the pins contact is established with thousands of test points within its circuitry. The drawback of this approach is that its developing is expensive and is difficult to change. Furthermore, the

testing of boards having high density of components is difficult to achieve using these fixtures.

Another method for in circuit testing involves a roving or flying probe. The board is held by a simple fixture and the probes move around the board and when required contacts are established. The software controls the movements of the probe and any board updates can be easily accommodated by simply changing the programming. Unlike the functional testing ICT does not check the board functionality. ICT is totally based on the assumption that if the PCB designing and assembling is carried out correctly then it should work flawlessly.

In circuit test merits:

- *Easy detection of manufacturing defects:* Since most boards problems originate in manufacturing- insertion of wrong component, incorrect values of component, wrong orientation of transistors or ICs, open circuits and short circuits etc. All these effects are easily identified using ICT as the tester carries out the checks on components, continuity etc.
- *Simple generation of programme:* The programming of the in circuit tester is very easy. By taking the files from the PCB layout most of the programme is developed.
- *Easy interpretation of the test results:* The system flags a particular node either short or open circuited, or flag a specific component as being faulty- this does not demand highly dexterous test staff.

In-circuit test demerits

- *Costly fixtures:* The fixtures are mechanical and need wiring assembly which can be costly.
- *Difficulty in updating fixtures:* The fixture is a mechanical item with the probes mechanically fixed. If any update in the board requires the contact points to be repositioned it could be very costly.
- *Difficulty in test access:* With the ever decreasing size of the boards, the access to nodes is becoming very challenging. Because of the miniaturization the special

contact points available in an ideal system are hardly available. Some nodes may have contact points which are not even accessible.

CHAPTER 7

CONCLUSION AND FUTURE ASPECTS

Validation of a platform developed for any electronic device from the remote location requires heavy infrastructures and ultimately cost of such infrastructure. So, debuggers face many limitations to debug failure if they can't physically reach the platforms. Typically, there is a critical requirement that debuggers should continuously test their codes to debug an issue during the development process itself. But, it's unfortunate that all the developers don't sit next to platforms all the time. So, debug limitations, constrained platforms, easy way to extract power information are among the few challenges that design engineers face during platform monitoring and its validation. In this dissertation work, we propose an architecture of a remote debugging tool that helps in monitoring as well as debugging the platform from the remote end. This remote debugging tool acts as an interface between a targeted platform and a host machine. In our proposed tool, we have developed a small add-in card that could be connected to the platform to be validated or monitored. Then, this add-in card is responsible for the collection of the data from the platform first and then it could send the data to a remote location through servers.

The Results for the system are listed below but not limited to these.

1. Get the boards fabricated with the final Gerber.
2. Use these systems to deploy remote system debug and monitoring options for next-gen Intel SoC.
3. Scale this solution to customer platform, thereby making debug / system triage easier.

The top view and side view of SMT PCB is shown in Figure 7.1 and Figure 7.2 respectively.

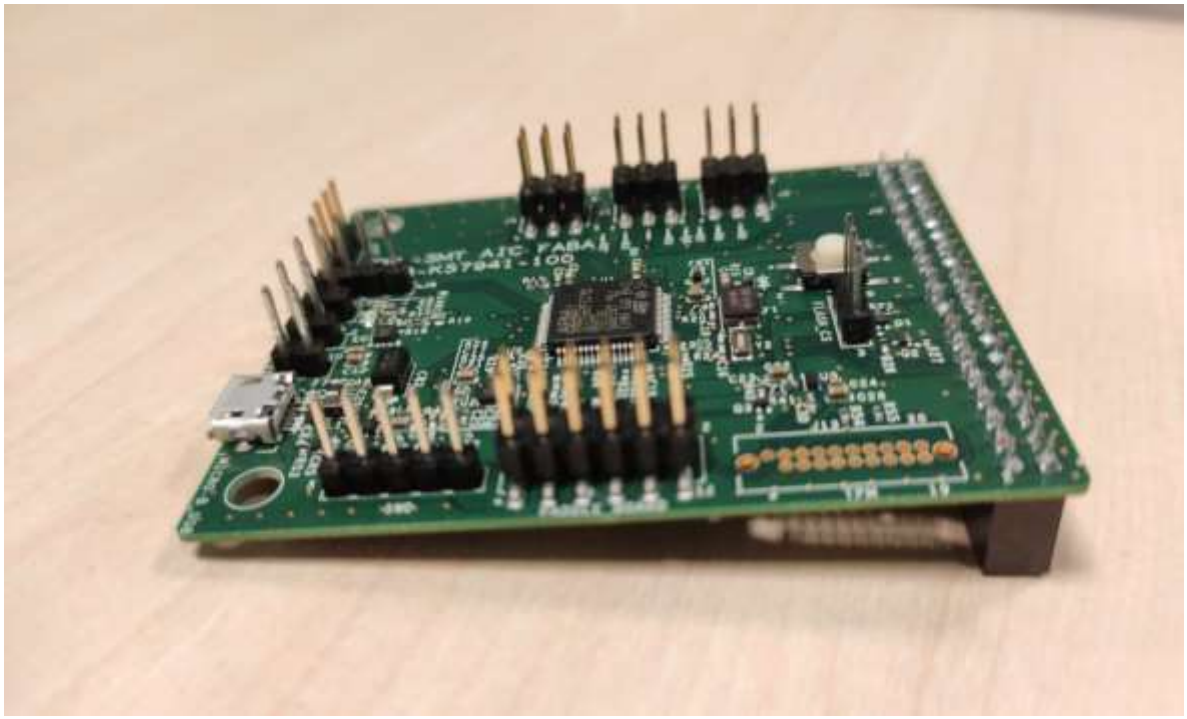

Figure 7.1 SMT PCB Side View

Figure 7.2 SMT PCB Top View

After discussion of results and conclusion, let us discuss some of the future scopes of this dissertation work. A huge set of use cases get enabled with the advent of this card. We plan to enable more features onto the product like JTAG so that validation/testing

becomes easier. The addition of Ethernet or some other connectivity solution onto the card can directly enable the system to talk to the server/cloud without the involvement of a host machine.

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