LOW FREQUENCY NOISE REDUCTION IN ANALOG CMOS IC

A thesis submitted in partial fulfillment of the requirements

for the degree of Master of Technology

in VLSI Design

by

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Under the supervision of

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Certificate

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology, Jaipur

This is to certify that the thesis work entitled " **LOW FREQUENCY NOISE REDUCTION IN ANALOG CMOS IC**" has been carried out by **Teena Meena** for the degree of Master of Technology in VLSI Design at Malaviya National Institute of Technology under my supervision.

The thesis in my opinion, is worthy of consideration for award of the degree of Master of Technology (M.Tech) in accordance with the regulations of the Institute. To the best of my knowledge, the results embodied in this thesis have not been submitted to any other University or Institute for the award of any other Degree or Diploma.

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June 2019

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Abstract

Compared to other technology, analog performance of CMOS technology is not good. If we are going to design a high performance analog IC using CMOS technology, there are many drawbacks, which we have to overcome. If we are going to design an analog circuit using CMOS technology, then there is only one advantage that the system could be low cost. From the early research it is found that for the flicker noise reduction, if we implement the architecture using device physics effect. It will cause the reduction of flicker noise, because in this technology, MOS transistor fluctuates between two states.

That is the inversion and accumulation region. This on-off switching of MOS transistor causes the reduction of flicker noise. In this thesis the basic principle of flicker noise reduction in two stage op-amp is discussed. Here is the detailed discussion of the main idea behind the implementation of the proposed two stage operational amplifier, design consideration etc. The functioning of COMPLEMENTARY SWITCHED MOSFET is also disused. Here we will measure the flicker noise in classic operational amplifier and proposed two stage operational amplifier.

Contents

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Abbreviations

1/F	**F**licker **N**oise
VGS	**G**ate **T**o **S**ource **V**oltage
VT	**T**hreshold **V**oltage
GM	**G**ain **M**argin
PM	**P**hase **M**argin
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
Fc	**C**orner **F**requency
VGSon	**G**ate **T**o **S**ource **O**n **V**oltage
VGSoff	**G**ate **T**o **S**ource **O**ff **V**oltage

Chapter 1

Introduction

1.1 Motivation

Now a days, CMOS technology is common in analog-mixed signal and radio frequency applications. This technology provides high power saving on digital part of a chip. Scaling down active area of MOSFET in CMOS technology is equal to enhancement of analog mixed signal and radio frequency performance of device. There are so many advantages of CMOS technology, but this technology is highly noisy, because this technology shows higher flicker noise. In CMOS circuit, there are several techniques for flicker noise reduction. There are some methods to reduce 1/f noise from the circuit. Chopper stabilization and correlated double sampling are two known techniques to minimize flicker noise. But these two techniques are only for low frequency circuit applications. Other method is enlarging active area of MOSFET. But this technique decreases the performance of the device. These days device-physics effect is widely used technique for flicker noise reduction. This effect defines the on-off switching of MOS transistor, which leads to reduction of flicker noise.

1.2 Related and Previous Work

In this section, flicker noise reduction techniques in analog CMOS IC'S will be discussed. There are so many techniques of flicker noise reduction in MOS devices. Enlarging active area of MOSFET can reduce the flicker noise. Other methods are CDS (correlated double sampling) and CHS (chopper stabilization). Device-physics related effect technique is the new method for 1/f noise reduction.

1.3 Switched Bias Technique

This switching technique of MOSFET between strong inversion and accumulation region for noise reduction in CMOS circuit is first given by Klumperink of Twente University in the Netherland. This principle is named "the switched bias technique". This switched bias technique is applicable in a circuit, in which a bias current is needed only during a certain time interval. Oscillators are these type of circuits, because transistors in an oscillator are the circuits which contribute to the operation of the circuit during only a fraction of the period of oscillation. The viability of this technique is illustrated in a six stage coupled saw tooth oscillator working at 120 kHz. Each stage of saw tooth oscillator produces a rising ramp voltage across the capacitor. Phase noise in the saw tooth oscillator is basically because of the noise, present on the capacitor's charge current. When the power consumption is reduced by more than 30%, then flicker noise-induced phase noise is reduced by nearly 8dB. This technique is not applicable for discrete-time circuits. This is only suitable for continuous signal processing circuits (e.g. operational amplifier).

1.4 Scope

The technique of low frequency noise reduction in linear analog CMOS IC'S is suitable for a continuous signal processing operation. The main purpose of this technique is flicker noise reduction in CMOS IC'S. Now a day's Device physics-based effect method is mostly used technique. In MOSFET mainly four types of noise is present i.e. Nyquist noise (also

called thermal noise or Johnson noise), shot noise (also called Poisson noise), generation-recombination noise, and flicker noise (low frequency noise). In chapter 2 of this thesis, setup for low flicker noise reduction principle in CMOS IC'S and censorious issues in measuring 1/f noise is discussed. In which, the main principle of 1/f noise scaling down technique in linear analog CMOS IC'S that is suitable for a continuous signal processing operation, using the device physics-based effect is discussed. This effect defines on-off switching of MOSFET. This 1/f noise reduction technique is detailed discussed from works of literature. A mathematical description for the 1/f noise scaling down behavior is also described here. Later on, 1/f noise reduction principle, "complementary switched MOSFET architecture" is described for a CMOS IC. In the next chapter the several issues in the physical implementation and the design consideration of the two stage CMOS miller operational amplifier are discussed. A modified two stage operational amplifier is implemented. This is also discussed with some mathematical elucidation. In upcoming chapters, classic op-amp and modified two stage operational amplifiers are discussed.

Chapter 2

Fundamentals of Noise

2.1 Introduction

The information signal in wireless communication is affected by disturbance. Noise can be defined as unwanted disturbance that affects the original and desired signal. These fluctuations are always unused. Mainly noise is of two types. One is artificial and another one is intrinsic noise. Intrinsic noise is generated in a circuit by device physics related fluctuation of carrier charges. Artificial noise is generated by surroundings. Examples of artificial noise are Magnetic coupling and electrostatic coupling between a circuit and power line. Intrinsic noise is mainly generated in Electronic devices. And other devices, which are operating on the same circuit, can also generate intrinsic noise. 1/f noise, thermal noise (Nyquist noise), shot noise (poison noise), generation-recombination noise are the noises present in MOSFET. Here intrinsic noise is discussed. Mainly intrinsic flicker noise is generated in a MOSFET. This intrinsic noise is hard to remove from the circuit. But can be deterioration by filtering, shielding, varying the layout of the circuit component etc.

2.2 Type of Noise in MOSFET

Noise is the undesired signal which disturbs the original signal. These are the fluctuations which occur in a signal. Basically these can be removed from the circuit or device by some techniques. We are going to discuss different types of noise present in MOSFET. Which are shot noise (poison noise), flicker noise (low frequency noise), generation-recombination noise etc.

2.2.1 Shot Noise

Shot noise is generated by reverse biased junction. So this noise is provoked by random charge carriers across the junction. Mainly there are two conditions, which are required to arise shot noise in analog MOS IC. One is Potential barrier and another is flow of direct current. This noise mainly occurs when the carriers cross the barriers. This is not depend on the arrival of previous charges or the succeeding until will arrive. In 1918, Schottky described that shot noise is not generated in linear device. This could only be generated in nonlinear device. Shot noise, (also called poison noise) affiliated with the leakage current of the drain-source reverse diodes.

2.2.2 Generation-Recombination Noise

Generation recombination noise is basically an electrical signal, which is generated by vacillation of electrons in the device. This noise is called generation and states. The generation recombination noise mainly formulated form bulk silicon and silicon dioxide interface imperfection. Carriers fluctuating between two states participate in current flow in the device. Charge carriers are released and captured by the trap, which causes current flow in device. This switching of charge carriers between two energy states could be modeled in the time domain.

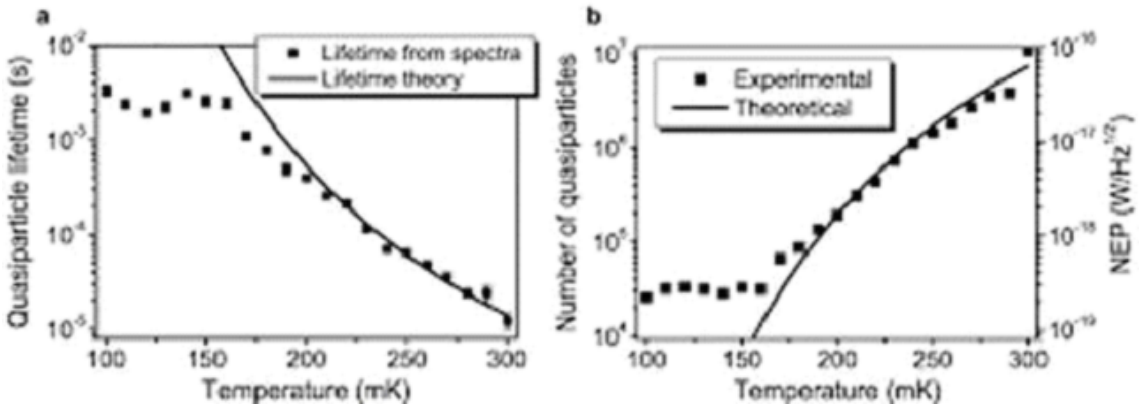

FIGURE 2.1: generation-recombination noise spectrum as a function of temperature

2.2.3 Flicker Noise

Flicker noise is also called pink noise or low frequency noise. From the early search it is hinged that the low frequency noise is the noise which occurs at the lower part of the frequency spectrum. It is also called pink noise. This noise is occurred at below several kHz. This noise is also characterized by the power spectrum density, which is reciprocal to the frequency and directly proportional to the wave length. Means at higher frequency this noise does not occur. So this could be calculated below kHz. Flicker noise is a narrowband low frequency noise. Flicker noise is a type of electronic noise with a 1/f power spectral density, therefore often cited as pink noise or 1/f noise. Flicker noise in current or voltage is usually related to a direct current, by Ohm's law fluctuations are transformed to voltage or current fluctuations. There is also a 1/f component in resistors with no direct current through them, likely due to temperature changes.

Flicker noise is often specified by the corner frequency (Fc). This is the flicker noise spectrum in MOSFET. MOSFET have a giant corner frequency than JFETs or bipolar transistors, which is usually below 2 kHz. The Corner frequency region Supreme by low-frequency flicker noise and high-frequency noise. Since flicker noise is related to the level of DC, if the current is kept low, thermal noise will be the uppermost effect in the resistor, It's all depends on frequency window that resistors used in the circuit will affect noise level or not.

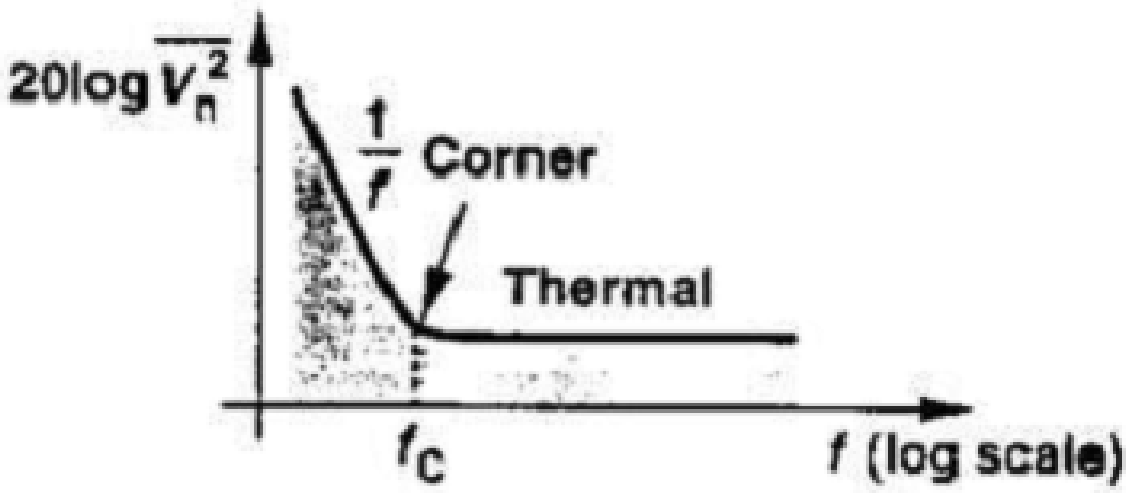

FIGURE 2.2: flicker noise spectrum in MOSFET

Flicker noise occurs due to arbitrarily trapping/de-trapping of carriers near the silicon/ silicon dioxide interface. So the 1/f noise current occurs due to traps at interface. The carriers can oscillate between trapped (no current contribution) and Free states (contribution to current), when both states have roughly equal free energy for the carriers. Only the traps whose energy is approximately equal to the Fermi-level of the free charge carriers in silicon contribution to the noise. Flicker noise arises from fluctuations in the carrier (hole and electrons), this fluctuation sequentially gives up rise to fluctuations in the conductivity of the material. I.e. noise voltage will be developed whenever direct current flows through the semiconductor, and the mean square voltage will be proportional to the square of the direct current.

2.3 Principle of Flicker Noise Measurement in OP-AMP

Here the principle of flicker noise measurement of an operational amplifier is discussed. In the next chapter the measurement setup of 1/f noise computation of proposed two stage operational amplifier is given and described.

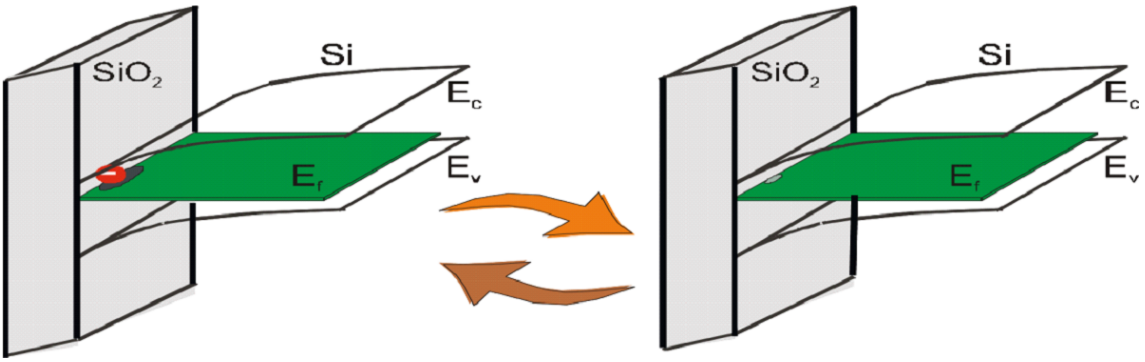

FIGURE 2.3: energy band diagram in MOSFET to show the trapping and de- trapping between Si/Sio2.

2.3.1 Flicker Noise Model in OP-AMP

We can depict the external noise source in an operational amplifier to internal noise sources. At the feed in node of the operational amplifier, the noise module puts a noise current and voltage source. If the op-amp is a differential type of op-amp, then there will be differential inputs. Means four noise sources are required. The interdependency between two sources on one input and on the other input is weak. These noise sources are correlated. If it is assumed that source impedance is equal for all the inputs of operational amplifier, then the two noise current sources are taken over by a single differential noise current source. If the op-amp responds only to the differential input voltage, then the two noise voltage sources in the classic model can be substituted by a single noise voltage source.

2.3.2 Low Noise Amplifier

If the operational amplifier is having differential inputs, means there will be four inputs, two voltage noise source and two current sources. The general op-amp is having two inputs that is, one is noise source and another is noise voltage source. So this differential amplifier could be replaced by general amplifier. To get the general op-amp from differential operational amplifier, replace the two noise current sources by single noise current source. Similarly two noise voltage sources by single noise voltage source.

On one input, interdependency between two noise sources is not good. In general noise sources are interconnected. So both the inputs are not correlated very well. To get the

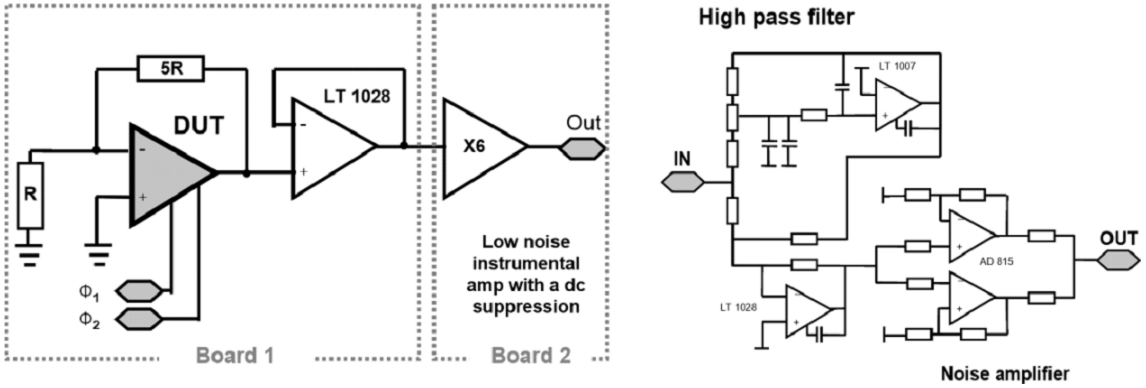

FIGURE 2.4: low noise amplifier with high pass filter .

general operational amplifier two noise current sources are substituted by a differential single noise current source. Op-amp model is shown in above figure. Here it is assumed that impedance of both the inputs of operational amplifier is same. Here neglect the current noise. Because the current is very small, so do not consider the current noise of source.

Chapter 3

Flicker Noise Reduction Technique

3.1 Introduction

Detailed discussion of the principle of flicker noise reduction technique in two stage operational amplifier in discussed. So a new circuit arrangement of MOSFET for flicker noise scaling down is implemented. But this technique is only for the linear analog signal. The principle of flicker noise reduction is built on a known device physics-related mechanism. For this purpose a complimentary switched MOSFET architecture is implemented. Basically flicker noise is causes by inputs of the operational amplifier. Because in practical op-amp the input voltage is nearly below 10mV so it is affected by some effects. As we know that we put transistor as the input of the operational amplifier. So the input current could be made very small at lower frequency. As we know 1/f noise is the low frequency noise. Means the input signals are also narrow band low frequency signal. In linear CMOS IC at low-frequency, flicker noise could be present. So in this chapter the principle of flicker noise reduction technique in two stage operational amplifier is discussed.

3.2 Flicker Noise Under Non-Equlibrium State

When on-off switching take place in MOSFET. The MOSFET will not in equilibrium state. It will fluctuate between two regions. In this condition the MOSFET swing between

inversion region and accumulation region. This causes reduction of flicker noise.

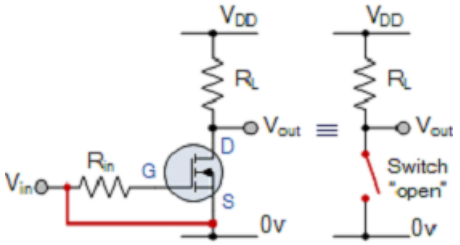

FIGURE 3.1: Concept of fluctuation of MOSFET in ON and OFF region.

This is the circuit for on-off switching of MOSFET. Here we can see in diagram that it is having three terminals. We get output from drain terminal. So let assume that threshold voltage of the transistor is Vt. A pulsating DC wave of voltage is applied at the gate node of the MOSFET. This voltage source is having high level and low level voltage values. This applied voltage at input node switches the gate-to-source voltage VGS of the MOSFET between two bias states. Now we apply a square wave which is having two levels of voltage. Here we are having two voltage states that is higher voltage state (VGSon) and lower voltage state (VGSoff). When we apply a gate to source voltage at the input node, which is high compare to the threshold voltage of the MOS transistor, then MOS transistor will be ON. Means it is in strong inversion region. When the applied voltage at the input is lesser than the threshold voltage of the transistor, it will off. Means it is in accumulation region. Switching of MOSFET ushers to an unspecified reduction of intrinsic low frequency noise of these MOS devices. In this condition MOSFET is not in equipoise operating state. Low level voltage Vgsoff ascertain a bias point of a MOSFET which accord with inversion, weak inversion or accumulation on the other half period. 1/f noise curtailment is maximized when the MOSFET is revolved from strong inversion via weak inversion to accumulation region. Amount of the flicker noise lowering depends on Vgsoff. For lower Vgsoff additional curtailment in low frequency noise occurs.

3.2.1 Noise Reduction Principle

Flicker noise is occurred due to random trapping and de-trapping of charge carriers near the silicon/ silicon dioxide interface. So the flicker noise current occurs due to traps at interface. The carriers can oscillate between trapped (no current contribution state)

and de-trapped/free states (contribution to current state), when both states have roughly equivalent free energy for the carriers. Only the traps whose energy is nearly equivalent to the Fermi-level of the free carriers in silicon bestows to the noise. Flicker noise arises from fluctuations in the carriers (holes and electrons), which gives upswing to fluctuations in the conductivity of the material. I.e. noise voltage will be developed whenever direct current flows through the semiconductor, and the mean square voltage will be proportional to the square of the direct current. The fluctuation probability is reduced, when the operating point of a MOSFET and the gate to source voltage is changed strongly from accumulation region to strong inversion region. When applied gate to source voltage is changed, the Fermi level of the free charge carriers also changed.

This trap causes the flicker noise in the device. So this on-off switching between two states leads to reduction of flicker noise.

3.3 Complementary Switched MOSFET Architecture

Here in this chapter the proposed new circuit configuration of MOSFET to reduce the flicker noise is discussed. This proposed architecture is called complementary switched architecture. New circuit configuration is helpful in reducing flicker noise from the device. So the older design is replaced by complementary switched MOSFET architecture.

3.3.1 1/f Noise Reduction Principle

In flicker noise reduction technique, a complementary switch MOSFET is designed. To implement this circuit we replace the n type MOSFET with complementary MOSFET. In the below figure we can see that the simple NMOS is replaced by another circuit, which is having two n type MOSFET. I.e. T11 and T12. The modified circuit consists two clocks (ϕ 1 and ϕ 2), which are complementary to each other. There are two switches I.e. SW1 and SW2. Transistor T11 and T12 are identical to transistor T1. We are doing this to reduce the noise contribution of the input transistor T1. During the half clock period, these two switches (SW1 SW2) and two clock pulses (1 and 2) connects the gate of the transistor T11 or T12 to the gate of the transistor or GND. In the new circuit when the applied

potential at gate terminal is high compare to the threshold voltage of the transistor T11, the transistor T11 is forced to operate in strong inversion region. Means if the applied voltage at input of T11 transistor is more than threshold voltage, it will be ON. At this time the transistor T12 is connected to GND. Means this transistor is OFF. And it will be in accumulation region. Now both the transistor will fluctuate between two states. They will switch between strong inversion region and accumulation region. We know this on-off switching of the input transistors is causes the reduction of flicker noise.

The gate terminal of transistor T11 and T12 fluctuate between nodes G (on stage) and the node VDD (off state). So when transistor T11 is operating in ON state the other one (T12) operates in OFF state. This happens when clock pulse is applied. As shown in the above figure that there is a disruption in the drain current of transistor T1. This could be because of the duty cycle mismatch of clocks (1 and 2). This discontinuity is very small. Under non-equilibrium state of the transistor, we do not take flicker noise into consideration. This technique is only valid for analog CMOS IC'S. So using this technique, flicker noise of operational amplifier can be reduced. The complementary switched MOSFET to reduce the flicker noise from the circuit is implemented. Nearly 9-10 dB flicker noise is reduced, while using complementary switched MOSFET architecture.

3.4 Application to Linear Analog CMOS IC's

For flicker noise reduction technique in analog circuit, take the example of two stage operational amplifier. So from the name, we can say that this is two stage circuits. First circuit is differential amplifier and another stage is common source amplifier, first stage, which is differential amplifier having two input transistor T1 T2. And the current mirror circuit, which is having two transistors T3 T4. Transistor T1 T2 are the input transistors. Current mirror is working as active load. As we know that the conductivity of n type MOSFET is greater than the conductivity of p type MOSFET. So p type MOSFET is widely used in high speed application. In classic two stage op-amp, output of differential stage is connected to the input of the source follower of two stage op-amp. The second stage is source follower, which is having two transistors T6 and T7. Here transistor T6 is operating as a driver and T7 is performing as an active load. The first stage gives the

differential gain. That is fed up to second stage, where it is compensated by the capacitor Cc. This is called the miller capacitance. That is also called compensation capacitance. Below the basic principle of flicker noise reduction in two stage operational amplifier is discussed.

3.4.1 Proposed OP-AMP Architecture

Here designed the two stage op-amp with complementary switched MOSFET as an input. Here is the "modified" operational amplifier design after the principle is petition to the "classical" CMOS two stage operational amplifier. The input transistors are substituted by the proposed four transistors (T11 T12 T21 T22), and switches (S11 S12 S21 S22). Here we are applying two clocks, which are complementary to each other. When applied clock pulse 1 is equal to VDD and another clock pulse 2 is VSS. In this situation transistors T11 and T12 operates in inversion region (means in ON state). At that time transistors T12 T22 are switched off (means working in accumulation mode). Now when the next clock pulse is applied, this makes a periodic ON-OFF transition of transistors T11 and T12, and T21 and T22 between inversion (operation mode for signal processing) and accumulation mode (RELAX mode). This also makes a continuous operation of the operational amplifier.

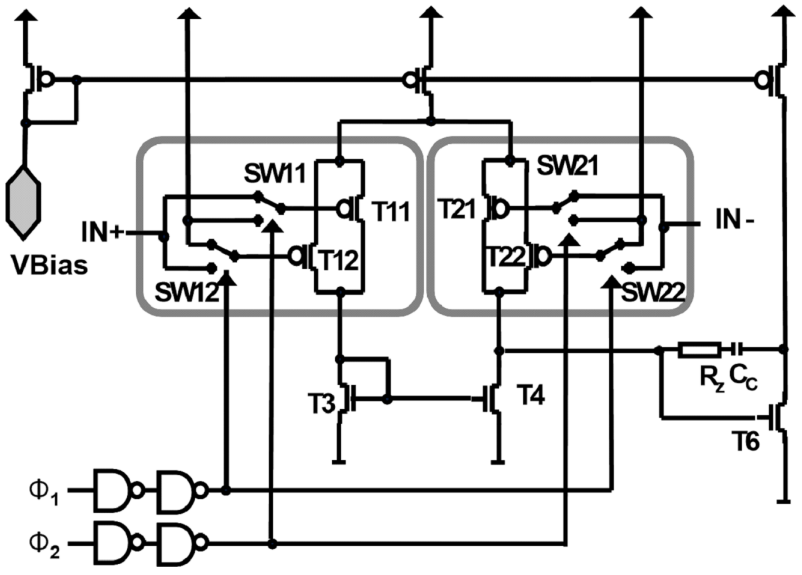

FIGURE 3.2: Modified operational amplifier for flicker noise reduction

The current mirror circuit is having two MOS transistors T3 T4. These are working as an active load in the circuit. Here we replaced the feed in transistor with T1 and T2. Only input transistors T1 T2 and two load transistors T3 T4 contribute to flicker noise of the circuit. In flicker noise reduction two feed in transistors T1 T2 have the strongest sequel on the low frequency noise deportment. Transconductance of transistor (T1, T2) and (T3, T4) are identical. So gm1 and gm3 should be chosen, such that flicker noise of op-amp is persistent by the input device T1 and T2.gm1 should be greater than gm3.

3.5 Implementation of OP-AMP Architecture

In this chapter, detail discussion of the design implementation issues and design inspection for flicker noise reduction is done. A classic two stage CMOS op-amp and proposed op-amp is designed. From which we will know the flicker noise reduction idea. The classic two stage miller CMOS op-amp is modified into the proposed op-amp to reduce flicker noise. The input transistors of the classic operational amplifier are replaced with the proposed transistors for flicker noise reduction. Difference between classic operational amplifier and proposed two stage op-amp is also examined. So here classic operational amplifier is working as a cited of for the proposed operational amplifier.

3.6 Physical Considerations to Design Miller OP-AMP

To design the linear CMOS analog circuit, some cogitation should be taken into our brain. We should take into consideration that drain node to source node voltage should be enough high so that inversion layer should not extend over form drain to source. We should also note that the transistors should be saturation region. If the drain to source voltage is enough high then the mode charge stay constant. And the drain current is also constant in saturation region. It does not depend on drain to source voltage, whether the drain to source voltage is rising or not. This transistor acts as voltage controlled current source. The drain current in saturation depend on the gate to source and drain to source voltage. The transconductance and the output transconductance I.e. gds of the transistor are also the important parameters, which should be taken into consideration. The ration of

these two determines the amplification of the signal. As we know that both the transistor fluctuates between two states. So this swing of transistors may reduce the performance. So the PMOS transistor should be chosen very carefully. So for the flicker noise reduction it is very necessary to configure an op-amp.

3.6.1 Implementation of OP-AMP

Before implementing the design remember that input voltage should be low for low input Capacitance. As we know that the main source of flicker noise is the input. Before applying the flicker noise reduction principle to the op-amp, take care of gate current and source to drain current of the two MOS transistors. These two are the major considerations, which we should take care. The gate current is periodic impulse current. We should also take care of source to drain current first. By the charge administration effect, the periodic gate current is defined at every clock pulse. The drain to source current of both the transistors T1 and T2 is an implicit phenomenon which assigns to applied clock pulses. As we know that there will be some voltage at gate node when we apply the external voltage. So the voltage at gate on transistor T11 and T12 are VG11 and V12 respectively. And two clock pulses are also applied, which are complementary to each other. Note that the clocks should have 50% duty cycle. So when we apply first clock at the node G, which is high compare to the threshold voltage of the transistor T11. Now it will in inversion means it will ON. And another transistor T12 will be in accumulation, means it will be turn OFF. When the applied voltage is less compare to the threshold voltage of the transistor T12, it will in inversion and another transistor T11 will be in accumulation. As we can see that both the transistors are fluctuating between two regions, which cause reduction of flicker noise.

From this above spectrum it can be determined that gate current is induced by charge injection in MOS transistor. Here let assume that there is no charge injection effect in the switch S1. As we know that both the switches are transmission gate. Now apply a clock pulse, when it is big, the switch S2 turns OFF and it bridges the gate node to VG of T11 transistor. At this time the switch S2 is turn on. Now the switch S2 releases the charge Q11 to the gate of the transistor T11. And S1 switch draws the charge Q12 from the gate

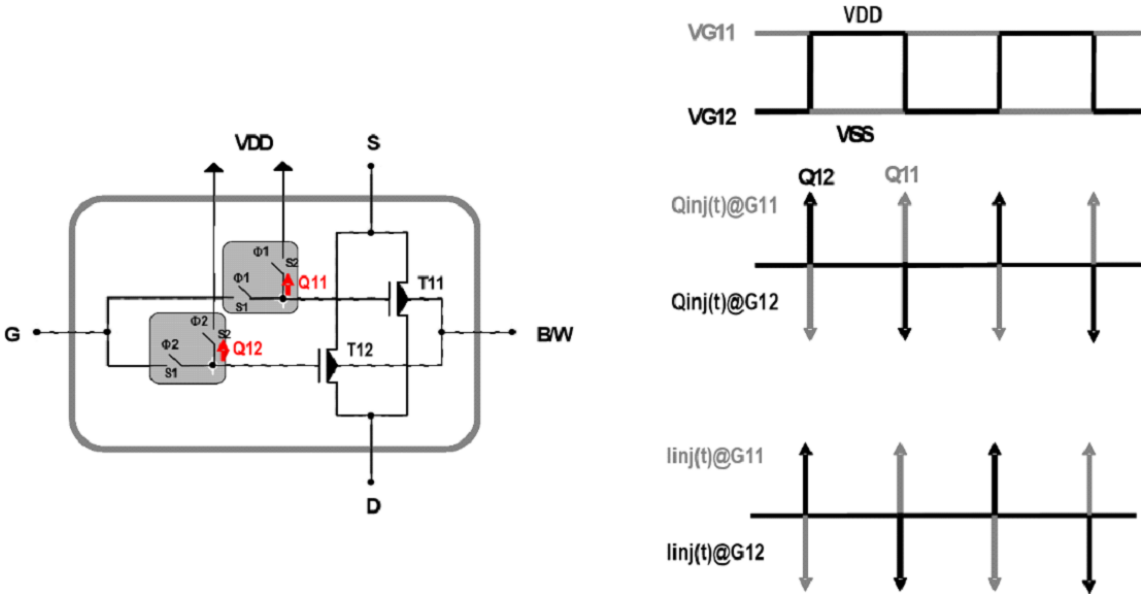

FIGURE 3.3: induced gate current principle and spectrum

of T12 transistor. The amount of charge is equal as of switch S2 releases. So this method generates the periodic impulse gate current at the gate of each transistor.

Chapter 4

Simulation Results

4.1 Introduction

In antecedent part of this chapter, a proposed two stage op-amp is designed, to reduce the flicker noise in Analog CMOS IC. So here all the results which we calculated will be shown below. First design the circuit that is classic two stage op-amp circuit and the proposed two stage operational amplifier. Then find the noise present in both the circuit and then compare these two. Apart from noise gain margin, phase margin, gain bandwidth product etc. all the experimental results are shown below with schematic.

4.2 Classic OP-AMP in Brief

Here is the general two stage operational amplifier, which consists two levels. First level is differential amplifier and second stage is common source follower. There are two input transistors T1 and T2, which causes the flicker noise in the circuit. There is a current mirror also with T3 and T4 transistors.

The current at the drain node of transistor T3 is equal to current at drain node of transistor T4. The second stage is source follower, in which transistor T6 is acting as a load.

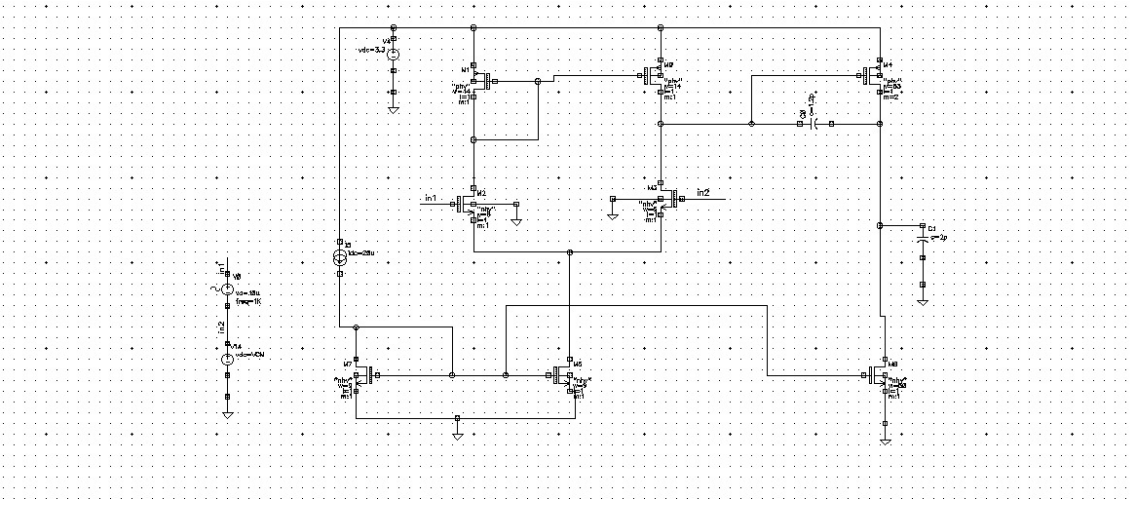

FIGURE 4.1: Classic two stage operational amplifier

4.2.1 Phase Margin and Gain Margin

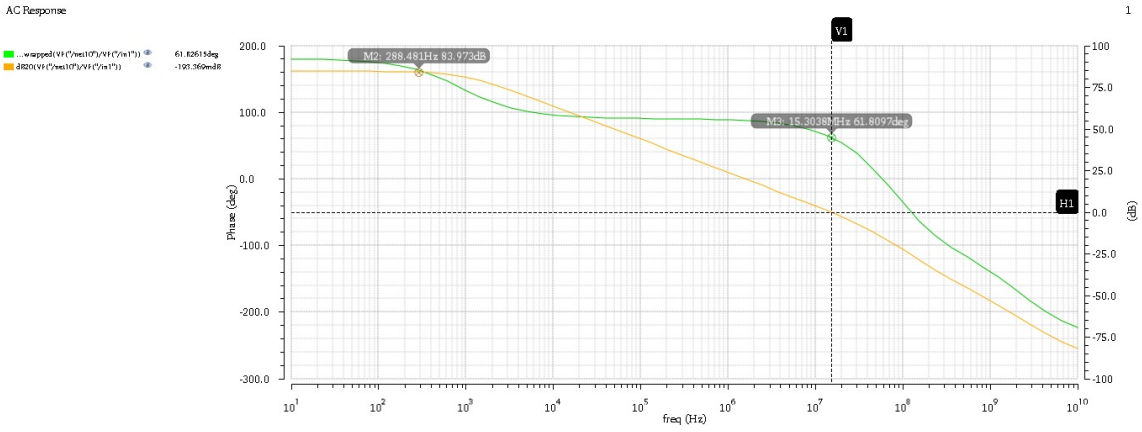

FIGURE 4.2: Gain margin and Phase margin spectrum

Phase margin of classic two stage operational amplifier is approximately 61.8097deg and the gain margin is nearly 83.973dB.

4.2.2 Flicker Noise in Two Stage OP-AMP

Here we are going to measure flicker noise in two level operational amplifier. As we know that flicker noise is measure at the corner frequency. As we can see fc is 101.17Hz and the value of flicker noise is 584.15 uV/Hz. The value of flicker noise in dB is 55dB.

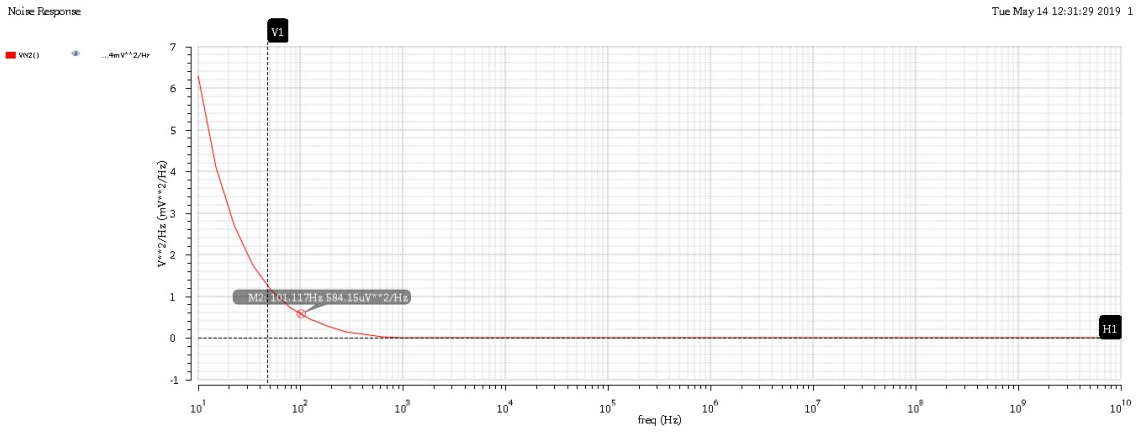

FIGURE 4.3: Flicker noise spectrum in two stage op-amp

4.3 Proposed Two Stage OP-AMP

Our main purpose is to reduce flicker noise in two stage op-amp. So we modify the classic operational amplifier. Input of the classic op-amp is replaced by COMPLEMENTARY SWITCHED MOSFET. Now we are going to discuss the design and working of complementary switched MOSFET. It is having inverter, SP2 switch, Circuit working as NMOS etc.

4.3.1 SP2 Switch

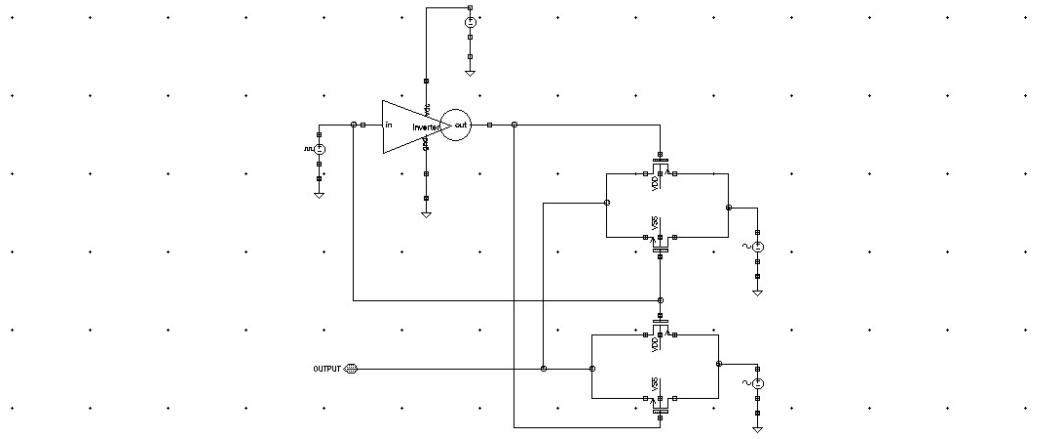

FIGURE 4.4: Schematic of SP2 switch

This is the SP2 switch, which is having an inverter and two transmission gates. A control signal is applied to inverter. Each time the output of the inverter is inverted. Below is the simulation result of SP2 switch.

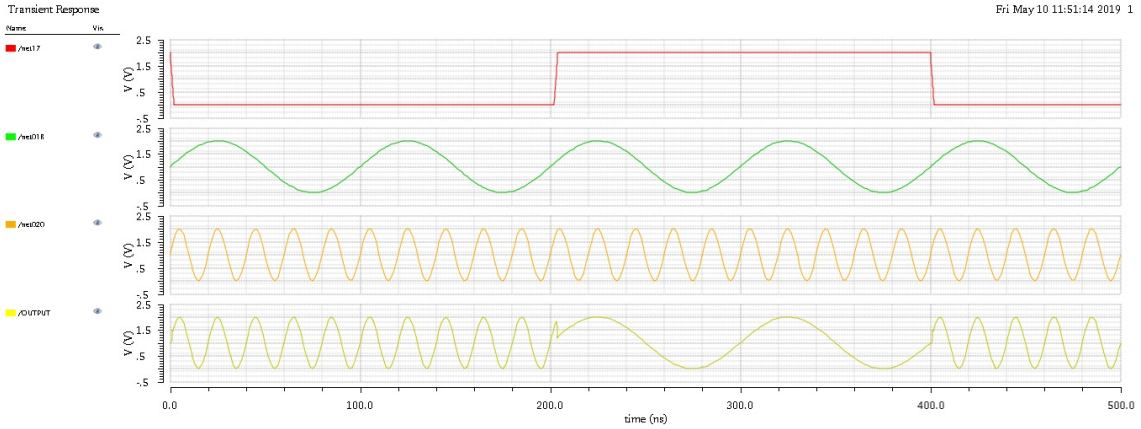

FIGURE 4.5: Simulation result of SP2 switch

In SP2 switch we are applying two inputs having different frequency. When control signal is low, at the output of the switch we get only one input signal. Because when control signal is high second transmission gate will be on and another will be off. So we get only one output at a time. When the control signal is high, we get another signal as output. Means output is the input of upper transistor. So we can say that this is working as SP2 switch.

4.3.2 Circuit Working as NMOS

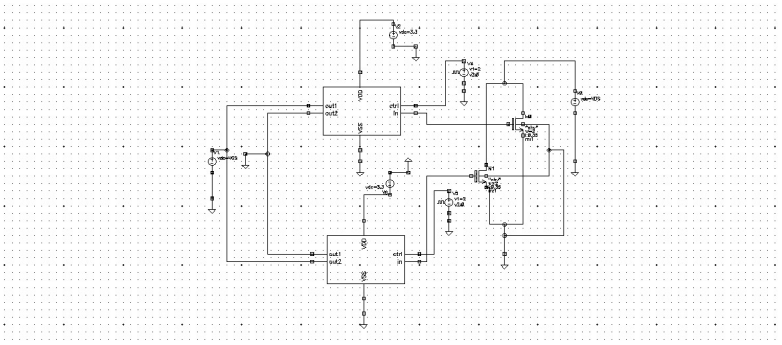

FIGURE 4.6: Schematic of circuit working as NMOS

This is the schematic which is working as NMOS. Id vs Vgs characteristic of this schematic is same as the Id vs Vgs of NMOS. Below is I-V characteristic of the above circuit, which is working as NMOS

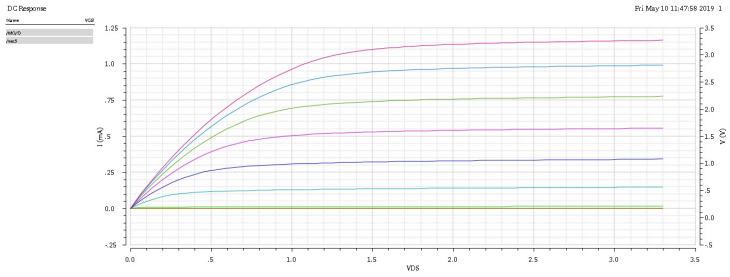

FIGURE 4.7: I-V Characteristics of circuit working as NMOS

4.4 Proposed Two Stage OP-AMP Architecture

Our main purpose is to design the two stage operational amplifier, so that flicker noise should be reduced. So here is the circuit which is designed so that flicker noise is minimized. In classic two stage op-amp, we made some modifications to implement the proposed operational amplifier.

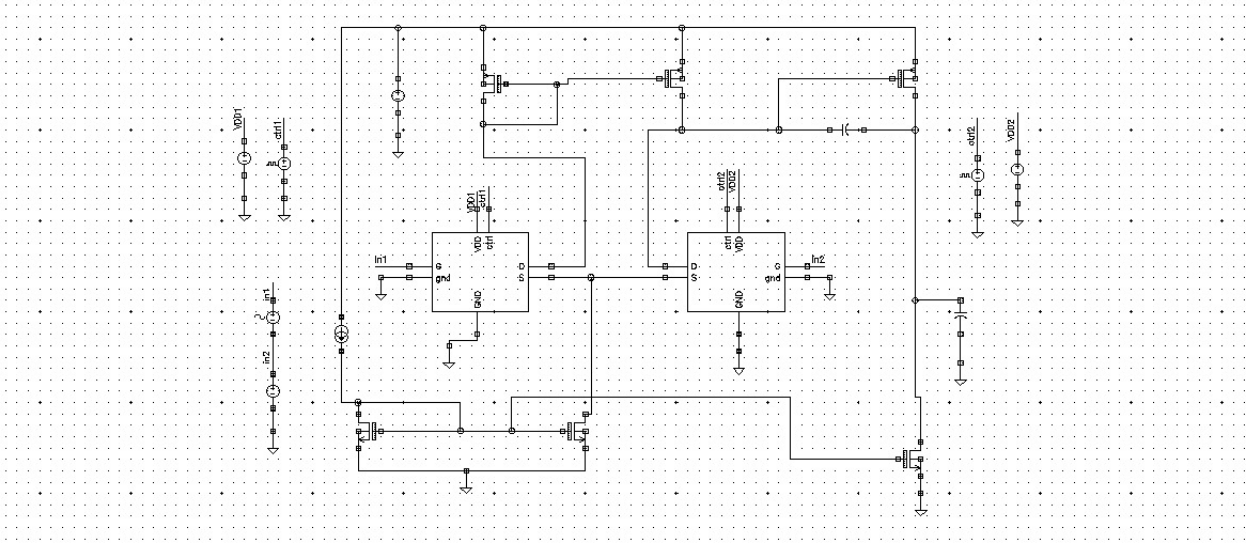

FIGURE 4.8: schematic of proposed two stage op-amp

This is the proposed two stage operational amplifier, which is having two stages, one is differential amplifier and second stage is source follower. In this circuit only the inputs are replaced by the COMPLEMENTARY SWITCHED MOSFET. This input is working same as NMOS. As we have seen the characteristics of this complementary MOS is same as the NMOS. Our main purpose to replace NMOS with this modified circuit is to reduce the flicker noise from the circuit.

4.4.1 Gain Margin and Phase Margin

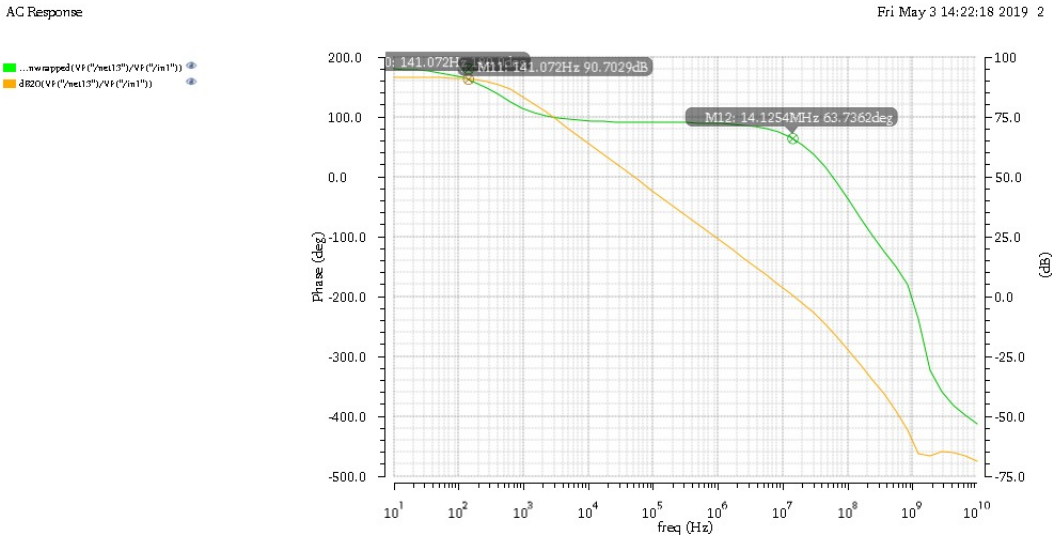

FIGURE 4.9: phase margin and gain margin of the modified two stage op-amp

The phase margin of this circuit is nearly equal the classic two stage operational amplifier. The value of phase margin is 61.205deg. The gain margin of the circuit is higher than the classic op-amp. That is 90.800dB. Means gain margin in modified two stage operational amplifier is greater than classic op-amp.

4.4.2 Flicker Noise in Modified OP-AMP

We know flicker noise is calculated at the corner frequency. The corner frequency is 94.4061 Hz and flicker noise is 135.863 uV/Hz. The value of flicker noise in dB is 42.66. Now we can compare the flicker noise in both the circuits. As we can see that in classic op-amp flicker noise is 55dB and in modified circuit it is nearly 42.66dB.

Our main purpose is to design the two stage operational amplifier, so that flicker noise should be reduced. So here is the circuit which is designed so that flicker noise is minimized. In classic two stage op-amp, we made some modifications to implement the proposed operational amplifier.

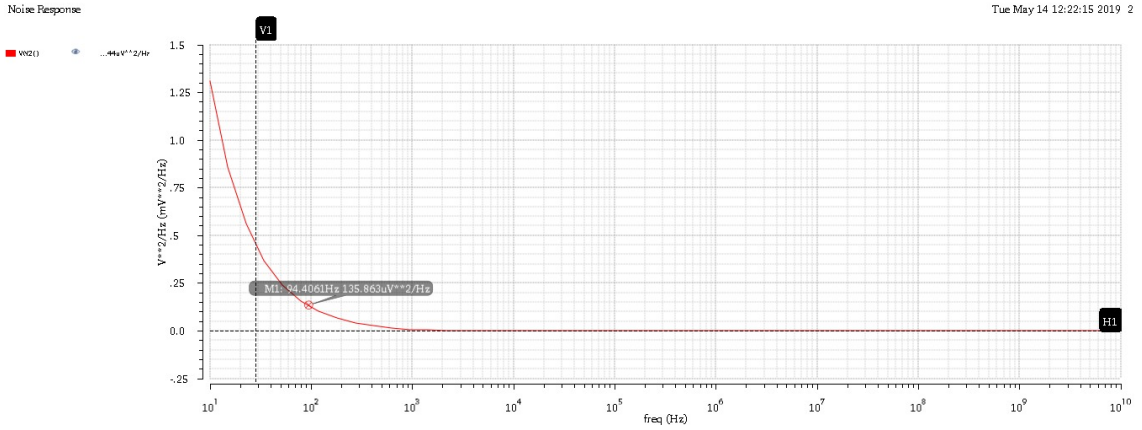

FIGURE 4.10: flicker noise in modified op-amp

Chapter 5

Conclusion

To reduce flicker noise from two stage operational amplifier. A two stage operational amplifier is designed. Now the input transistors are replaced by COMPLEMENTARY SWITCH MOSFET. Means transistor T1 and T2 are replaced by this circuit, which is having four transistors and four switches. I.e. in modified operational amplifier the input transistors are T11, T12, T21, T22 and switches are SW11, SW12, SW21, SW22. So in this thesis we discussed the basic principle of flicker noise reduction in two stage operational amplifier. In this chapter we have discussed all the possible results related to flicker noise reduction in two stage op-amp. In classic two stage op-amp the flicker noise is nearly 55dB and in modified two stage op-amp is 44.66dB. So we can say that flicker noise in classic op-amp is higher than the modified op-amp. The flicker noise is reduced by nearly 9dB. In this thesis gain margin and phase margin of two stage op-amp is also discussed in both the conditions. There is no change in phase margin but gain margin is increased in modified two stage op-amp.

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