

A
DISSERTATION REPORT
on
DESIGN AND CHARACTERIZATION OF ANALOG
MULTIPLEXER

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partial fulfilment for the degree of
Master of Technology
in
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CERTIFICATE

This is to certify that the dissertation report entitled **Design and Characterization of Analog Multiplexer** composed by **Mr. Satyendra Kumar (2015PEV5262)**, in the partial fulfilment of the Degree Master of Technology in **VLSI** of Malaviya National Institute of Technology, Jaipur is the work completed by him under my supervision, hence approved for submission during academic session 2016-2017. The contents of this dissertation report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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DECLARATION

I, **Satyendra Kumar**, declare that this dissertation titled, "**Design and Characterization of Analog Multiplexer** " and the work presented in it is my own. I confirm that:

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- Where any part of this Dissertation has previously been submitted for a degree or any other qualification at MNIT or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
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- I have acknowledged all main sources of help.

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ABSTRACT

In this research, I have designed and characterized the suitable technique for an improved analog multiplexer with the help of CMOS analog switch. The best suited architecture of an analog multiplexer is designed and then compared with the other present analog multiplexers. After making the comparison with the help of certain parameters like ON-Resistance of the switch, the proper selection of the switch is made for the designing of analog multiplexer. The circuits for the testing of on-resistance of an analog switch, crosstalk and furthermore the break-before-make switching condition for improved analog multiplexer have been proposed. To study the effects of process variation and the effects of temperature on the switch we also performed the parametric analysis. The significant commitment of this research is the implementation and usage of break-before-make switching condition with the help of only 4 transistors for a single switch. In the designing of analog multiplexer we have used CMOS transmission gate and applied the input signal of 20KHz with 3.3 Volts dual power supply in CMOS 180nm technology. For the simulation and implementation of test circuits, Cadence Virtuoso Analog Design Environment is used.

KEYWORDS: Analog Multiplexer, Transmission Gate, Analog Switch, CMOS Technique, ON-Resistance, Parametric Analysis, Crosstalk, Break-Before-Make Switching Condition

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CHAPTER 1

INTRODUCTION

1.1 Background

In the present situation when a satellite is propelled into the space it has to set in a specific orientation in its orbit for a powerful correspondence and communication. After the launching process and establishment of spacecraft in its orbit I will be bothered by different strengths of the sun, moon, earth, the surroundings temp and so on. Consequently the reorientation of shuttle (satellite) is important by consistently checking and monitoring its orientation. With the help of sensors the required data of orientation has been obtained. The sensors senses the light intensity and the temperature of surroundings etc. and correspondingly produces the output which is analog in nature.

1.2 Objective

The basic and fundamental block diagram of data acquisition system that incorporates different simple analog modules is appeared in Figure 1. Every output obtained by the sensors around the spacecraft are firstly converted into electrical signals with the help of transducer and then given as contributions to the simple analog multiplexer.

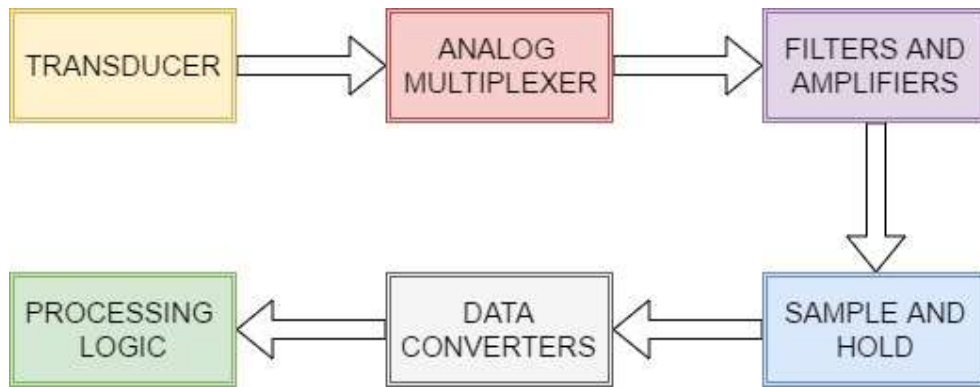


Figure 1: Block diagram of Data Acquisition System [1]

The outputs obtained from the sensors are multiplexed and go through the filter and amplifiers stage. Then filtered signal has to pass through sample and hold circuits and held for a time frame and after that given to analog to digital converter. After transformation the digital signals are given to the final block for the further processing logic of signals.

With the help of analog multiplexer we can reduce the computational power and complexity of analog to digital converter [12]. In this research work, I have only focused upon the designing of analog multiplexer. The circuit is designed and simulated in cadence virtuoso tool to compute the several parameters like on-resistance of the switch and crosstalk for the analog multiplexer. In addition to that switching conditions with break-before-make has been proposed for analog multiplexer to reduce the crosstalk from the system.

1.3 Overview

Beginning with the design specification for the analog multiplexer have been discussed in chapter 2. The basic principle of analog multiplexing and the test circuits of on-resistance for designing of best suited switch have been discussed in chapter 3. Furthermore the parametric analysis is also done to study and examine the effects of process variation and the effect of temperature on the switch of analog multiplexer. In chapter 4, I have discussed about the crosstalk and the test setup to study the effect and then proposed the design to overcome the crosstalk from the adjacent channel by implementing break-before-make condition. Experimental results are shown in chapter 5 and then the conclusion is depicted in chapter 6 [1].

CHAPTER 2

DESIGN SPECIFICATION OF ANALOG MULTIPLEXER

2.1 Basic Design Specification

The analog multiplexer has been developed for data acquisition system in satellites [1]. In Table 1, all the design specification for the designing of an analog multiplexer are shown. The design has to be simulated in cadence virtuoso tool with these specification. The design strategies has been applied utilizing CMOS transmission gates where the simple analog input with frequency 20KHz and 3.3V double power supply in CMOS 180 nm innovation technology. The parametric examination analysis is performed by changing the temperature from -55°C to 125°C and the aspect ratio of transistor (width of nMOS) from $5\ \mu\text{m}$ to $20\ \mu\text{m}$. On-resistance, crosstalk and break-before-make switching condition test circuits are designed and the outcomes are noted.

In the designed circuits CMOS Technology with 180nm minimum channel length of the transistor has been used. The input signal given to the switch is of amplitude -2Volts to 2Volts with the sinusoidal frequency of 20 KHz has been applied. Then by calculating the drop across the switch and the current across the resistor I have calculated the on-resistance of the switch.

Table 1: Basic Specification for proposed Analog Multiplexer [1]

CMOS Design Technology	180nm
Input Voltage swing	-2Volts to 2Volts
On-Resistance	Less than 75 Ω
Crosstalk	Less than 100 dB
Dual supply voltage	3.3 Volts
Multiplexer should satisfy	Break-Before-Make Condition for switching
Analog Input Signal Frequency	20KHz
Simulation Tool	Cadence Virtuoso

According to the given specification for analog multiplexer I have designed the test circuit and then simulated it in Cadence Virtuoso analog environment tool.

Further by doing the parametric analysis I also examine the temperature effects on the switch and also the process variation effects on the switch. Then by comparing among the switches I have selected the best suited switch for analog multiplexer and designed the circuit for analog multiplexer with transmission gate switch and then calculated the crosstalk exist in the design.

To overcome this Break-Before-Make switching condition has been implemented. I have used the double power supply of 3.3 Volts in our entire design.

CHAPTER 3

CMOS ANALOG SWITCH

3.1 Basic Fundamental of CMOS analog switch

In the recent year, incorporated analog switches have offered better switching characteristics qualities, low down supply voltages, and small packaging in littler bundles [2]. Since such a large number of execution alternatives and extraordinary capacities are accessible, the very much good informer item planner has to finding only the correct part for a specific application

CMOS Analog switch is a basic fundamental block which is basically used to design an analog multiplexer in outlining. It will specifically blocks the signals or pass the signals coming from input to output. The conductivity of gate and source terminals is completely controlled by the gate signal given to the transistor [4]. The capacitances between source/drain and gate are ignored since the entryway terminal does not draw any current. Henceforth the signal gone through switch is not exasperates by gate control signal. In a perfect world, a zero resistance way is formed when the switch is turned ON. However, basically the resistance of the switch relies on the input signal given to the switch [1]. Condition (1) gives the on-resistance of the transistor regarding input voltage.

Connecting to an n-channel MOSFET in parallel to a p-channel MOSFET allowing a signals to pass in both directions with equal ease. Whether the n- or the p-channel devices carry the more signal current it totally depends upon the ratio of input to output voltages. Because the switch has no preferred direction for current flow, it has no preferred inputs

or outputs. The two MOSFETs are switched on and off by internal inverting and noninverting amplifiers. These amplifiers level-shift the digital input signal as required according to whether the signal is CMOS- or TTL-logic-compatible and whether the analog supply voltage is single or dual.

Equation [1] shows the relation between the on-resistance of the transistor and the input voltage applied to the source of the transistor [1].

$$R_{ON} = \begin{cases} \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th,n})} & \text{For } nMOS \\ \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{gs} - V_{th,p})} & \text{For } pMOS \end{cases} \quad (1)$$

Where

- C_{ox} : gate – oxide capacitance
- $V_{th,n}$: Threshold voltage for nMOS
- $V_{th,p}$: Threshold voltage for pMOS
- μ_n : Mobilty of an electron in nMOS transistor
- μ_p : Mobilty of a hole in pMOS transistor
- V_{gs} : Gate to source voltage of the transistor

The bulk or substrate of nMOS is connected and associated with the most negative supply and substrate of pMOS is connected to most positive supply. The most important and essential parameters of a simple analog switch are on-resistance and input/output voltage

swing. The procedure of characterization system for on-resistance of the switch, transient behaviour, parametric analysis, DC sweep of an analog simple switch are performed.

3.2 Test setup for On-Resistance of the switch

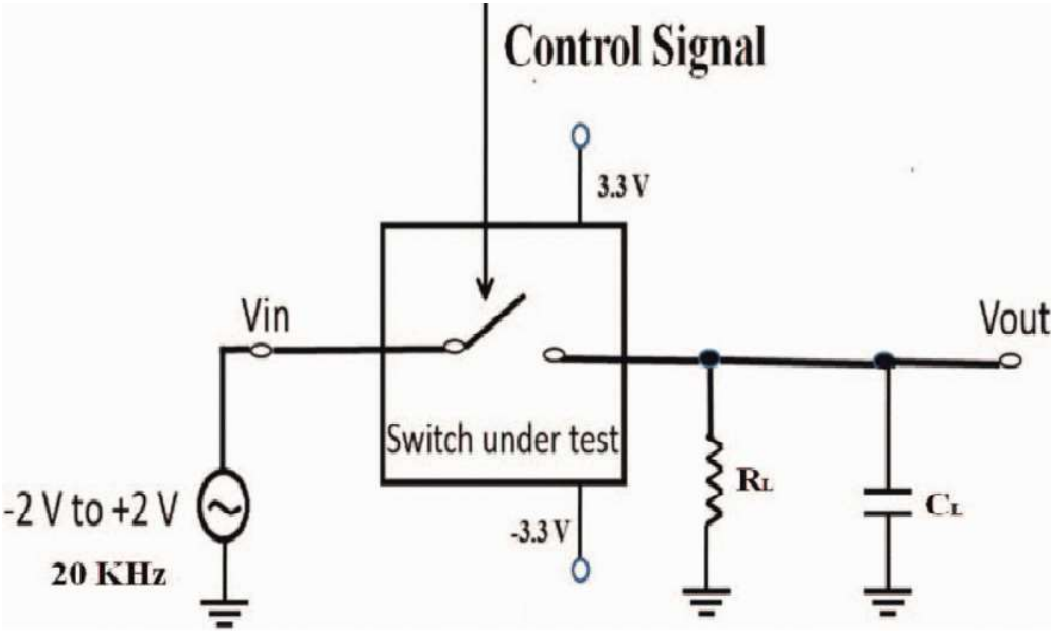


Figure 2 : On-resistance versus Input Signal [1]

Figure 2 shows the test setup for the measurement of on-resistance of an analog switch [1]. The analysis of DC sweep with input signal for R_{ON} is performed by varying voltage from $-2V$ to $2V$. For each and every value of voltage of the input signal, I have calculated the corresponding output voltage. Load resistor R_L is also introduced in the circuit above to provide a closed path for the current to be measured. The source, the switch and the load resistance forms a loop which allowing the same current through all of them [1].

The on-resistance is calculated by the ratio of voltage difference across the switch to the current flowing through the switch. The load resistance R_L is $10\text{K}\Omega$; however, I can also choose any arbitrary value that does not reflect on the obtained results [1].

3.2.1 Schematic of Transmission Gate in Cadence

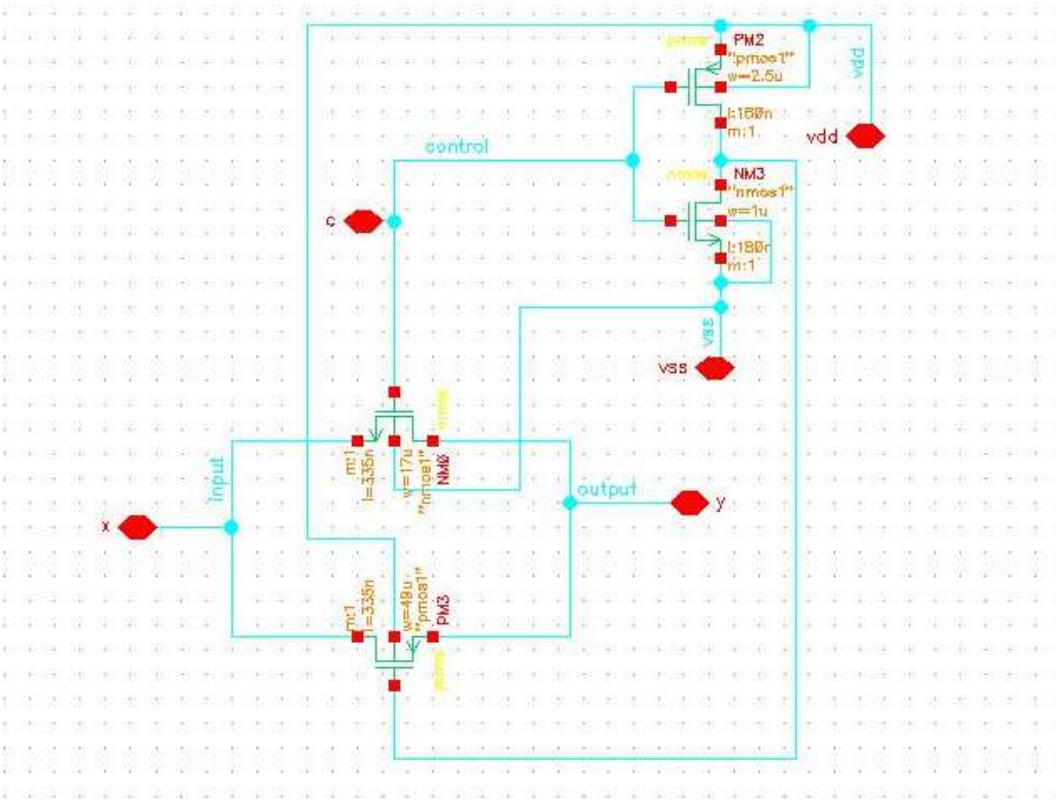


Figure 3: Schematic of Transmission Gate Switch

Figure 3 shows the schematic of transmission gate switch which is designed and simulated in cadence virtuoso analog environment.

The design methodology begins with the 3.3V double supply. The minimum channel length for pMOS and nMOS (L_p , L_n) and the load capacitance are taken as $0.335\ \mu\text{m}$ and 100pF individually [1]. From Equation (1) the width of nMOS transistor is ascertained to be $17\ \mu\text{m}$ for the switch to calculate on-resistance. The width of pMOS transistor is ascertained to be 3 times the width that of nMOS transistor, as I know the mobility of electrons is around 3 times the mobility of the holes. The bulk or substrate of nMOS is connected with the most negative supply that is -3.3 Volts which is VSS as shown in the schematic and substrate of pMOS is connected to most positive supply that is 3.3 Volts which is called VDD.

3.2.2 Basic operation of Transmission Gate

The transmission gate basically consist of parallel combination of nMOS and pMOS. The control signal is directly given to one of the transistor and the inverted control signal is given to another transistor. Depending upon the control signal voltage the transistor will be ON or OFF and the corresponding input is transferred to output through the transmission gate switch. If no control signal is given then the switch remains OFF and no data transfer will takes place. The basic function of transmission gate is shown in Figure 4.

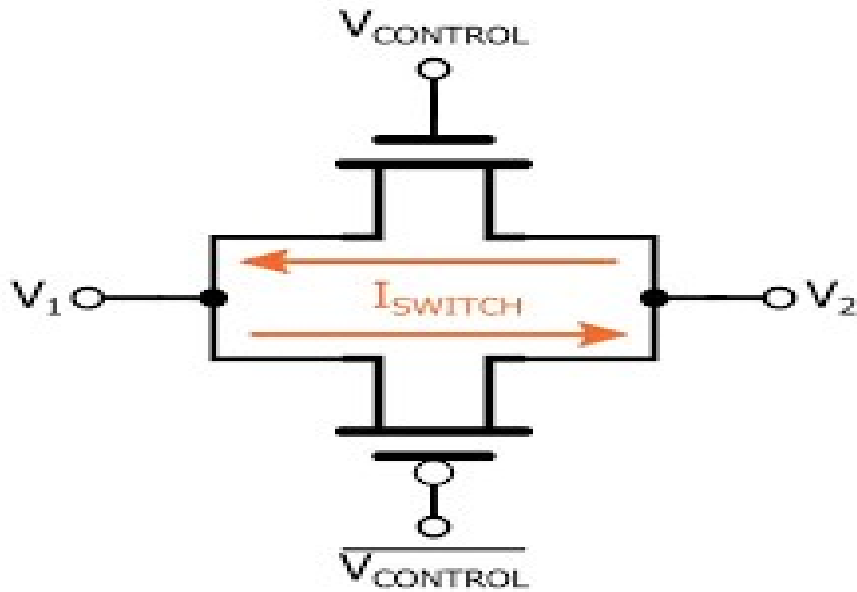


Figure 4 : Transmission Gate basic operation

3.2.3 Symbol of Transmission Gate and its operation

In Figure 5, the schematic of transmission gate switch is replaced by the symbol of transmission gate and the operation of switch is also shown here by adding the load resistance and the capacitance for drawing the output current. The dual power supply of 3.3 Volts is used as shown in the Figure 5 for the biasing purpose of the switch as positive supply of V_{DD} and negative supply of V_{SS} . Input signal of frequency 20 KHz and voltage from -2 Volts to 2 Volts is applied. The control signal with DC voltage is also applied for successful operation of the switch.

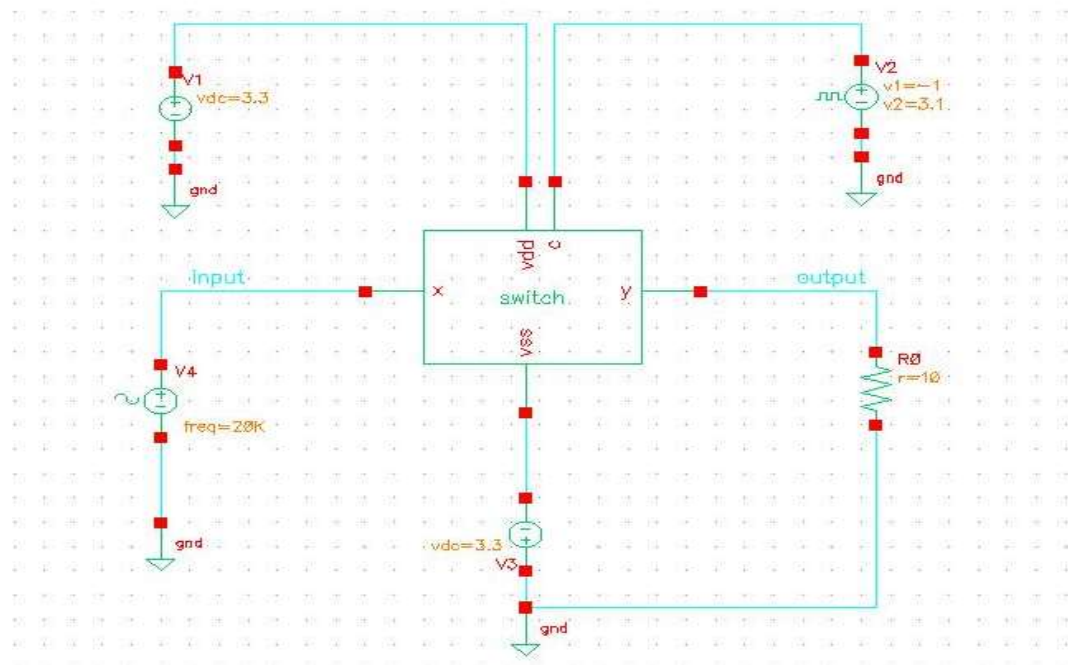


Figure 5 : Symbol of Transmission Gate Switch in Cadence Virtuoso

3.2.4 ON-Resistance of nMOS, pMOS and Transmission Gate

Figure 6, Figure 7 and Figure 8 shows the characteristics of nMOS, pMOS and Transmission Gate switch respectively in terms of On-Resistance Vs input voltage applied to the switch. . Input signal of frequency 20 KHz and voltage from -2 Volts to 2 Volts is applied. The control signal with DC voltage is also applied for successful operation of the switch. Then by doing the DC analysis the component parameter input voltage of the switch which varies from -2 Volts to 2 Volts and after DC simulation I have calculated the value of On-resistance for nMOS, pMOS and transmission gate switch.

From Figure 6, the On-resistance is minimum at 0 volts and at 2 volts On-resistance is maximum. So I can take the minimum On-resistance 91.81 Ohms for nMOS curve when the nMOS of the switch is turned ON. It is calculated by doing the DC analysis the component parameter input voltage of the switch is varies from -2 Volts to 2 Volts and after DC simulation I have calculated the value of On-resistance for nMOS.

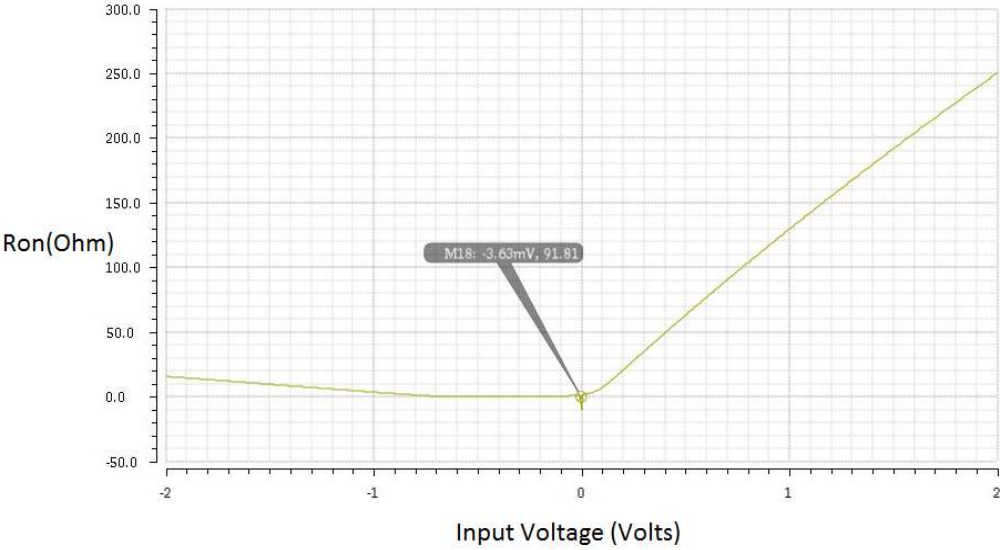


Figure 6 : On-resistance Vs Input Signal Voltage for nMOS

From Figure 7, I can see that the On-resistance is minimum at 0 volts and at -2 volts On-resistance is maximum. So I can take the minimum On-resistance 61.68 Ohms for pMOS curve when the pMOS of the switch is turned ON. It is also calculated by doing the DC analysis the component parameter input voltage of the switch is varies from -2 Volts to 2 Volts and after DC simulation I have calculated the value of On-resistance for nMOS.

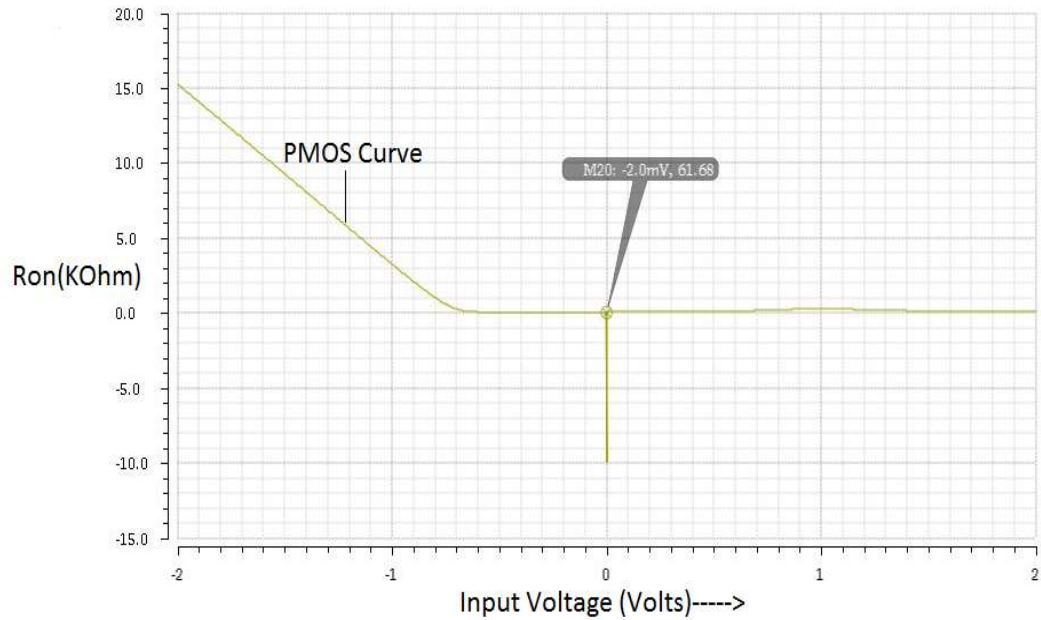


Figure 7 : On-resistance Vs Input Signal Voltage for pMOS

From Figure 8, the On-resistance is minimum at 0 volts and the On-resistance is maximum at -2 Volts and at 2 Volts. So I can take the minimum On-resistance 43.03 Ohms for transmission gate curve when both the MOSFETS of the switch (nMOS and pMOS) are turned ON. It is also calculated by doing the DC analysis the component parameter input voltage of the switch is varies from -2 Volts to 2 Volts and after DC simulation I have calculated the value of On-resistance for nMOS.

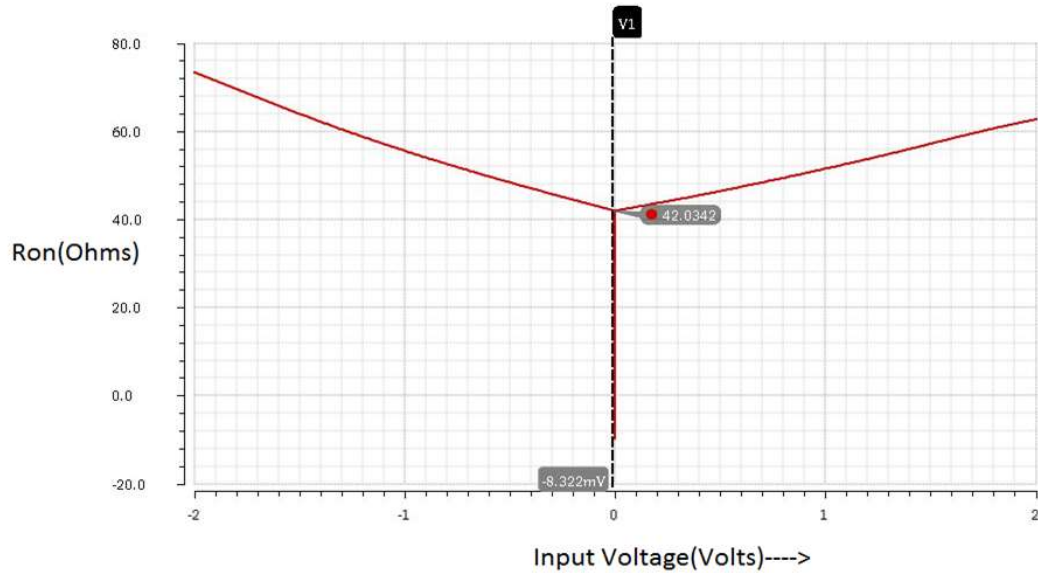


Figure 8 : On-resistance Vs Input Signal Voltage for Transmission Gate

3.2.5 Switch comparison between nMOS, pMOS and Transmission Gate

Transmission gates are always preferred over the pass transistor (nMOS and pMOS switch) because with the help of transmission gate it is possible to obtain a proper output voltage swing. The nMOS switch can only produce the output in the range of 0 to $(V_{DD} - V_{th, n})$ whereas the pMOS switch can only produce the output in the range of $V_{th, p}$ to V_{DD} . But when I came to transmission gate it will block or pass the signals completely from 0 to V_{DD} [7]. I have also seen that the on-resistance of the transmission gate is also low as compared to the pass transistor (nMOS or pMOS) switch and it is because the transmission gate is basically the parallel combination of both nMOS and pMOS switches. Thus transmission gate is best suitable and chosen for the design of the basic analog multiplexer.

3.3 Parametric Analysis of an analog switch

In this section mainly, the parametric analysis is performed by varying the two important parameters one is the temperature and another is the aspect ratio W/L of nMOS transistor. The temperature is varied in 6 steps size from -55°C to 125°C and the values of corresponding On-resistance is noted at the input voltages of 0 Volt, -2 Volt and 2 Volt as shown in Table 2. For a wide range of the temperature change, I obtained the region of operation of the resistance.

3.3.1 Variation of On-resistance (R_{ON}) for different Temperature

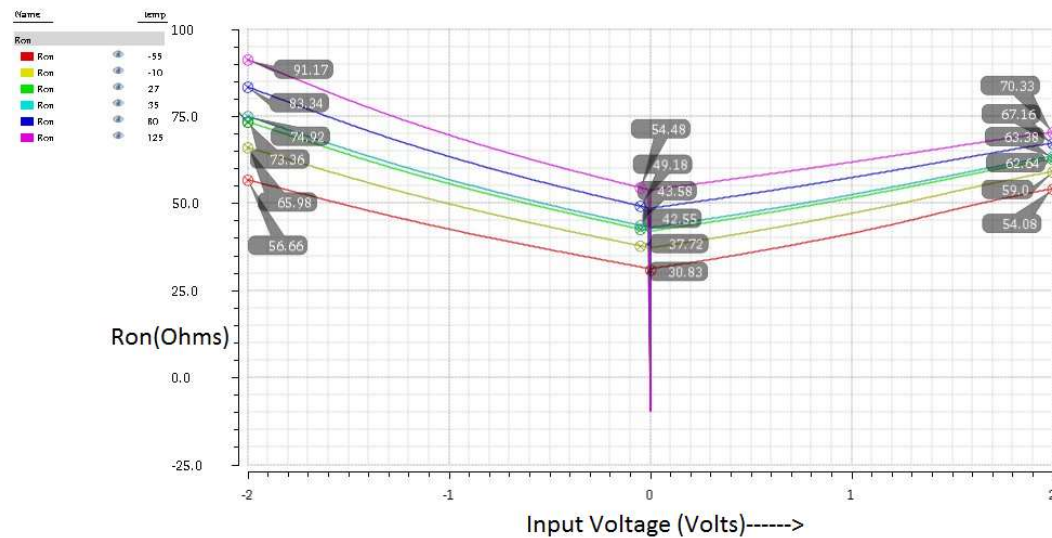


Figure 9 : Parametric analysis by varying the temperature with respect to input voltage

Figure 9 shows the parametric analysis of transmission gate switch where the temperature is varying from -55°C to 125°C . Input voltage is also varied from -2 Volts to 2 Volts. Characteristics between the On-resistance and input voltage is shown above in Figure 9.

From Table 2 I can see that the On-resistance of the switch is also depends upon the operating temperature. I have taken the different values of temperature in the range of -55°C to 125°C in six steps and at each point of temperature I have noted down the voltage drop across the switch and the value of current through load resistance and then from these values I have calculated the On-resistance of the switch at 3 input values of 0 Volts, -2 Volts and 2 Volts. By analysing the Table 2 I can see that on increasing the temperature the value of On-resistance is always increases. Hence I can say that the switch possess the positive temperature coefficient (PTC) of resistance.

Table 2 : Variation of R_{ON} with respect to Temperature

Temperature (°C)	$R_{ON}(\Omega)$ $V_{in} = 0 \text{ V}$	$R_{ON}(\Omega)$ $V_{in} = -2 \text{ V}$	$R_{ON}(\Omega)$ $V_{in} = 2 \text{ V}$
-55	30.83	56.66	54.08
-10	37.72	65.98	59.0
27	42.55	73.36	62.64
55	43.58	74.92	63.38
80	49.18	83.34	67.16
125	54.48	91.17	70.33

3.3.2 Variation of On-resistance (R_{ON}) with width of nMOS transistor

The aspect ratio of the nMOS transistor (W/L) has been varied by varying the width (W_n) from $5\mu\text{m}$ to $20\mu\text{m}$ (whereas the value of length of transistor (L) is maintained at $0.335\mu\text{m}$) and then the parametric analysis of transmission gate switch where the width of nMOS transistor is varying from $5\mu\text{m}$ to $20\mu\text{m}$. The input voltage is also varied from -2 Volts to 2 Volts and the corresponding values of the On-resistance for the given range of the width is noted as shown in the Table 3.

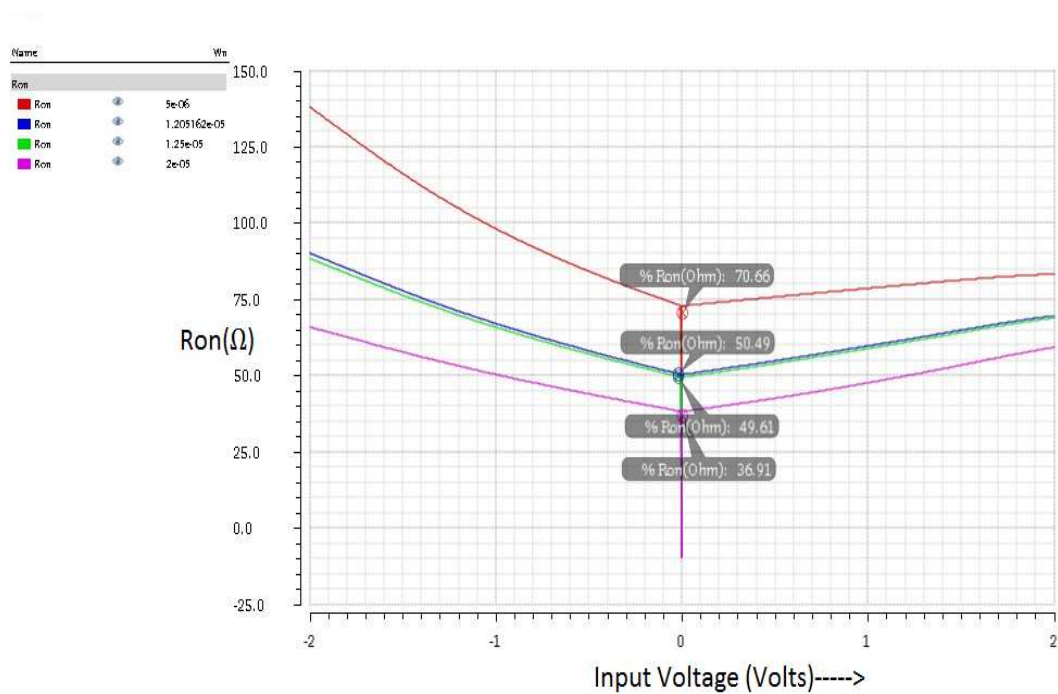


Figure 10 : Parametric analysis by varying the width of nMOS transistor with respect to input voltage

Figure 10 shows the characteristics diagram of On-resistance versus input signal voltage applied to the switch. This diagram is obtained by doing the parametric analysis in Cadence Virtuoso tool.

From Table 3 it can be seen that the On-resistance is directly proportional to the width of nMOS transistor. On increasing the width of nMOS transistor, the On-resistance of the switch increases.

Table 3 : Variation of R_{ON} with respect to width of nMOS transistor

W_n (μm)	R_{ON}(Ω)
5	70.66
12.05162	50.49
12.5	49.61
20	36.91

CHAPTER 4

DESIGN OF ANALOG MULTIPLEXER

4.1 Introduction to Analog Multiplexer

A multiplexer (also sometimes spelled as multiplexor) is a device that can select a signal from several different input signals and transmit either one or more output signals. Analog multiplexers are used in several real time applications such as data acquisition systems in satellites, in automatic test equipment systems (ATES), in audio signal routing (ASR), in battery powered systems, in medical instrumentation systems and also in single supply systems etc.

Analog Multiplexer is preferred over digital multiplexer because generally the signal available to us are analog in nature and I can directly process those signals without changing its domain with the help of analog multiplexer. It is easy to design and also decreases the complexity of the system. No need to convert the analog signal into digital domain and then digital to analog. So I do not need to design the extra circuitry of analog to digital converter (ADC) and digital to analog converter (DAC).

Analog systems have very high level of accuracy, that is the most basic and important use of analog systems. Of course with digitalisation comes high noise immunity but at a price of less accuracy. Hence trade-off between accuracy and noise immunity exists.

4.2 Architecture comparison

I have already compared between pass transistor (nMOS and pMOS) switch and the transmission gate in Chapter 3 and it is found that transmission gate is best for designing of analog multiplexer. From the design specification given in Table 1, the input signal frequency I have taken is 20 KHz.

There are two sorts of architecture to design and fabricate a simple analog multiplexer. Out of them one is single stage architecture and another one is multistage structure. For low frequency applications, the appropriate architecture is single stage architecture and it is because the fact that the On-resistance (R_{ON}) and load capacitance (C_L) form a low pass filter. For the proper functioning of low pass filter the cut off frequency of the channel ought to be greater than the input signal frequency. This is also known as Nyquist criteria. So let us take the cut off frequency of the filter is 10 times than the input signal frequency for the proper operation of output swing. Hence for $R_{ON}=75\Omega$, I can calculate the load capacitance is 100pF.

If I compare both the architecture I can simply say that for low frequency application single stage architecture is best suited whereas for high frequency applications I preferred multi stage architecture for designing of analog multiplexer. This is the main advantage of single stage architecture over multi stage architecture because the On-resistance and the propagation delay of single stage is less as compared to multistage. For high frequency applications the single stage design comes up short and multistage design is generally preferred [4].

4.3 Test setup for Crosstalk measurement

Crosstalk is basically the amount of signal cross coupling from an “OFF” state of analog input to the output of another “ON” state of channel output. Crosstalk is generally measured in decibels (dB). Crosstalk is an undesired phenomenon caused by the coupling capacitances exists between the channels and it leads to a significant distortion in the output signal.

Equation (2) provides the basic formula to calculate the amount of crosstalk in decibels (dB).

$$\text{Crosstalk (dB)} = 20 \log \frac{V_{\text{out}}}{V_{\text{in1}}} \quad (2)$$

Considering a 2:1 simple analog multiplexer as appeared in Figure 11. A sinusoidal Input1 signal of frequency 20 KHz with peak to peak amplitude of 2 Volts is applied to channel 1 or Switch 1 (S1) and there is no input signal is applied to channel 2 or Switch 2 (S2) that is Input2 is grounded. Hence the switch of second channel is closed. In ideal case, the output of analog multiplexer must be 0 Volts for channel 2. But once I did the simulation practically it is found that there is a distortion of μV range in the output of analog multiplexer. It is due to the adjacent channel input [4].

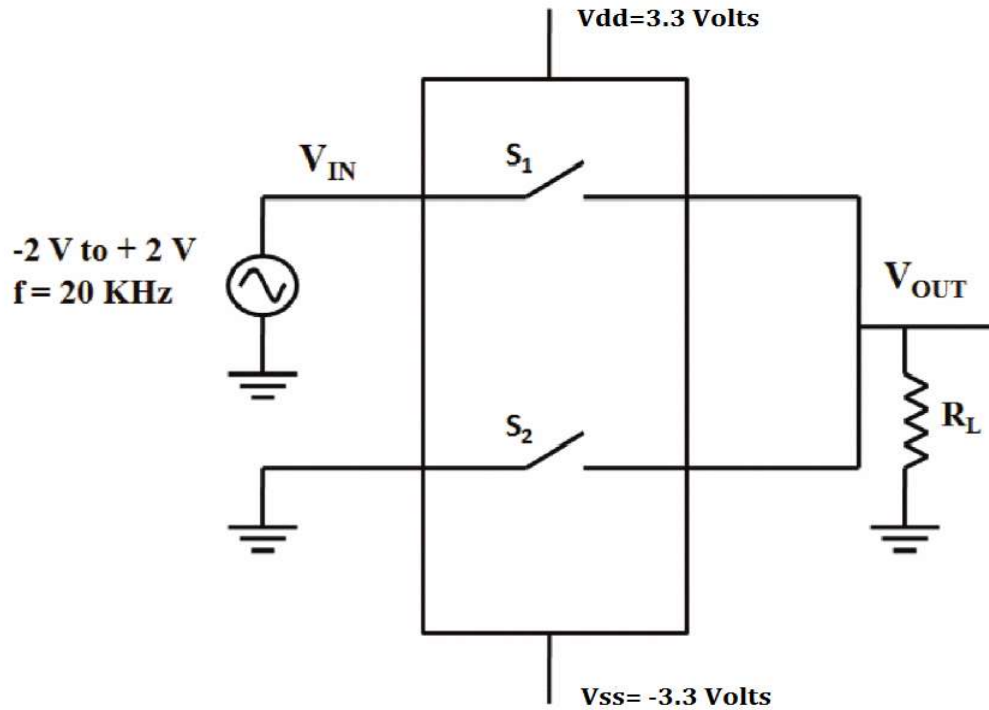


Figure 11 : Test setup for Crosstalk measurement

The crosstalk output of analog multiplexer is shown in Figure 13. If I increase the number of input channels then the crosstalk will also be increased and this will cause a huge amount of distortion in the output. Hence to overcome this issue, one alternate best solution has been proposed. So to avoid the distortion at output break before make switching condition for designing of analog multiplexer is proposed. In the case of break before make condition, it will break the output of the present channel before changing to the output of next channel. The waveforms for crosstalk is obtained by performing the Transient analysis in Cadence.

Figure 12 shows the schematic circuit diagram of 2:1 analog multiplexer. This diagram is designed in Cadence Virtuoso tool. From the diagram I can see that there are two switches in parallel to form two channels for analog multiplexer. Each switch is connected to dual power supply of 3.3 Volts as VDD and VSS as shown in the Figure. Input 1 is applied to switch 1 and Input 2 for switch 2 is grounded. Control signal also applied to both the switches. Control signal directly given to switch 1 whereas the inverted control signal is applied at switch 2. At output to measure the voltage load resistance (R_L) of $10K\Omega$ is connected.

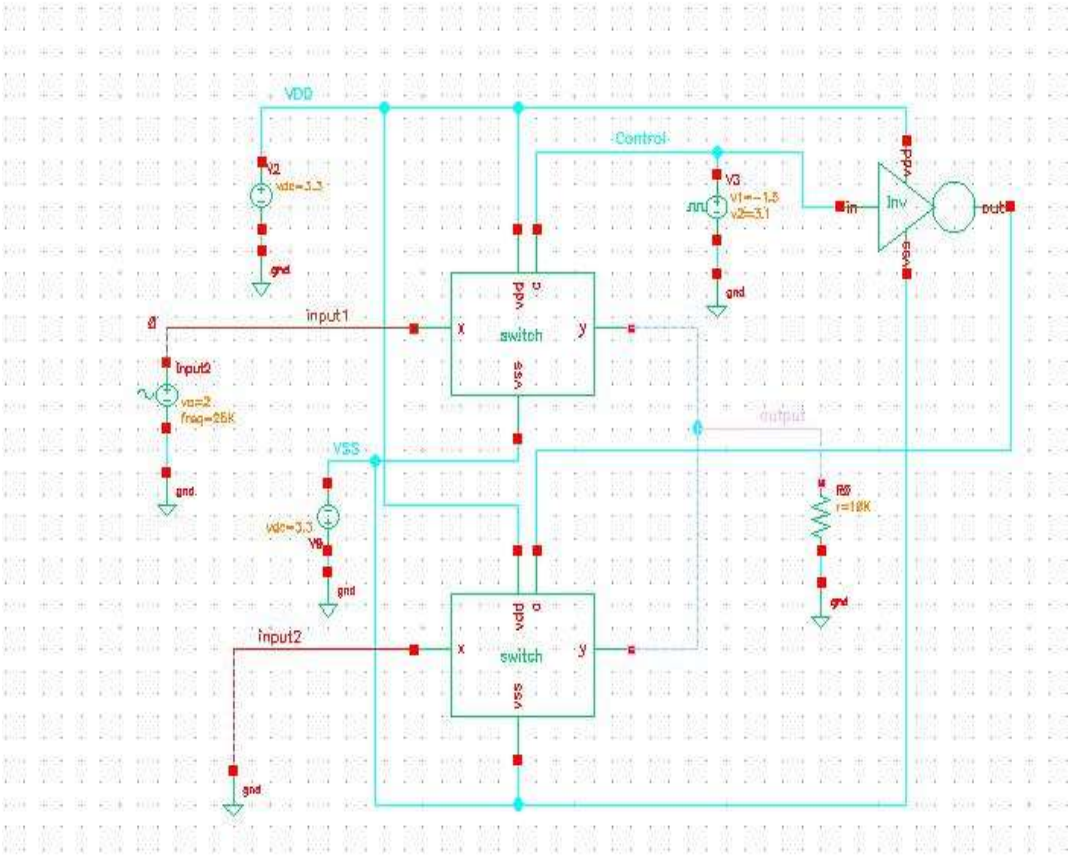


Figure 12 : Schematic circuit diagram in Cadence for Crosstalk measurement

Figure 13 shows the crosstalk output waveform for analog multiplexer. The input signal of frequency 20 KHz is applied at channel 1 and input to channel 2 is 0 Volts. After applying the input select the Transient analysis in cadence from 0 to 800 μ sec. All the signal at input and output is plotted with respect to time and the waveform is shown in figure. From the figure I can see that when the input of channel 2 is at 0 Volts then also in the output waveform I are getting the distortion of 1.60684 μ V. It is due to the crosstalk exists in the circuit. I can measure this crosstalk amount in decibels (dB). This leads to a significant amount of distortion in output.

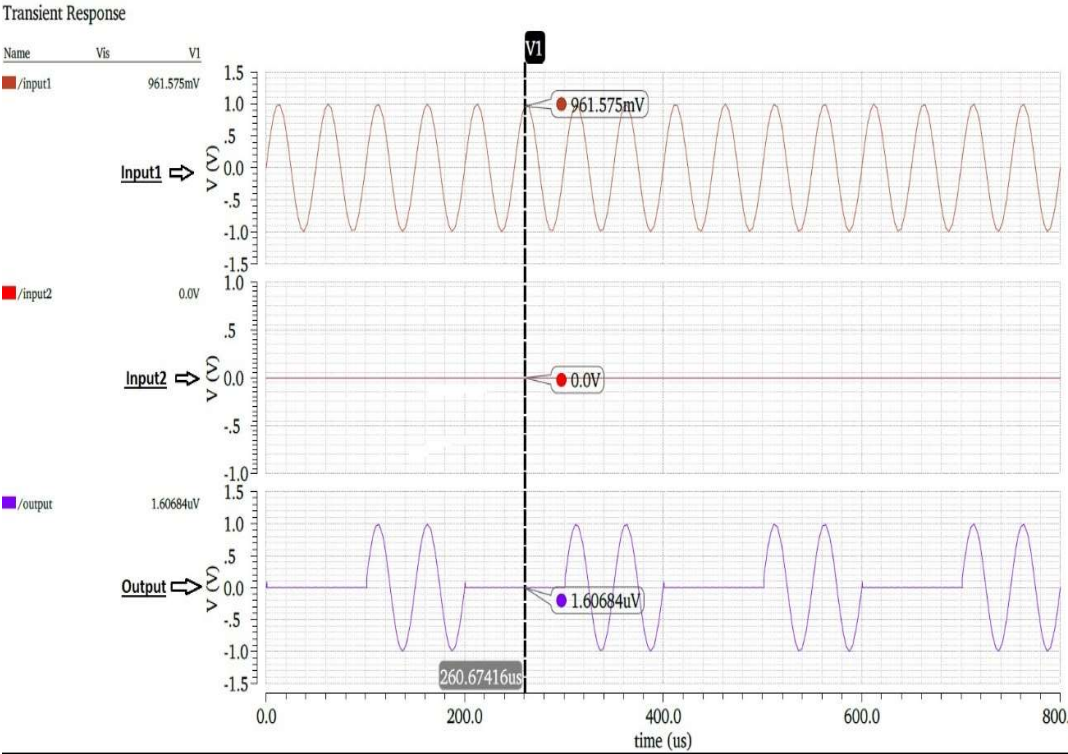


Figure 13 : Crosstalk Output waveform

4.4 Break-before-make Condition for an analog multiplexer

4.4.1 Need of Break-before-make switching condition

When I are going to increase the number of input channels to an analog multiplexer it leads to crosstalk that is signal of one channel try to overlap with the signals of another channel at the output. Hence to reduce or overcome this crosstalk issue it is proposed to implement the analog multiplexer with break before make switching condition.

The basic concept of break-before-make switching condition is that whenever the switch closes it must be closed gradually with a significant delay but at whatever point a switch opens it should open immediately as soon as possible. This is why the on-time (T_{ON}) of the switch must be greater than off-time (T_{OFF}) [5], [6], [7], [8].

4.4.2 Logic diagram of Break-before-make condition

In the datasheet of NXP Semiconductors 74HC4067/74HCT4067 [9], the logic diagram of break-before-make switching condition has been implemented. In which CMOS invertors and digital logic gates are used as a control signals to control the select lines of input channels of the analog multiplexer. In this thesis I also used the same logic to implement the break-before-make logic by reducing the number of transistors. Here the 2 to 1 analog multiplexer logic is implemented with the help of only 4 transistors. CMOS inverter is simply implement by 2 transistors (nMOS and pMOS) and dual power supply of 3.3 Volts. Digital logic gates are also implemented with the help of transistor-transistor logic.

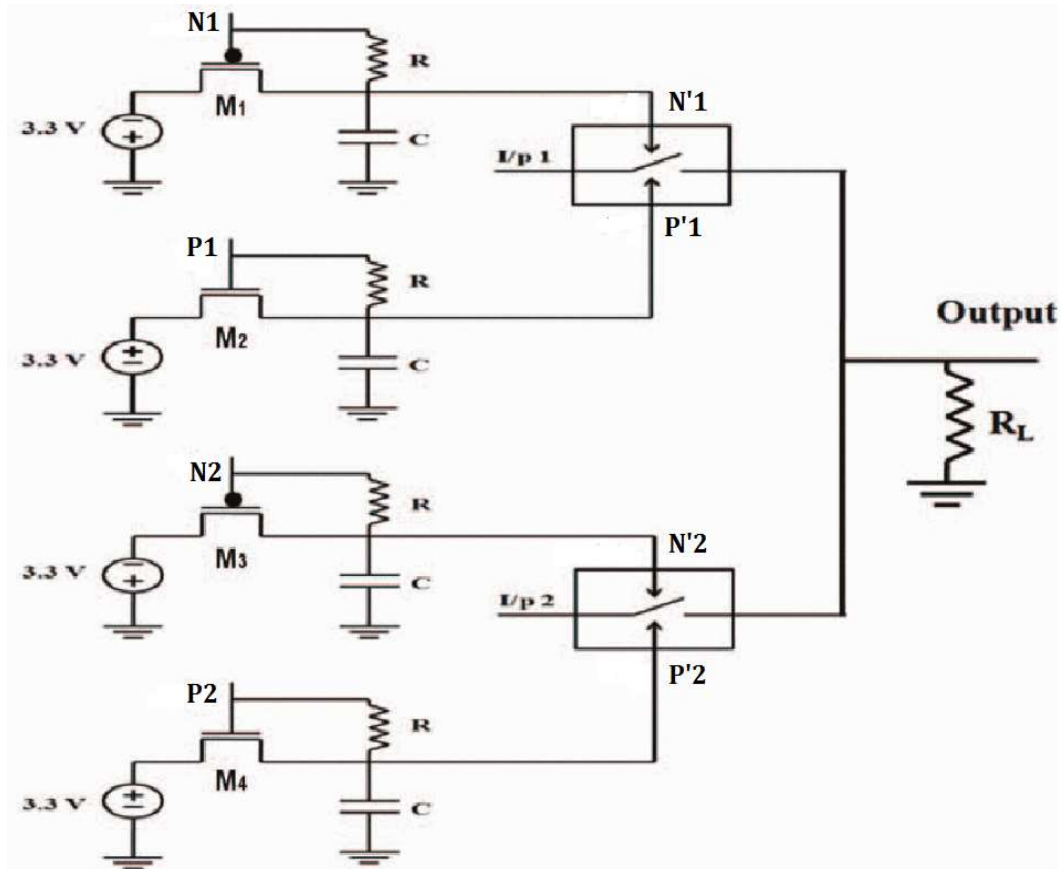


Figure 14 : Logic diagram of Break-before-make condition [1]

Figure 11 shows the logic diagram of break before make switching condition for analog multiplexer. There are two switches and input signal is applied to both the switch. The control signal for analog multiplexer is implemented by two basic signals at each switch. For switch 1 control signal is generated by N'1 and P'1 and for switch 2 control signal is generated by N'2 and P'2 respectively. These 4 signals are obtained by a special logic so that the ON time of the switch is greater than the OFF time of the switch. Hence the switch opens immediately and closes slowly with a time delay of 100 ns and the break before make switching is so implemented.

Figure 15 shows schematic diagram of Break-before-make switching condition which is designed in cadence virtuoso analog environment tool. Output is taken across the load resistance of 10 K Ω . Dual supply of 3.3 Volts is used for biasing purpose.

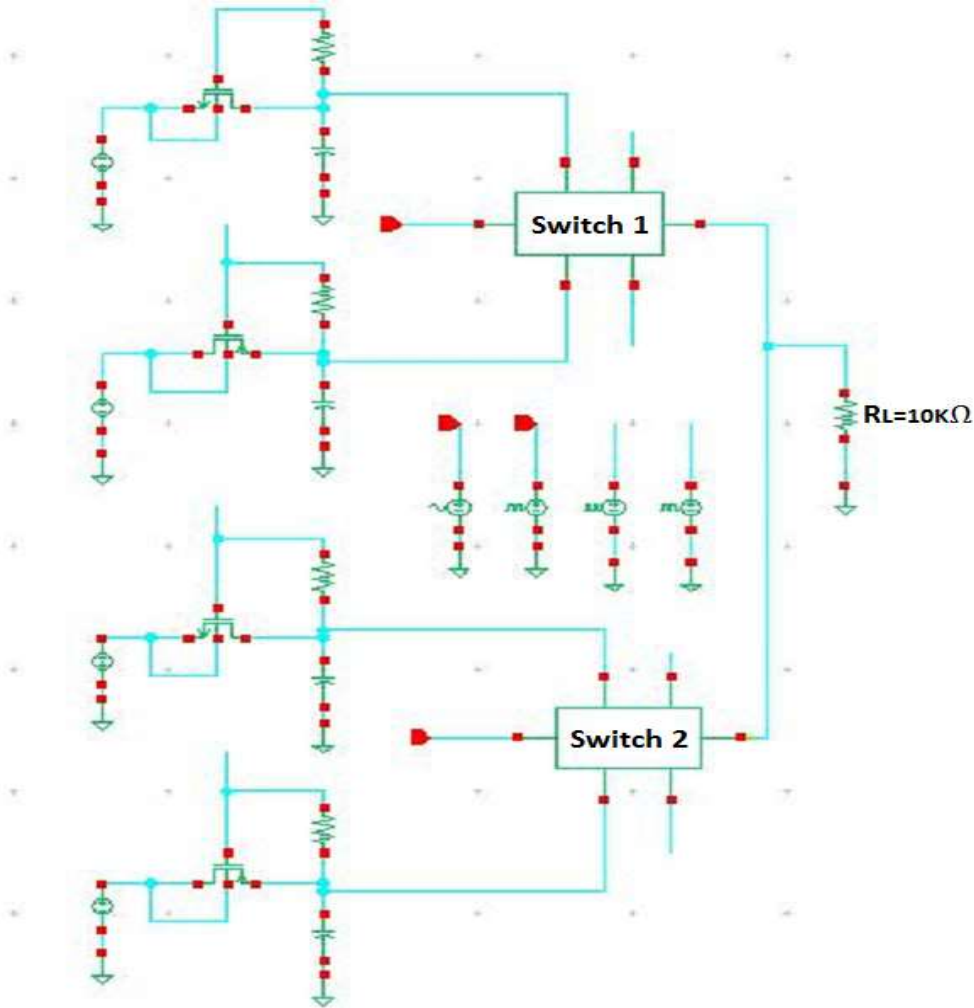


Figure 15 : Schematic diagram of Break-before-make condition in Cadence

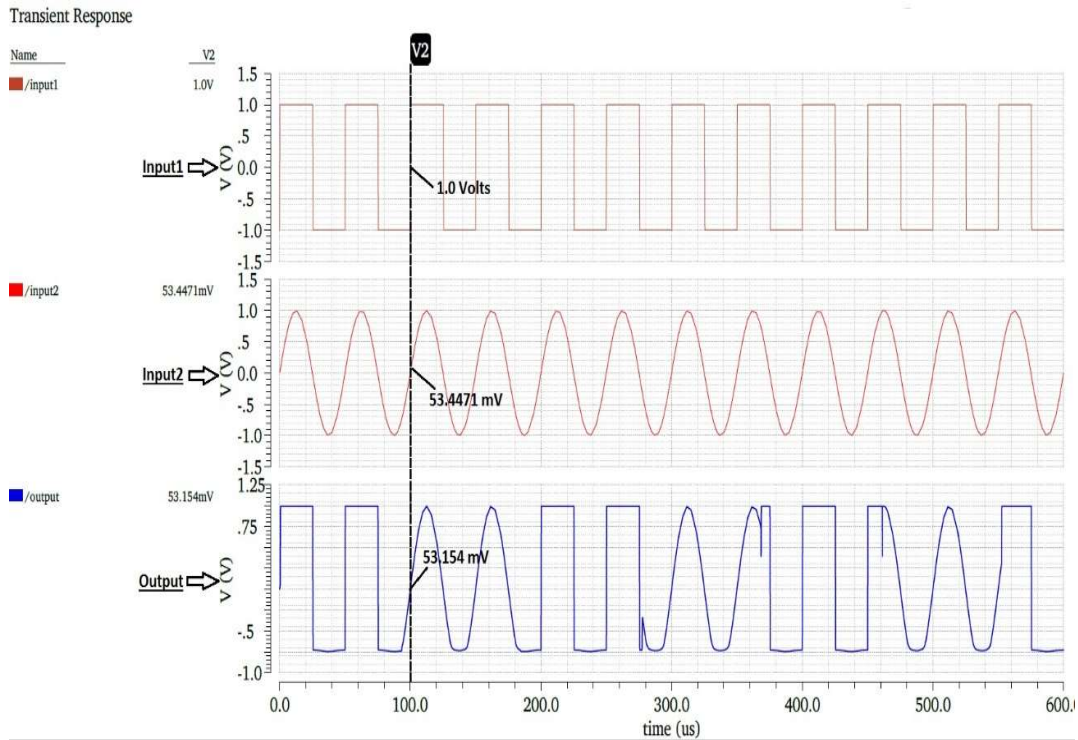


Figure 16 : Output waveform with break before make condition

The circuit presented in Figure 15 has met break-before-make switching condition. There are the 128 digital control signals from (N1, P1) to (N64, P64). These signals are given to gate terminals of nMOS and pMOS transistors of corresponding switches S1 to S64. Whenever N1 goes high (P1 goes low), the transistor M1 opens (M2 opens) hence the N1 (P1) signal passes through an RC circuit [1].

For the break before make switching delay of 100 ns, assuming the value of capacitance $C=10\text{pF}$ and thus the value of resistance $R=10\text{K}\Omega$ is chosen. Hence the switch (S1) closes slowly. Similarly whenever N1 goes low (P1 goes high), the transistor M1 closes (M2 closes) thus the switch (S1) opens immediately. Hence the break before make switching condition is implemented. This method described here is

applied to all 128 control signals (both for nMOS and pMOS) and the corresponding break-before-make switching condition output is shown in Figure 16 [1].

CHAPTER 5

EXPERIMENTAL RESULTS AND COMPARISON

5.1 Experimental Analysis

The test circuits of on-resistance of the switch of analog multiplexer, crosstalk of analog multiplexer, the input and output capacitances, the gate capacitance and the break-before-make switching condition are implemented and simulated successfully in Cadence Virtuoso Analog Design. The results are arranged and compared with other designs also as shown in Table 4 with meeting all the design specifications that are shown in Table 1. A comparative analysis of our multiplexer design with Intersil HS-1840ARH and Intersil ISL71840SEH is shown in Table 4 [1]. Both HS-1840ARH and ISL71840SEH are analog multiplexers for space applications [10], [11].

For the proposed analog multiplexer the value of On-resistance is around 75Ω . The input voltage is -2 Volts to 2 Volts. The delay for break-before-make switching condition of proposed analog multiplexer is 100ns. The supply voltage I have used in our circuit is 3.3 Volts.

**Table 4 : Compare results of proposed multiplexer with HS-1840ARH
and ISL71840SEH**

Specification	Intersil HS-1840ARH	Intersil ISL71840SEH	Proposed Multiplexer
Supply Voltage	±15 Volts	±10.8Volts to ±16.5Volts	±3.3 Volts
Input Voltage range	VCC to 5Volts	±15 Volts	±2 Volts
Ron	300Ω	700Ω	Less than 75Ω
Crosstalk	-	47 dB	104 dB
Break before make delay	25ns	50ns	100ns

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

I have discussed analog switch characteristics and its main parameters like On-resistance and crosstalk. After the characteristics of analog switch I also compared single stage architecture and multistage architectures of analog multiplexers. I also provided the test setup to compute R_{ON} and crosstalk of analog multiplexer.

Parametric analysis of analog switch is performed by varying the temperature and aspect ratio (W/L) of the nMOS transistor and plotted the characteristics between On-resistance and input voltage for different temperature from -55°C to 125°C in total 6 steps.

Moreover with the help of parametric analysis and by varying the width of nMOS transistor I have plotted the characteristics between On-resistance and input voltage for different at different values of width of nMOS transistor in total 4 steps as shown in the Table [2] and Table [3].

In this research paper I have mainly focused on the designing of analog multiplexer only and overcome the issue of crosstalk in the system by implementing the break-before-make switching logic which is achieved by using only 4 transistors for single switch with the help of Cadence Virtuoso analog environment tool.

The crosstalk of proposed analog multiplexer is obtained 104 decibels which is better than any other analog multiplexer present.

In the same way the other analog modules of data acquisition system like filters, amplifiers, data converters, sample and hold circuits I have shown in Figure 1 can be designed appropriately by meeting all the respective design specifications which helps in building up a complete data acquisition system. This system can be used for an effective communication with the satellites.

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