A

DISSERTATION REPORT

on

DESIGN AND ANALYSIS OF LOW VOLTAGE HIGH SPEED DOUBLE TAIL COMPARATOR

Submitted in

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Master of Technology in Very-Large-Scale Integration

to

Supervisor:
Dr.C.Periasamy
Assistant Professor

Submitted by:
Ansh Agrawal
2015PEV5342

Department of Electronics and Communication Engineering
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Malaviya National Institute of Technology, Jaipur

Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that the dissertation report entitled "**Design and analysis of Low Voltage High Speed Double Tail Comparator"** composed by **Ansh Agrawal (2015PEV5342)**, in the partial fulfilment of the degree master of technology in **Very-Large-Scale Integration** of Malaviya National Institute of Technology Jaipur, is the work completed by him under my supervision, hence approved for submission during academic session 2015-2017. The contents of this dissertation report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Place: Jaipur

Date:

C. Periasamy

Assistant Professor

Dept. of Electronics and Communication

Malaviya National Institute of Technology

Jaipur, India

DECLARATION

I, **Ansh Agrawal**, declare that this dissertation titled , "**Design and Analysis of Low Voltage High Speed Double Tail Comparator**" and the work presented in it is my own.
I confirm that:

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- ✓ Where any part of this dissertation has previously been submitted for a degree or any other qualification at M.N.I.T. Jaipur or any other institution, this has been clearly stated.

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- ✓ Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this Dissertation is entirely my own work.

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Abstract

As today's world has become smart i.e. digitalization has been spreading rapidly, there is a need for ultra- high speed ,low power and area efficient analog -to-digital converters(ADCs).This is pushing towards the use of clocked regenerative comparator to enhance the speed and power efficiency. This paper presents , a dynamic double tail comparator with positive feed-back for latch regeneration has been designed with high-speed. Idea behind this design of CMOS comparator is to increase the latch regeneration speed by increasing the voltages of intermediate stages. For this purpose, two control transistors (Mc1 and Mc2) are added to the first stage in a cross-coupled manner. The results were simulated in Hspice 180nm, 90nm and 45nm technology. The modified comparator shows significant reduction in power dissipation and delay compared to the other dynamic comparators. The average power of proposed comparator in 45nm technology is reduced by 67.28% than at 90nm technology due to the decrease in channel length of the transistors. The delay of proposed comparator is reduced by 15.70% in compare to the double tail dynamic latch comparator in 90nm technology. Thus, the proposed transistor is energy efficient when compared to other topologies at 45nm, 90nm and 180nm technologies.

Index Terms— Clocked regenerative comparators, Conventional Single tail dynamic comparator, Conventional double tail dynamic comparator, Flash ADC, Pre-amplifier based comparator.

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Chapter 1

Introduction

1.1 Motivation

As we know that in most of the analog-to-digital converters (ADCs), Comparator is one of the fundamental building block. Due to requirement of comparators, which are having good speed and consumes less power ,in many high speed ADCs such as flash type ADCs, CMOS clocked regenerative comparator are very useful. These comparator have less power dissipation, high speed, high input impendence and rail to rail output swing. To change a input voltage difference of small order to a full scale digital level , these comparator make use of positive feedback mechanism, in which two inverters are connected back-to-back, also called latch, to enhance the latch regeneration time.

However, due to device mismatching for example difference in threshold voltage V_{th}, current gain factor β and parasitic and output load capacitance, an input-referred latch offset voltage (hence offset voltage) limits the accuracy of these comparators [5], [6]. Being this reason, one of the important parameter for the designing of latched comparator is offset voltage. In order to minimize mismatch, larger devices can be used in latching stage but it increases the power dissipation as well as delay. More practically, if we use a cross coupled inverters (i.e. latch) after the pre amplifier stage, the offset voltage can be minimize. Figure 1 shows this type of configuration. It is able to amplify a difference of small order in input voltage to a voltage which is enough to minimize the latch offset voltage [11].

Due the fact that the supply voltage in the modern CMOS technology is scaled but the threshold voltage is not scaled at the same pace, comparator of good speed in ultra-deep sub-micrometer CMOS technology suffer from low supply voltages[3]. So to design high speed comparator at low supply voltage is a challenging task. In other words, for a particular technology , to enhance the speed, transistor of larger size are required in order to compensate the reduction of supply voltage, On the other hand it also implies that we need more area of the die and power.

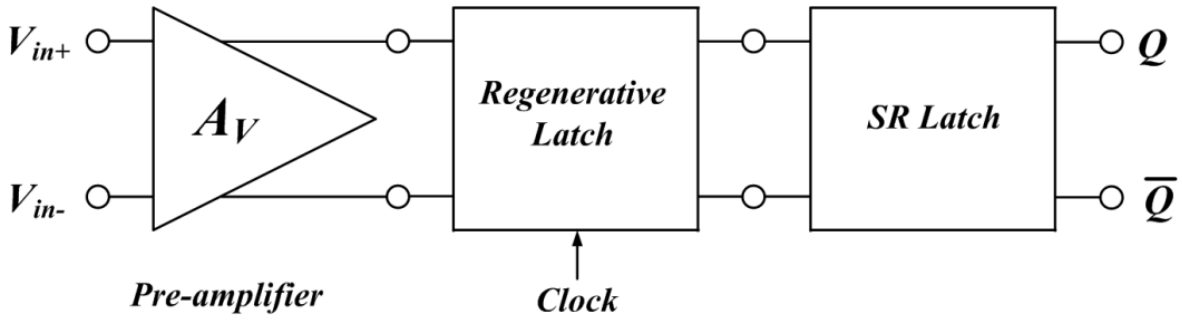


Figure 1: Typical block diagram of a high-speed voltage comparator [30]

In the literature, various kinds of CMOS comparators can be found. These comparators can be classified into three category namely: *Open-loop Comparators* (op-amps without compensation), *Pre-amplifier Based Latched Comparators* and Clocked regenerative *Comparator*. In this paper, different types of clocked regenerative comparator topology will be fully analyzed along with their pros and cons and also their operating principles and experimental results of the speed and power consumption will be discussed.

1.2 Thesis Organization

A new dynamic latched comparator is discussed in this thesis which gives high speed and low power compare to conventional double tail and single tail dynamic latched comparators. The other parts of this thesis are organized as follows. **Chapter 2** reviews the important features of a voltage comparators, and also different types of voltage comparator are introduces. **Chapter 3** explains the operation principles of each comparator and compares them in terms of speed and power consumption. **Chapter 4** presents simulation results and conclusion. **Chapter 5**.Models files for 180nm and 45nm technology and HSPICE netlist files for each comparator circuit are attached in the Appendix.

Chapter 2

Literature Review

Important features of a voltage comparator will be reviewed in this chapter. In addition, a different kind of comparator architectures will be reviewed after classifying them into three: *Open-loop Comparator, Pre-amplifier Based Latched comparator,* and *Clocked Regenerative Comparator*. Especially, the clock regenerative comparators will be discussed in detail.

2.1 Voltage Comparator

Basically a comparator is used to compare an analog signal with a reference or any other analog signal. Based on the comparison it gives a binary output (logic "0" or logic "1").Distribution of voltage over a large no of comparator is easier than the distribution of current, most of the converters employ comparison of voltage[9]. A voltage comparator is nothing but a 1-bit analog-to-digital-converter (ADC).

Symbolic representation along with the ideal and practical voltage transfer curves of a voltage comparator are shown in **Figure 2**. In this **Figure 2 (b)**, output is V_{OH} (logic level high "1" = V_{DD}) when Vinp − Vinn− > +ve(>0) Otherwise its outputs is V_{OL} (logic level low "0" = 0V (or – V_{SS})).An ideal comparator has infinite gain, zero offset voltage and zero RMS noise. But in the case of practical comparator which is shown in **Figure 2 (c)**, outputs is V_{OH} when Vinp − Vinn− > V_{IH} + V_{OS} (+ |Vnoise|) and it outputs V_{OL} when Vinp − Vinn− < V_{IL} (− |Vnoise|). A practical comparator has finite gain, non-zero offset voltage and RMS noise.

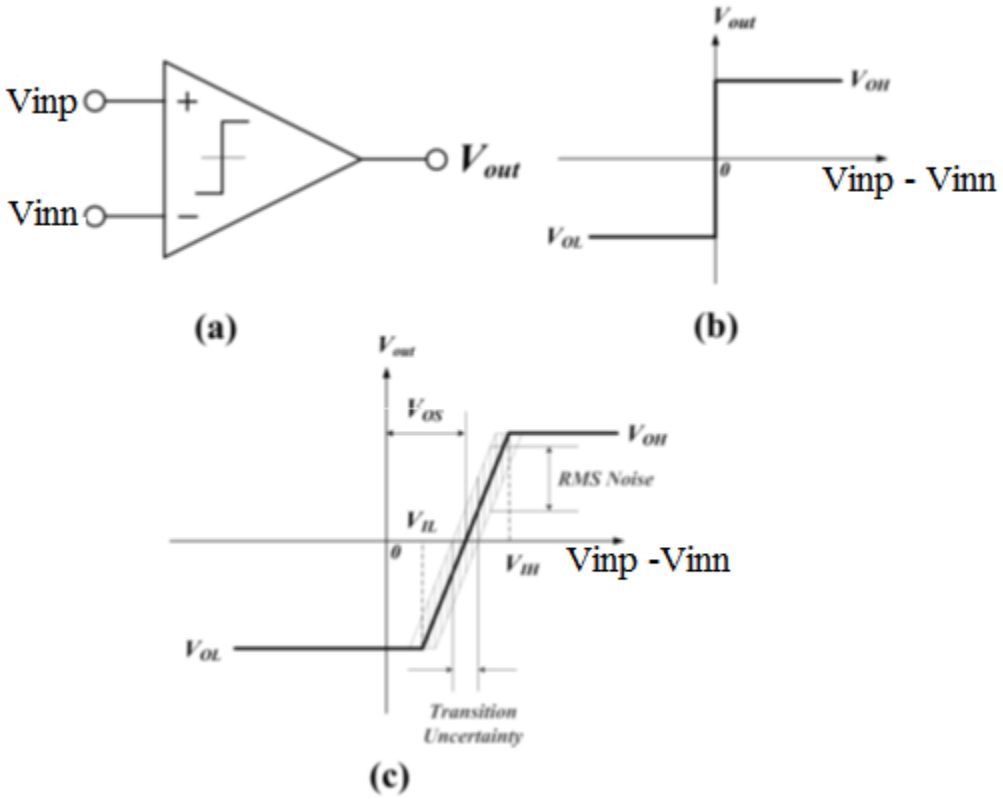


Figure 2: Comparator **(a)** Circuit symbol, **(b)** voltage transfer curve(Ideal), and **(c)** voltage transfer curve(Practical) [8].

2.2 Comparator Architectures

2.2.1 Open-Loop Comparators [8], [9], [10]

Open-loop, continuous time comparators, shown in **Figure 3** [8], are the type of op-amp (operational amplifier) in which no feedback is there. Open- loop comparators are those in which no frequency compensation is there so as to obtain the maximum bandwidth which is possible, hence time response is improved. But on the other hand, due to limited gain bandwidth product, these comparator are too slow for many application. With the same gain, cascading of open loop amplifiers results in larger product of gain and bandwidth compare to a single stage amplifier. But

still, cascading is not practically advantageous for many application because it costs more area and power consumption.

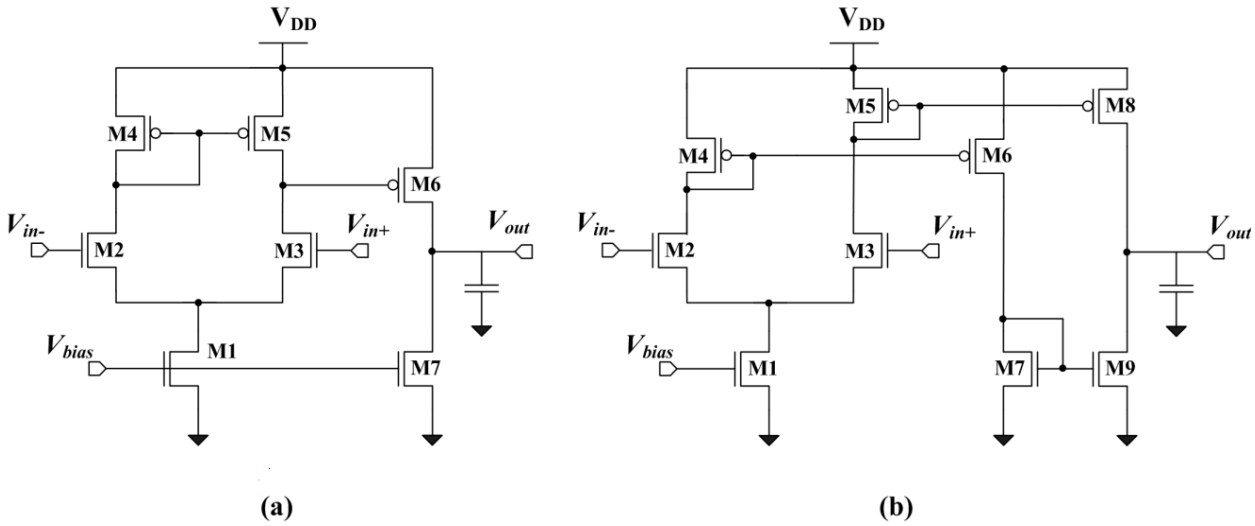


Figure 3: (a) Two-stage open-loop comparator circuit **(b)** Push-pull output open-loop comparator circuit [8]

2.2.2 Pre-amplifier Based Latched Comparators

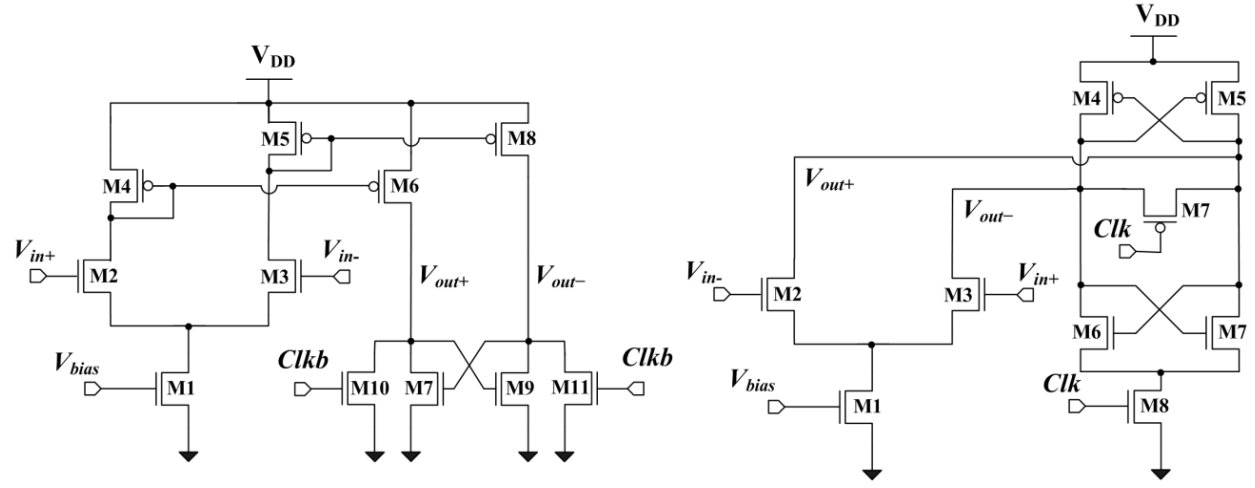


Figure 4: (a) A static latched comparator [16] **(b)** A class-AB latched comparator [25]

Figure 4 shows typical types of pre-amplifier based latched comparators [11]. The most important advantages of the these type of comparators are their fast speed compare to open loop comparator. Typically, a pre-amplifier, which has one or two stages of an open-loop comparator, has a gain of 4 - 10 V/V and it can reduce the input-referred latch offset voltage by its gain. For example, if a pre-amplifier has gain of 10 V/V and a latch stage has an offset voltage of 50mV, then the input-referred latch offset voltage will be 5 mV. Latched comparators commonly employ one or two clock signals (*Clk* and *Clkb*) to determine the mode of operation:

Track Mode : Also known as reset phase, resets the output and tracks the input.
Latch Mode : Also known as evaluation phase, toggles the output by using a positive feedback.

For the operation of the circuit shown in **Figure 4 (a)** [16-22], during reset phase (Clkb=0V), both complementary output V_{out+} and V_{out-} are reset to 0V by reset (switch) transistor M10 and M11. During evaluation phase (Clkb=V_{DD}), as the reset transistors are off, the comparison will be performed by a positive feedback from transistor M7 and M9. While this comparator present relatively large static power consumption and slow regeneration due to its limited current operation make it less attractive [16]. Similarly, the operation for the circuit shown in **Figure 4 (b)** [25-29], during reset phase (Clk=0V), pMOS reset transistor M7 will be shorted and make both outputs equal: $V_{out+} = V_{out-}$ while nMOS transistor M8 is off. During evaluation phase (Clk=V_{DD}), as the reset transistor M7 is off and the tail transistor of the latch M8 is on, the comparison will be made by a positive feedback formed from back-to- back cross coupled inverter pairs (M4/M6 and M5/M7). While this comparator shows faster speed and consumes less power, it generates more kickback noise and during reset phase both outputs (V_{out+}, V_{out-}) are not reset exactly to either V_{DD} or 0V [11].

It can be concluded that pre-amplifier based latched comparators, which is a combination of a pre-amplifier and a latch, offer fast speed and low offset but still consumes static power.

2.2.3 CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparator are widely used in many high speed ADCs. They have strong positive feedback in the regenerative latch so they are able to make decisions fast. In the analysis presented in the recent years, the performance of these comparators from different aspects were investigated. This section presents a comprehensive delay analysis; the delay time of two conventional comparator, i.e., conventional single tail dynamic comparator and conventional double-tail dynamic comparator are analyzed. Based on the analysis a new proposed comparator will be presented.

2.2.3.1 Conventional Dynamic Comparator

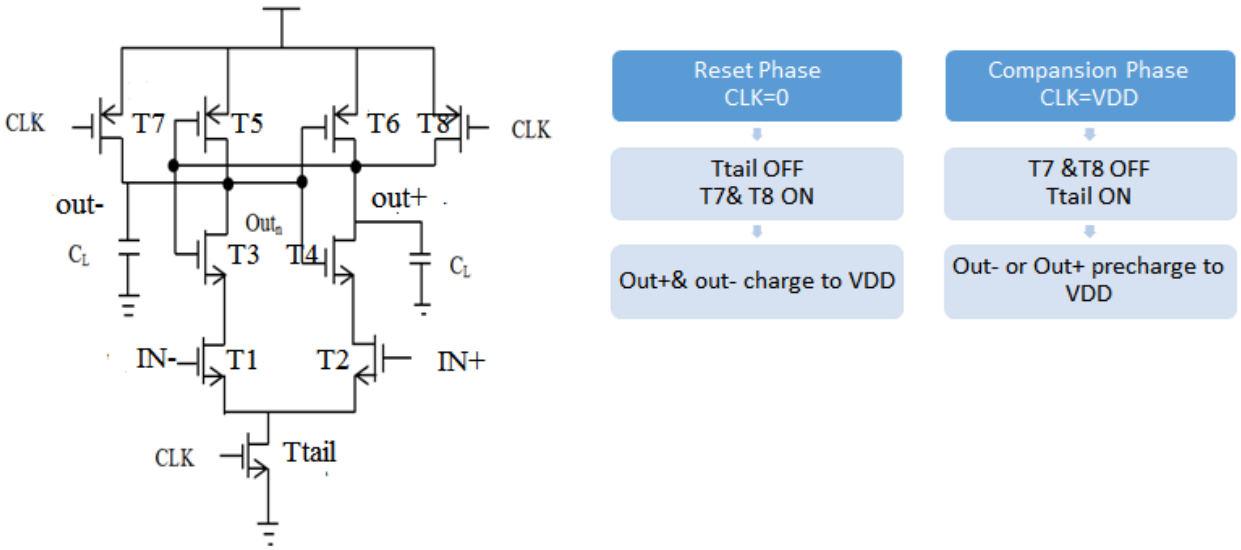


Figure 5: (a) Conventional Single tail Dynamic Comparator [3] (b) Flow Chart

The schematic diagram of the conventional single tail dynamic comparator is shown in Fig. 5(a) [3].It is widely used in ADCs. It has high input impedance, rail-to-rail output swing and no static power consumption. The working of this comparator can be understand as: When CLK =0 (logic

low="0V") i.e. reset phase , T_{tail} is off, reset transistors (T7&T8) push both output nodes out+ and out- to V_{DD}(logic high). It defines the initial condition. When CLK=V_{DD} (logic high="1") i.e. evaluation phase, reset transistors T7 and T8 are off while T_{tail} turns on. Depending on the input voltage IN- & IN+ applied at T1 &T2 respectively, Output voltages out+ & out- starts discharging with different rates. Assume the condition: VIN+ > VIN-, discharging of out+ is faster than out-. So out+ (discharged by drain current (I2) of transistor T2), falls down to V_{DD}–$|V_{thp}|$ before out- (discharged by drain current (I1) of transistor T1). This will turn on pMOS transistor (T5) and latch regeneration caused by back-to-back inverters (T3, T5 and T4, T6) is initiated. This pulls out- to V_{DD} and out+ discharges to ground. For the condition VIN+ < VIN-, the circuits works vice versa. Operation of conventional dynamic comparator is summarized in Flow chart diagram 5(b).

From the figure Fig. 5(a), the total delay of this comparator is comprised of two delay units, t_0 and t_{latch}. Where t_0 represents the capacitive discharging of the load capacitance C_L until the first p-channel transistor (T5/T6) turns on. For the condition: voltage at node IN+ is higher than INN- (i.e., VIN+ > VIN-), out+ discharges (discharged by I_2) faster than out- (discharged by I_1) Consequently, the discharge delay (t_0) is given by

$$t_0 = \frac{C_L . |V_{thp}|}{I_2} \cong \frac{2C_L . |V_{thp}|}{I_{tail}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

In (1), since $I_2 = \frac{I_{tail}}{2} + \Delta I_{in} = \frac{I_{tail}}{2}$ + gm1, 2 ΔV_{in}, for a small value of input difference voltage (ΔV_{in}), I_2 is approximately equal to the half of the tail current and constant. The second term (t_{latch}) is the latching delay of two back to back connected inverters. Generally a voltage swing of $V_{out} = \frac{V_{DD}}{2}$ has to be obtained from an initial voltage difference V_0 at the output which is falling (e.g., out+).As half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [3]. Hence, the delay time of latch is, [3]

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \quad \text{.....(2)}$$ where

$g_{m,eff}$ is the effective trans-conductance of the cross coupled inverters. From the equation (2), we can say that t_{latch} has a dependency on the initial voltage difference (V_0) in a logarithmic manner at the time when the regeneration is started (i.e., at t = t_0). On the basis of (1), V_0 is

$$V_0 = |V_{out+(t=t_0)} - V_{out-(t=t_0}|$$
$$= |V_{thp}|\left(1 - \frac{I_2}{I_1}\right) \quad \text{..... (3)}$$

The difference in current, ΔI_{in}= $|I_1 - I_2|$, between the two branches is much smaller than I_1 and I_2. So, I_1 is approximately equals to the $\frac{I_{tail}}{2}$ so total delay

$$t_{delay} = t_0 + t_{latch}$$
$$= \frac{2C_L \cdot |V_{thp}}{I_{tail}} + \frac{2C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\,\Delta V_{in}} \cdot \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \text{..... (4)}$$

In the equation (4), $\beta_{1,2}$ is the current factor of input transistors and I_{tail} is dependent on input common mode voltage (V_{cm}) and V_{DD}. The impact of various parameters on delay can be explained by equation (4). The total delay of the comparator has direct relation with the load capacitance C_L and inverse relation with the input difference voltage (ΔVin). Apart from this, the delay has a dependency on the input common-mode voltage (V_{cm}) in a indirect way. When the V_{cm} is decreases, there is an increase in delay t_0 because lowering V_{cm} results smaller bias current (I_{tail}). It also shows that the increase in initial voltage difference (V_0), due to delayed discharge with smaller I_{tail} , results in reduction of t_{latch}. Simulation results confirms that reduction in V_{cm}, increases t_0 but reduces t_{latch} , ultimately leads to an increase in total delay. In [22], it has been shown that an input common-mode voltage (V_{cm}) which is 70% of the supply voltage is optimal regarding speed and yield. This circuit topology has the advantages like high input impedance, no static power consumption, rail-to-rail output swing, and good robustness against noise and mismatch [6].But it has some disadvantages like: due to stacking of transistors, a sufficiently high supply voltage is needed for a proper delay time. The cause is that, initially, only transistors T3

and T4 of the latch contribute to the positive feedback until the voltage level of one of the output node (out+/out-) has dropped below a level small enough to turn on transistors T5 or T6 to initiate latch regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage (V_{gs})for transistors T3 and T4, where the gate-source voltage of T5 and T6 is also small; thus, the delay time of the latch becomes large due to lower trans-conductance.

Another disadvantage of this comparator is that it has only one path of current,via tail transistor Ttail(I_{tail}), which defines the current for both the differential amplifier and the latch. In practical, we need a low value of tail current in order to keep the differential pair in weak inversion and a high value of tail current in order to enable fast regeneration in the latch [24]. But, as far as Ttail operates mostly in linear region, the tail current (I_{tail}) depends on input common-mode voltage, which is not accepted for regeneration.

2.2.3.2 Double Tail Dynamic Comparator

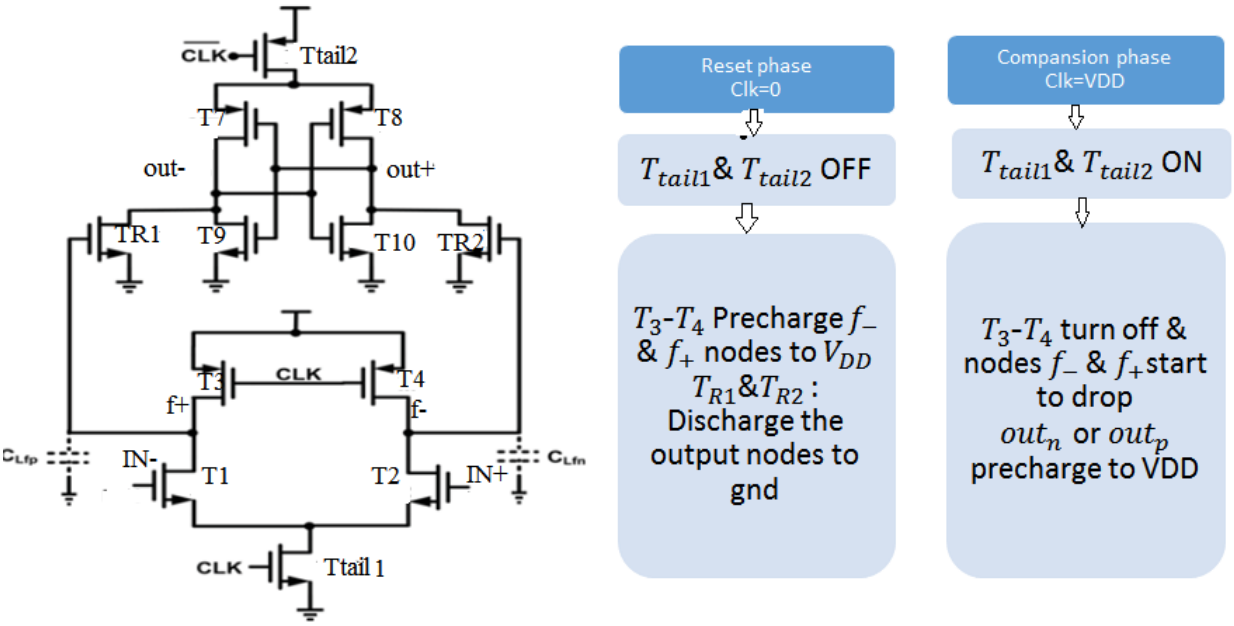


Figure 6: (a) Conventional Double Tail Comparator [6] (b) Flow Chart

To overcome the disadvantages of the single tail dynamic comparator, a double tail dynamic comparator with two stage (input-gain stage and output-latch stage), shown in **Figure 6 (a)**, was first introduced in [6]. Due to separate input and output stage this comparator has a lower and more stable offset voltage over wide common-mode voltage (V_{com}) ranges and operate at a lower supply voltage (V_{DD}) as well. Reason is that the sizes of tail transistors (Ttail1 and Ttail2) are designed in a way to obtain a smaller tail current (Itail1) for the input stage, so that a long integration time can be obtained, and a large tail current (Itail2) for the output stage to make the regeneration faster.

For its operation, during reset phase (*Clk=0V, Clkb=*V_{DD}), pMOS transistor pair T3 and T4 pre-charge f+ and f- node capacitances up to V_{DD} (sequentially, the input transistor pair for the output stage TR1 and TR2 are turned on and *Out* nodes are reset to 0V) while the both tail transistors (T_{tail1} and T_{tail2}) in the input stage and output latch-stage are off. During comparison phase (*Clk=*V_{DD}, *Clkb=0V*), once the input-stage tail transistor Ttail1 is turned on, each $f_{+,-}$ node voltage starts to discharge from V_{DD} to ground with different currents which are proportional to each applied input voltage. This results in voltage difference between f- and f_+ nodes. Then, the voltage difference built between $f_{+,-}$ nodes is passed to *out* nodes in the output latch-stage through the input transistor pair (TR1 and TR2) of the output latch-stage.

As expected, since this comparator requires Clk signal as well as inverse clk signal (clkb) for its operation, high synchronization between the two signals is require because the output stage has to detect the voltage difference between the f_+ and f- nodes of the input stage at very limited time. In the present structure, the intermediate stage transistors (TR1 and TR2) will be ultimately in cut-off, (since both output nodes, f_+ and f-, of input stage discharges to the ground) and hence they do not improve the effective trans-conductance of the latch. Apart from this, during reset phase, these nodes causes power consumption as they have to be charged from ground to V_{DD}.

Chapter 3

3.1 Proposed Double Tail Dynamic Comparator

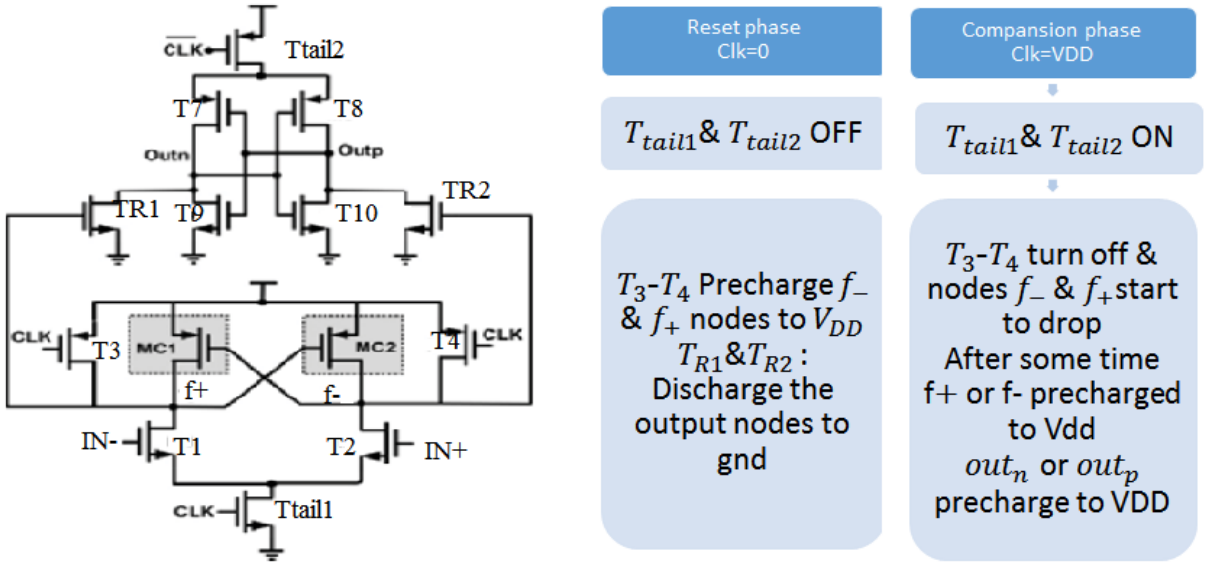


Figure 7: (a) Proposed double tail comparator [6] (b) Flow Chart

The working of the proposed comparator (fig 7(a).) is shown in flow chart (fig. 7(b)).Its operation can be described as: When CLK=0 (i.e. reset phase) , tail transistors Ttail1 and Ttail2 are off, which avoids static power, both f- and f_+ nodes are pulled to V_{DD} by T3and T4 respectively , which leads to control transistor (Mc1 and Mc2) in off stage. Sequentially, both latch outputs are reset to ground by Intermediate stage transistors (TR1 and TR2).

When CLK=V_{DD} (i.e. evaluation phase, Ttail1and Ttail2 are on), transistors T3 and T4 turn off. At the starting of this evaluation phase, the control transistors (Mc1, Mc2, T5 and T6) are still off (since output nodes of first stage, f- and f_+, are about V_{DD}). So, voltages at f- and f_+ start to drop with different current in proportion to the applied input voltages. Assume the condition: VIN+ > VIN-, results in faster discharging of f- node than f_+ node, (since I(T2)>I(T1)). As long as f-

continues to fall, the pMOS control transistor corresponding to f- (Mc1 in this case) starts to turn on, which pulls f_+ node voltage to V_{DD}; so second control transistor (Mc2 in this case) remains off, so f- node discharged to ground. In the case of conventional double-tail dynamic comparator, $\Delta Vf_{+,-}$ is just a function of input transistor trans-conductance and ΔVin [3], but in the case of proposed comparator as soon as the comparator detects that for instance node f- discharges faster, the corresponding pMOS transistor (Mc1 in this case) turns on, which pulls the other node f_+ to V_{DD}. As the time passes, the voltage difference between nodes f- and f_+ ($\_\Delta Vf_{+,-}$) rises in an exponential manner [3], so the latch regeneration time is reduces. Even though the idea of proposed comparator is effective, but when one of the control transistors (e.g., Mc1) turns on, a current path is there from V_{DD} to the ground via T1 and T_{tail} which results in static power consumption.

3.2 MODIFIED COMPARATOR

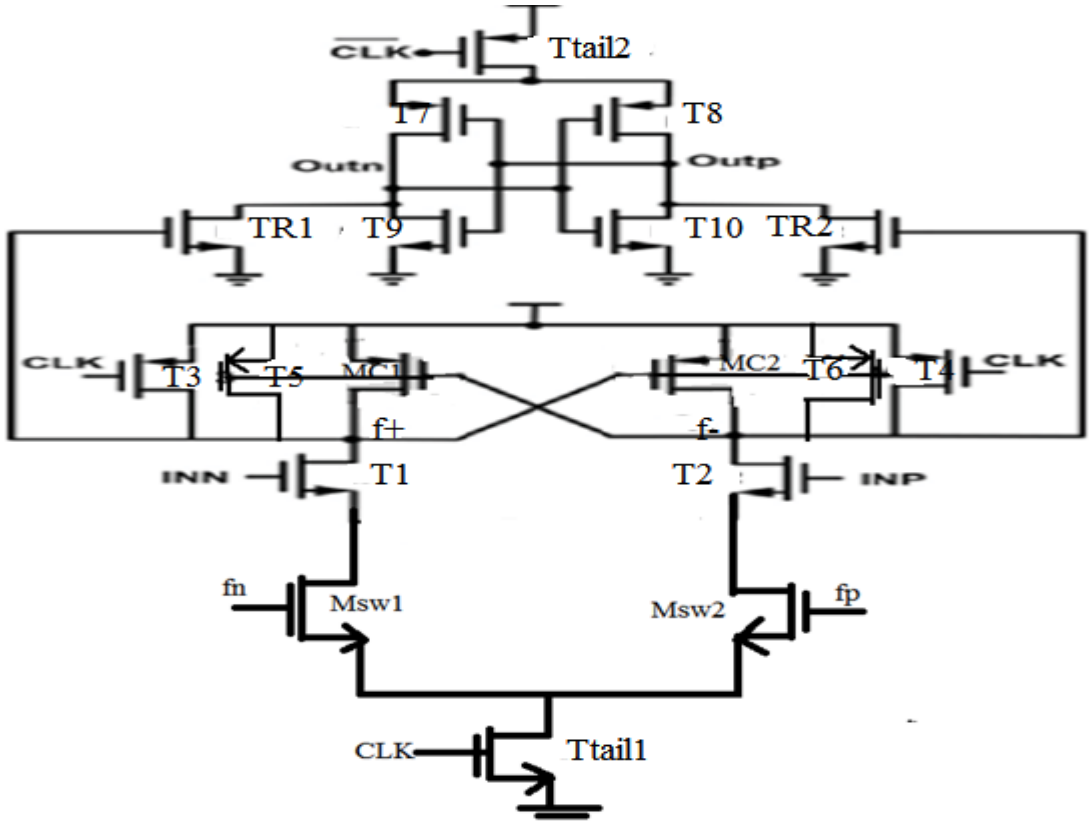


Figure 8: Modified proposed double tail comparator [3]

To mitigate power consumption problem in fig 7(a), two nMOS transistors (Msw1 and Msw2) are added just below T1 and T2 [see fig. 8]. When CLK=V_{DD} (i.e. evaluation phase), due to the fact that during the reset phase both f+ and f- nodes have been pre-charged to V_{DD}, Msw1 and Msw2 are closed and f+ and f- starts to decrease with different currents. As soon as the comparator senses that one of the node (f+/f-) is discharging faster, control transistors increases the voltage difference between the nodes. Assume the case: f+ is pulling to V_{DD} and f- is discharging to ground, the transistor switch in the charging path of f+ will be off (to prevent path from V_{DD} to ground) but the another transistor connected to f- will be on to allow the discharging of f- node to ground.

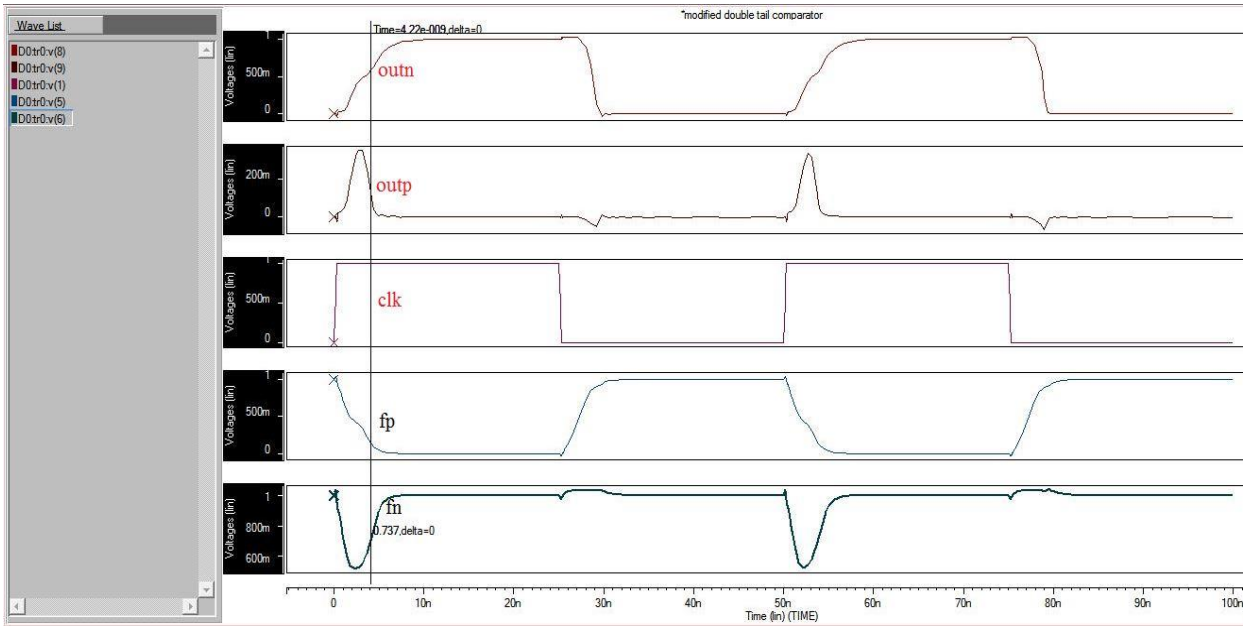
Chapter 4

Simulation Results

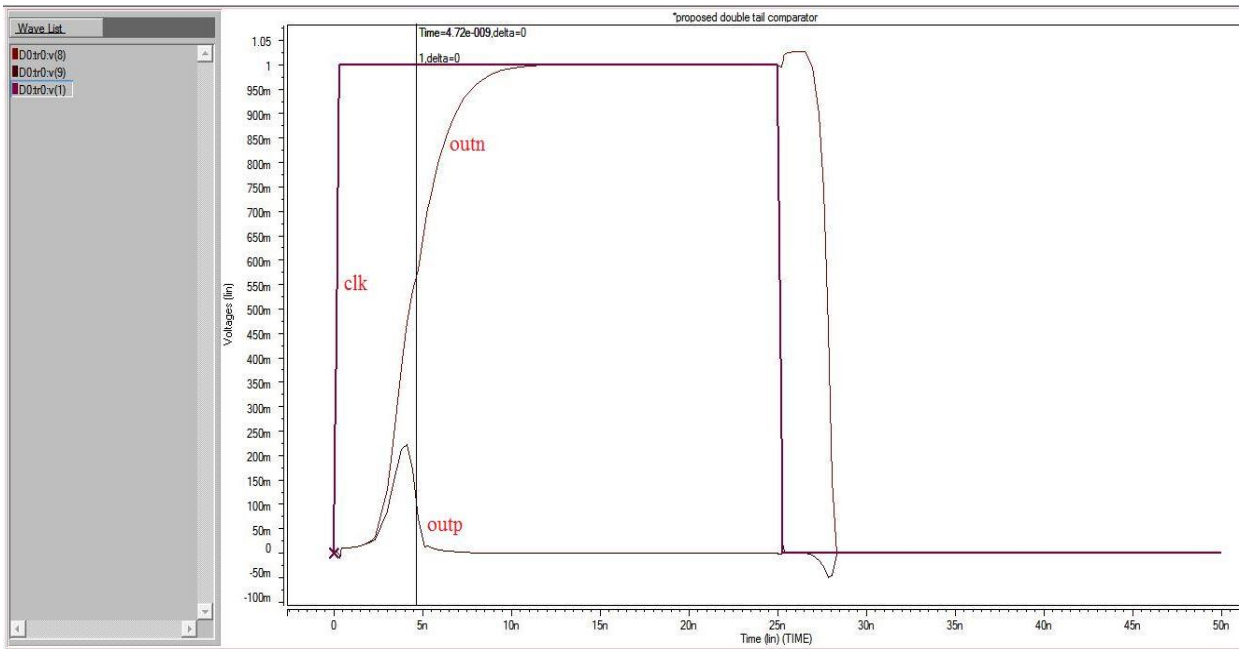
To compare the performance of proposed comparator with the single tail and double tail dynamic comparator, all circuits have been simulated in a 180nm CMOS technology for the same V_{DD}=1V and V_{cm}=0.7V.Performance of the proposed comparator is also compared for different values of input difference voltage(i.e. ΔVin) .With the increase in ΔVin delay of the comparator is reduced. All circuits are also simulated for 90nm and 45nm CMOS technology. Comparison of all comparator circuit in different technology is shown in table 1.In a given technology the delay and power delay product of modified proposed comparator is reduced significantly then single tail and double tail dynamic comparator.

Performance comparison table 1

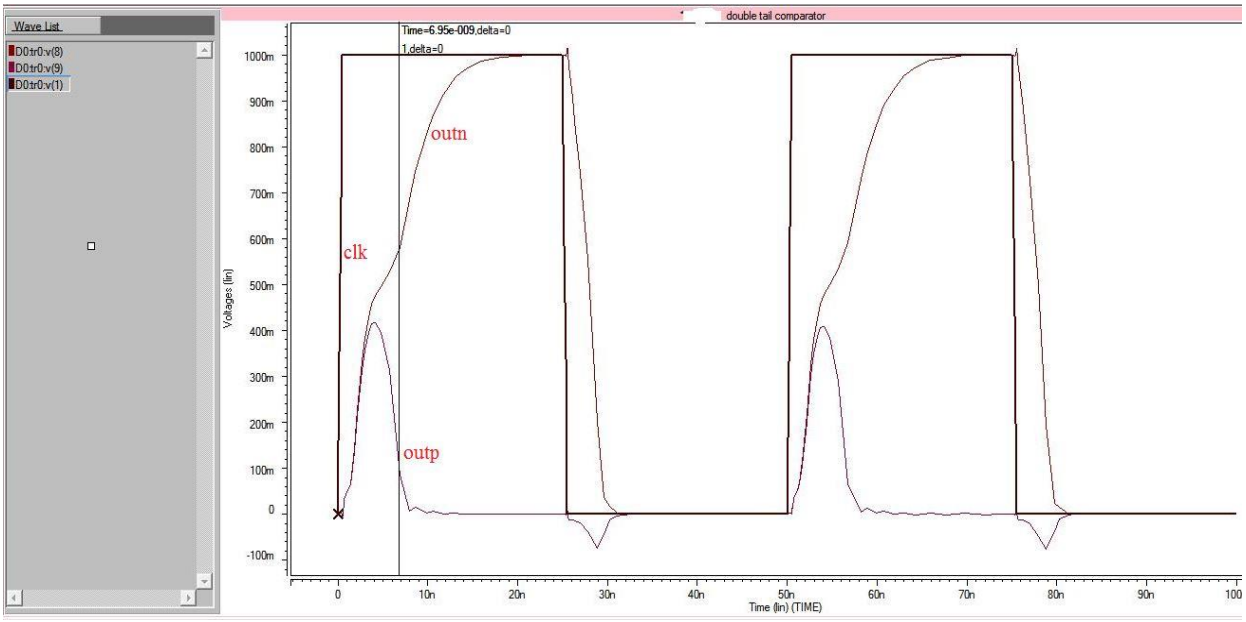
	Modified comparator			**Double tail dynamic comparator**			**Single tail dynamic comparator**		
Technology(nm)	180	90	45	180	90	45	180	90	45
Average power(μW)	5.1	2.14	0.7	3.8	1.97	0.6	3.41	1.4	0.41
Delay(ns)	4.15	0.408	0.204	6.95	0.484	0.33	12.9	0.873	0.47
Speed	240.9MHz	2.45GHz	4.9GHz	143.8MHz	2.06GHz	3.03GHz	77.5MHz	1.15GHz	2.13GHz
Power delay product (fJ)	21.1	0.87	0.143	26.4	0.95	0.192	43.9	1.21	0.197


Wave List
D0:tr0:v(8)
D0:tr0:v(9)
D0:tr0:v(1)
D0:tr0:v(5)
D0:tr0:v(6)
*modified double tail comparator
outn
outp
clk
fp
fn
Voltage: (lin)
Time (lin) (TIME)

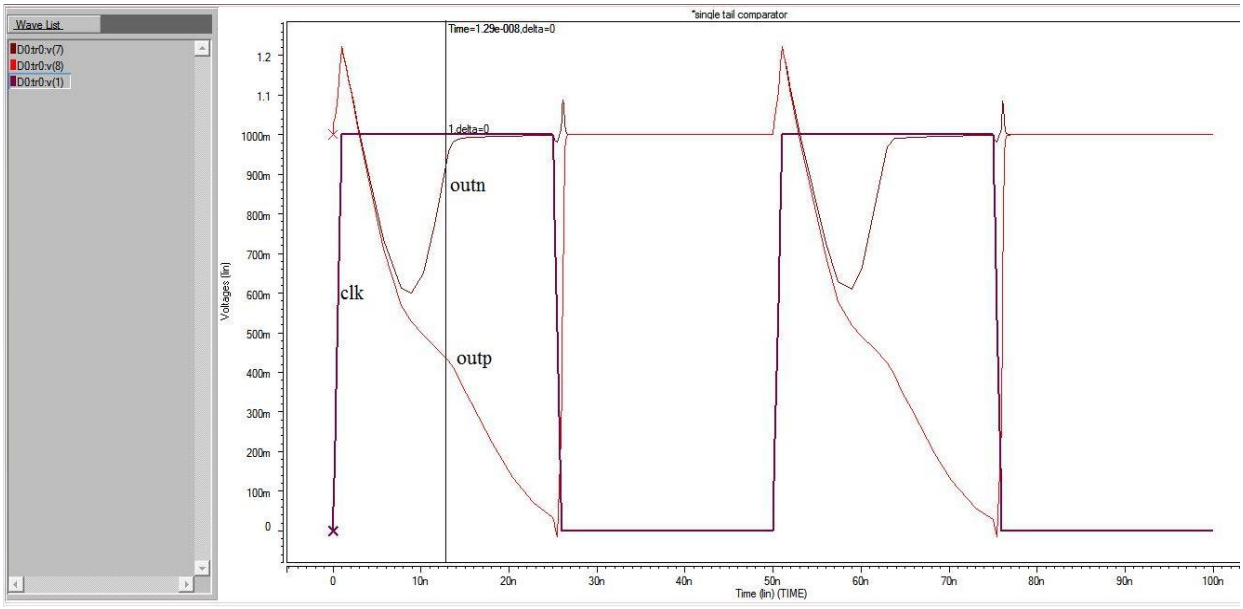
(a)


Wave List
D0:tr0:v(8)
D0:tr0:v(9)
D0:tr0:v(1)
*proposed double tail comparator
Time=4.72e-009,delta=0
outn
clk
outp
Voltage: (lin)
Time (lin) (TIME)

(b)

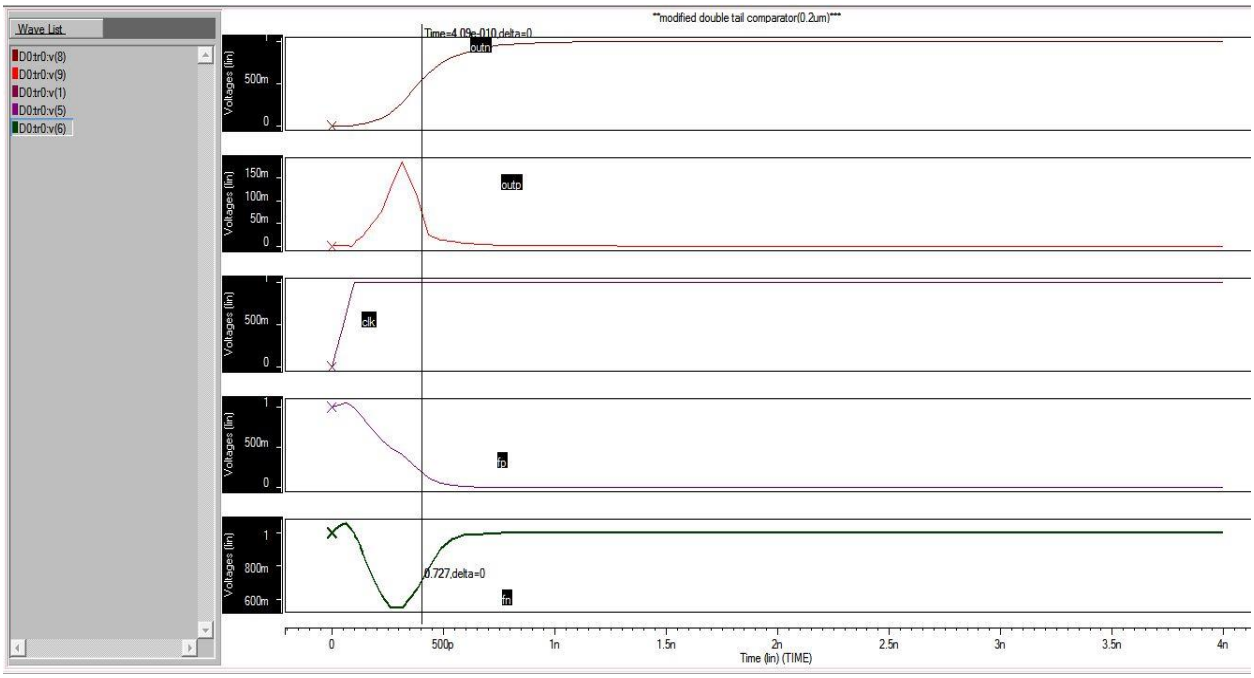


(c)

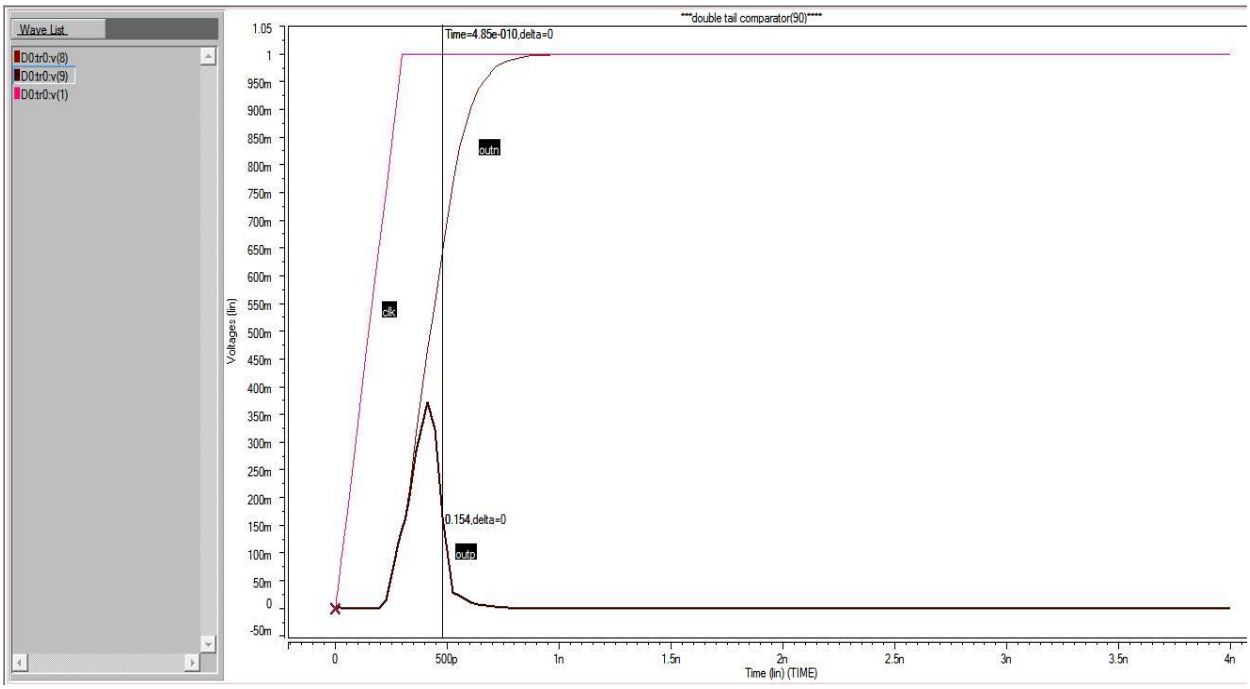


(d)

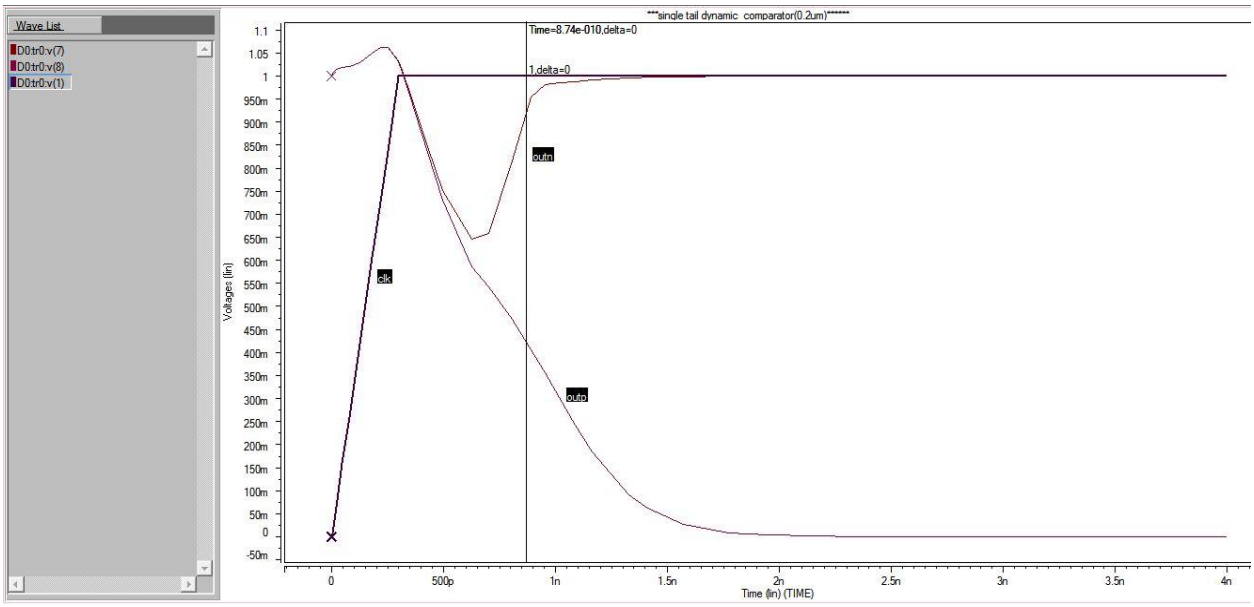
Figure 9: Transient simulation of comparators (180nm) for input voltage difference of ΔVin=10mv, Vcm=700mv and V_{DD}=1V (a)Modified comparator (b)proposed comparator (c)double tail dynamic comparator (d)single tail dynamic comparator


Wave List
D0:tr0:v(8)
D0:tr0:v(9)
D0:tr0:v(1)
D0:tr0:v(5)
D0:tr0:v(6)
modified double tail comparator(0.2um)*
Time=4.09e-010,delta=0
outn
outp
clk
in
0.727,delta=0
Voltages (lin)
Time (lin) (TIME)

(a)

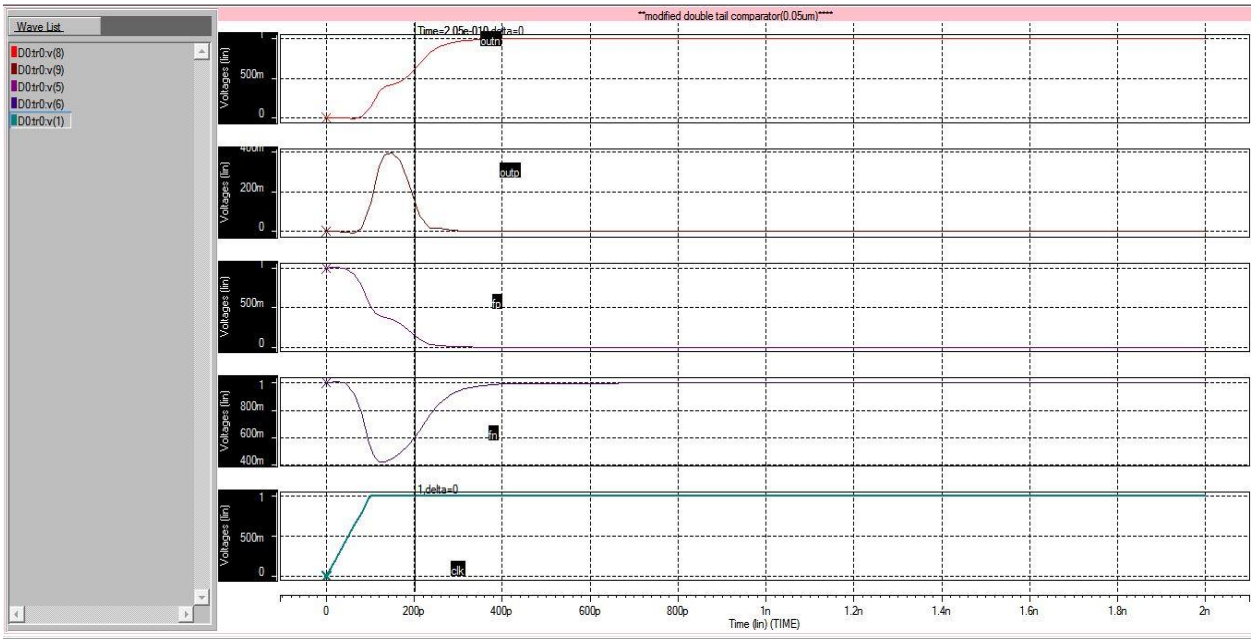

Wave List
D0:tr0:v(8)
D0:tr0:v(9)
D0:tr0:v(1)
double tail comparator(90)*
Time=4.85e-010,delta=0
outn
clk
0.154,delta=0
outp
Voltages (lin)
Time (lin) (TIME)

(b)

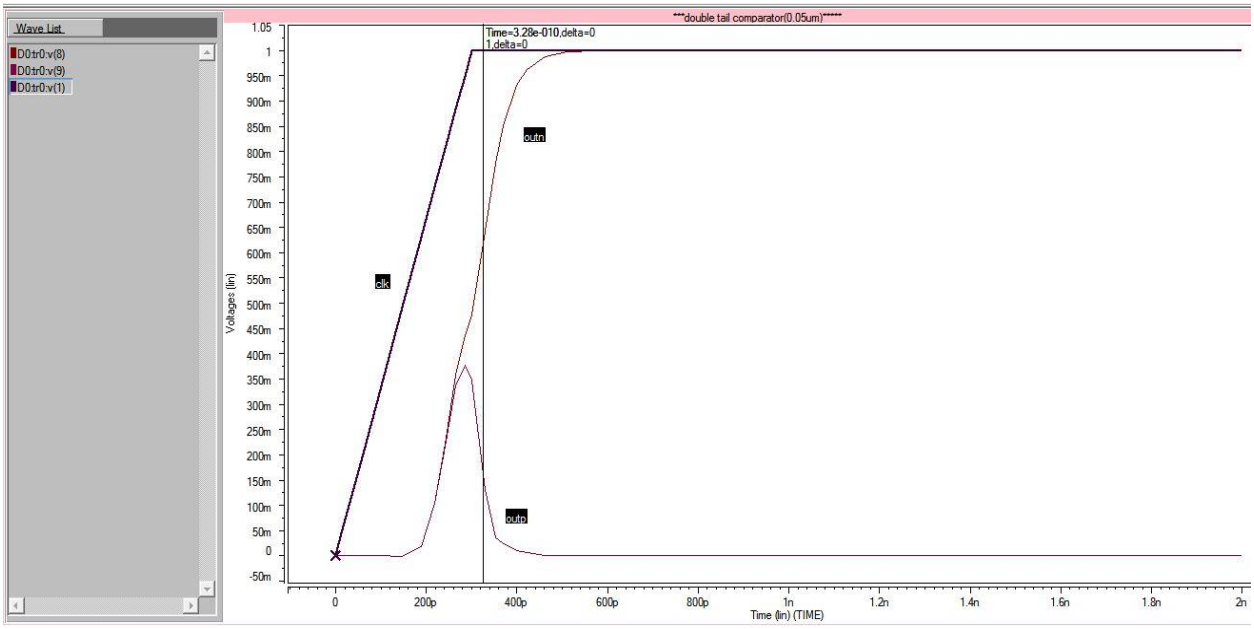


(c)

Figure 10: Transient simulation of comparators (90nm) for input voltage difference of ΔVin=10mv, V_{cm}=700mv and V_{DD}=1V (a) Modified comparator (b) double tail dynamic comparator (c) single tail dynamic comparator



(a)



(b)

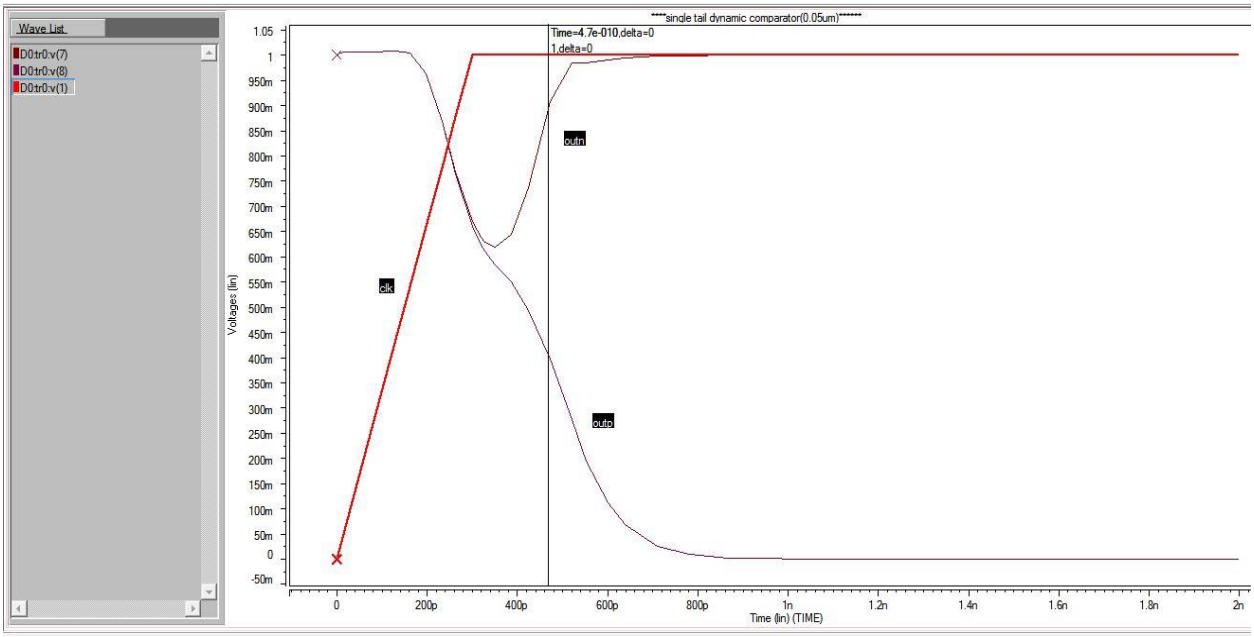


Figure 11: Transient simulation of comparators (45nm) for input voltage difference of ΔVin=10mv, Vcm=700mv and V_{DD}=1V (a) Modified comparator (b) double tail dynamic comparator (c) single tail dynamic comparator

The delay, power and power delay product of conventional single tail dynamic comparator, double tail dynamic comparator and modified comparator is shown in Figure 12, Figure13 and Figure 14 respectively at 180nm, 90nm and 45nm technology

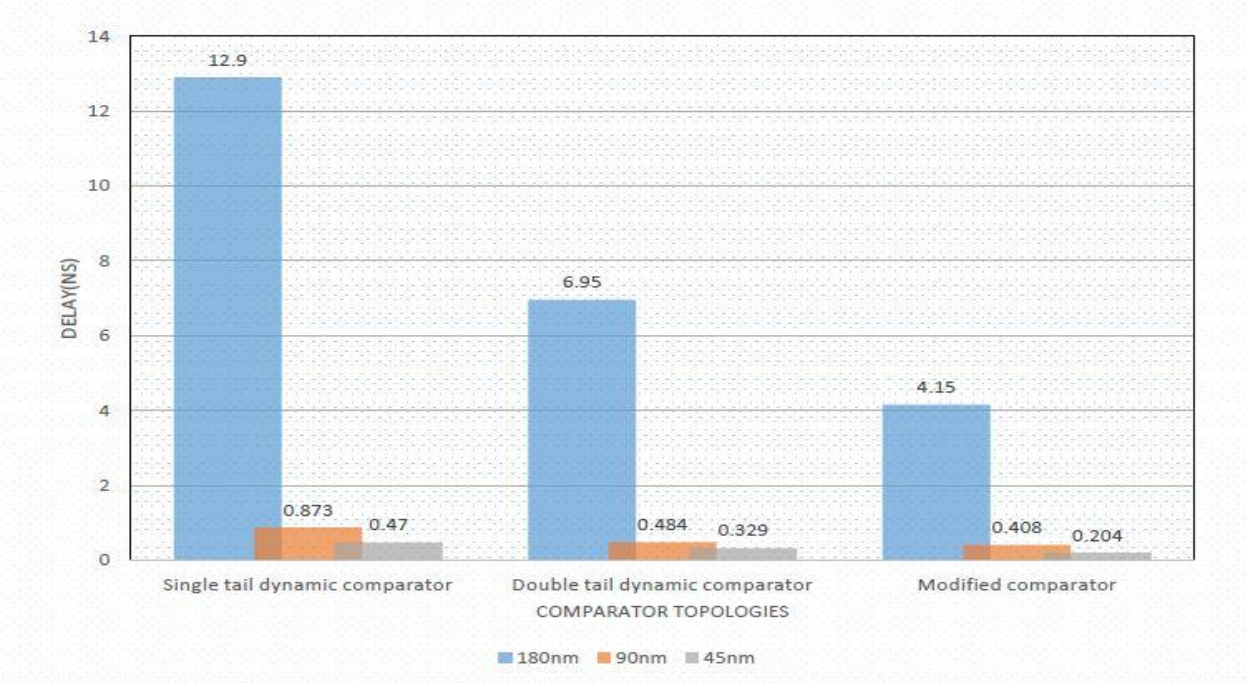


Figure 12: Delay of comparator topologies

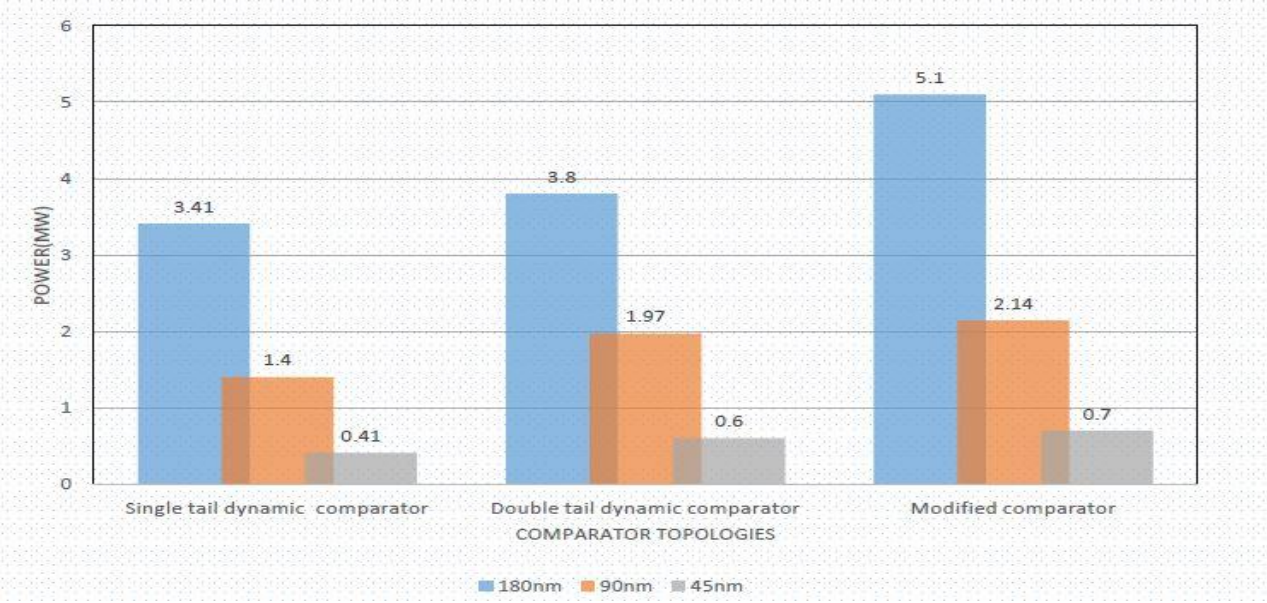


Figure 13: Power of comparator topologies

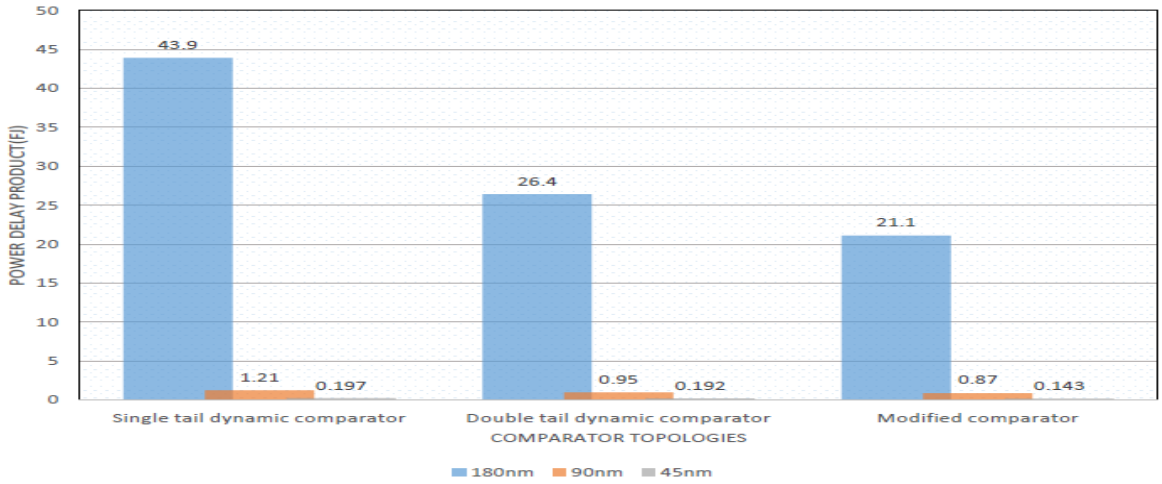


Figure 14: power delay product of comparator topologies

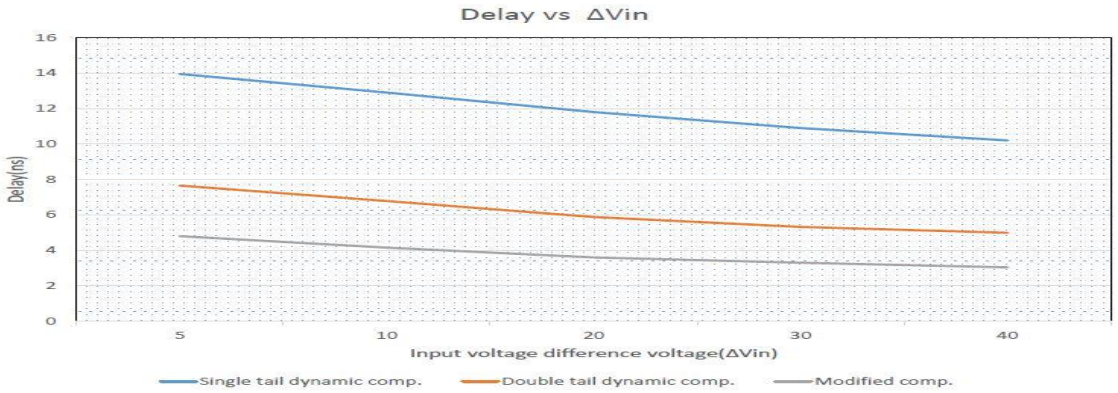


Figure 15: Variation of delay with input voltage difference (ΔVin)

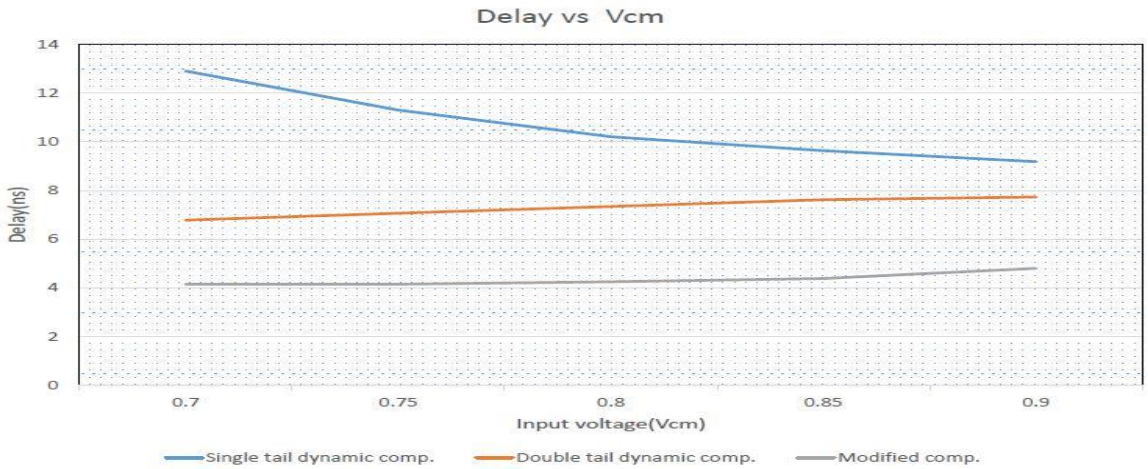


Figure 16: Variation of delay with input common mode voltage (V_{cm})

Chapter 5

Conclusion

A comprehensive delay analysis of comparator is analyzed. The modified proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators. The power delay product of proposed comparator in 180nm technology is reduced by 20% than the double tail dynamic comparator. The average power of proposed comparator at 45nm technology is reduced by 67.28% then 90nm technology due to the decrease in channel length of the transistors. The delay of proposed comparator is reduced by 40.28 % when compared to the double dynamic tail comparator in 180nm technology. Thus, the proposed comparator is energy efficient when compared to other topologies at 45nm, 90nm and 180nm technologies.

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Appendix A

```
* Long channel models from CMOS Circuit Design, Layout, and Simulation,
* Level=3 models VDD=5V, see CMOSedu.com
*
 .MODEL N_1u NMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.5
+ PHI    = 0.7            VTO    = 0.8           DELTA  = 3.0
+ UO     = 650            ETA    = 3.0E-6        THETA  = 0.1
+ KP     = 120E-6         VMAX   = 1E5           KAPPA  = 0.3
+ RSH    = 0              NFS    = 1E12          TPG    = 1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
.MODEL P_1u PMOS LEVEL  = 3
+ TOX    = 200E-10        NSUB   = 1E17          GAMMA  = 0.6
+ PHI    = 0.7            VTO    = -0.9          DELTA  = 0.1
+ UO     = 250            ETA    = 0             THETA  = 0.1
+ KP     = 40E-6          VMAX   = 5E4           KAPPA  = 1
+ RSH    = 0              NFS    = 1E12          TPG    = -1
+ XJ     = 500E-9         LD     = 100E-9
+ CGDO   = 200E-12        CGSO   = 200E-12       CGBO   = 1E-10
+ CJ     = 400E-6         PB     = 1             MJ     = 0.5
+ CJSW   = 300E-12        MJSW   = 0.5
*
*
* Short channel models from CMOS Circuit Design, Layout, and Simulation,
* 50nm BSIM4 models VDD=1V, see CMOSedu.com
*
.model  NMOS  nmos  level = 54
+binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2          igcmod  = 1          igbmod  = 1          geomod  = 0
+diomod  = 1          rdsmod  = 0          rbodymod= 1          rgatemod= 1
+permod  = 1          acnqsmod= 0          trnqsmod= 0
+tnom    = 27         toxe    = 1.4e-009   toxp    = 7e-010     toxm    = 1.4e-009
+epsrox  = 3.9        wint    = 5e-009     lint    = 1.2e-008
+ll      = 0          wl      = 0          lln     = 1          wln     = 1
+lw      = 0          ww      = 0          lwn     = 1          wwn     = 1
+lwl     = 0          wwl     = 0          xpart   = 0          toxref  = 1.4e-009
+vth0    = 0.22       k1      = 0.35       k2      = 0.05       k3      = 0
+k3b     = 0          w0      = 2.5e-006   dvt0    = 2.8        dvt1    = 0.52
+dvt2    = -0.032     dvt0w   = 0          dvt1w   = 0          dvt2w   = 0
+dsub    = 2          minv    = 0.05       voffl   = 0          dvtp0   = 1e-007
+dvtp1   = 0.05       lpe0    = 5.75e-008  lpeb    = 2.3e-010   xj      = 2e-008
+ngate   = 5e+020     ndep    = 2.8e+018   nsd     = 1e+020     phin    = 0
+cdsc    = 0.0002     cdscb   = 0          cdscd   = 0          cit     = 0
+voff    = -0.15      nfactor = 1.2        eta0    = 0.15       etab    = 0
+vfb     = -0.55      u0      = 0.032      ua      = 1.6e-010   ub      = 1.1e-017
+uc      = -3e-011    vsat    = 1.1e+005   a0      = 2          ags     = 1e-020
+a1      = 0          a2      = 1          b0      = -1e-020    b1      = 0
+keta    = 0.04       dwg     = 0          dwb     = 0          pclm    = 0.18
+pdiblc1 = 0.028      pdiblc2 = 0.022      pdiblcb = -0.005     drout   = 0.45
+pvag    = 1e-020     delta   = 0.01       pscbe1  = 8.14e+008  pscbe2  = 1e-007
```

```
+fprout  = 0.2          pdits   = 0.2          pditsd  = 0.23         pditsl  = 2.3e+006
+rsh     = 3            rdsw    = 150          rsw     = 150          rdw     = 150
+rdswmin = 0            rdwmin  = 0            rswmin  = 0            prwg    = 0
+prwb    = 6.8e-011     wr      = 1            alpha0  = 0.074        alpha1  = 0.005
+beta0   = 30           agidl   = 0.0002       bgidl   = 2.1e+009     cgidl   = 0.0002
+egidl   = 0.8
+aigbacc = 0.012        bigbacc = 0.0028       cigbacc = 0.002
+nigbacc = 1            aigbinv = 0.014        bigbinv = 0.004        cigbinv = 0.004
+eigbinv = 1.1          nigbinv = 3            aigc    = 0.017        bigc    = 0.0028
+cigc    = 0.002        aigsd   = 0.017        bigsd   = 0.0028       cigsd   = 0.002
+nigc    = 1            poxedge = 1            pigcd   = 1            ntox    = 1
+xrcrg1  = 12           xrcrg2  = 5
+cgso    = 6.238e-010   cgdo    = 6.238e-010   cgbo    = 2.56e-011    cgdl    = 2.495e-10
+cgsl    = 2.495e-10    ckappas = 0.02         ckappad = 0.02         acde    = 1
+moin    = 15           noff    = 0.9          voffcv  = 0.02
+kt1     = -0.21        kt1l    = 0.0          kt2     = -0.042       ute     = -1.5
+ua1     = 1e-009       ub1     = -3.5e-019    uc1     = 0            prt     = 0
+at      = 53000
+fnoimod = 1            tnoimod = 0
+jss     = 0.0001       jsws    = 1e-011       jswgs   = 1e-010       njs     = 1
+ijthsfwd= 0.01         ijthsrev= 0.001        bvs     = 10           xjbvs   = 1
+jsd     = 0.0001       jswd    = 1e-011       jswgd   = 1e-010       njd     = 1
+ijthdfwd= 0.01         ijthdrev= 0.001        bvd     = 10           xjbvd   = 1
+pbs     = 1            cjs     = 0.0005       mjs     = 0.5          pbsws   = 1
+cjsws   = 5e-010       mjsws   = 0.33         pbswgs  = 1            cjswgs  = 5e-010
+mjswgs  = 0.33         pbd     = 1            cjd     = 0.0005       mjd     = 0.5
+pbswd   = 1            cjswd   = 5e-010       mjswd   = 0.33         pbswgd  = 1
+cjswgd  = 5e-010       mjswgd  = 0.33         tpb     = 0.005        tcj     = 0.001
+tpbsw   = 0.005        tcjsw   = 0.001        tpbswg  = 0.005        tcjswg  = 0.001
+xtis    = 3            xtid    = 3
+dmcg    = 0e-006       dmci    = 0e-006       dmdg    = 0e-006       dmcgt   = 0e-007
+dwj     = 0e-008       xgw     = 0e-007       xgl     = 0e-008
+rshg    = 0.4          gbmin   = 1e-010       rbpb    = 5            rbpd    = 15
+rbps    = 15           rbdb    = 15           rbsb    = 15           ngcon   = 1
*
.model  PMOS  pmos  level = 54

+binunit = 1            paramchk= 1            mobmod  = 0
+capmod  = 2            igcmod  = 1            igbmod  = 1            geomod  = 0
+diomod  = 1            rdsmod  = 0            rbodymod= 1            rgatemod= 1
+permod  = 1            acnqsmod= 0            trnqsmod= 0
+tnom    = 27           toxe    = 1.4e-009     toxp    = 7e-010       toxm    = 1.4e-009
+epsrox  = 3.9          wint    = 5e-009       lint    = 1.2e-008
+ll      = 0            wl      = 0            lln     = 1            wln     = 1
+lw      = 0            ww      = 0            lwn     = 1            wwn     = 1
+lwl     = 0            wwl     = 0            xpart   = 0            toxref  = 1.4e-009
+vth0    = -0.22        k1      = 0.39         k2      = 0.05         k3      = 0
+k3b     = 0            w0      = 2.5e-006     dvt0    = 3.9          dvt1    = 0.635
+dvt2    = -0.032       dvt0w   = 0            dvt1w   = 0            dvt2w   = 0
+dsub    = 0.7          minv    = 0.05         voffl   = 0            dvtp0   = 0.5e-008
+dvtp1   = 0.05         lpe0    = 5.75e-008    lpeb    = 2.3e-010     xj      = 2e-008
+ngate   = 5e+020       ndep    = 2.8e+018     nsd     = 1e+020       phin    = 0
+cdsc    = 0.000258     cdscb   = 0            cdscd   = 6.1e-008     cit     = 0
+voff    = -0.15        nfactor = 2            eta0    = 0.15         etab    = 0
+vfb     = 0.55         u0      = 0.0095       ua      = 1.6e-009     ub      = 8e-018
+uc      = 4.6e-013     vsat    = 90000        a0      = 1.2          ags     = 1e-020
+a1      = 0            a2      = 1            b0      = -1e-020      b1      = 0
+keta    = -0.047       dwg     = 0            dwb     = 0            pclm    = 0.55
+pdiblc1 = 0.03         pdiblc2 = 0.0055       pdiblcb = 3.4e-008     drout   = 0.56
+pvag    = 1e-020       delta   = 0.014        pscbe1  = 8.14e+008    pscbe2  = 9.58e-007
+fprout  = 0.2          pdits   = 0.2          pditsd  = 0.23         pditsl  = 2.3e+006
```

+rsh = 3 rdsw = 250 rsw = 160 rdw = 160
+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 3.22e-008
+prwb = 6.8e-011 wr = 1 alpha0 = 0.074 alpha1 = 0.005
+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002
+egidl = 0.8
+aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
+eigbinv = 1.1 nigbinv = 3 aigc = 0.69 bigc = 0.0012
+cigc = 0.0008 aigsd = 0.0087 bigsd = 0.0012 cigsd = 0.0008
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1
+xrcrg1 = 12 xrcrg2 = 5
+cgso = 7.43e-010 cgdo = 7.43e-010 cgbo = 2.56e-011 cgdl = 1e-014
+cgsl = 1e-014 ckappas = 0.5 ckappad = 0.5 acde = 1
+moin = 15 noff = 0.9 voffcv = 0.02
+kt1 = -0.19 kt1l = 0 kt2 = -0.052 ute = -1.5
+ua1 = -1e-009 ub1 = 2e-018 uc1 = 0 prt = 0
+at = 33000
+fnoimod = 1 tnoimod = 0
+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1
+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 5e-010
+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001
+xtis = 3 xtid = 3
+dmcg = 0e-006 dmci = 0e-006 dmdg = 0e-006 dmcgt = 0e-007
+dwj = 0e-008 xgw = 0e-007 xgl = 0e-008
+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15
+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

**** TSMC 180nm CMOS models ****
.MODEL NMOS NMOS (LEVEL = 49

+VERSION = 3.1 TNOM = 27 TOX = 4E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.364506
+K1 = 0.5791992 K2 = 3.521434E-3 K3 = 3.206013E-3
+K3B = 1.7518342 W0 = 1E-7 NLX = 1.745374E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.3115714 DVT1 = 0.4129209 DVT2 = 0.024362
+U0 = 264.0644125 UA = -1.460442E-9 UB = 2.481296E-18
+UC = 7.327293E-11 VSAT = 1.02353E5 A0 = 2
+AGS = 0.4587051 B0 = 7.565193E-8 B1 = 1.513445E-6
+KETA = -0.0145632 A1 = 0 A 2 = 0.9036502
+RDSW = 105 PRWG = 0.4562016 PRWB = -0.2
+WR = 1 WINT = 1.939451E-9 LINT = 1.362953E-8
+XL = 0 XW = -1E-8 DWG = -2.857622E-9
+DWB = 6.278785E-9 VOFF = -0.0941712 NFACTOR = 2.3749925
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 3.186986E-3 ETAB = 9.310602E-6
+DSUB = 0.0208131 PCLM = 0.7619812 PDIBLC1 = 0.1604459
+PDIBLC2 = 2.449706E-3 PDIBLCB = -0.1 DROUT = 0.7135573
+PSCBE1 = 4.283914E10 PSCBE2 = 2.467637E-9 PVAG = 0.0774246
+DELTA = 0.01 RSH = 6.8 MOBMOD = 1

```
+PRT     = 0                 UTE     = -1.5              KT1     = -0.11
+KT1L    = 0                 KT2     = 0.022             UA1     = 4.31E-9
+UB1     = -7.61E-18         UC1     = -5.6E-11          AT      = 3.3E4
+WL      = 0                 WLN     = 1                 WW      = 0
+WWN     = 1                 WWL     = 0                 LL      = 0
+LLN     = 1                 LW      = 0                 LWN     = 1
+LWL     = 0                 CAPMOD  = 2                 XPART   = 0.5
+CGDO    = 8.6E-10           CGSO    = 8.6E-10           CGBO    = 1E-12
+CJ      = 9.523381E-4       PB      = 0.8               MJ      = 0.3789075
+CJSW    = 2.620943E-10      PBSW    = 0.8               MJSW    = 0.1406578
+CJSWG   = 3.3E-10           PBSWG   = 0.8               MJSWG   = 0.1406578
+CF      = 0                 PVTH0   = -1.452607E-3      PRDSW   = -0.9998826
+PK2     = 4.931039E-4       WKETA   = 2.110945E-3       LKETA   = -5.82039E-3
+PU0     = 4.5744857         PUA     = -4.96443E-12      PUB     = 0
+PVSAT   = 1.196096E3        PETA0   = 1.003159E-4       PKETA   = 2.170319E-3    )
*
.MODEL PMOS PMOS (                  LEVEL   = 49

+VERSION = 3.1              TNOM    = 27                TOX     = 4E-9
+XJ      = 1E-7             NCH     = 4.1589E17         VTH0    = -0.3830653
+K1      = 0.5526551        K2      = 0.0320636         K3      = 0
+K3B     = 7.3466224        W0      = 1E-6              NLX     = 1.36025E-7
+DVT0W   = 0                DVT1W   = 0                 DVT2W   = 0
+DVT0    = 0.5922956        DVT1    = 0.2373154         DVT2    = 0.1
+U0      = 115.7940036      UA      = 1.555236E-9       UB      = 1.35139E-21
+UC      = -1E-10           VSAT    = 2E5               A0      = 1.7679712
+AGS     = 0.3739476        B0      = 4.133992E-7       B1      = 1.434059E-6
+KETA    = 0.0158442        A1      = 0.5080834         A2      = 0.3
+RDSW    = 236.9205988      PRWG    = 0.5               PRWB    = 0.3466813
+WR      = 1                WINT    = 0                 LINT    = 2.427225E-8
+XL      = 0                XW      = -1E-8             DWG     = -2.213783E-8
+DWB     = 4.021425E-10     VOFF    = -0.0954776        NFACTOR = 2
+CIT     = 0                CDSC    = 2.4E-4            CDSCD   = 0
+CDSCB   = 0                ETA0    = 0.1116222         ETAB    = -0.055645
+DSUB    = 1.333722         PCLM    = 2.4627079         PDIBLC1 = 9.70124E-4
+PDIBLC2 = 0.0208974        PDIBLCB = -9.536244E-4      DROUT   = 1E-3
+PSCBE1  = 3.195565E9       PSCBE2  = 9.248005E-10      PVAG    = 15
+DELTA   = 0.01             RSH     = 7.8               MOBMOD  = 1
+PRT     = 0                UTE     = -1.5              KT1     = -0.11
+KT1L    = 0                KT2     = 0.022             UA1     = 4.31E-9
+UB1     = -7.61E-18        UC1     = -5.6E-11          AT      = 3.3E4
+WL      = 0                WLN     = 1                 WW      = 0
+WWN     = 1                WWL     = 0                 LL      = 0
+LLN     = 1                LW      = 0                 LWN     = 1
+LWL     = 0                CAPMOD  = 2                 XPART   = 0.5
+CGDO    = 6.4E-10          CGSO    = 6.4E-10           CGBO    = 1E-12
+CJ      = 1.106243E-3      PB      = 0.8376666         MJ      = 0.4113568
+CJSW    = 2.212431E-10     PBSW    = 0.8227331         MJSW    = 0.338019
+CJSWG   = 4.22E-10         PBSWG   = 0.8227331         MJSWG   = 0.338019
+CF      = 0                PVTH0   = 4.347904E-3       PRDSW   = 15.650799
+PK2     = 3.698084E-3      WKETA   = 0.0258501         LKETA   = -3.187672E-3
+PU0     = -2.4807326       PUA     = -9.27991E-11      PUB     = 1E-21
+PVSAT   = -50              PETA0   = 9.968409E-5       PKETA   = -6.725059E-4    )
*
```

Appendix B

HSPICE Netlist Files for Simulated Comparator Circuits**:**

1. Single tail dynamic comparator

A. **********Single tail dynamic comparator(180nm)*******

**********Include model file**********

.include 'cmos_180_model.txt'

**********netlist**********

mt 2 1 0 0 NMOS w=0.3u l=0.5u

m1 5 3 2 0 NMOS w=0.78u l=0.5u

m2 6 4 2 0 NMOS w=0.78u l=0.5u

m3 8 7 5 0 NMOS w=5u l=0.5u

m4 7 8 6 0 NMOS w=5u l=0.5u

m5 8 7 9 9 PMOS w=15u l=0.5u

m6 7 8 9 9 PMOS w=15u l=0.5u

m7 8 1 9 9 PMOS w=15u l=0.5u

m8 7 1 9 9 PMOS w=15u l=0.5u

**********power supply**********

VDD 9 0 dc 1

**********input signal**********

vinp 3 0 pulse(695m 705m 0 1n 1n 24n 50n)

vinn 4 0 pulse(705m 695m 0 1n 1n 24n 50n)

vclk 1 0 0.5 pulse(0 1 0 1n 1n 24n 50n)

.cl 7 0 7f

.cl1 8 0 7f

**********analysis**********

.tran 5p 100n

.meas tran avgpower AVG power from =0.01ns to =50ns

.op

.option post

.end

**********END**********

B.******************Single tail dynamic comparator(90nm)************

**********include model file**********

```
.include 'cnmos_90_model.txt'
.include 'cpmos_90_model.txt'
```

**********netlist**********

```
mt   2 1 0 0    NMOS    w=0.32u    l=0.2u
m1   5 3 2 0    NMOS    w=0.6u     l=0.2u
m2   6 4 2 0    NMOS    w=0.6u     l=0.2u
m3   8 7 5 0    NMOS    w=2u       l=0.2u
m4   7 8 6 0    NMOS    w=2u       l=0.2u
m5   8 7 9 9    PMOS    w=5.5u     l=0.2u
m6   7 8 9 9    PMOS    w=5.5u     l=0.2u
m7   8 1 9 9    PMOS    w=5.5u     l=0.2u
m8   7 1 9 9    PMOS    w=5.5u     l=0.2u
```

**********supply voltage**********

```
VDD  9 0 dc 1
```

**********input signal**********

```
vinp 3 0  pulse(695m 705m 0 0.3n 0.3n 19.7n 40n)
vinn 4 0  pulse(705m 695m 0 0.3n 0.3n 19.7n 40n)
vclk 1 0 0.5 pulse(0 1 0 0.3n 0.3n 19.7n 40n)
.cl 7 0 7f
.cl1 8 0 7f
```

**********analysis**********

```
.tran 5p 4n
.meas tran avgpower AVG power from =0.01ns to =40ns
.op
.option post
.end
```

**********END**********

C. ********Single tail dynamic comparator(45nm)********

**********include model file**********

```
.include 'cmosedu_models.txt'
```

**********netlist**********

```
Mt  2 1 0 0    NMOS    w=0.22u    l=0.05u
```

```
m1  5 3 2 0    NMOS    w=0.19u    l=0.05u
m2  6 4 2 0    NMOS    w=0.19u    l=0.05u
m3   8 7 5 0     NMOS      w=0.5u     l=0.05u
m4  7 8 6 0      NMOS      w=0.5u     l=0.05u
m5  8 7 9 9      PMOS      w=1.1u     l=0.05u
m6  7 8 9 9      PMOS      w=1.1u     l=0.05u
m7  8 1 9 9      PMOS      w=1.1u     l=0.05u
m8  7 1 9 9      PMOS      w=1.1u     l=0.05u

**********supply voltage**********

VDD 9 0 dc 1
**********input signal**********

vinp 3 0  pulse(695m 705m 0 0.3n 0.3n 24.7n 50n)
vinn 4 0  pulse(705m 695m 0 0.3n 0.3n 24.7n 50n)

**********clock signal**********
vclk 1 0 0.5 pulse(0 1 0 0.3n 0.3n 24.7n 50n)

.cl 7 0 7f
.cl1 8 0 7f
**********analysis**********
.tran 5p 2n
.meas tran avgpower AVG power from =0.01ns to =50ns
.op
.option post
.end
**********END**********
```

2.Double tail dynamic comparator

A. ********* double tail dynamic comparator(180nm)**********

```
**********include model file**********
.include 'cmos_180_model.txt'
**********netlist**********
mt1    2 1 0 0      NMOS    w=0.15u    l=0.5u
m1     5 3 2 0      NMOS    w=0.39u    l=0.5u
m2     6 4 2 0      NMOS    w=0.39u    l=0.5u
m3     5 1 7 7      PMOS     w=2u        l=0.5u
m4     6 1 7 7      PMOS     w=2u        l=0.5u
mr1    8 5 0 0      NMOS    w=0.4u     l=0.5u
mr2    9 6 0 0      NMOS    w=0.4u     l=0.5u
m7     8 9 10 7    PMOS     w=15u       l=0.5u
m8     9 8 10 7    PMOS     w=15u       l=0.5u
```

```
m9    8 9 0 0     NMOS   w=5u      l=0.5u
m10   9 8 0 0     NMOS   w=5u      l=0.5u
mt2   10 11 7 7   PMOS   w=0.9u    l=0.5u
M11   11 1 0 0    NMOS   w=5u      l=0.5u
M12   11 1 7 7    PMOS   w=15u     l=0.5u

**********supply voltage**********
VDD 7 0 dc 1
**********input signal**********
vinn 3 0 pulse(695m 705m 0 0.5n 0.5n 24.5n 50n)
vinp 4 0 pulse(705m 695m 0 0.5n 0.5n 24.5n 50n)
vclk 1 0 0.5 pulse(0 1 0 0.5n 0.5n 24.5n 50n)
.cln   5 0 7f
.clp   6 0 7f
.clop  8 0 7f
.clon  9 0 7f
**********analysis**********
.meas tran avgpower AVG power from=0.01n to 50n
.tran 10p 50n
.op
.option post
.end
**********END**********
```

B.**********Double tail comparator(90nm)**********

```
**********include model file********
.include 'cnmos_90_model.txt'
.include 'cpmos_90_model.txt'
**********netlist**********
mt1    2 1 0 0     NMOS    w=0.14u   l=0.2u
m1     5 3 2 0     NMOS    w=0.27u   l=0.2u
m2     6 4 2 0     NMOS    w=0.27u   l=0.2u
m3     5 1 7 7     PMOS    w=0.5u    l=0.2u
m4     6 1 7 7     PMOS    w=0.5u    l=0.2u
mr1    8 5 0 0     NMOS    w=0.5u    l=0.2u
mr2    9 6 0 0     NMOS    w=0.5u    l=0.2u
m7     8 9 10 7    PMOS    w=5.5u    l=0.2u
m8     9 8 10 7    PMOS    w=5.5u    l=0.2u
m9     8 9 0 0     NMOS    w=2u      l=0.2u
m10    9 8 0 0     NMOS    w=2u      l=0.2u
mt2    10 11 7 7   PMOS    w=2u      l=0.2u
```

```
M11   11 1 0 0     NMOS     w=2u          l=0.2u
M12   11 1 7 7     PMOS     w=5.5u        l=0.2u
```

```
**********supply voltage**********
VDD 7 0 dc 1
**********input signal**********
vinn 3 0 pulse(695m 705m 0 0.3n 0.3n 19.7n 40n)
vinp 4 0 pulse(705m 695m 0 0.3n 0.3n 19.7n 40n)
**********clock signal**********
vclk 1 0 0.5 pulse(0 1 0 0.3n 0.3n 19.7n 40n)
.clp 8 0 7f
.clo 9 0 7f
.cln 5 0 7f
.clp 6 0 7f
**********analysis**********
.meas tran avgpower AVG power from=0.1n to 40n
.tran 10p 4n
.op
.option post
.end
**********END**********
```

B.**********double tail dynamic comparator (45nm) **********

**********include model file**********

```
.include 'cmosedu_models.txt'
**********netlist**********
mt1    2 1 0 0      NMOS    w=0.0925u    l=0.05u
m1     5 3 2 0      NMOS     w=0.105u    l=0.05u
m2     6 4 2 0      NMOS     w=0.105u    l=0.05u
m3     5 1 7 7      PMOS      w=0.2u      l=0.05u
m4     6 1 7 7      PMOS      w=0.2u      l=0.05u
mr1    8 5 0 0      NMOS      w=0.2u      l=0.05u
mr2    9 6 0 0      NMOS      w=0.2u      l=0.05u
m7     8 9 10 7     PMOS      w=1.1u      l=0.05u
m8     9 8 10 7     PMOS      w=1.1u      l=0.05u
m9     8 9 0 0      NMOS      w=0.5u      l=0.05u
m10    9 8 0 0      NMOS      w=0.5u      l=0.05u
mt2    10 11 7 7    PMOS     w=0.524u     l=0.05u
M11   11 1 0 0      NMOS      w=0.5u      l=0.05u
M12  11 1 7 7       PMOS      w=1.1u      l=0.05u
```

```
**********supply voltage**********
VDD 7 0 dc 1
**********input signal **********
vinn 3 0 pulse(695m 705m 0 0.3n 0.3n 24.7n 50n)
vinp 4 0 pulse(705m 695m 0 0.3n 0.3n 24.7n 50n)
vclk 1 0 0.5 pulse(0 1 0 0.3n 0.3n 24.7n 50n)
.clp 8 0 7f
.clo 9 0 7f
.cln 5 0 7f
.clp 6 0 7f
**********analysis**********
.meas tran avgpower AVG power from=0.01n to 50n
.tran 10p 2n
.op
.option post
.end
**********END**********
```

3. Proposed comparator

A.**********proposed double tail comparator(180nm)**********

**********include model file**********

```
.include 'cmos_180_model.txt'
**********netlist**********
Mt    2 1 0 0        NMOS     w=0.6u    l=0.5u
m1    5 3 12 0       NMOS     w=3u      l=0.5u
m2    6 4 13 0       NMOS     w=3u      l=0.5u
m3    5 1 7 7        PMOS     w=0.5u    l=0.5u
m4    6 1 7 7        PMOS     w=0.5u    l=0.5u
mc1   5 6 7 7        PMOS     w=0.5u    l=0.5u
mc2   6 5 7 7        PMOS     w=0.5u    l=0.5u
mc3   5 6 7 7        PMOS     w=0.5u    l=0.5u
mc4   6 5 7 7        PMOS     w=0.5u    l=0.5u
mr1   8 5 0 0        NMOS     w=2u      l=0.5u
mr2   9 6 0 0        NMOS     w=2u      l=0.5u
m5     8 9 0 0       NMOS     w=5u      l=0.5u
m6     9 8 0 0       NMOS     w=5u      l=0.5u
m7     8 9 10 7      PMOS     w=14.5u   l=0.5u
m8     9 8 10 7      PMOS     w=14.5u   l=0.5u
m9    11 1 0 0       NMOS     w=5u      l=0.5u
m10   11 1 7 7       PMOS     w=14.5u   l=0.5u
```

```
mt2   10 11 7 7    PMOS      w=1.94u   l=0.5u
msw1 12 6 2 0     NMOS      w=3u       l=0.5u
 msw2   13 5 2 0   NMOS     w=3u       l=0.5u
**********supply voltage*******************
VDD 7 0 dc 1
**********input signal*********************
vinn 3 0 pulse(695m 705m 0 0.3n 0.3n 24.7n 50n)
vinp 4 0 pulse(705m 695m 0 0.3n 0.3n 24.7n 50n)
vclk 1 0 0.5 pulse(0 1 0 0.3n 0.3n 24.7n 50n)
***************analysis*********************
.meas tran avgpower AVG power from=0.01n to 50ns
.cl1 5 0 7f
.cl2 6 0 7f
.clon 8 0 7f
.clop 9 0 7f
.tran 10p 100n
.op
.option post
.end
*****************END**********************
```

B. **********proposed double tail comparator (90nm)*************

**********include model file******

```
.include 'cnmos_90_model.txt'
.include 'cpmos_90_model.txt'
****************netlist*********************
Mt      2 1 0 0       NMOS    w=0.29u     l=0.2u
m1      5 3 12 0      NMOS    w=0.5u      l=0.2u
m2      6 4 13 0      NMOS    w=0.5u      l=0.2u
m3      5 1 7 7       PMOS    w=0.5u      l=0.2u
m4      6 1 7 7       PMOS    w=0.5u      l=0.2u
mc1     5 6 7 7       PMOS    w=0.2u      l=0.2u
mc2     6 5 7 7       PMOS     w=0.2u     l=0.2u
mc3     5 6 7 7       PMOS     w=0.2u     l=0.2u
mc4     6 5 7 7       PMOS     w=0.2u     l=0.2u
mr1      8 5 0 0       NMOS     w=0.8u     l=0.2u
mr2      9 6 0 0       NMOS     w=0.8u     l=0.2u
m5      8 9 0 0       NMOS     w=2u       l=0.2u
m6      9 8 0 0       NMOS     w=2u      l=0.2u
m7      8 9 10 7      PMOS     w=5.5u     l=0.2u
```

```
m8      9 8 10 7     PMOS      w=5.5u     l=0.2u
m9      11 1 0 0     NMOS      w=2u       l=0.2u
m10    11 1 7 7     PMOS    w=5.5u   l=0.2u
mt2     10 11 7 7    PMOS    w=1u     l=0.2u
msw1  12 6 2 0     NMOS    w=0.5u   l=0.2u
msw2  13 5 2 0     NMOS    w=0.5u   l=0.2u

**********supply voltage**********
VDD 7 0 dc 1
**********input signal**********
vinn 3 0 pulse(695m 705m 0 0.1n 0.1n 19.9n 40n)
vinp 4 0 pulse(705m 695m 0 0.1n 0.1n 19.9n 40n)
vclk 1 0 0.5 pulse(0 1 0 0.1n 0.1n 19.9n 40n)
**********clock signal**********
.meas tran avgpower AVG power from=0.01n to 40ns
.cl1 5 0 7f
.cl2 6 0 7f
.clon 8 0 7f
.clop 9 0 7f
.tran 10p 40n
.op
.option post
.end
**********END**********
```

C. *********proposed double tail comparator (45nm) **********

*********include model file********

```
.include 'cmosedu_models.txt'
**********netlist**********

mt      2 1 0 0      NMOS     w=0.28u      l=0.05u
m1     5 3 12 0     NMOS     w=0.315u     l=0.05u
m2     6 4 13 0     NMOS     w=0.315u     l=0.05u
m3     5 1 7 7      PMOS     w=0.05u      l=0.05u
m4     6 1 7 7      PMOS     w=0.05u      l=0.05u
mc1    5 6 7 7      PMOS     w=0.05u      l=0.05u
mc2    6 5 7 7      PMOS     w=0.05u      l=0.05u
mc3    5 6 7 7      PMOS     w=0.05u      l=0.05u
mc4    6 5 7 7      PMOS     w=0.05u      l=0.05u
mr1     8 5 0 0     NMOS     w=0.1u       l=0.05u
mr2     9 6 0 0     NMOS     w=0.1u       l=0.05u
```

```
m5      8 9 0 0     NMOS       w=0.5u          l=0.05u
m6      9 8 0 0     NMOS       w=0.5u          l=0.05u
m7       8 9 10 7     PMOS       w=1.1u          l=0.05u
m8       9 8 10 7     PMOS       w=1.1u          l=0.05u
m9       11 1 0 0     NMOS      w=0.5u          l=0.05u
m10     11 1 7 7     PMOS       w=1.1u          l=0.05u
mt2      10 11 7 7   PMOS       w=0.524u      l=0.05u
msw1   12 6 2 0      NMOS      w=0.315u      l=0.05u
msw2   13 5 2 0      NMOS      w=0.315u      l=0.05u

**************supply voltage******************

VDD 7 0 dc 1

*************input signal*********************
vinn 3 0 pulse(695m 705m 0 0.1n 0.1n 19.9n 40n)
vinp 4 0 pulse(705m 695m 0 0.1n 0.1n 19.9n 40n)

**************clock signal*********************
vclk 1 0 0.5 pulse(0 1 0 0.1n 0.1n 19.9n 40n)

***************analysis***********************
.meas tran avgpower AVG power from=0.01n to 40ns
.cl1     5 0 7f
.cl2     6 0 7f
.clon   8 0 7f
.clop   9 0 7f
.tran   10p 2n
.op
.option post
.end
************************************************END************************************************
```