NBTI AWARE SUPPORT VECTOR MACHINE BASED SURROGATE MODEL FOR ANALOG CIRCUITS

Ph.D. Thesis

SAPNA KHANDELWAL

2012REC9045

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY, JAIPUR

September, 2018

NBTI Aware Support Vector Machine Based Surrogate Model For Analog Circuits

Submitted in

fulfillment of the requirements for the degree of

Doctor of Philosophy

by

Sapna Khandelwal

ID - 2012REC9045

Under the Supervision of

Prof. Dharmendar Boolchandani

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY, JAIPUR

September, 2018

DECLARATION

I, **Sapna Khandelwal**, declare that the thesis entitled, "**NBTI Aware Support Vector Machine based Surrogate Model for Analog Circuits**" and the work presented in it, are my own. I confirm that :

- This work was done wholly or mainly while in candidature for a research degree at this university.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this university or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself, jointly with others. I have made clear exactly what was done by others and what I have contributed myself.

Date : **Sapna Khandelwal**

(2012REC9045)

CERTIFICATE

This is to certify that the thesis entitled "***NBTI Aware Support Vector Machine based Surrogate Model for Analog Circuits***", being submitted by **Sapna Khandelwal (2012REC9045)** is a bonafide research work carried out under my supervision and guidance in fulfillment of the requirement for the award of the degree of **Doctor of Philosophy** in the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur, India. The matter embodied in this thesis is original and has not been submitted to any other University or Institute for the award of any other Degree.

Place : Jaipur

Date :

Dr. Dharmendar Boolchandani
Professor
Department of Electronics and Communication Engineering
Malaviya National Institute of Technology,
Jaipur-302017, India.

ACKNOWLEDGMENT

The completion of my dissertation and subsequent Ph.D. has been a long journey. Completion of this doctoral dissertation was possible with the support of several people. I would like to express my sincere gratitude to all of them. First and foremost I am extremely grateful to my research guide, Dr. Dharmendar Boolchandani, Professor, ECE Department MNIT Jaipur, for his warm, sincere, approachable support, patience, and encouragement during my research work. I consider it as a great opportunity to do my doctoral programme under his guidance and to learn from his research expertise. He is a person with an amicable and positive disposition. His patience, flexibility, genuine caring and concern, and faith in me during the dissertation process, hold me boosted. I would like to thank you for all your contributions of time, insightful discussion about the research, giving me a freedom to pursue my work and allowing me to grow as a research person. Thanks for all motivational talks, guidances and listening to me all the times. Thank you Sir!

I would like to thanks my DREC members, Dr. Vineet Sahula (Professor), Dr. Lava Bhargava (Associate Professor) and Dr. C. Periasamy (Assistant Professor) for serving my committee members and providing me valuable comments and suggestions to nurture my work. Their academic support and input and personal cheering are greatly appreciated. Thank you! The thesis would not have come to a successful completion, without the help I received from the staff of the ECE Department of Institute. I like to thank them for all non-technical and technical support to carry out my research work. Thank you!

Another stanch supporter and is a special friend of 9 years, Lokesh garg. His support and belief in me were a treasure. I would like to thank him for all discussions, research guidance, encouragement, editing my papers and listening to me patiencely everytime. Thank you! My gratitude is also extended to another firm supporter and a special friend Niketa Sharma. She has always been a tremendous help no matter the task or circumstance. I couldn't have completed my thesis writing work and submitted it within time without her motivation. Her constant faith in me, keep me going. Thank you for your motivation, belief and all the prayers you did for me and listening to me patiently. thank you dear!

My colleagues, Ramakrishna, Ashish, Shashikant, Yogendra, Arjun, Arun, Bharat

and Shanky all have extended their support in a very special way, and I gained a lot from them, through their personal and scholarly interactions, their suggestions at various points of my research programme. I would like to thank them for all tea time discussions, all lunches and dinners, all pizza parties and all editing work. Thank you! My time at MNIT was made enjoyable and enriched by many of the M.Tech students, who come across these last five years. I take this time to thank Nupur, Swaraj, Kamini, Alka, Somendra, Prakhar, Ankush, Mohit, Vikas and Gaurav for all those precious memories, discussions at canteen, lunchs & dinners and memorable trips. Without all of you my Ph.D. would not have be so much fun. Thank you!

I would like to extend my sincere gratitude to my in-laws especially my late Father-in-law and Mother-in-law for their tremendous support to accomplish my thesis work. I owe a lot to them. Thank you Papa and Ma!. I would also like to thank to my brothers-in-law and sisters-in-law for their understanding and support. My nieces Poorvi, Gunnu and Shona and my nephew laddu are very dear to me. I want to pay my heartfelt and deepest gratitude to my husband Brijendra for his consistent support, understanding, unconditional love and encouragement from past 2.5 years which made this dissertation possible. His faithful support during the final stages of this Ph.D. is so appreciated. Thanks for your patience and belief in me. Thank you love!

Last but not the least, I am very much indebted to my family who encouraged and helped me at every stage of my personal and academic life and longed to see this achievement come true. My deepest thanks to my Parents, Chacha, Chachi, Mamta Di, Jiju, Shankar Bhaiya and Bhawna Bhabhi, Bittu and Cheenu for their love, prayers, support and belief in me. My nieces Kriti and Aanya and nephews Ananya and Chaitanya are twinkle of my eyes. They have re-energized and given me a much-needed reprieve from work. Thanks and Love you all !

Above all, I owe it all to Almighty God for granting me the wisdom, health and strength to undertake this research task and enabling me to its completion. Thank you God!

(Sapna Khandelwal)

ABSTRACT

In the pursuit of satisfying Moore's law, technology development has witnessed relentless scaling of CMOS transistors feature sizes and increasing number of transistor per chip. Reliability issue which took the back seat has fronted as a threat for present and future technology nodes. Reliability is defined as the probability of a circuit that it will perform its required function according to its specifications, for a stated period of time, under specified conditions. Time based reliability degradation of solid state devices is called aging. Bias Temperature Instability (BTI) is treated as one of the most severe aging degradation mechanism nowadays. BTI has a deleterious impact on threshold voltage and drive current of MOS transistor. Negative BTI (NBTI) which affects the PMOS transistor is worse than the Positive BTI (PBTI) which affects the NMOS transistor. NBTI has become a major reliability concern for both analog and memory circuit design. Analog circuits like differential amplifier or current mirror and memory circuit SRAM (Static Random Access Memory) are particularly sensitive to reliability issues due to their use of matched transistors.

New technology demands the quick understanding of aging phenomenon at the circuit level. To cut the cost and to analyze the aging impact at circuit level, a circuit reliability simulation is required, for both analog circuits and SRAM. For reliability simulation device tools presented in the literature are built around the standard SPICE circuit simulator to find the degradation of the transistor in the circuit. SPICE based reliability simulation methods uses two step simulation in which nominal simulation is followed by aging analysis which is a computation intensive phenomenon. The objective of this thesis, to improve simulation efficiency has been the motivation behind efforts to develop surrogate models; which are as accurate as SPICE and at the same time have shorter simulation time. Several surrogate modeling technique have been developed and reported in the literature. Among such techniques Support Vector Machine (SVM) based surrogate models are found less complex and more accurate.

Analog circuits use threshold voltage (V_{TH}) matched transistor pairs. Mismatches introduced due to NBTI in the V_{TH} and I_D (drain current) mismatches of these transistors, could be dominant failure mechanism in these devices. We have developed NBTI aware surrogate model for performances of the analog circuit using SVM regressor. We have also developed feasibility model using SVM classifier to find the feasibility design

space for final regressor model. The accuracy of a surrogate model is affected by number of samples. Every sample attribute to costly CPU simulation time. We have proposed sampling scheme that includes Latin Hypercube Sampling (LHS) and Adaptive Learning to generate samples efficiently. Error driven adaptive learning methodology is used to generate the samples adaptively in the large error areas. This combined scheme build SVM models using less number of training samples, thus reducing model simulation time without loss of accuracy. The impact of aging on IC remains for a long term e.g. 5 years or more. The need for long term model arises to predict the degradation after many cycles of operation. Predicting circuit degradation during long term simulations using single and long step leads to erroneous results. Constant step size can cause either inefficiency or inaccuracy, where smaller steps increases simulation time and larger steps may cause prediction errors. We have proposed a dynamic time step algorithm, to obtain the accurate time step where the stress conditions gets updated during long term simulations. We have also developed SVM based long term model at the transistor and circuit level for electrical and performance parameter of an analog circuit.

SRAM transistors are more prone to BTI phenomenon due to their symmetric topologies. Each memory cell either store 0 or 1 at all times, creating unbalanced stress all times, causing a reduction in SRAM cell reliability characteristics. Moreover, BTI also affects the performance of SRAM peripheral circuitry which results in timing mismatch between SRAM cell and its peripheral circuits that lead to unreliable access operations. NBTI majorly affects the read static noise margin of SRAM cell (RSNM). There are several mitigation techniques proposed in the literature to compensate this NBTI effect like guard banding, word line/bit line control, dual supply voltage and body bias control. We have proposed a new mitigation technique which is a combination of two previously proposed techniques i.e., supply voltage (V_{DD}) upscaling and bit line voltage (V_{BL}) reduction. To implement this technique a hybrid model is developed comprised of both V_{DD} and V_{BL}. This hybrid model improves read stability while avoiding the degradation of other parameters related to read operation like read power and read current or delay. One of the most critical SRAM peripheral circuits is the sense amplifier, which is related to the read access time of the SRAM. Process variations and time based degradations introduces the mismatch between transistors of the sense amplifier, finally hampering the read operation. Thus, it is necessary to predict the sensing delay of the

sense amplifier at the design stage itself considering the presence of reliability issues. We have developed variability and reliability aware surrogate model for sensing delay of sense amplifier. We have also studied the effects of process corners on sensing delay.

NBTI aware surrogate models are proposed for analog circuits like a differential amplifier, common source amplifier and sense amplifier. A dynamic time step algorithm is proposed to obtain the long term surrogate model for analog circuits. A new mitigation technique is proposed to improve the read stability of SRAM. An adaptive learning methodology is used to generate SVM surrogate models efficiently.

Contents

List of Figures

List of Tables

List of Algorithms

Nomenclature

I_D	:	Drain Current
V_{gs}	:	Gate to Source Voltage
V_{ds}	:	Drain to Source Voltage
V_{DD}	:	Supply Voltage
V_{BL}	:	Bit Line Voltage
T_{OX}	:	Oxide Thickness
P_{READ}	:	Read Power
I_{READ}	:	Read Current
V_{gs}	:	Gate to Source Voltage
V_{MIN}	:	Minimum Operating Voltage
V_{TH}	:	Threshold Voltage
μ	:	Mobility
ANN	:	Artificial Neural Network
BL	:	Bit Line
BTI	:	Bias Temperature Instability
HCI	:	Hot Carrier Injection
LHS	:	Latin Hypercube Sampling
LS-SVM	:	Least Square Support Vector Machine
MOSRA	:	MOSFET Reliability Analysis
NBTI	:	Negative Bias Temperature Instability
PBTI	:	Positive Bias Temperature Instability
PTM	:	Predictive Technology Model
RSM	:	Response Surface Model
RD	:	Reaction Diffusion
SRAM	:	Static Random Access Memory

SVC	:	Support Vector Classifier
SVM	:	Support Vector Machine
SVR	:	Support Vector Regression
T	:	Time
TD	:	Trapping Detrapping
TDDB	:	Time Dependent Dielectric Breakdown
W	:	Channel Width
WL	:	Word line

Chapter 1

Introduction

In the pursuit of satisfying Moore's law [1], technology development has witnessed relentless scaling of CMOS transistors feature sizes leading to increased number of transistors per chip. While shrinking dimension has reached the demarcation line of charge and granularity of matter, but it has a dark side too; variability and issues of reliability [2]. The reliability and quality of the end product is more demanding than ever. The introduction of the new gate and channel materials pose unknown reliability threats. Furthermore due to the atomistic size of the transistor, gate oxide electric field and current densities have also increased to maintain the effective performance. Their values are reached to the levels where reliable circuit operation is not guaranteed anymore. These wear out mechanisms manifest gradually and produce time dependent shift in circuit electrical parameters which leads to circuit failure, especially in analog circuits and SRAM's which are quite sensitive to even small variations. These issues not only affects design goals but poses a limit on circuit and product lifetimes, so need to be taken into account at design time. Thus the reliability issue which took the back seat has fronted as a threat for present and future technology nodes and have become a major issue in the latest ITRS guidelines [3].

1.1 Reliability: An Overview

ITRS mentions reliability as one of the "Design Technology Challenges". Reliability is defined as the probability of a circuit that it will perform its required function according to its specifications, for a stated period of time, under specified conditions. As the

device dimensions have reached to the deep sub-micron technology, adverse degradation phenomenon appears for many device and circuit parameters. To overcome the scaling limitations, different device structures, processing conditions and materials have been used which further enhances the complexity and reduces the reliability of the circuit, right after production and during its lifetime. The failure rate of a circuit or a product can be represented using the "bath tub" curve [4] as shown in Figure 1.1.

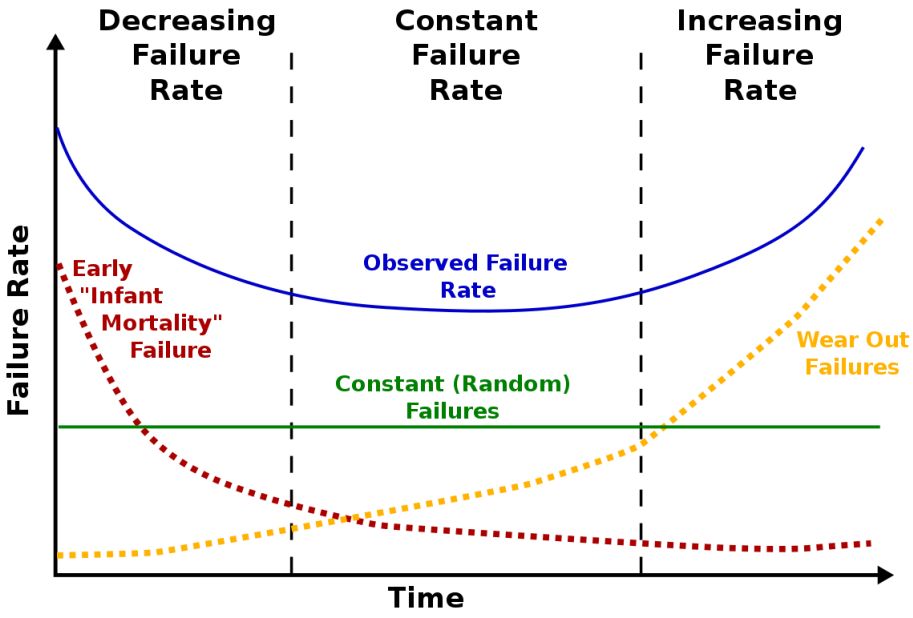


Figure 1.1: The Bath Tub Curve [4]

It shows the failure rate of the product over its entire life span. The initial period showing the high and decreasing failure rate, right after production, is called "infant mortality period". These failures are due to oxide defects, mask defects, solder defects, improper bonding, contamination and variability. By screening the early failures, overall product reliability can be improved. The second period in which the failure rate remains constant is called the "constant failure period". It is the useful life of the product. The constant failure rate is due to cross talk and transient errors. After this period the product starts to wear out and failure rate increases due to aging effect. This period is called as "wear out failure period". The focus of this work is on this wear out period which develops with every new CMOS generation. CMOS reliability issues [5] as shown in Figure 1.2 can be broadly divide into two parts -

1) Spatial Unreliability Effects - These are also called process variability effects

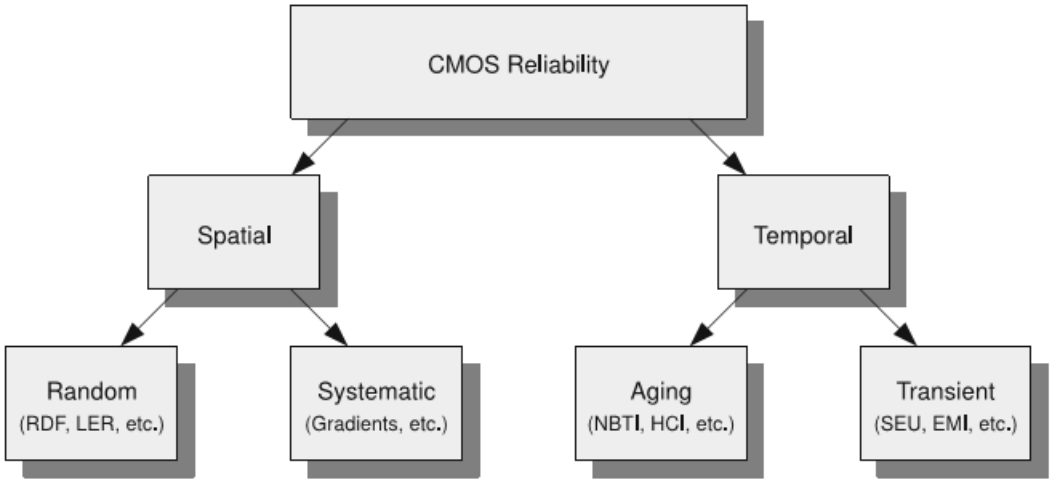


Figure 1.2: Sources of Variations [5]

which are the main cause of the infant mortality period of the bathtub curve. These effects are fixed in time and appears just after production. The impact of these effects can be measured in terms of parametric yield. Process variability affect the physical parameters such as gate oxide thickness, dielectric thickness and channel length which in turn affects the electrical parameters like threshold voltage (V_{TH}) and drain current (I_d) of the transistor. These electrical parameters finally affect the circuit performance parameter. Two main sources of process variability are Interdie (Global) and Intradie (Local) effects. Global variations include lot to lot, wafer to wafer and die to die variations. All devices on a single die get effected by the same type of variation but it varies from one die to another. This variation shifts the mean value of design parameter for e.g., in a single die changing the length of all transistors either larger or smaller than the nominal value. Local variations include with in die variations and affects all transistor on a single circuit in a different manner, causing some transistors to have smaller length while others to have bigger than the nominal value. These variations can be divided into systematic and random variations. The former variations are layout dependent, hence deterministic by nature. The latter are statistical fluctuations in process parameters such as line edge and width roughness, random dopant fluctuations, oxide thickness variation. They are indeterministic by nature. Due to the relentless scaling local variations are more significant than global variations.

2) Temporal Unreliability Effects - These are also called aging effects which are the main cause of the wear out failure period of the bathtub curve. These effects appears

over a period of time when the circuit is used at a particular temperature, workload and certain environment conditions. They directly degrade the circuit electrical parameters such as threshold voltage (V_{TH}), mobility (μ) and transconductance (g_m) of the transistor which in turn affects the performance parameter. The impact of this effects can be either temporary or permanent. Two major sources of temporal unreliability are Aging and Transient effects. Aging causes gradual degradation of transistor parameter, resulting in circuit malfunction and some part of the damage is permanent. Aging became an issue due to aggressive scaling of the device geometries and increasing electric fields. Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB) are the prominent failures mechanisms due to aging. Transient effect hampers the normal circuit operation for a limited period of time. Noise and Electromagnetic Interference are the main cause of transient effect. Once the noise source is removed circuit starts showing the same performance as before. The focus of this thesis is the most dominant failure mechanism due to aging i.e., BTI.

1.2 Aging: The Bias Temperature Instability

Every circuit should perform reliably for a defined period of time. Transistor degradation is more prononuced with technology scaling, which further deviates performance parameters from its specified value. One of the dominant aging mechanisms is BTI which mainly affects device V_{TH} [6] and manifest itself as performance parameter degradation. This V_{TH} shift under negative stress is termed as NBTI (PMOS) and under positive stress is termed as PBTI (NMOS). NBTI is a more severe phenomenon in comparison to PBTI. NBTI poses significant reliability concerns for analog and digital circuits. It was found by Deal et al. [7] for the first time, and since then evolution has been progressing on the modeling of NBTI. No universal model is adopted to understand the behavior of NBTI. Few effects that intrigue the device and circuit designers towards NBTI [8, 9, 10] are :

- Mismatch of scaling of Supply Voltage (V_{DD}) with Oxide Thickness (T_{OX}) which results in higher fields that enhances NBTI.
- Mismatch of scaling of device V_{TH} with V_{DD} which results in reduction in Drain Current (I_D).

- Scaling of Power requirements does not match with increasing transistor densities which leads to increased on chip temperature at an alarming rate that enhances NBTI.
- Introduction of nitrogen into the gate dielectric to reduce gate leakage and to hamper boron penetration in a thin oxide, increases NBTI.

Two types of traps contribute to NBTI are:

1. **Interface Traps:** Defects present at the silicon/silicon dioxide (Si/SiO_2) interface.
2. **Oxide Traps:** Defects present in the SiO_2 layer of the MOS structure.

When a PMOS transistor is subjected to negative bias at elevated temperature, positive charge builds up because of the both types of traps mentioned above. This charge leads to degradation of transistor performance. NBTI phenomenon is divide into two phases; stress and recovery. During stress phase the interface traps are generated due to the dissociation of $Si-H$ bonds at the Si/SiO_2 interface. Dissociation is preceded by the capture of the inversion layer holes (via field assisted tunneling) by the $Si-H$ bonds. This makes the $Si-H$ bond weak, which can easily broken at higher temperature. This process yields positively charged dangling Si bonds at the Si/SiO_2 interface, that is responsible for higher V_{TH}. The new H atoms then form H_2 molecules which diffuse away from the interface. The trap generation is model by the following equation

$$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si\bullet + H_2 \tag{1.2.1}$$

The NBTI effect on transistor parameters is directly proportional to the stress period and is modeled by an increase in V_{TH} . This V_{TH} shifts follow a t^n power law time dependence with n value ranging from 0.17-0.3. When stress is removed some interface traps anneal itself and passivate dangled Si bonds, that results in partial recovery. This is called recovery phase. Thus NBTI phenomenon can be classified as Static and Dynamic NBTI. Static NBTI under constant application of DC voltage is more severe for analog circuits. Dynamic NBTI under AC stress leads to less severe parameter's shift with time. Due to the switching activity, Dynamic NBTI affects more on digital circuits. Most authors agree that there are actually two degradation component : permanent and recovery. Permanent degradation depends on many factors such as :

- Material of the gate dielectric
- Duty factor of stress and no stress
- Used technology
- Temperature
- Duration and amount of applied gate voltage stress

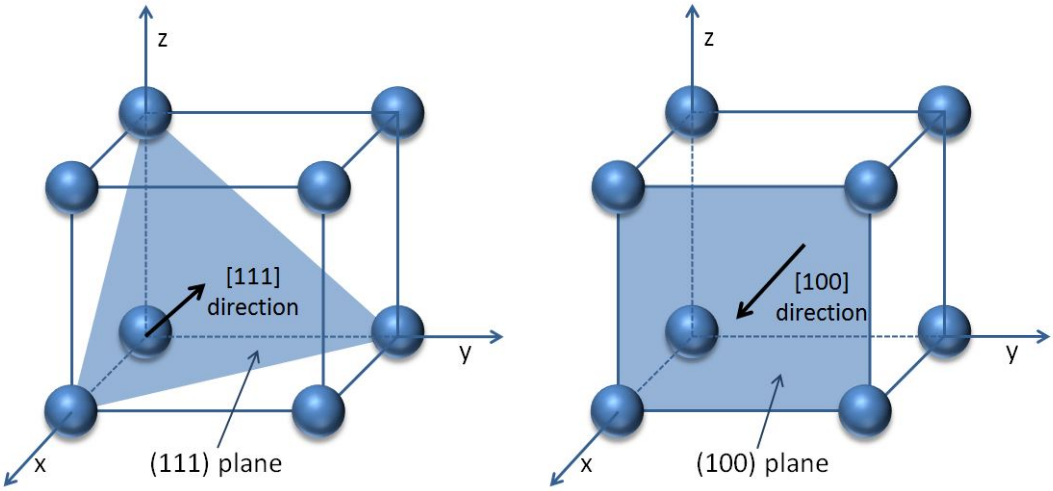
The impact of NBTI on transistor parameters are :

- Increase in absolute value of threshold voltage (V_{TH})
- Increase in off current (I_{off})
- Decrease in transconductance (g_m)
- Decrease in drain current (I_D)
- Decrease in mobility (μ)
- Decrease in subthreshold slope (S)

Thus NBTI has become an crucial reliability concern with significant implications for both analog and digital circuits. PBTI remain negligible for NMOS transistor and have become significant with the introduction of High-k Metal Gate (HKMG) technology. Generation of negative charges in High K layer is responsible for PBTI in such devices. It occurs due to the electron trapping in pre-existent oxide traps [11], combined with a trap generation process. However, PBTI exhibits less V_{TH} degradation [12] in comparison to NBTI.

1.2.1 Physical Mechanism of NBTI

The dynamic properties of thermally grown Si/SiO_2 interface, on a pure silicon crystal is the primary cause of the continuous success of CMOS technology. This interface has a very low defect density and is of high quality [13]. The important property of the silicon substrate is the crystal orientation which is either in $< 100 >$ or $< 111 >$ form as shown in Figure 1.3.



(a) (b)

Figure 1.3: The Monocrystalline Silicon (a) <111> crystal plane (b) <100> crystal plane [13]

1.2.1.1 Interface Traps : Silicon Dangling Bonds

The *Si* atom requires four bonds to saturate the valence shell. In the deep atomic structure, each silicon atom creates bonds to nearby four atoms. At the surface atoms are missing, hence traps are created which are known as interface traps [14] or interface states as shown in Figure 1.4(a). They are usually denoted [15] as

$$Si_3 \equiv Si\bullet \tag{1.2.2}$$

where $'\equiv'$ represents three complete paired bonds to other *Si* atoms and $'\bullet'$ represent the unpaired (fourth) electron in dangling orbital (dangling bond). Interface traps are designated as $N_{IT}(cm^{-2})$, $Q_{IT}(C/cm^{-2})$ or $D_{IT}(cm^{-2}eV^{-1})$. The density D_{IT} of these traps is $\approx 10^{14}cm^{-2}eV^{-1}$ [16]. These traps cannot be recoverable over a period of time. On the top of the *Si* substrate, a thin film of insulation is deposited, with the process of thermal oxidation. This process occurs at an elevated temperature of 900°to 1200°in an oxidation furnace. There are two types of oxidation -

(1) Dry Oxidation - It is performed in the presence of O_2. It achieves higher density of the SiO_2 [17].

$$Si_{(solid)} + O_{2(gas)} \Rightarrow SiO_{2(solid)} \tag{1.2.3}$$

(2) Wet Oxidation - It is performed in the presence of H_2O. It is a faster process in

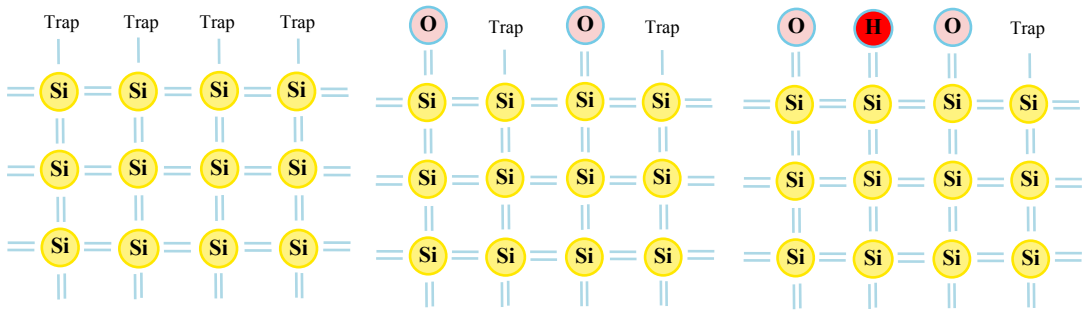


Figure 1.4: The Interface Traps [14]

comparison of dry oxidation. In wet oxidation some *Si* atoms bond to hydrogen atoms.

$$Si_{(solid)} + H_2O_{(gas)} \Rightarrow SiO_{2(solid)} + 2H_{2(gas)} \tag{1.2.4}$$

During the oxidation, Si/SiO_2 interface is formed which is essential for NBTI process. After oxidation, most traps are bonded with oxygen atoms (Figure 1.4(b)). Now SiO_2 has tetrahedron structure with an angle of 109°[18] between each oxygen and *Si* atom as shown in Figure 1.5. The *Si* atom bonded to four oxygen atoms. Each *O* atom is bond to another *Si* atom from different tetrahedrons. The angle between two tetrahedrons varies between 120° and 180° with an average value of 150° which when varies causes the bond to weakened. These weak bonds break easily producing a trivalent *Si* atom with unsaturated valence electron known as interface traps. Due to this process, a large number of unbound *Si* atoms are created which are known as silicon dangling bonds. The region in which these bonds are created is known as an interface. After oxidation density of the traps changes to $D_{IT} \approx 10^{12} cm^{-2} eV^{-1}$ which shows the improvement of interface quality but still a large number of dangling bond exists. Each active interface state causes degradation of transistor parameters such as mobility, threshold voltage and on current.

These dangling *Si* bond at Si/SiO_2 interface termed are as P_b center. These P_b centers are donar like traps and attract holes. The abbreviation *P* comes from the paramagnetic nature of these bonds in the presence of magnetic field. Initially three defects P_a,P_b and P_c were identified, but finally P_b has been correlated with *Si* dangling bond. P_a and P_c appear due to process related effects. In $< 111 >$ lattice structure only P_b centers exists, while P_{b1} and P_{b2} exists in $< 100 >$ orientation. The difference between P_{b1} and P_{b2} lies

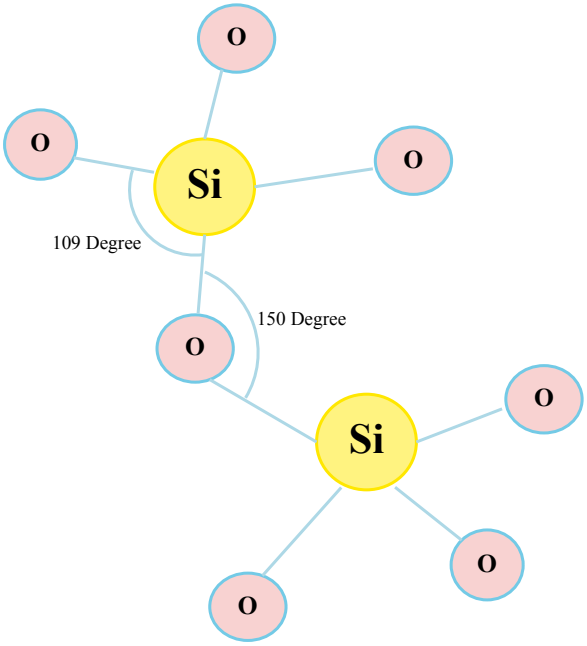


Figure 1.5: The SiO_2 structure [18]

in their spin momentum. All these types of *Si* dangling bonds are of amphoteric in nature which means they can be occupied by one or two electrons or can remain unoccupied and have become positive, negative or neutrally charged respectively. These *Si* dangling bonds or P_b center can lead to poor device characteristics. Thus it is necessary to reduce the number of interface traps. It is done by applying the gas annealing to the interface in order to passivate the P_b centers as given by the Equation (1.2.5) and Equation (1.2.6)

$$Si + H_2 \Rightarrow SiH + H \tag{1.2.5}$$

$$Si + H \Rightarrow SiH \tag{1.2.6}$$

The dangling *Si* bonds are converted to $Si-H$ bonds (Figure 1.4(c)) and density of interface traps reduces to $D_{IT} \approx 10^{10} cm^{-2} eV^{-1}$ which is an acceptable number. The hydrogen atom eliminates the activity of *Si* dangling bonds by shifting its energy level out of the silicon band gap, therefore passivating the defects. These $Si-H$ bonds have lower binding energy and break quickly at high temperature and electric fields, producing interface traps again. This leads to an additional charge at the interface and degradation of transistor parameters like V_{TH} of the transistor.

1.2.1.2 Oxide Traps

Impurities in manufacturing process create oxygen vacancies in the oxide. Under high temperature and negative bias there will be electric field in vertical direction, that allows hole capture from the *Si* inversion layer which tunnel through the dielectric. The positive oxide trapped charge is formed due to the trapping of holes at oxygen vacancies [19]. After hole capture, the oxide trap can crack molecular hydrogen which is important for the dissociation of Si-H bonds. V_{TH} is degraded due to charge accumulation by these holes in the oxide. At the removal of stress, the oxide traps will be annealed which further restored V_{TH} value to some extent.

1.2.2 Reaction Diffusion (RD) Model

NBTI can be described as the generation of interface charges N_{IT} at the Si/SiO_2 interface, which in turn degrade the V_{TH} of the transistor. This V_{TH} shifts follow the power law dependence with time

$$\triangle V_{TH} \propto t^n \tag{1.2.7}$$

where n varies from 0.16 to 0.3. The process of NBTI needs to be explained through some analytical model. Among the various proposed models in the literature, only RD model is consistent with power law dependence of NBTI. The RD mechanism was first introduced by Jeppson and Svensson (1977) [20, 21]. It is one of the most popular NBTI model which describes the creation and annealing of *Si* dangling bond at the Si/SiO_2 interface. It consists of two critical steps -

REACTION - This part interprets the chemical reaction like $Si-H$ bonds dissociation and reformation [22] taking place at the interface. When a PMOS transistor is biased in strong inversion region under vertical electric stress, the holes in the inversion layer reacts with the $Si-H$ bonds and finally weakens the bond. At high temperature this mechanism tends to dissociate H atoms, forming the interface traps as shown in Figure 1.6. This electrochemical reaction is an exponential function [23] of field and temperature and trap generation rate is given by differential equation as

$$\frac{dN_{IT}}{dt} = k_F(N_O - N_{IT})P - k_R N_H(0) N_{IT} \tag{1.2.8}$$

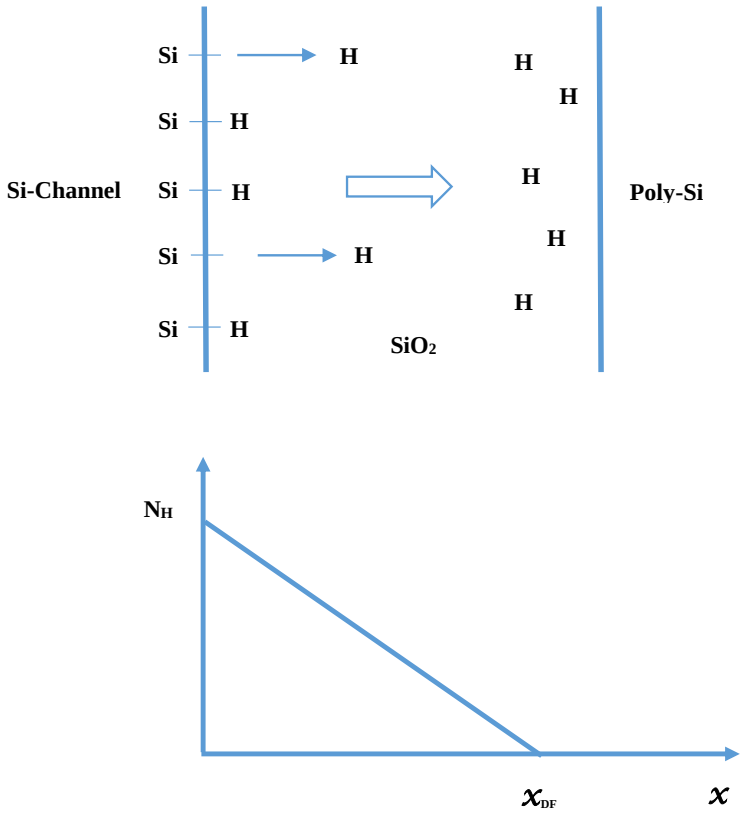


Figure 1.6: The Dissociation of $Si-H$ bonds [8]

where k_F is the oxide field dependent forward dissociation rate, k_R is the reverse annealing rate, N_O is the initial concentration of unbroken $Si-H$ bonds, P is the concentration of inversion carriers and $N_H(0)$ is the hydrogen concentration at the $x=0$ interface. The broken Si bond act as a donor atom and increases V_{TH}. On the other hand, annealing takes place under positive stress. The second term in Equation (1.2.8) describes how the released hydrogen atoms can anneal the broken bonds $(\equiv Si-)$ at Si/SiO_2 interface which lowers N_{IT} which will further reduce V_{TH}. With the continued process, two H atoms combine to generate a H_2 molecule. The concentration of H_2 , i.e., N_{H_2} is given as

$$N_{H_2} = k_H N_H^2 \tag{1.2.9}$$

where k_H is H to H_2 conversion rate. The Figure 1.7 shows the overall change in V_{TH} due to continuous stress and recovery phase.

DIFFUSION - This part interprets the transport of hydrogen species in the oxide and the gate. In this phase, the reaction generated species, diffuse away from the interface

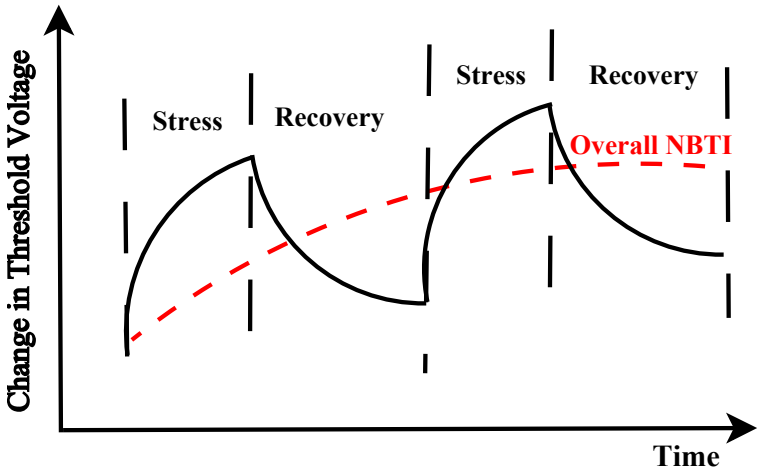


Figure 1.7: The Stress Recovery Phenomenon [35]

toward the gate. This phenomenon is governed by the gradient of the density. This process influences the balance of the reaction and is governed by -

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \tag{1.2.10}$$

where D_H is the diffusion constant and N_H is the total hydrogen concentration in the oxide. The hydrogen diffuses into oxide with t^n time dependence, where $n \sim 0.25$ for neutral hydrogen species.

During the initial period of stress phase, the trap generation rate is slow. Therefore,

$$N_{IT} \ll N_O \tag{1.2.11}$$

$$\frac{dN_{IT}}{dt} \approx 0 \tag{1.2.12}$$

Hence Equation (1.2.8) reduces to

$$N_H(0) N_{IT} \approx \frac{k_F}{k_R} N_O \tag{1.2.13}$$

Further, after an initial reaction-diffusion process, hydrogen diffusion controls the trap generation process. In this regime, the diffusion front is located at (see Figure 1.6)

$$x_{DF}(t) = \sqrt{D_H t} \tag{1.2.14}$$

Also, the number of generated interface traps is equal to the number of diffused hydrogen atoms

$$N_{IT} = \int_0^{\sqrt{D_H t}} N_H(x,t)dx = \frac{1}{2}N_H(0)\sqrt{D_H t} \tag{1.2.15}$$

Finally combining Equation (1.2.13) and (1.2.15) results in

$$N_{IT} = \left(\frac{k_F}{k_R}\frac{N_O}{2}\right)^{1/2}(D_H t)^{1/4} \tag{1.2.16}$$

A shift in V_{TH} is caused by the interface trap generation, can be expressed as

$$\triangle V_{TH} = \frac{qN_{IT}}{C_{ox}} \tag{1.2.17}$$

where q is the electron charge, C_{ox} is the gate oxide capacitance.

In RD model, value of time exponent depends on diffusion species [24] and stress time [10]. For lower stress time ($\sim 100s$) and H diffusion species, power law exponent is 0.25. As stress time increases ($\sim 10^6 s$) its value changes from 0.25 to 0.16. Recent models assume that two H atoms always tend to form H_2 molecule , providing power law exponent 0.17 which is better for measurements.

1.2.3 PBTI vs NBTI

BTI is observed in both PMOS and NMOS transistors. However, PMOS transistor under negative bias is the most severely affected. Holes are responsible for NBTI degradation. NMOS biased in accumulation region [15], also have holes at the surface, but they do not exhibit the same V_{TH} degradation as PMOS transistor. The authors in [25] proposed a model to explain this phenomenon. According to this model, positively charged protons or H atoms (H^+) reacts with $Si-H$ and forms interface trap given by the following equation

$$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si\bullet + H_2 \tag{1.2.18}$$

The proton or H is assumed to generate from phosphorus-hydrogen ($P-H$) bonds in the $n-Si$ substrate. These bonds have high activation energy, but are weak in the

depletion region. During NBTI, PMOS transistor remains into inversion, so depletion region is formed. Thus $P-H$ bond breaks and H atom on the way to interface "picks up" a hole to become H^+. Then it reacts with the H from the $Si-H$ bond and finally forms H_2 leaving behind an interface trap. This H_2 diffuses from the interface to the oxide/gate and later passivate the interface trap by diffusing back to the interface, on the removal of stress bias. Hence V_{TH} also shifts due to depassivation. Under positive stress no depletion region is formed, resulting in no H atoms, hence less degradation.

In NMOS, substrate is usually doped with boron. The only way to obtain H atoms is from $B-H$ bonds, whose binding energy is very high even in the depletion region. Thus NMOS are less prone to BTI effect, regardless of the stress voltage. Figure 1.8 shows the effect of NBTI and PBTI on V_{TH} degradation in 45nm technology node for one year.

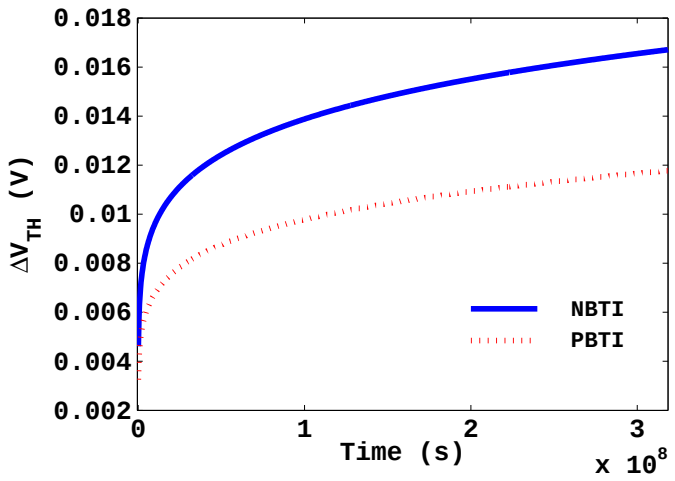


Figure 1.8: Effect of NBTI and PBTI on V_{TH} degradation

1.3 Motivation

CMOS transistors are expected to age with the time that causes the circuit performances to deviate from its specified values. New technology demands the quick understanding of reliability phenomenon and aging behavior beyond the transistor level i.e., further extended to circuit level. Accurate prediction of performance degradation is required at design phase to avoid the expensive design re-spins and computationally intensive simulations. With time BTI affects the performance of analog circuits and SRAM's, so

there is need to predict the aging degradation due to BTI at design phase itself.

1.3.1 BTI effect on Analog Circuits and SRAM

BTI has become a dominant reliability concern for both analog and memory circuit design. Analog circuits like differential amplifier or current mirror and SRAM's are particularly sensitive to reliability issues. Analog components consume only 20% of the integrated circuits (IC) area [26] but they require most of the design efforts due to their knowledge intensive nature. Device matching plays a significant role in the designing of analog circuits [27]. Furthermore, each transistor faces a different kind of stress. So their degradation behavior are different which finally affects the circuit performance. Thus they show more complex degradation behavior than digital circuits. In analog circuits, matched PMOS transistors uses a longer length transistors for V_{TH} and I_D matching. Analog circuits like current mirror or differential amplifier are very sensitive to these V_{TH} and I_D mismatches. BTI could be the dominant degradation mechanisms for these devices [28]. For symmetrically loaded analog circuits device voltages are very small, so change in V_{TH} is very less (order of mV). Analog circuits are sensitive to these small changes. For asymmetrically loaded change in V_{TH} is already high (order of tens of mV) which further affects the circuit performance in a drastic way [29]. Analog circuits use DC voltages for biasing purpose irrespective of the input signal which makes them more susceptible to BTI. The impact of BTI is more pronounced in the transistors which;

1. Operates continuously,

2. Operates under large voltages.

Both of these phenomenon make them more prone towards BTI.

In the memory subsystem SRAM's mostly influence the overall system performance by executing timely and reliable operations. SRAM's include many sub circuits such as bit cell, logic circuits like decoders, read/write access timing control circuit, precharge circuit and sense amplifier. A functional cell should perform the fast read/write operations to pass the product specific requirements. SRAM transistors are more prone to BTI phenomenon due to their symmetric topologies. SRAM cells are composed of cross coupled inverters. Each memory cell either store 0 or 1 at all times, creating unbalanced stress and one of the PMOS transistor (due to NBTI) and one of the NMOS transis-

tor (due to PBTI) are always under stress causing a reduction in SRAM cell reliability characteristics. This introduces asymmetric V_{TH} shift in both PMOS devices which degrades the performance of SRAM cell. Moreover, BTI also impact the performance of SRAM peripheral circuitry. It leads to shifting the trip points of peripheral circuits and degradation of signal propagation delay. As a result timing mismatch occurs between SRAM cell and its peripheral circuits, resulting in unreliable access operations.

1.3.2 Need to develop a Surrogate model

In order to achieve reliable circuit operation in the modern era, the ever rising reliability issues demand solution at the circuit level. Till now, research work on reliability has been active only within the communities of device and reliability physics. This is mainly due to lack of CAD tools, design knowledge and complexity of the aging phenomenon. To cut the cost and to analyze the aging impact at the circuit level, a circuit reliability simulation is necessary for both analog circuits and SRAM's. This type of simulation is required at circuit design time, to evaluate the effect of reliability on circuit performances. Leading companies have developed their commercial tools (e.g., BERT, ELDO, RelXpert) and models which are technology specific. Some device tools presented in the literature combine device model with the standard SPICE simulator for reliability analysis [30]. The SPICE based reliability simulation methods use two step simulation in which nominal simulation is followed by aging analysis. It is a computation intensive phenomenon. Additionally, for variability analysis Monte Carlo sampling techniques have been used in the SPICE simulator which again requires excessive amount of time, especially in the presence of intensive reliability simulation.

Due to an increasing demand of low failure rate in the presence of reliability issues, existing reliability simulation techniques have become too expensive. Now a designer needs a statistical circuit analysis tool that includes reliability concern [30]. This tool should be fast as well as accurate. Moreover, a designer must be able to find the information in order to i) improve the design ii) implement countermeasures. There is need for more capable solution to analyze the reliability issues at the circuit level. A surrogate model of circuit performances is widely accepted to replicate the behavior of complex simulation model while being computationally efficient. Surrogate models can be used in place of time consuming circuit level reliability SPICE simulations. They are built on

the data obtained from SPICE simulations. It establishes the connection between input and output space, which are non linearly correlated, using a group of sample vectors and their corresponding outputs. These models should be developed with a minimum number of training samples and optimal set of parameters. Thus, effective strategies are required to build these models. A surrogate model can be a machine learning model which is a black box model. Its output parameter are trained for every input sample vector or also can be a basis function with several coefficients to be optimized.

1.4 Scope of the work

In this thesis, we have concentrated on the development of reliability aware SVM based surrogate model for performance parameters of analog circuits. Surrogate models are useful to visualize the design space and can be used in place of real circuits to predict the output performance parameters such as gain in case of amplifier circuit. These performance based surrogate model should be valid in functionally correct design space. Feasibility space identification is necessary to build the final performance model as it screens out infeasible design. The problem of representing feasibility function is a classification problem for which we have used SVM classifier. The output of this classifier is applied to SVM regressor model to generate final performance model. In order to develop a surrogate model that is valid for entire design space a good sampling scheme is required. We have used sampling scheme which includes Latin Hypercube Sampling (LHS) and adaptive learning.

First, we have developed NBTI aware surrogate model for gain and slew rate of a differential amplifier. To develop these models, we have generated initial samples of width (W) and time (T) through LHS sampling. NMOS channel width is varied between [1μ, 20μ], PMOS channel width is varied between [1μ, 80μ] and T is varied between 0 to 10 years. Further samples are added through error driven adaptive learning methodology. Then SVM classifier is developed to filter out all the samples that are not in the feasible design space, reducing the simulation complexity and simulation time. The accuracy of the classifier and regressor model is improved by adaptive learning, which generates the samples in the area of maximum error. These SVM models are the black box kind of models and do not provide any equation related to input and output

data. We have developed NBTI aware surrogate model for analysis of the long term aging simulation of a common source amplifier. For the long term, entire simulation time interval is divided into a number of time steps using either constant or logarithmic step. At each step, stress conditions of transistors are updated to include the effect of real time operating conditions. In this regard, we have proposed a dynamic time step algorithm to divide the entire simulation time interval. Further, we have developed SVM based long term transistor level model of $\triangle V_{TH}$ degradation for all PMOS transistors of the given circuit. In order to develop these models width samples of PMOS transistors are obtained through LHS sampling by applying 10% variation in nominal width. Time samples are obtained through proposed dynamic time step algorithm. Then by using these individual transistor level model, combined circuit level model is developed which includes the V_{TH} degradation for all PMOS transistors. This circuit level model shows the effect of V_{TH} degradation on gain of the common source amplifier for every width. The accuracy of both models has been improved by adaptive learning. The effect of different process corners on V_{TH} degradation have also been studied.

Further, we have proposed a new mitigation technique to compensate the NBTI effect on SRAM read stability. Proposed technique is comprised of two other mitigation techniques i.e., supply voltage and bit line voltage tuning. A hybrid model is developed to implement this technique which improves the read stability without affecting the other parameters related to read operation i.e., read power and read current. Then we have developed the variability and reliability aware surrogate model for sensing delay of the SRAM sense amplifier. Width samples are generated through Gaussian distribution for variability analysis. To include the BTI effect time samples are generated through LHS sampling and the corresponding degradation in threshold voltages of NMOS/PMOS transistors are obtained. These width and threshold voltages samples are used to develop a surrogate model. The accuracy of the model has been improved by adaptive learning. Effect of different process corners on sensing delay has also been studied.

1.5 Thesis Preview

Chapter 2 represent the landscape of the literature review. It includes different modeling approaches and theories that have been proposed for NBTI modeling. Different

aging simulation techniques have been discussed. The importance of aging evaluation of analog circuits, SRAM cell and its peripheral circuitry have also been highlighted. This review also includes the different surrogate modeling approaches presented in the literature. Advantages and limitations of different surrogate models are discussed. The necessity of adaptive learning methodology to develop the efficient and accurate machine learning models has been elaborated.

Chapter 3 discusses the importance and development of the surrogate model. It presents the description of machine learning based SVM surrogate models. The effectiveness of both feasibility model and performance model have been presented, which are developed using SVM classifier and SVM regressor respectively. The merits and flaws of different reliability simulator have been discussed, which suggests that Synopsys MOSFET Reliability Analysis (MOSRA) model, integrated with HSPICE is best suited. Sample selection method to develop the SVM models efficiently have been discussed. The concept of adaptive learning methodology is elaborated. Through various experiments, it has been observed that our proposed NBTI aware SVM surrogate model outperforms other model with respect to the simulation time. These experimental results exhibit the improvement of simulation time by using adaptive learning methodology.

Chapter 4 discusses the significance of including real time operating conditions during long time aging simulation. It also features the benefits and restrictions of different step sizes used during long term simulation. The proposed dynamic time step algorithm to update the real time stress conditions is also presented. The proposed algorithm is also compared with various step size approaches. It shows that results obtained through our proposed algorithm closely matches with that obtained using minimum constant step size, using less simulation time. The flow of proposed NBTI aware transistor and circuit level long term SVM based surrogate models have been discussed.

Chapter 5 includes the importance of NBTI simulation for SRAM cell and its peripheral circuits. Several NBTI compensation approaches have been discussed to improve the read stability. A mitigation technique has been proposed which is a combination of two approaches for read stability improvement. The proposed technique is compared with the approaches through which it is developed. Our technique outperforms the other methodologies by simultaneously improving the read stability and avoiding the degradation of other parameters. Effect of variability and aging on sensing delay of the sense

amplifier is studied. The methodology to develop the variability and reliability aware SVM model for sensing delay of the sense amplifier is elaborated. Effect of different process corners on sensing delay is also explored.

Chapter 2

Landscape of the Literature

The exponential scaling of CMOS devices has aggravated the BTI leading to reliability issue of analog and memory circuits. This BTI affects transistor model parameters, which translates into circuit performance degradation finally leading to circuit failure. In the past few years, there has been increased efforts in BTI modeling and characterization at transistor and circuit level. At transistor level no general agreement has been made and physical origin of BTI is still under debate. Zafar in [31] presented that BTI is a statistical mechanism where stress and recovery parts are inseparable. It is reported that due to the change in the charge state of the oxide traps, recovery phase occur. On the other hand Alam in [32] presented an analytical model, based on classical RD model where BTI is defined as an electrochemical process. It suggested that BTI is only governed by channel vertical field. The effect of the environment and electric parameters on the interface trap generation was studied. This analytical model estimates the number of interface traps for a single stress and relaxation phase (i.e., the length of only two cycles), with the assumption of infinite oxide thickness. A numerical solution model is further used to extend it for multicycle operation. It has been shown that in comparison to DC, AC stress produces less degradation, which suggests that long term degradation depends on the nature of applied stress. This model predicts a 50% reduction in V_{TH} when the stress and relaxation time is equal and does not capture the decrease in the hydrogen concentration initially. Yang et al. [33] expand it by introducing the effect of channel lateral field which enhances NBTI effect at high drain bias potential. Kumar et al. [34] provide the multicycle analytical model for NBTI. The model exhibits that over a large period of time, the amount of trap generation is

independent of frequency. This model does not match well with experimental data, specifically in initial few seconds of recovery. This analytical modeling is developed under infinite oxide thickness assumption which is not valid in present technologies. Moreover, BTI degradation is studied under low frequency i.e., 10Hz to 10MHz, which is not valid in today's GHz systems. Vattikonda et al. [35] developed a framework in which NBTI model depends on the key process (L, V_{TH},T_{OX}) and design parameters (V_{DD},V_{ds}, duty cycle). It was also based on infinite oxide thickness. The model uses a constant δ to capture the rapid decrease in the number of interface traps. There is no analytical means provided to calculate the value of this constant. Bhardwaj et al. [36] also proposed a multicycle model that includes the finite oxide thickness effect and different H_2 diffusion rates in poly and oxide. However, the value of ξ is assumed constant which leads to unexpected results.

There are several new NBTI modeling approaches that have been proposed in recent years. Velamala [37] proposed a "hole trapping/de-trapping (TD)" based model. Grasser [38] proposed a "two-stage" model. A "parallel diffusion pass way" model is proposed by Kufluoglu [39]. Despite the debate about various theories regarding NBTI modeling, few studies [40, 41] have shown that RD model is the one which agrees with long time measurements.

At device level numerous physical models have been developed for BTI. But there is a gap between device and circuit level design. Thus, the reliability of newly designed circuit cannot be easily estimated. Analog circuits are sensitive to the device mismatch which makes the situation more critical to estimate the aging impact of device parameters on circuit parameters. Aging simulation is necessary to obtain real risk evaluation for circuit design reliability qualification. To cover this gap few work has been reported. Yan et al. [42] analyzed the impact of various aging mechanism on circuit performance of 90nm flash ADC and identified the most severe mechanism and reliability critical devices. To inject degradation, they have used physical models and did not take into account the randomness in the degradation process. Authors in [43] have developed reliability simulation framework for different analog circuits in 90nm technology node. The effect of changing voltage and temperature on failure rate have taken into account. In [44] authors have considered the effect of both variability and aging on analog circuits. They have used Monte Carlo analysis, Response Surface Model (RSM) and de-

sign of experiments for simulation framework. Similar circuit level aging simulations of the current mirror, D/A converter, comparator and operational amplifier circuits are presented in [45]. The necessity of close matching of the transistor is highlighted. NBTI alters the matching characteristics of transistors in operational amplifier which affects the output performance in comparison to time zero process variability [46].

2.1 Reliability Simulation Models

Reliability simulation methods can be classified as SPICE based and Behavioral reliability simulation methods. The SPICE based simulation uses two step simulation in which nominal simulation is followed by aging analysis. One class of circuit level reliability simulation approach are FaRBS (Failure rate based SPICE [47]) and MaCRO (Maryland circuit reliability oriented [48]). They both utilized the degradation model based on a failure circuit models and on a series of accelerated lifetime models. They used SPICE to calculate the degradation and other electric parameters of fresh and aged devices. Although these approaches provide device level degradation which further can be used to identify most sensitive devices. But they consider worst case temperature conditions rather than actual operating temperature. SPICE based simulations take a long time, especially for large circuits. In addition both methods are developed by assuming that failure rate is constant, which is not the case otherwise. Authors in [49] used a semi empirical linear prediction model to see the impact of aging on the analog circuits. This model is further improved by authors in [42], which uses quadratic lifetime prediction model. Although these models show the degradation with time but they did not consider stochastic degradation effects and separate reliability simulation is required for each process corner. For analog circuits authors in [43] used Monte Carlo loop at every lifetime point for each random sample, and further SPICE is used to obtain voltage waveforms. These waveforms are placed into the degradation model to get the degraded circuit netlist and performances. Though the method is accurate but is simulation intensive, which makes it difficult to include new data and provide less feedback for further improvement. Same authors in [44] use statistical screening to find useful circuit parameter, so the simulation time improves. Further, RSM for the time dependent behavior is built, which increases the speed. Even though the methodology

is accurate but it still requires few samples in the reduced factor space to get the degradation distribution information. Besides, RSM grows exponentially with a number of parameters and each circuit is modeled by different parameter so analysis consistency is not maintained.

Behavioral reliability simulation approach unifies nominal and aging simulations so no separate simulator is required to determine the aging degradation. At the circuit level, aging model are based on electrical circuit simulation. Here the aim is to see the change in transistor parameters and how this change translate into circuit and performance parameters. Behavioral simulations are further divided into transistor and circuit level simulations. At the circuit level the goal is to construct the behavioral model of a given circuit to visualize the design parameter degradation. VHDL-AMS, a behavioral modeling language with analog extension, is used to simulate the aging mechanism. VHDL simulator is event driven so more efficient in comparison to SPICE simulator which is node driven. Authors in [50] propose built in reliability behavioral model, based on VHDL-AMS to simulate its aging under given operating conditions. Although the method is fast but it uses a single translation factor to convert the electrical time scale to aging time scale, but in realistic scenario degradation model itself is non-linear and depends on node voltages so this translation factor should be dynamic. Authors in [51] used transistor level behavioral simulation. In this method at different time points the BSIM parameters μ_0 and V_{TH0} are updated and their values are used in the simulation of the differential amplifier. Here the transistor electrical model construction is difficult and only possible for small models.

2.2 Surrogate Modeling

The standard circuit level SPICE based reliability simulation approach can only be used when a circuit size is small or designer have sufficient time for running simulations. Reliability simulations for complex circuits require many days to weeks to complete. Hence, the quest to shorten the design cycle and to avoid the multiple iterations has led to surrogate or metamodel approach which is widely used in many technical fields. Surrogate model is a mathematical model which act as a substitute for the original model. Surrogate models provide a simpler way to understand the circuit behavior and are faster

and easier to conduct simulations. The objective of this work is to simplify the circuit level reliability simulation using the least possible amount of circuit simulations. There are many types of metamodels available in the literature which includes Artificial Neural Network (ANN), Support Vector Machines (SVM), kriging methods, polynomials, splines and gaussian process. The choice of any model depends on trade off between speed and accuracy.

Surrogate Models (SM) are used in plenty of problems and applications. In literature several works at circuit level using surrogate model is presented. For statistical wire length estimation surrogate modeling approach has been used [52]. For microwave components, an automatic multivariate mathematical modeling [53] is proposed and tested. A gaussian process based machine learning model [54] is used for the synthesis of the differential amplifier. Wen et al. [55] used a neural network to create memristor based learning synapses. Same authors in [56] have studied the passivity of a non-linear system and developed a neural network adaptive controller. To estimate the output of the operational amplifier from high level perspective neural network is [57] used. A feed forward dynamic neural network [58] is created for amplifier and mixer circuits. In [59, 60] authors have proposed standard two layers feed forward ANN to model output performance parameters of several op amp topologies. The number of the hidden layers were adjusted manually, to obtain high accuracy and generalization on training and testing data sets. A bayesian regular training [60] and hyperbolic tangent sigmoid [59] function have been used as a transfer function for all hidden layer neurons. For all output layer neurons, linear transfer function was used. Back propagation algorithm has been used to set the training pattern. The generated surrogate models can approximate the nonlinear performance characteristics of all the op amps efficiently and using less simulation time. However, to accurately replicate the behavior of the circuit, the large number of sample points are required. For a complex circuit having high dimensions, the number of sample points increases exponentially, due to grid based sampling. In our proposed work, we have developed an algorithm to choose the training samples efficiently which reduces the model development time. Also, ANN models have limited generalization ability, which results in over fitting of data. Although neural networks does not require any assumption about system behavior so are useful for a complex system. But they suffer from the problem of local minima and it is difficult to choose

the number of hidden units.

Gorissen et al. [61] compared the accuracy of kriging model using different hyper parameter optimization and sampling scheme on low noise amplifier circuit. In [62], based on the samples collected from an analytical model of LNA circuit, several surrogate models are compared. Yelten et al. [63, 64] developed kriging model of dc drain current for variability and reliability analysis. The proposed model captures the dc current response in terms of eleven parameters including process parameters, terminal voltages, temperature and device age. Although kriging model is well suited for numerical experiments and has higher performance for large scale problems but model construction time is very high. A correlation matrix of size (N x N) is required to be saved (where N is the sample size) with kriging model which increases its evaluation time. In [65] to find the design parameter in order to maximize the circuit life quadratic polynomial method is proposed. In [66] SVM surrogate model is proposed instead of expensive circuit simulations. Boolchandani et al. [67] used support vector machine (SVM) for variability analysis and design centering to enhance the yield for different analog circuits. Ciccazzo et al. [68] analyzed the behavior of SVM based surrogate model for industrial electronics circuits. SVM can be used for two types of problems i.e., Support Vector Classification (SVC) to build feasibility model and Support Vector Regression (SVR) to build performance model. ANN employs Empirical Risk Minimization (ERM) which minimizes the maximum error in training data. In contrast, SVM employs Structural Risk Minimization (SRM) which is better than ERM because it minimizes the maximum error in predicting the output. SVM has high generalization ability with larger data size. SVMs convert the regression and classification problem into an optimization problem which is solved by using the kernel. A positive definite kernel creates the optimum separating hyperplane and increases the dimensionality of the problem by solving it in this new high dimensional feature space where each data point denotes one feature and maps the solution back into original dimension space. Kernel function operates in feature space by directly calculating the inner products between all data pairs, instead of computing the coordinates which makes it computationally cheaper. SVM uses quadratic programming instead of gradient based optimization (used by ANN), to solve this problem. Simple training process, faster model generation, smaller size and ability to approximate non-linearity makes SVM a good choice to

develop the surrogate models for analog circuits.

The accuracy of the surrogate model is affected by number of samples. Every sample attribute to costly CPU simulation time. There is a trade off between sample size and accuracy of the model. Active or adaptive learning is well motivated in machine learning problems. The key concept behind adaptive learning is that a machine learning algorithm with fewer training samples can achieve a better accuracy if it is allowed to choose samples from which it learns [69]. It reduces the sample size and increases accuracy due to learner's control over training data set. Learning starts with few number of training samples, new samples are added according to the requested query maintaining the low error rate with minimum training samples. Tong et al. in [70] used active learning with SVM which is based on version space reduction for text classification. In [71], to optimize expected future error, active learning is applied. Authors in [72] proposed time domain active learning support vector regression in which active learning principle is extended to the time domain. The next sample for training data set is selected from the limited future time frame from the current point in time. The length of the time frame is limited by the computational cost associated with each additional point in the time domain. In [73] two machine learning based surrogate model (gaussian process and ANN) are constructed online to create the performance model, saving a lot of simulation time. In the online surrogate modeling, training data are generated adaptively in the optimization process. Maricau et al. [74] used uncertainty predictor $D(.)$ which is measured by the distance between the input to input, output to output and model to model. In our methodology, we have used adaptive learning to generate new training samples around maximum error sample to achieve the target accuracy of SVM model using smaller sample size. SVM models should be developed using a sufficient number of training samples. It's efficiency and accuracy also depends on efficient sampling techniques, as number of training samples affect the run time. We need to develop a model, for the desired accuracy using a minimum number of training samples. Various sampling methods such as random sampling, brute force, Latin Hypercube Sampling (LHS) have been used to generate the fixed number of training samples. The models developed using LHS sampling have shown better accuracy than other sampling methods.

Performance models are useful for visualizing the design space and can be used in place of real circuit performance response. They are built by directly approximating the

circuit performances with design variables. Performance models that facilitates accelerated analog circuit simulations should be valid in functionally correct design space. Feasibility design space identification is necessary to build final performance model as it screens out infeasible design. Feasibility models are developed to identify the feasible design space i.e., space of interest. Feasibility model is a combination of circuit specifications and circuit performances which defines the feasibility space. It is a multidimensional space in which every point representing a design, satisfies all design constraints. In [75] surrogate model based performance and feasibility models are created by using gaussian based kriging model template. Adaptive learning technique is used to generate the samples iteratively to construct the performance model. Authors in [76, 77] used SVM to create performance and feasibility model. MOS transistors in the analog circuit typically operates in the saturation region to maintain the linear output. In our work, we define saturation region of MOS transistors as a feasibility design space. Design feasibility check is again requires computationally expensive solution, hence feasibility model is approximated. The problem of representing feasibility function is treated as a classification problem for which a SVM classifier is a good candidate. Classifier helps in reducing the complexity of final regressor model by providing samples only in feasible design space. This results into lower model development time without loss in accuracy.

2.3 Long Term Model of Aging

The impact of aging on IC exists for 5 to 10 years. Thus, the short term models can not be used to evaluate the long term aging effect on IC. The need of long term model arises to predict the degradation after many cycles of operation. Such a long term model should be sensitive to the real time circuit bias conditions. Previously available models measured aging degradation for a long term by performing measurements in a short period of time under accelerated stress conditions. Further extrapolation is used to predict the lifetime degradation. In this extrapolation, the stress conditions are considered constant. That is, the internal node voltages of each device are considered to be same over the whole time interval of extrapolation. However, this is not the case and stress conditions do change during the circuit lifetime. There is a strong feedback between

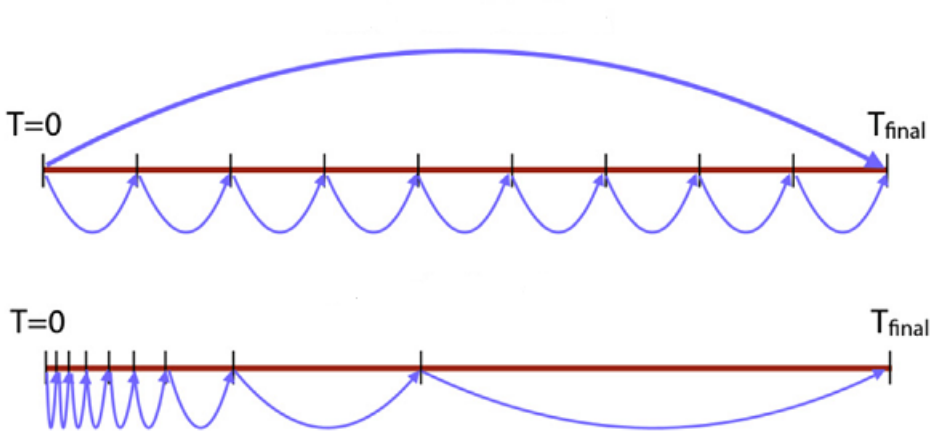


Figure 2.1: Different methods to update stress conditions: Linear Scale (above), Logarithmic Scale (below) [78]

device aging and device biasing. Thus to improve the accuracy, the number of time steps should be used to update the stress conditions through new transient simulations, by including the transistor degradation.

Toro-Frias et al. [78] made a comparison between linear and logarithmic scale as shown in Figure 2.1 with respect to CPU time and information content per step. An aging experiment is performed on ring oscillator to obtain the degraded oscillator frequency at the output. In case of logarithmic scale, maximum variation in a single step is <0.3% but in case of linear scale, the first step produces 5.5% variation in the mean frequency value. However, the total variation in both cases is 6%. This means in linear scale, the subsequent steps generate very less information about variations in the stress conditions. In the logarithmic scale, only few steps do not provide significant variation and a large number of steps produces a similar variation. Here it is shown that one linear step provides most of the information while all log steps cumulatively contributes an equal amount of information. Using one step to predict circuit degradation may cause a large inaccuracy. The error decreases by increasing the number of steps. However, the importance of each step is not the same, which may cause unnecessary waste of CPU time.

In [64] for aging simulation, entire time interval is divide into two ranges one for short and another for long term simulation. For a short term, the time period from zero to eight months is partitioned into five equal time intervals. For a long term, the time period from eight months to ten years is separated into 31 equally spaced intervals.

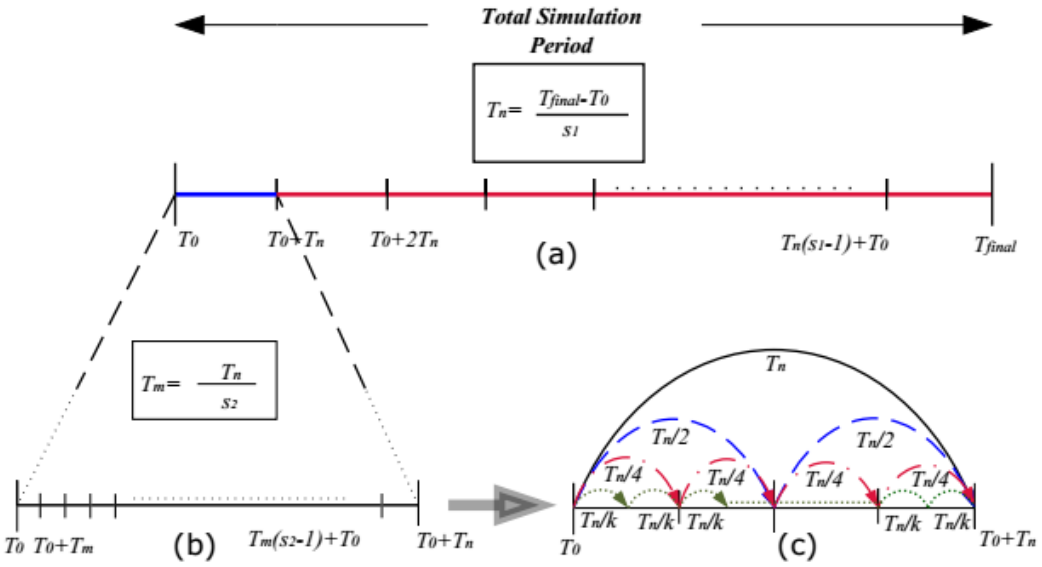


Figure 2.2: Step count determination for aging simulation [79]

However no methodology has presented about the time intervals selection.

In [79] implementation based on transistor degradation is presented rather than performances variations. It suggests dynamic step size instead of static one to improve the time efficiency of design automation tools. Aging mechanism follows the saturated power law, so maximum degradation occurs during the initial time period of usage. Therefore, the entire simulation time (T_{final}- T_0) is initially divided into equal time intervals by using certain step size (s_1) as shown in Figure 2.2(a) [79]. Then an aging simulation is processed for first time period (T_0, $T_0 + T_n$), using a large number of step size (s_2) as in Figure 2.2(b). Meanwhile, in the same first time period an aging simulation is carried out using minimum step count $s_{min} = 2$ as in Figure 2.2(c).

Then an absolute error is calculated between the two as

$$E = \sum_{i=1}^{j} |\triangle V_{TH(j.accurate)} - \triangle V_{TH(j,adaptive)}| \tag{2.3.1}$$

where j denotes the number of transistors. $\triangle V_{TH(j,accurate)}$ and $\triangle V_{TH(j,adaptive)}$ denotes the degradation amount for the former and later analysis. If (E > predefined tolerance), then later analysis is repeated by increasing the step count i.e. $s_{min} > 2$, till the (E $\leq$ predefined tolerance). At this moment the present value of the step count become the prime value to perform the complete analysis. The clarity about step size $s_1$and s_2 was not provided which can introduce inaccuracy. If $s_1$and s_2 are too less then

simulation overhead increases or vice verse. Moreover, for every time period, to find new step count is again a time consuming burden.

Eghbalkhah et al. [80] proposed aging aware simulation which considers the effect of both dynamic workload and operating temperature. Here the adaptive step size is used for aging simulations. For simulation purpose entire lifetime is divided into N time stamps. As degradation decreases with time, the length of time stamps increases; making it adaptive. The n^{th} time stamp is obtained as

$$T_n = T_{n-1} + 2n\frac{lifetime}{N(N+1)} \tag{2.3.2}$$

The Equation (2.3.2) provides the length of the n^{th} interval. It was mentioned that this equation gives minimum simulation error and reasonable simulation time, but the authors do not provide any comparison regarding this. Moreover, no proof of origin of this equation is presented.

In [5], the step size is selected by degradation of performance parameters rather than transistor degradation. Selecting new step size is based on the choice between minimum step size or an empirical formula which depend on the amount of performance change. An error is calculated as

$$\overrightarrow{\varepsilon} = \mid \frac{P^{i-1} - P^{i}}{min\,(P^{i-1}, P^{i})} \mid \tag{2.3.3}$$

The step size h is defined as

$$h = max\left(h_{min}, h_i\left[\frac{0.9\varepsilon_{max}}{max\,(\overrightarrow{\varepsilon})}\right]\right) \tag{2.3.4}$$

where h_{min} is the minimum step size and ε_{max} is the maximum tolerable error. Here the step size calculation scheme is based on degradation of performance parameter which cannot be generalized. It is a circuit dependent approach. If performance parameters are insensitive to aging effect for a particular circuit, then simulator uses large time step otherwise small which may cause inaccuracy.

Another approximation to obtain a long term model is presented in [81], where an adaptive two time evaluation scheme is used to take into account different mission profiles. A mission profile defines the effect of input signals and environmental conditions, on a system during its lifetime. The authors proposed two time simulator for time ($t + T$

), where t shows the first time and T shows the age or second time. All iterative simulations for aging are executed at increasing second times T_i. Here a time dependent function L_T is defined for a restricted time interval [0, T], whose value is used to determine the second time step. The value of this function is calculated using extrapolation which again limits its accuracy. There is no clear description provided to decide the tolerance limit to obtain the second time. Ketul et al. [82] proposed a long term model for analog circuits with feedback using constant time step. In our work, we have proposed a dynamic time step algorithm which accurately matches with minimum constant step size.

Few analytical long term models are also proposed. Bhardwaj [36] proposed RD based and Yu Cao [83] proposed TD based long term model for the digital circuits. In [84] RD and TD based long term models are developed for the digital circuit using random stress inputs. Most of these models are for digital circuit, less work is proposed in the direction of analog circuit for BTI failure mechanism. In our work, we have proposed machine learning based long term model for the analog circuits.

2.4 NBTI Compensation Techniques for SRAM

Memory circuits are more affected by aging because its transistors switch less frequently. Some works have dealt with the impact of aging on SRAM operations. Authors in [85, 86] analyzed the impact of NBTI/PBTI on SRAM cell operation and lifetime and concluded that read stability decreases with aging. Li et al. [87] applied SPICE for simulation, design and modeling of SRAM. The normalized lifetime of all transistors with failure models is calculated and concludes that NBTI mainly degrades the cell transistor speed. Kang et al. [88] provided a thorough study on reliability issues in SRAM arrays. Carlson et al. [89] investigated that minimum operating voltage (V_{MIN}) and Static Noise Margin (SNM) sensitivity increases at low voltages. Kim et al. [90] designed SRAM reliability test macro for statistical measurements of V_{MIN} degradation for different SRAM failure modes such as the SNM-limited and Time-limited. The impact of stress voltage on time of data flip was measured. All these previous works did not propose any method to compensate the aging effect.

Several approaches have been introduced to compensate the NBTI degradation. The

compensation techniques are broadly divided into three categories. a) Transistor Level b) Control Voltage Level c) Architecture Level. The focus of our work is on control voltage level techniques because they have been proven to be effective without changing the cell design. So we will discuss the previous techniques for control voltage level. The conventional approach is guard banding in which operating period or voltage is increased at design time to accommodate aging effect. In order to tolerate 10% degradation, 10% V_{DD} overhead may be required but higher V_{DD} increases the power consumption and temperature, hence increases NBTI effect [91]. Others [92, 93] addressed the issue by appropriate use of voltage scaling during active intervals using guard banding mechanism. By voltage upscaling, delay decreases which compensate the delay increased by aging. Few works [94, 95] proposed the power managed states using voltage scaling and power/ground gating at standby intervals to reduce NBTI impact. These works sacrifice energy (due to higher V_{DD}) and are more applicable to general logic circuits where aging directly affects performance, not to SRAM's where the reliability of SRAM cell is affected by aging rather than its performance. A scheduled voltage scaling [96, 97] is proposed in which operating voltage is increased slowly during operation, which allows a V_{DD} that is lower than required value by guard banding. It maintains a given error rate by applying the different voltages in different interval of time at the expense of area, power and delay. Wear rate due to NBTI is decreased directly by voltage reduction and indirectly by temperature reduction.

Singh et al. [98] proposed 6T NMOS SRAM cell, in which NBTI effected pull up PMOS transistors are replaced by NMOS transistors to compensate the aging effect. In the same circuit NMOS access transistors are replaced by PMOS transistors to improve the poor logic level at the storage nodes. Lin et al. [99] considered both NBTI and PBTI and inferred that read margin degrades and write margin improves. The impact of asymmetric degradation on SNM is also investigated. It is claimed that upscaling V_{MIN} reduces the aging effect but it is undesirable for low power applications. In [100] effect of each transistor of SRAM cell on V_{MIN} is studied and suggested that strong NMOS and weak PMOS has the highest impact. Kim et al. [101] explained SNM and Time limited V_{MIN} and shows that SNM limited V_{MIN} is more prone to NBTI and can be mitigated by controlling the word line pulse width and voltage at the cost of power and speed. In [102] various read/write circuit assist techniques are discussed to

improve V_{MIN}. These techniques includes dual V_{DD}, word line voltage lowering, read modify write, bit line and word line pulsing scheme or either changing the structure of SRAM cell (7T-10T). Authors in [103] proposed the short term cell flipping technique to compensate the aging effect. Because of the symmetric nature of SRAM cell, one of the load transistor is always stressed. It tries to make the stress probability of load transistor to 50% by flipping the content of the SRAM cell at short intervals, about 50mV V_{TH} mitigation is reported. Authors in [104] also used cell flipping technique and applied it to caches. This technique has two modes; one is normal where the original data is written to the cache and another is the flip mode, where the data is once flipped then written. The periodical cell flipping may be expensive in terms of delay due to the introduction of XOR gate in the read/write data path.

An internal node control technique is applied to limit the NBTI stress [105]. Internal node control can be inserted at the output of individual gates to force them to specific values during standby. This method imposes a timing penalty; the additional circuitry required for node control introduces a small delay. Khellah et al. [106] proposed pulsed word line and pulsed bit line techniques to improve SRAM cell failure rates at low voltages for 65nm CMOS designs. Dual supply voltage schemes were suggested to enhance the cell stability by circuit technique [107]. A column based dynamic power supply has been integrated into high frequency 70MB SRAM. These schemes utilize higher supply voltage for memory cell array and lower voltage level for peripheral blocks to improve the read margin. Authors [108] introduces self repairing SRAM which uses body bias to improve operating margin. However, this scheme does not correct the ratio of the V_{TH} values of NMOS and PMOS which is essential for SRAM operations. Authors in [109] proposed read/write assist techniques against V_{TH} variations but assist circuit requires special treatment and incur substantial design costs. Mostafa et al. [110] used adaptive body biasing circuit but at the expense of area overhead. A body bias [111] SRAM is created in which PMOS and NMOS body biases are separately controlled to maintain the operating margin at the target value by maintaining the ratio between the V_{TH} values of NMOS and PMOS. Further bit line voltage adjustment design technique is proposed to improve V_{MIN} [112] at the expense of speed and power. In our work, we have proposed a combined technique to improve the read stability.

A SRAM system consists of the cell array and its peripheral circuits which includes

read/write circuits, row/column decoders and sense amplifiers. The sense amplifier is responsible for correct data reading from the cell array. Most of the work is published on the aging affect and its compensation on SRAM cell array. Limited work has been published on the SRAM peripheral circuitry. Some authors have focused on the address decoders reliability analysis. Hamdioui et al. [113] presented the complete analysis of spot defects in SRAM address decoders. Khan et al. [114] analyzed the BTI and resistive defects impact on SRAM address decoders. Authors in [115] considered the effect of zero and run time variability on the offset voltage of sense amplifier. In [116] authors introduced a scheme based on offset distribution measurements to determine the signal margins for DRAM sense amplifier. Menchaca et al. [117] analyzed the impact of BTI on current and voltage mode sense amplifier in 32nm technology node by flipping a wrong value as a reliability metric. Agbo et al. [118] investigated the BTI impact in 45nm, 65nm and 90nm using different supply voltages on sensing delay and sensing voltage of latch type sense amplifier. Same authors [119] presented the combined effect of voltage, temperature and BTI on sensing delay of the standard latch type sense amplifier in 45nm technology node. Reliability verification is necessary in the early design phase to ensure the circuit functionality for its lifetime. A variability and reliability aware surrogate model of sensing delay of the sense amplifier is presented in our work.

Chapter 3

NBTI Aware Surrogate Model for Analog Circuit

3.1 Surrogate Model

The circuit design is a part of manufacturing process. Today's electronic circuit design requires long design cycles to calculate the circuit performances using computationally intensive transistor level simulations. The simulation time depends on the complexity of the circuit; varies from a minute to several days to complete [120]. Further, the introduction of reliability issues increases the complexity of the circuit, hence simulation time. However, these simulations should be performed quickly due to strict temporal constraints on industrial sector time to market. This motivates to speed up the circuit design phase by employing the surrogate models instead of time consuming simulations. Surrogate model or metamodel replaces the original high fidelity model or fine model by a surrogate, which is computationally cheap and accurate [121]. It increases the efficiency of the design process by enabling the rapid analysis of alternative designs, therefore reducing design cycle time and cost. These models can be applied in different phases and aspect of engineering design process like design performance analysis, design optimization, architecture simulations, multidisciplinary (Aeronautics, Chemical, Geology, etc.) analysis and optimization.

The basic idea behind developing the surrogate is to replace the high fidelity model with a less expensive approximate model [122]. Surrogate modeling is a black box modeling. The high fidelity model is represented by the functional relation

$$y = f(x) \tag{3.1.1}$$

where x is the design (input) parameter vector and y is the performance (output) parameter. The mapping in Equation (3.1.1) resides in a black box which conceals the physics behind the conversion of vector x into scalar quantity y. This black box can take the form of either physical (real) or numerical (computer) experiment. Now the surrogate model which is cost effective is expressed as

$$\hat{y} = \hat{f}(x, \alpha) \approx f(x) \tag{3.1.2}$$

Here α is an undetermined parameter vector that must be evaluated before applying the surrogate. The generic solution method is for set of inputs $x^1, x^2, \ldots, x^n$, collect the outputs $y^1, y^2, \ldots, y^n$ and find the black box mapping $\hat{f}(x)$ based on these observations.

The use of surrogate model has number of advantages

a. Less expensive

b. No modification required in analysis code

c. Can be used in variety of tools like MATLAB,

3.1.1 Surrogate Model Classification

According to the approximation strategy, surrogates can be broadly classified as [123]

1. **Black Box Approach** - In this approach only input and output of the black box are of concern. The underlying high fidelity analysis code (spice model) cannot be modified. The approximation model uses a few samples to build a less expensive model which replicates the original expensive input-output relations.

2. **Physics Based Approach** - This approach exploits the underlying code to some extent and modifies the governing equations to make them simple and computationally less expensive.

The black box approach can be classified into two main categories -

i) **Depending on the nature of unknown parameter α, can be parametric or non parametric.**

- Parametric models use initial training data set to find the unknown parameter α. Once it is done, the initial training set is no longer used to predict the response

at new points. Only the known parameters are used to make the prediction at new points. Multivariate Adaptive Regression Splines (MARS) and Polynomial Regression (PR) methods are the part of this category.

- Non parametric models use initial training data set to find the unknown parameter α and continue using the same training set to predict the response at new design points. The response at new points depends on both, all the training data set and the parameters. SVM, ANN and Kriging are the part of this category.

ii) **Depending on the technique used to build the surrogate, either regression or interpolation technique.**

- Regression models are initially designed for physical experiments (where the error is random), but further, they are used with numerical experiments (where the error is deterministic) also. In this technique, a single function is defined to incorporate all points in the training set. To account the noise an error term is added to the model. SVM, ANN, PR and MARS are the regression models.

- Interpolation models are used with numerical experiments. A simple base function (low order polynomial) interpolating the training set points, is added to another function which represents the local deviations at each point. Radial Basis Function (RBF) and Kriging are the interpolation models.

3.1.2 Surrogate Model Construction

Surrogate modeling follows [121] these steps for construction -

1. Data Generation or Sampling
2. Model Template Selection
3. Parameter Estimation
4. Model Validation

3.1.2.1 Sampling

Sampling or data generation is a key step in the obtaining robust and accurate surrogate model. A good sampling plan improves the performance of the surrogate model by

choosing samples efficiently for fitting. It considers the fact that number of samples should be limited to constrain computational expense. The samples which are used to construct the surrogate model is called training data set. The number of points or samples in the training data set increases with the degree of nonlinearity between input and output, model accuracy and the number of design parameters.

Sampling faces two conflicting targets:

a. Choosing few samples to keep the low computational cost at the expense of accuracy, as every sample attribute to expensive high fidelity simulation

b. Incorporate large training set to increase the model accuracy.

Sampling techniques are broadly classified according to two criterion [123] -

i) **According to the location of selected samples. Samples can be random, classic or in space filling fashion.**

- **Random** - Monte Carlo is the simplest random sampling plan. The samples are selected at random in the design space. The major disadvantage of the random technique is that generated samples are not space filling. There is no guarantee that generated samples belongs to the region where significant variation occurs and large region of the design space remain unexplored.

- **Classic** - This sampling plan was initially designed for physical experiments where random errors occur. But now they are also used in numerical experiments. The samples are selected from the extreme of design space. It is simple and easily implemented but not suitable for irregular design space. This technique doesn't guarantee space filling which is the preliminary requirement for numerical experiments. Additionally, the number of samples grows exponentially with number of design parameters. Full Factorial Design (FFD), Partial Factorial Design (PFD), and Face Centered Cubic (FCC) are examples of the classical technique.

- **Space Filling** - In this sampling plan all the samples tries to cover entire design space equally rather than clustering on extremes only. This approach is more suitable for numerical experiments where deterministic error occurs. This technique is more sophisticated in implementation. Latin Hypercube Sampling (LHS) and Orthogonal Arrays (OA) are the examples of space filling technique. In this work, LHS sampling plan is used.

ii) **According to the building strategy of the training set. Samples can be either generated once (one-shot) or sequentially (stage-wise).**

- **One-shot** - All samples in the training set are selected and evaluated at the beginning of the surrogate construction process, by the high fidelity code. No other samples are added during the modeling process. It is simple but less flexible and computationally expensive in designing the surrogate model.

- **Stage-wise** - In this technique new samples are continuously added iteratively to the training data set. It is more complicated but more flexible and continuously incorporates the non-linearity between input-output. Adaptive learning is the example of this technique which is used in this work.

3.1.2.2 Model Template Selection

After the sample selection, they are applied to high fidelity model for evaluation, to finally form the surrogate model. The model template selection step decides the type and complexity of the surrogate model. There are numerous choices (parametric, non-parametric, regression or interpolation) available for this purpose. Parametric models are easier to implement. Nonparametric models are good with complex input-output relations. Regression models are easier to develop and implement. The computational cost increases with complex input-output relations because more points are added to the training set and higher polynomial must be used. Interpolation models are complicated in development and implementation but are more flexible and deal better with computer experiments and complex input-output relations.

3.1.2.3 Parameter Estimation

After the appropriate template selection which is believed to simulates accurately, the parameter α, must be estimated. The concept used here is "maximum likelihood" and is applied by minimizing a suitable error fuction. In case of Gaussian error, the maximum likelihood reduces to the least square error function. There are many options available to reduce the error function.

3.1.2.4 Model validation

The last step is the model validation step that establishes the predictive capabilities of the models and estimates their accuracy or inversely the estimation error of the model. Two popular error metrics are (i) the maximum absolute error (MAE), which provides an understanding of the maximum local deviation of the model estimation from the actual output; and (ii) the root mean squared error (RMSE), which is a global error measure and provides an understanding of the model accuracy over the entire design domain.

3.2 Surrogate Modeling Flow

An automatic modeling flow is developed [124] to generate the performance model from intensive transistor level circuit simulations which is shown in Figure 3.1. Initially set of input and output parameters are defined. Then modeling strategy is configured which includes the sampling strategy (e.g., LHS and Adaptive Learning), the model template selection and error measurement technique. An accuracy target is also predefined. At the beginning of the modeling process, initial samples are generated which is called training set. Then transistor level SPICE simulations are performed on this initial training set and output performances f_i are collected at ith sample which is used to develop the model. Once the sampled data is obtained, surrogate models are constructed and validated. If the models can meet the target accuracy, then final performance model is developed which can be further used for optimization. If the desired accuracy is not achieved, then adaptive learning is evoked to add a new set of samples in the area of maximum error. This process continues till the target accuracy is achieved.

3.3 Support Vector Machine

Support vector machine as proposed by Vapnik et al. [125] is a set of supervised learning methods based on the principle of structural risk minimization. Machine learning is a learning structure from data. SVMs were initially applied for classification problems but soon after, the formulation was extended to regression problems. Support vector machines seem to offer superior generalization properties on real-life regression and classification problems. SVM exhibits excellent performance in a variety of learning

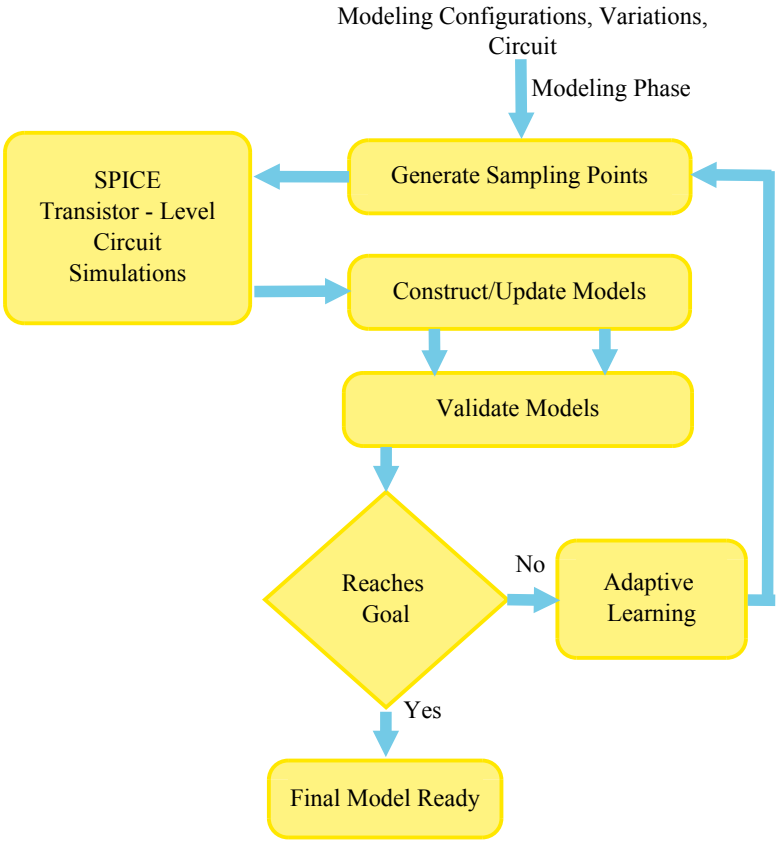


Figure 3.1: Flow of Surrogate Modeling [124]

problems, hence have generated a lot of interest in machine learning community, e.g. image analysis, bankruptcy prediction, bio-informatics problems, text categorization, interconnect modeling for microwave packaging structures, feasibility & performance modeling and design automation of analog circuits, and design of microwave antenna structures [72]. These are the black box kind of models and do not provide the equation relating the input and output parameters. SVM's has some outstanding advantages -

1. It is suitable for both linear and nonlinear data processing.
2. It has special generalization ability, especially for problems of small sample size.
3. SVM has no trouble of local minima.
4. It provides an effective way to overcome the curse of dimensionality for solving multivariate problems.
5. It performs well on data sets that have many attributes (no upper limit on number of attributes)

3.3.1 Support Vector Classifier (SVC)

An analog circuit maps a set of input design parameters to a set of performance parameters. Another type of model is considered here; a feasibility model. It is a combination of circuit specifications and circuit performances which defines the feasibility space. It is a multidimensional space in which every point representing a design, satisfies all design constraints. Performance models that facilitate accelerated analog circuit simulations should be valid in functionally correct design space. Feasibility design space identification is necessary to build final performance model as it screens out infeasible design. Design feasibility check requiers a computationally expensive solution, hence feasibility model is approximated. The problem of representing feasibility function treated as a classification problem for which a SVM classifier is a good candidate [126]. SVM is used to represent the feasibility space of analog circuits. The feasibility function is evaluated through simulations and its range defines the feasibility space of the circuit. Instances from simulations are used to train a selected model with the objective of minimizing the classification error on the training set. De Bernardinis et al. [76] used SVM to generate feasibility models for analog circuits.

For a given circuit topology, three types of constraints can be posed [127] -

Geometric constraints C_g are posed directly to the device sizes i.e., width and length. The constraints on device sizes are usually in terms of lower and upper bounds. So geometric constraints can take the form of equation

$$C_{g=}\{lb_i \leq x_i \leq ub_i, i = 1 \ldots n_g\} \tag{3.3.1}$$

where x is a design variable.

Functional constraints C_f ensures the desired functionality of the circuit. They are posed in terms of biasing voltages v and currents i in analytical form and can be represented as

$$C_f = \{\mathbf{x} : f_i(v,i) \leq 0, i = 1 \ldots n_f\} \tag{3.3.2}$$

where $\mathbf{x}$ is a vector of design variable.

Performance constraints C_p are posed on the performance parameters like gain, delay etc. and can be represented as

$$C_p = \{\mathbf{x} : f_i(p) \leq 0, i = 1 \ldots n_p\} \tag{3.3.3}$$

The feasibility space $S \subseteq R^n$ is defined as

$$S = \{\mathbf{x} : \mathbf{x} \in R^n, C\}, \quad C = C_g \cup C_f \cup C_p \tag{3.3.4}$$

A feasibility function $y(x)$ is defined which only take two values {+1,-1} depending on whether $\mathbf{x} \in S$,

$$y(x) = \left\{ \begin{array}{l} +1 \, if \, \mathbf{x} \in S \\ -1 \, if \, \mathbf{x} \notin S \end{array} \right\} \tag{3.3.5}$$

SVM is used for classification problems on (typically large) sets of data which have an unknown dependence on (possibly many) variables. Let consider each data point $x_k \in R^n, k = 1, \ldots, N$ is assigned with a label $y_k \in \{+1, -1\}$, which classifies the data into one of the two sets. Then the classifier $y(x)$ is represented by the construction of hyperplane $\omega^T . x_k + b = 0$, separating two classes by providing maximal separation of $\frac{2}{||\omega||^2}$ between points x_k belonging to the two classes. This gives rise to an optimization problem for minimum ω and b as

$$P : min_{\omega,b} \quad \frac{1}{2}\omega^T \omega \quad s.t. \quad y_k[\omega^T . x_k + b] \geq 1, \tag{3.3.6}$$

where the $\frac{1}{2}\omega^T \omega$ represents a cost function to be minimized to maximize separation. The constraints are formulated such that the nearest points x_k with labels {+1,-1} are at least $\frac{1}{||\omega||^2}$ distant from the separating hyper-plane. To solve this 'primal' minimization problem, we construct the dual maximization of Equation (3.3.6) using the Lagrangian form

$$D : \max_{\alpha} \mathscr{L}(\omega, b; , \alpha) \tag{3.3.7}$$

where

$$\mathscr{L}(\omega, b; e) = \frac{1}{2}\omega^T \omega - \sum_{k=1}^{N} \alpha_k (y_k[\omega^T x_k + b] - 1) \tag{3.3.8}$$

and α_k are the Lagrange multipliers. After applying the conditions for optimality

$$\frac{\partial \mathscr{L}}{\partial \omega} = 0, \quad \frac{\partial \mathscr{L}}{\partial b} = 0, \quad \frac{\partial \mathscr{L}}{\partial \alpha_k} = 0 \tag{3.3.9}$$

and eliminating ω by expressing it in terms of $\alpha = [\alpha_1, \ldots, \alpha_N]$, we arrive at a Quadratic Programming (QP) problem:

$$min(\alpha Q \alpha + B\alpha) \tag{3.3.10}$$

for suitably defined matrices Q, B. Having solved for α, the following classifier representation is obtained:

$$y(x) = sign\left[\sum_{k=1}^{\#SV} \alpha_k y_k x_k^T x + b\right] \tag{3.3.11}$$

where $\#SV$ represents the number of non-zero Lagrange multipliers α_k, called support values, corresponding to the input data x_k. The SVM representation will be sparse if only a few of the input data, called support vectors, are 'near' to the separating hyperplane.

A key feature of Support Vector Machines is the ability to replace the input data by a (non-linear) function $\phi(x)$ operating on the input data. This may be viewed as mapping the input data to a higher (possibly infinite) dimensional space, to enable classification of data that is not linearly separable in the original input space. To do this, we formally replace $x_k^T x$ (the dot product between a support vector x_k and any point x of the input space) in Equation (3.3.11) by $\phi(x_k)^T \phi(x)$ to represent the action of this mapping, obtaining:

$$y(x) = sign\left[\sum_{k=1}^{\#SV} \alpha_k y_k \phi(x_k)^T \phi(x) + b\right] \tag{3.3.12}$$

In the case where $\phi(.)$ is infinite-dimensional, we invoke the so-called 'kernel trick': the expression $\phi(x_k)^T \phi(x)$ may under certain conditions be replaced by a kernel function $K(x_k, x)$. As a result, one can work in high dimensional feature space without actually having to do the explicit computation in that space. Problem is formulated in the primal weight space with high dimensional feature space by applying transformation $\phi(.)$. The problem is not solved in primal weight space but the dual space of Lagrage multipliers after applying the kernel trick. So the kernel function allows the SVM rep-

resentation to be independent of the dimensionality of the input space. There are many kernel function available in the literature [128] that provide the SVM, the ability to model the complex separation hyperplanes. Here Radial Basis Function (RBF) kernel is well suited.

3.3.2 Support Vector Regression (SVR)

SVR identifies a function $f(x)$ (using support vectors that are essentially sample vectors) for all training patterns x, has a minimum deviation e from the target values y and has a minimum margin. Thus SVM convert the regression problem into an optimization problem [126]. In order to solve this optimization problem, a kernel is introduced which increases the dimensionality of the problem, solves it in this new space, and maps the solution back to the actual dimensionality of the problem. Kernels can take different forms but they should be positive definite. The optimization problem considers a linear regression between the input and output vector. The solution to this problem minimizes the magnitude of the weight vectors for a predefined level of error e. This has been achieved in a computationally efficient way using Least Squares SVM.

An enhanced version of SVM i.e., Least Squares Support Vector Machine (LS-SVM) has been proposed in [129]. The main advantage of LS-SVM is that it is computationally efficient while possess the important properties of SVM. LS-SVM uses the equality type constraints in the problem formulation, thus the solution is obtained through solving a set of linear solutions [130]. Therefore, LSSVM is free of local minima and also has low computational cost [131]. LS-SVM is efficient than classical SVM for modeling non-linear relationship between input and output parameters.

Consider a set of training data samples $\{(x_1,y_1),(x_2,y_2),.....(x_k,y_k)\} \subset R^n \times R$. where R^n denotes the input space, x_k is the input value and y_k is the the corresponding target value for k^{th} sample. By using the non-linear mapping ϕ, x_k is mapped to y_k using the following relation as follows.

$$\hat{y}(x) = \omega^T \phi(x) + b \quad with\ \omega \varepsilon R^n, b \varepsilon R \tag{3.3.13}$$

Here, $\phi(\cdot)$: $R^n \rightarrow R^{n_h}$ is the mapping of input space to some high dimensional feature space (potentially infinite). The approximation error of k^{th} sample can be given as

follows.

$$e_k = y_k - \hat{y}_k(x_k) \tag{3.3.14}$$

In LS-SVM, the minimization error is formulated as the primal problem.

$$\mathbf{P}: \quad min J_p(\omega, e) = \frac{1}{2}\omega^T\omega + \gamma\frac{1}{2}\sum_{k=0}^{N} e_k^2 \tag{3.3.15}$$

with equality constraint as follows.

$$y_k = \omega^T\phi(x_k) + b + e_k \qquad k = 1,2,3.....N \tag{3.3.16}$$

Here, γ is the regularization parameter. The first term of Equation (3.3.15) is L_2 norm on regression weights (cost function term) and determines the smoothness of the regression model. The second term represents the regression error of all samples governed by the parameter γ. This problem is nothing but ridge regression cost function formulated in feature space. When ω becomes infinite, it can not be solved. Therefore, dual problem is developed by constructing lagrangians:

$$\mathbf{D}: \quad max_\alpha \mathscr{L}(\omega, b, e, \alpha) \tag{3.3.17}$$

$$\mathscr{L} = J_p(\omega, e) - \sum_{k=1}^{N} \alpha_k \left\{\omega^T\phi(x_k) + b + e_k - y_k\right\} \tag{3.3.18}$$

Here, α_k's are the lagranges multipliers. The conditions for optimality can be given as follows.

$$\begin{cases} \frac{\partial \mathscr{L}}{\partial \omega}=0 \rightarrow \omega = \sum_{k=1}^{N} \alpha_k \phi(x_k) \\ \frac{\partial \mathscr{L}}{\partial b} = 0 \rightarrow \sum_{k=1}^{N} \alpha_k = 0 \\ \frac{\partial \mathscr{L}}{\partial e_k} = 0 \rightarrow \alpha_k = \gamma e_k, \; k = 1,2.....N \\ \frac{\partial \mathscr{L}}{\partial \alpha_k} = 0 \rightarrow \omega^T\phi(x_k) + b + e_k - y_k = 0, \; k = 1,2.....N \end{cases} \tag{3.3.19}$$

By eliminating e_k and ω through substitution, following solution can be obtained as follows

$$\begin{bmatrix} \Omega + I_N/\gamma & 1_N \\ 1_N^T & 0 \end{bmatrix} \begin{bmatrix} \alpha \\ b \end{bmatrix} = \begin{bmatrix} y \\ 0 \end{bmatrix} \tag{3.3.20}$$

Here, $\Omega = Z^T Z$ and the kernel trick can be applied within α matrix as follows.

$$\Omega_{kl} = \phi(x_k)^T \phi(x_l) \tag{3.3.21}$$

$$\Omega_{kl} = K(x_k, x_l).....k, l = 1, 2....N \tag{3.3.22}$$

The resulting function is the weighted linear combination of the inner product between the training points and testing points.

$$y_k = \sum_{k=1}^{N} \alpha_k K(x_k, x) + b \tag{3.3.23}$$

Here, $K(x_k, x)$ is the kernel function and α_k and b are the solutions of the linear systems. For a function to be kernel function, it should be positive definite and must satisfy the Mercer condition for the problem to be convex to provide unique and optimum solution.

3.4 Reliability Simulator

As transistor aging effects have an ever increasing impact on circuit performance, circuit reliability simulator is another essential part of a modern design flow. One of the first reliability simulation tool BERT is developed by UC Berkely [132] (Tu. et al. 1993). This tool is basically used to measure the impact of HCI. The toolset is written around SPICE and follow these simulation steps to get the aging effect on circuit -

1. The fresh circuit is simulated and current and voltage waveforms are stored which effect the device degradation.

2. These waveforms are further used to generate degraded device models for each device.

3. Second SPICE simulation is run with aged device models to obtain degraded circuit performances.

The major disadvantage is that entire aging calculation occurs after the SPICE simulation and therefore requires extra time. Also, SPICE simulation needs to store the waveforms on every node in the circuit requiring memory and this slow down the SPICE

simulation itself. To overcome these issues Parthasarathy et al. [133] proposed integrated reliability simulation. In this case, reliability simulation is done simultaneously with transistor simulation. Aging of each transistor is calculated at each transient step while calculating operating points. Therefore simulator does not need to store all internal voltages and hence no extra SPICE simulation and time required to calculate circuit degradation. At the end of the SPICE simulation, the degradation is extrapolated to the desired lifetime. The circuit is evaluated again to extract the aged circuit performance.

Commercial reliability simulators, Eldo (by Mentor Graphics, 2001), RelXpert (by Cadence, 2003), and MOSRA HSPICE (by Synopsys, 2008) come with an integrated reliability analysis. These tools are intended to provide information about circuit performance shifts due to gradual transistor aging effects. Abrupt effects such as dielectric breakdown are therefore not supported. Eldo is capable of determining the degraded device parameters iteratively. In Eldo specified lifetime is divided into n time intervals (of equal length). The steps one and two are conducted in every time interval. This way the impact of the degraded waveforms on the circuit parameters are considered. RelXpert can consider the impact of HCI and NBTI. RelXpert also uses the iterative approach in which a large number of iterations are often needed to obtain the accurate modeling results. The simulator can calculate and output the degradation results to predict the lifetime of each MOSFET within a circuit. The main advantages of these Eldo and RelXpert are the accuracy and SPICE compatibility. However, their degradation equations are proprietary. Hence, the user has to trust the tool and cannot verify how the degradation is calculated. They put a burden on the product designers to correctly extract the device's degraded parameters, and an inaccurate extrapolation may lead to nonphysical trends, which limits their popularity in the reliability design process. Synopsis MOS Reliability Analysis (MOSRA) is a reliability simulator included in HSPICE, can consider both the HCI and NBTI effect. It uses the custom models developed by device modeling teams within a company. This tool also has compact models for both HCI and NBTI effect. Both models are fairly accurate when compared to the aging models offered by Eldo or Cadence. The BTI model includes a term for the partial recovery effect that is essential for BTI. To simulate the effect of NBTI an efficient simulation analysis and an accurate aging model is required. An aging model translates the amount of electrical stress into device parameter degradation. NBTI is

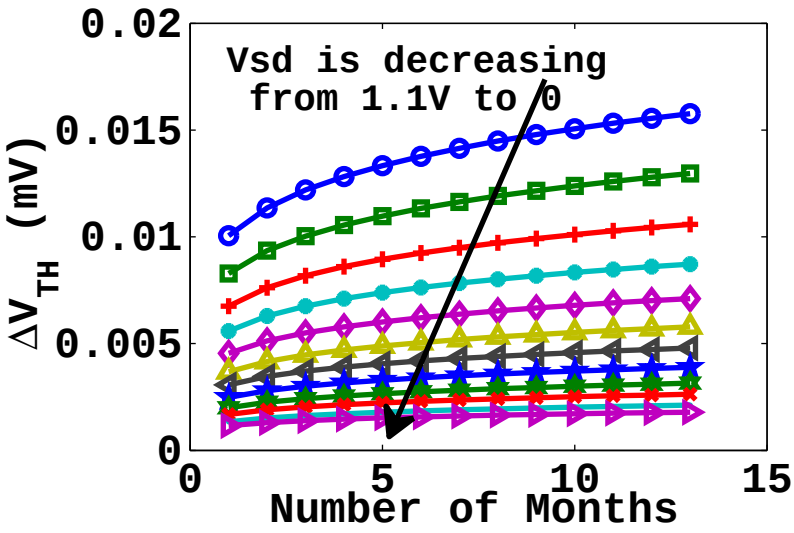


Figure 3.2: Effect of change in V_{ds} on V_{TH}

primarily the function of Time (T), Gate to Source Voltage (V_{gs}) and Drain to Source Voltage (V_{ds}). It is visible from Figure 3.2 that for fixed V_{gs} , how V_{TH} is changing over time for different Source to Drain (V_{sd}) values. It can be seen that by changing the drain bias, initial threshold voltage also changes due to drain induced barrier lowering (DIBL) effect [134]. Moreover in analog circuit change in V_{TH}, effects the node voltages which tends to change in V_{gs} and V_{ds}, which further changes V_{TH}. So a proper model is required to incorporate the effect of these changes. In this context, MOSRA reliability simulator integrated with HSPICE is used for aging simulations.

3.4.1 MOSFET Reliability Analysis (MOSRA) Reliability Simulator

MOSRA model is a function of device operating conditions (i.e., voltages, currents, and temperatures) as well as device geometries. These models are constructed with physics-based formulations and augmented with coefficient parameters, to improve the model accuracy and parameter extraction flexibility.

Here using the MOSRA model framework [135], change in V_{TH} in case of static BTI is given by Equation (3.4.1) & Equation (3.4.2)

$$\triangle V_{TH,IT} \sim \exp\left(-\frac{TITTD}{K.T}\right).\left[\frac{\varepsilon}{t_{OX}}(V_{gs}-V_{TH})\right]^{TITCE} \tag{3.4.1}$$

$$.\exp[TITFD.E_{OX}(V_{gs},V_{ds})].t^{NIT}$$

$$\triangle V_{TH,OT} \sim \exp\left[-\frac{TOTFD+\frac{TOTTD}{T}}{E_{OX}(V_{gs},V_{ds})}\right].t^{NOT} \tag{3.4.2}$$

Here Equation (3.4.1) is related to the contribution of interface traps and Equation (3.4.2) is related to the traps inside the dielectric layer. TITTD represents the equivalent activation energy associated with the interface traps contribution. TITCE models the inversion charge dependence of the interface traps contribution. TITFD is the electric field dependence coefficient of the interface traps contribution. TOTFD and TOTTD account for the electric field and temperature dependence of the dielectric traps contribution. NIT and NOT represent the stress time exponents of the interface and dielectric traps degradations, respectively.

Here $E_{OX}(V_{gs}, V_{ds})$ is the strength of the electric field of the dielectrics. It is given by Equation (3.4.3)

$$E_{OX}(V_{gs},V_{ds}) = \frac{V_{GS}-V_{TH}-TOTDD.V_{ds}^{TOTDE}}{t_{OX}} \tag{3.4.3}$$

The TOTDD and TOTDE parameters account for the V_{ds} dependence of the electric field.

In case of Dynamic BTI partial recovery effect occurs so change in V_{TH} become smaller and is given by Equation (3.4.4)

$$\triangle V_{TH,AC} = TTD0.\triangle V_{TH,DC}.\exp(TDCD.g_1(V,t)).g_2(f) \tag{3.4.4}$$

Here $\triangle V_{TH,DC}$ is the threshold voltage degradation under constant stress. TTD0 is the recovery model coefficient. TDCD is a parameter of the duty cycle dependence. $g_1(V,t)$ is a function of bias and time which represents a measure of the duty cycle of the waveform applied to the device during the transient simulation. $g_2(f)$ represents the dependence on the frequency of the waveform.

MOSRA Flow

MOSRA simulation flow is developed based on one single unified engine between aging computation and non-aging normal simulations, hence a seamless analysis flow.

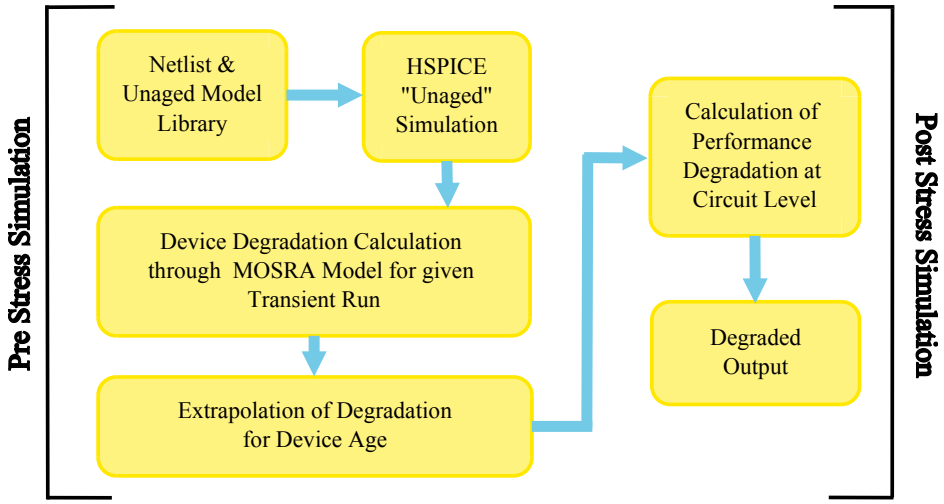


Figure 3.3: The MOSRA Flow [135]

The MOSRA flow consists of two phases: the pre-stress simulation phase and the post-stress simulation phase as shown in Figure 3.3. The two simulation phases can be executed either in the same simulator run or independently, as needed. In this work, NBTI model has been implemented using MOSRA flow in HSPICE simulator.

1. **Pre Stress Simulation** - In this fresh simulation phase, degradation of user defined MOSFET's are calculated. This degradation from the MOSRA equation is integrated over a user defined time interval, for the given transient analysis run time. This result is then extrapolated for user defined age (time of circuit operation). Then the total amount of electrical stress is converted into device performance degradation in two ways. a) Stress results converted into the degradation of model parameters (e.g., threshold voltage, mobility, etc.) which contribute to the degradation of device characteristics. b) Stress results directly converted into the degradation of device characteristics (e.g., direct degradation of the drain current).

2. **Post Stress Simulation** - Here a second simulation runs, and degradation of each device is combined, translating into the degradation of circuit performance. For example change in the voltage gain of differential amplifier. At each MOSRA circuit operation time step the flow considers the accumulated degradation information from previous time steps. As a result, the accumulated stress effect is taken into account implicitly, with no need for empirical "equation bending".

3.5 SVM Sample Selection Method

Sample selection method is based on two perspectives: the total number and the distribution of samples. The SVM models should be developed with minimum number of training samples to reduce the runtime of models. Equation (3.3.23) is used to evaluate the value of unknown samples. The number of α_k values are directly proportional to the number of training samples. These α_k values affect the computations required to evaluate the newly generated samples (i.e., other than training data). The adaptive learning method is used to generate new samples based on the error between the developed model with small training data-set and SPICE output. Initially we construct a very rough surrogate model and then improve it adaptively by generating new samples in the area of maximum error, which is driven by target accuracy. There are two conflicts arises here [73] -

1. The number of samples in the training data set should be very small for an initial surrogate model. As the number of samples grows, the accuracy of the surrogate models improves, but model complexity and development time also increases.

2. The entire design space should be covered as much as possible, because too sparse samples lead to less information about some area and initially no information of the exact response is available. Hence, the reliability of surrogate model will be poor.

To make a good trade off, LHS sampling is used. The LHS employs fewer samples to achieve more effective sampling, hence samples the design space uniformly. In our proposed framework, we have combined both LHS sampling and Adaptive Learning method to explore the design space in a guided manner [136]. We start training with fewer samples (LHS) and only generate two samples (Adaptive Learning) around maximum error sample to add them to previous training data.

3.5.1 Latin Hypercube Sampling

Latin Hypercube Sampling is a "space filling" design. It is developed by McKay [137]. It provides more evenly distributed sampling points and more accurate function estimation in the whole design space than random sampling. It is important to control the

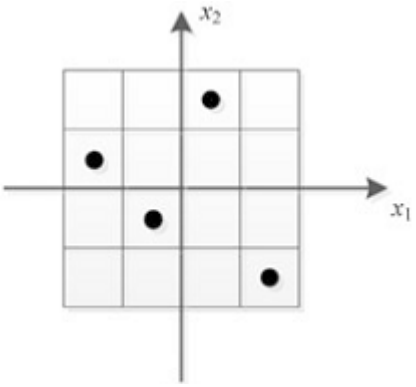


Figure 3.4: LHS sampling for $n = 2$ design parameter and $N = 4$ samples [137]

density of sample points so that the corresponding amount of evaluations is affordable and still maintain the good distribution in design space. A latin hypercube is a matrix of p rows and k columns. In two dimensional space, LHS enforces only one sample in each column and each row [138]. In higher dimensional space, the range of each design parameter is divided into required number of non-overlapping equiprobable intervals. In each interval of each design parameter, only single sample is allowed. This benefits most design space utilization because duplicate points can be avoided. If N samples need to be generated then each design parameter is divided into N equiprobable regions, each with a probability $1/N$. Then N different values are selected for each design parameter (one for each interval). This divides the n-dimensional design space into N^n cells (square) with a probability $1/N^n$ each [124]. Figure 3.4 shows an example of LHS sampling for $n = 2$ design parameters and $N = 4$ samples.

3.5.2 Adaptive Learning

Adaptive learning or query learning is a subfield of machine learning [139]. The key idea behind adaptive learning is that machine learning algorithm can achieve greater accuracy with fewer training data if it is allowed to choose the data from which it learns [69]. The adaptive learning sample selection algorithm minimizes the number of function evaluations and limit the expensive aging simulations. Algorithm 3.1 generates samples adaptively in the design space. This algorithm takes initial training data generated through LHS and provides the final training data set [72]. In our work SVM models are validated by finding the correlation coefficients. Correlation coefficient $(Corr)$ provides the measure of the strength of the linear relationship between actual and estimated

output. It's value ranges between 0 to 1, where low value represents no linear relationship and high value depicts the exact linear relationship. If $Corr_{est}$ of the initially trained model is greater than the target value $Corr_{final}$, then algorithm stops. Otherwise adaptive learning algorithm is activated which efficiently generates the training samples. These samples are added to initial training data set to improve the *Corr* between SPICE output $Y_{TEST,SPICE}$ and SVM output $Y_{TEST,SVM}$.

In order to generate new samples first, those samples need to be identified which provide error higher than the required value Err_{req}. Error related to every sample is calculated using equation

$$Err_{sample} = |Y_{TEST,SPICE} - Y_{TEST,SVM}|^2 \tag{3.5.1}$$

Instead of taking one sample at a time all samples which have $Err_{sample} > Err_{req}$ are used to guide the path for new samples through adaptive learning. This process improves the model development time and within two or three iterations target accuracy is achieved. Equation (3.5.1) automatically takes care of generation of samples in empty area of the input space and distance between estimated and actual output rather than taking two different functions for both purposes as in [74].

The initial input training set $X_{TRAIN,INITIAL}$ is obtained from LHS sampling. Transistor level SPICE simulations are used to evaluate the samples $Y_{TRAIN,INITIAL}$ for corresponding input set. Then the initial surrogate model is trained and tested (Line 1-2). The SVM model test output $Y_{TEST,SVM}$ is obtained for input testing data set X_{TEST} (Line 2). Then rough estimate of the accuracy is obtained by finding the *Corr* between actual testing data output $Y_{TEST,SPICE}$ (SPICE output corresponds to X_{TEST}) and $Y_{TEST,SVM}$ (Line 3). If estimated correlation coefficient $Corr_{est}$ is less than the desired $Corr_{final}$, then those error samples X_{ERROR} are identified which gives the error Err_{sample} greater than the required error Err_{req} (Line 7-9). All the n samples which have error greater than the Err_{req} will lead the path for new samples. Then adaptive learning is used to generate the fresh samples around these n (maximum length of X_{ERROR}) samples and stored in $X_{ADAPTIVE}$ (Line 11). By using SPICE simulations fresh output training samples $Y_{ADAPTIVE}$ are obtained corresponding to $X_{ADAPTIVE}$ (Line 12). These new input and output samples are added to initial training set to obtain the final training set $(X_{TRAIN,FINAL}, Y_{TRAIN,FINAL})$ (Line 13-14). Then the surrogate model is trained and

tested again and accuracy is compared (Line 17-21). This process continues till the desirable accuracy is achieved (Line 8). Adaptive learning ensures the final surrogate model with a fewer number of samples which reduces model run time.

Algorithm 3.1 Adaptive Learning Algorithm

Input : $(X_{TRAIN,INITIAL}, Y_{TRAIN,INITIAl}, RBF\ Kernel)$
Output : $(X_{TRAIN,FINAL}, Y_{TARIN,FINAL})$
1. **TRAIN_LSSVM** $(X_{TRAIN,INITIAL}, Y_{TRAIN,INITIAL}, RBF\ Kernel)$
2. $Y_{TEST,SVM} \leftarrow$ **TEST_LSSVM** (X_{TEST})
3. $Corr_{est} \leftarrow Corr\,(Y_{TEST,SPICE}, Y_{TEST,SVM})$
4. **if** $(Corr_{est} > Corr_{final})$
5. **then stop**
6. **else**
7. $Err_{sample} \leftarrow |Y_{TEST,SPICE} - Y_{TEST,SVM}|^2$
8. **while** $(Corr_{est} < Corr_{final})$
9. $X_{ERROR} \leftarrow$ Separate n samples for which $Err_{sample} > Err_{req}$
10. **for** 1: n
11. $X_{ADAPTIVE} \leftarrow$ Generate fresh samples around every sample of X_{ERROR}
12. $Y_{ADAPTIVE} \leftarrow$ **SIMULATE_SPICE** $(X_{ADAPTIVE})$
13. $X_{TRAIN,FINAL} \leftarrow (X_{TRAIN,INITIAL}, X_{ADAPTIVE})$
14. $Y_{TRAIN,FINAL} \leftarrow (Y_{TRAIN,INITIAL}, Y_{ADAPTIVE})$
15. **end**
16. **TRAIN_LSSVM** $(X_{TRAIN,FINAL}, Y_{TRAIN,FINAl}, RBF\ Kernel)$
17. $Y_{TEST,SVM} \leftarrow$ **TEST_LSSVM** (X_{TEST})
18. $Corr_{est} \leftarrow Corr\,(Y_{TEST,SPICE}, Y_{TEST,SVM})$
19. $Err_{sample} \leftarrow |Y_{TEST,SPICE} - Y_{TEST,SVM}|^2$
20. $X_{TRAIN,INITIAL} \leftarrow X_{TRAIN,FINAL}$
21. $Y_{TRAIN,INITIAL} \leftarrow Y_{TRAIN,FINAL}$
22. **end**

3.6 Proposed Work

The scope of this work is first to identify the feasible design space for an analog circuit using SVM Classifier and second, to develop SVM Regression model which would be fast and accurate as HSPICE. Models used for transistors are BSIM PTM (Predictive Technology Model) models in 45nm technology. The differential amplifier circuit as shown in Figure 3.5, is chosen to illustrate the effect of aging. Table 3.1 shows the related input parameters along with their nominal values. LS-SVM toolbox interfaced with MATLAB is used to develop both feasibility model and performance model.

Aging is a time dependent phenomenon so Time (T) is taken as one of the input parameter. As analog cells are very sensitive to channel length (L) variations, so it

is kept fixed. Channel width (W) is taken as another input parameter which can be further optimized to increase the yield. A known instance of all the input parameters is considered as a tuple. Hence (W,T) forms the input tuple which is represented as $X_i = f(W_p, W_n, T)$. Here W_p is a channel width of PMOS transistor and W_n is a channel width of NMOS transistor. Values of these input parameters are generated initially through LHS sampling within upper and lower bound to obtain a set of tuples. Time is varied between 0 to 10 years. W_p is varied in the range of $[1\mu, 80\mu]$ and W_n in the range of $[1\mu, 20\mu]$.

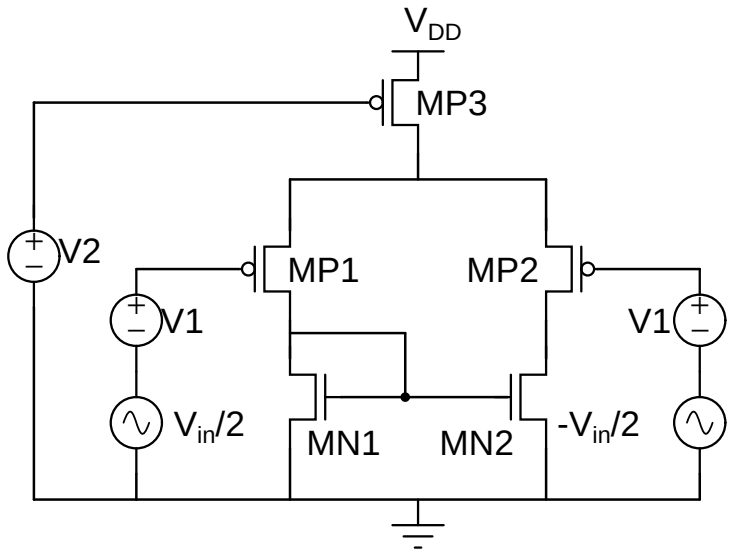


Figure 3.5: The Differential Amplifier

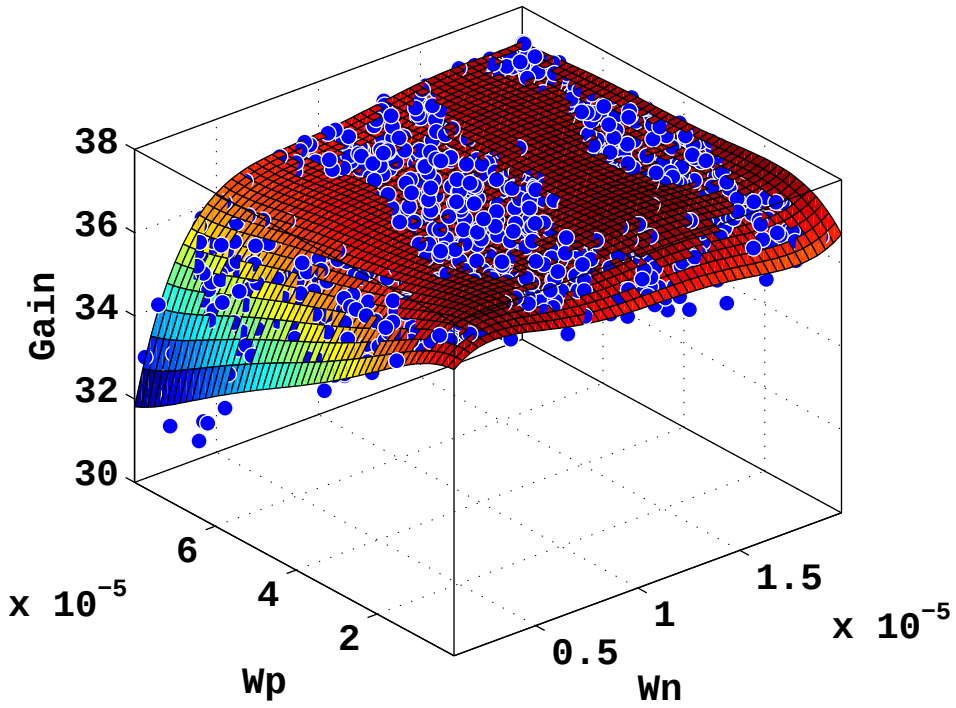
Table 3.1: Nominal Values of Input Parameters

Voltage Name	Voltage Value
V_1	0.4 V
V_2	0.56 V
V_{in}	20 mV
V_{dd}	1 V

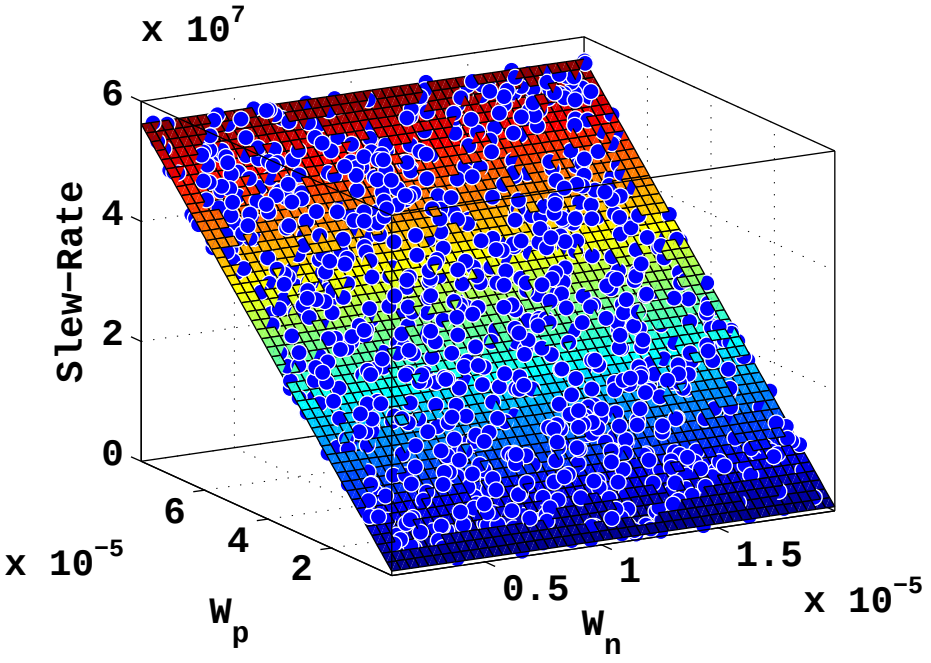
Device	W/L ($\frac{\mu m}{\mu m}$)
MN1	10/0.1
MN2	10/0.1
MP1	40/0.2
MP2	40/0.2
MP3	40/0.2

Miscellaneous	Values
V_{TH} (PMOS) at zero bias	-0.4118V
Temperature	27°C
Oxide Thickness	1.45nm

Variation of performance parameters with W is shown in Figure 3.6. Figure 3.7 shows the effect of NBTI on gain and slew-rate at nominal input parameters. Degradation in performance parameters due to NBTI are topology and biasing dependent. High fidelity is attained by using data from SPICE circuit simulations to fit the model, for predefined accuracy target.

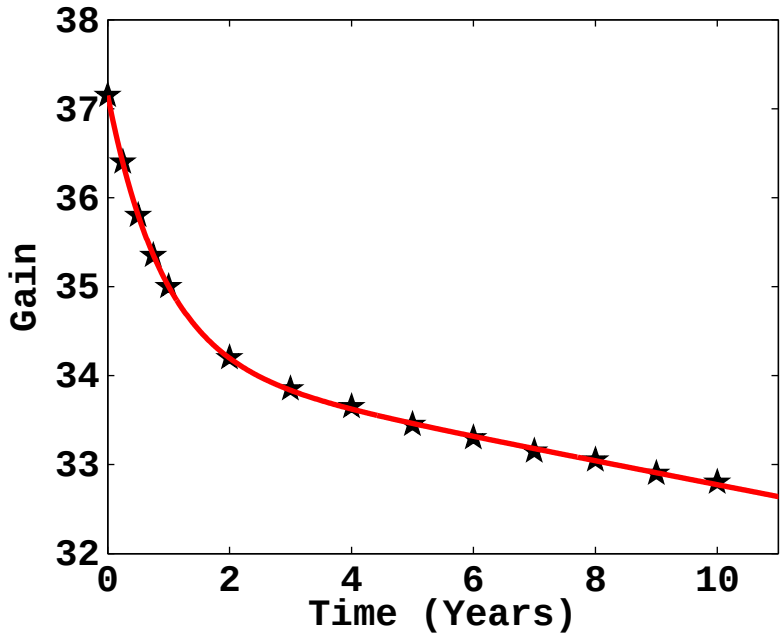


(a)

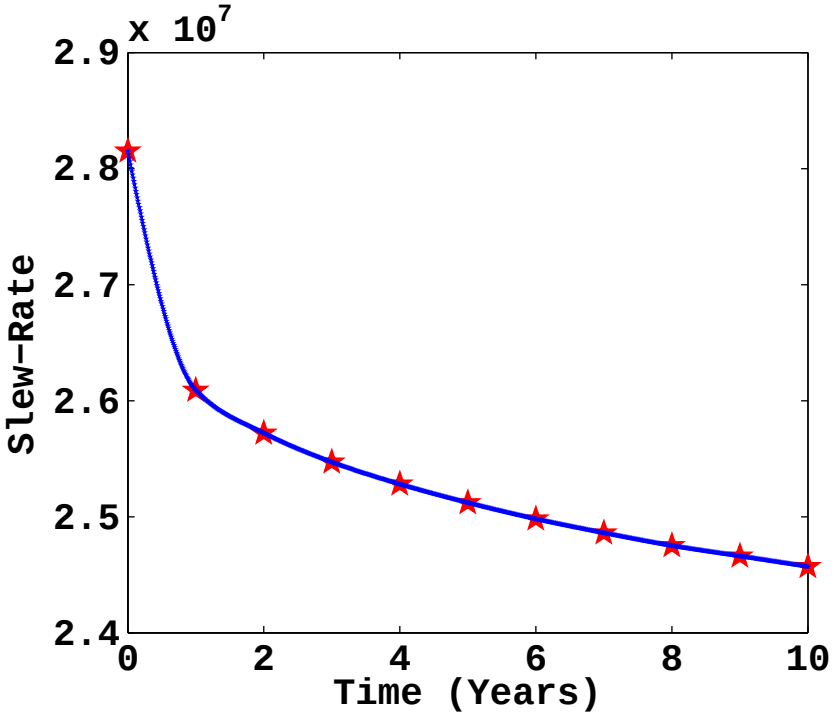


(b)

Figure 3.6: (a) Variation of Gain with Width (b) Variation of Slew-Rate with Width



(a)



(b)

Figure 3.7: (a) Variation of Gain with Time (b) Variation of Slew-Rate with Time

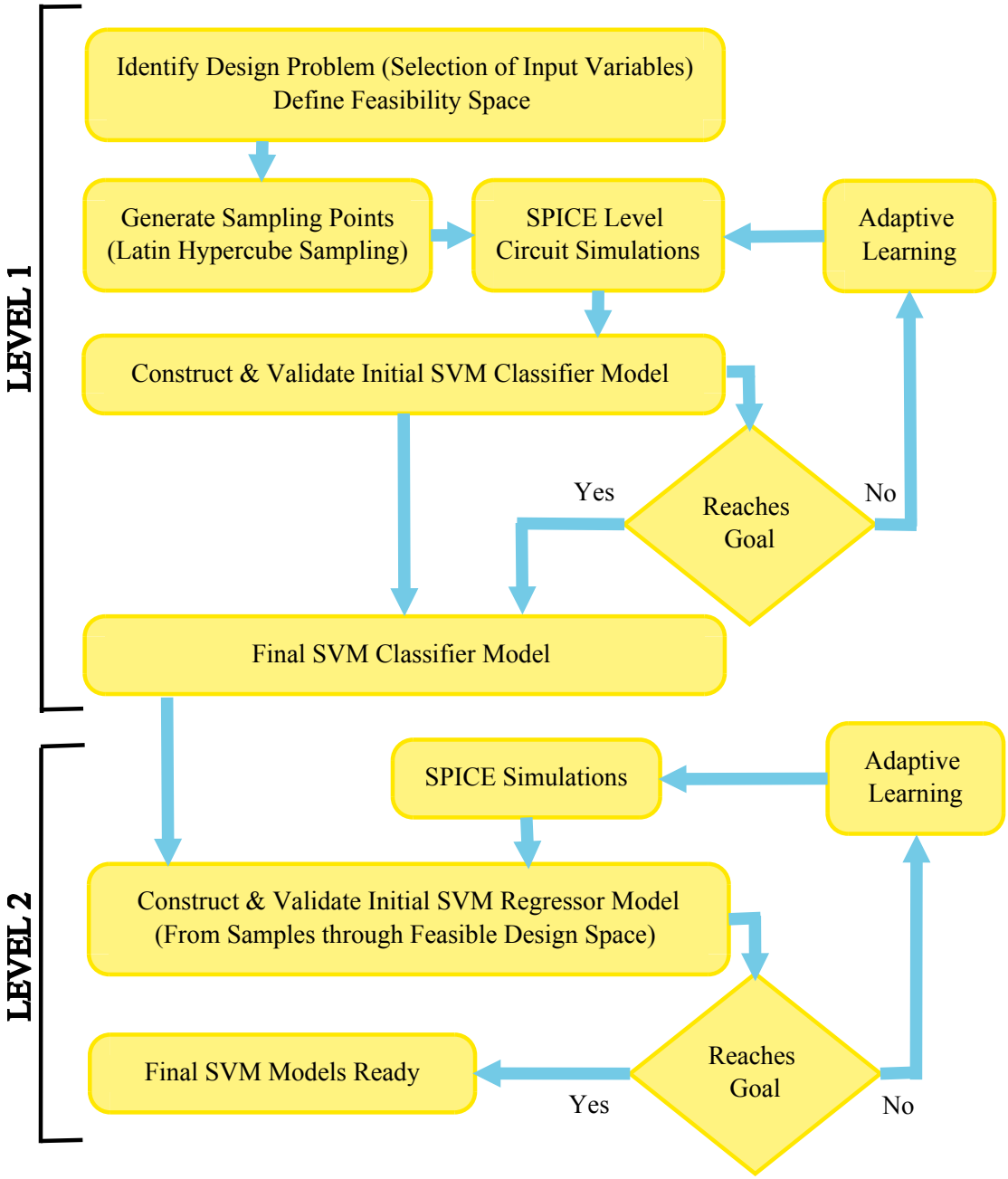


Figure 3.8: Flowchart of Proposed Methodology

Figure 3.8 shows the methodology to develop a reliability aware SVM model. We divide complete flow into two levels. In level 1, we initially identify the design problem, specify the variables of input sample vector and define feasibility space. Next, we generate input samples in the specified range through LHS sampling. LHS covers entire design space with less number of samples. Then circuit simulations are performed through HSPICE to generate performance data P_i for the ith sample. Feasibility constraints are verified using HSPICE simulations. Here F_i is a feasible design space, where all transistors of the circuit under test remains in saturation. For the given set of input tuples which satisfies feasibility constraints, their corresponding output is taken as 1 otherwise -1. Finally, SVM classifier is constructed. The output of this classifier contains only those input tuples which falls within feasible design space F_i. Classifier helps in reducing the complexity of final regressor model by providing samples only in feasible design space. This results in less simulation time of the model without loss in accuracy. In level 2, output of classifier is applied to train SVM regression model. Data sets which are used to train the models are termed as training data sets. Other data sets called testing data sets are used to validate the models by checking its accuracy. At both levels, accuracy of the models is validated by finding correlation coefficient between estimated output and actual output. At both levels we start model's training with less number of samples, build initial surrogate model and check the accuracy. If the models are accurate enough, they can be used for design purpose. Otherwise at both levels, adaptive learning section 3.5.2 scheme would be used to improve the accuracy of the model. A number of SPICE files, PERL scripts and MATLAB files are run to obtain the complete flow of simulation.

3.7 Results

Here SVM based surrogate model is developed for 45nm technology node. Initially, 5600 input tuples are generated through LHS sampling within the specified range. HSPICE is run for these 5600 input tuples and corresponding output performance parameters are obtained. Initially, 1000 training samples are used to develop the feasibility model, which is increased to 1118 samples by adaptive learning. 4600 testing samples are used to check the accuracy of the model. Feasibility constraints are verified using

Table 3.2: Correlation Coefficient and Model Development Time for Performance Model of Gain and Slew Rate

	Performance Parameter	Without Adaptive Learning	With Adaptive Learning
Correlation Coefficient	Gain	0.912	0.9979
	Slew-Rate	0.954	0.9997
Model Development Time	Gain	0.2292 s	708.11 s
	Slew-Rate	0.1315 s	185.04 s

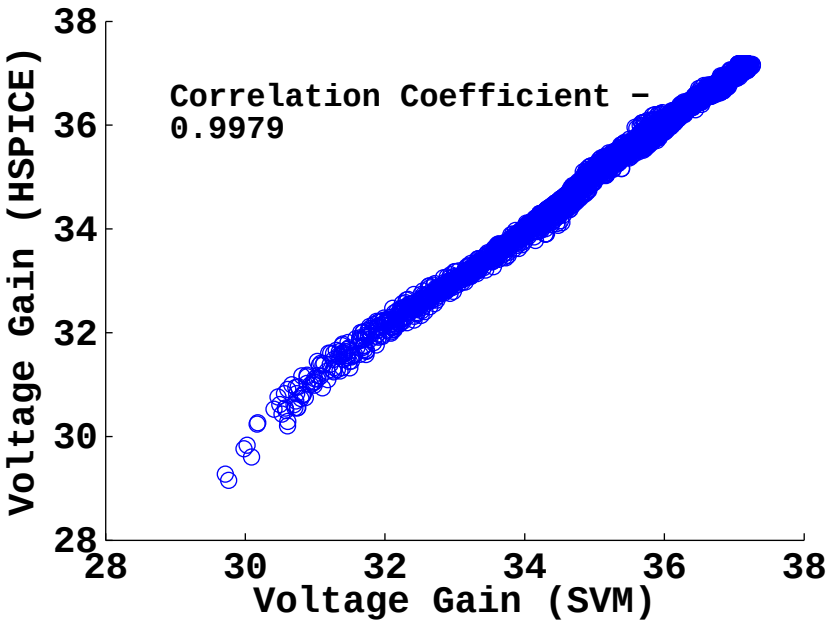
HSPICE simulation from which 3788 input tuples falls in feasible design space. Correlation coefficient obtained for classifier are 0.9730 and 0.9969 before and after adaptive learning respectively.

The output of the classifier is further used to develop SVM regression model for gain and slew-rate of the differential amplifier. For gain initially, 1500 training samples and 2288 testing samples are used to develop the performance model which results in low correlation coefficient. Then with adaptive learning, initially 300 training samples are taken to train the regression model, which is increased to 950 samples. 3488 testing samples are used to check the accuracy of the model. For slew-rate initially, 1000 training samples and 3438 testing samples are used to develop the performance model which results into low correlation coefficient. Then with adaptive learning, initially 550 training samples are taken which is increased to 700 samples. 3888 testing samples are used to check the accuracy of the model. Overall model development time and values of correlation coefficient for both performance models are shown in Table 3.2. It seems that due to adaptive learning, model generation time is higher but it is one time process per circuit per performance parameter.

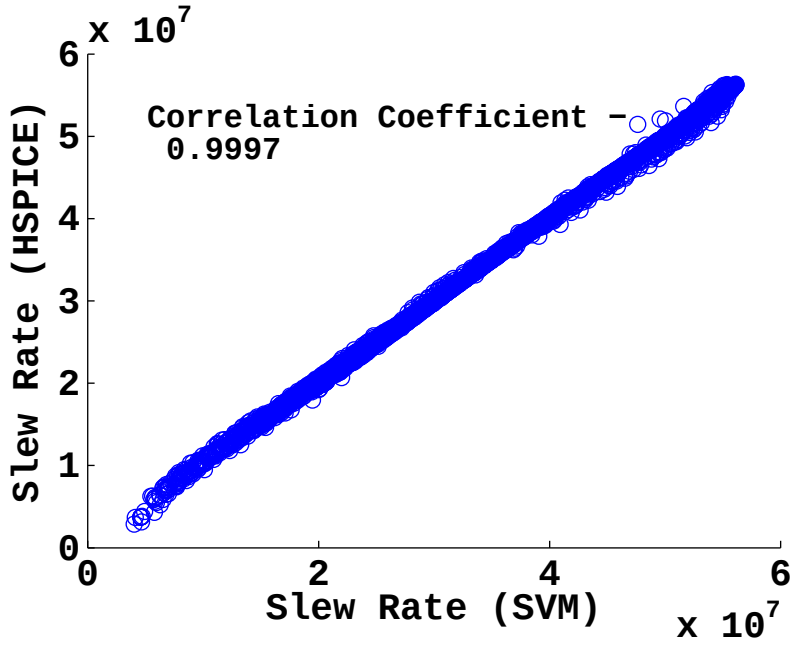
Correlation curves are shown in Figure 3.9, produced between HSPICE (actual output $Y_{TEST,SPICE}$) and SVM (estimated output $Y_{TEST,SVM}$) model. These curves are quite linear, shows that our SVM model finely matches with HSPICE output. Correlation curves also depicts that due to the effect of NBTI and width variation, gain ranges from 29.7 to 37.4 and slew-rate ranges from 5 V/μs to 55 V/μs. Table 3.3 shows the comparison of the run time of performance models for single sample, with and without adaptive learning. In [64] a single drain current evaluation of complete circuit using kriging surrogate model requires 2s using binary search method. So our method outperforms the existing methodology.

Table 3.3: Comparison of Run Time of Performance Models

Performance Parameter	#Training Samples without & with Adaptive Learning	Run Time without & with Adaptive Learning
Gain	1500 / 950	0.066 ms / 0.046 ms
Slew-Rate	1000 / 700	0.051 ms / 0.03 ms



(a)



(b)

Figure 3.9: Correlation Curves between SVM and HSPICE (a) Gain (b) Slew-Rate

3.8 Summary

In this chapter, a circuit level NBTI aware SVM based feasibility and performance model are developed for an analog circuit. Feasibility modeling is formulated as classification problem while performance modeling is formulated as regression problem. The effect of NBTI on the differential amplifier is simulated. Gain and slew-rate degrade within given range of time and width, which shows that aging poses the major concern in 45nm technology. Feasibility model is developed to initially identify feasible design space, which reduces the simulation time for performance model. Performance model for gain and slew-rate are then developed in feasible design space. A sampling scheme that includes LHS and adaptive learning is used, to develop the surrogate model. It is shown that accuracy and run time of performance models improve by using adaptive learning using less number of samples. Though it increases model development time but it is one time process which can be tolerated. Once the model is developed it would be fast and accurate too. A single performance parameter evaluation of complete circuit requires 0.046ms and 0.3ms for gain and slew rate respectively which shows major improvement over the previous methodology. The accuracy of these models is compared with actual HSPICE results through correlation coefficient. The values of correlation coefficient are 0.9979 and 0.9997 for gain and slew rate respectively, which shows that our models are highly accurate.

Chapter 4

NBTI Aware Machine Learning Based Long Term Surrogate Model for Analog Circuit

Aging phenomenon is not only the function of temperature and applied bias voltage at the gate terminal of the transistor, but also dependent on the voltages at the source and drain terminals. Most of the previous works focus on AC stress in terms of a square wave, but this is not the case in an analog circuit where stress is mostly sinusoidal. In digital circuits, internal node voltages either remain at 0 or V_{DD}. Thus, stress voltage at any node of the logic gate does not get affected by BTI induced V_{TH} shift. In the case of analog circuit, each transistor remains either in linear or saturation region. Therefore V_{TH} shift affects the internal node voltages which alter the V_{gs} and V_{ds} that further change the V_{TH} values and eventually forms the closed loop positive feedback between internal node voltages and V_{TH}. In analog circuits, each transistor faces a different level of stress. Therefore associated internal node voltages and degradation level is also different. These internal node voltages are also the function of temperature and device design parameter (e.g., Channel Width)[140]. Analog circuits like current mirror or differential pair, have matched PMOS transistors which are sensitive to V_{TH}, β and I_D matching [28]. Thus BTI could be a disastrous mechanism for these devices. Performance parameter like gain is also a function of width [141]. Channel width is also an important parameter for sizing [142] of the analog circuits. Therefore it is necessary to consider the changes in internal node voltages and width.

4.1 Effect of real time operating conditions

BTI induced aging phenomenon is greatly influenced by circuit real time operating conditions i.e., change in internal node voltages. This temporal shift in operating conditions is affected by the operating temperature, device geometry and supply voltage which dynamically changes the aging rate and further the performance parameters. The result of applied stress in BTI can be modeled on a circuit in two ways:

1. **Transistor Level** - In terms of change in MOSFET model parameters (mobility, threshold voltage, trans conductance)

2. **Circuit Level** - In terms of change in circuit performance parameters (gain, offset voltage, drain current, bandwidth)

The first approach which is more accurate but complex, leads to calculation of V_{TH}, μ and g_m degradation which in turn degrades the circuit performance parameters i.e., gain. Though the second approach is more simple but less accurate as it does not include the several internal effects (e.g., node voltages, thermal profile, bias runaway), which aggravates aging phenomenon.

The change in absolute value of threshold voltage (ΔV_{TH}) due to BTI is a function of

$$\Delta V_{TH} = f(Time, Temperature, Node Voltages) \tag{4.1.1}$$

where node voltages are given by

$$Node Voltages = (Drain Voltage\,(V_D), Gate Voltage\,(V_G), Source Voltage\,(V_S)) \tag{4.1.2}$$

The common source amplifier circuit shown in the Figure 4.1, is used to show the effect of internal node voltages on transistor as well as circuit level parameters. By applying the MOSRA model on this circuit, ΔV_{TH} degradation is calculated for one year.

Figure 4.2 shows the effect of internal node voltages i.e., V_{gs} and V_{ds} on the degradation of $\triangle V_{TH}$ on both PMOS transistors. It exhibits that in the presence of real time operating conditions $\triangle V_{TH}$ suffers more. Aging is a stochastic process. The breaking of $Si-H$ bond happens with a certain probability, which translates in a distribution of the

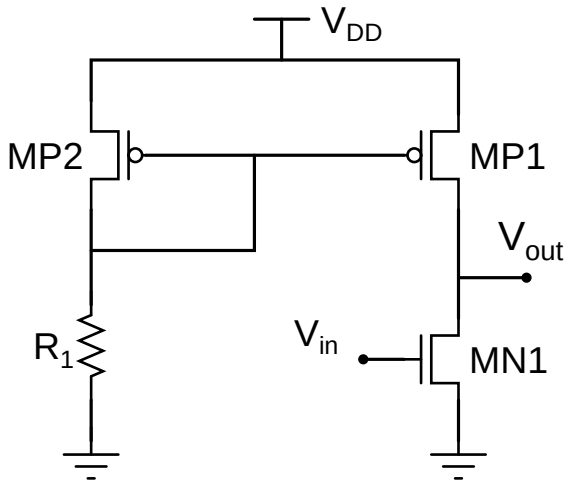


Figure 4.1: The Common Source Amplifier

threshold voltage drift. Hence, two matched transistors which are stressed identically do not have the same threshold voltage drift. Moreover, every transistor plays a different role to impact the circuit output. Thus it is required to calculate the degradation of every effected transistor in the circuit. Figure 4.3 shows the degradation of both PMOS transistor, which indicates that MP1 degrades more than MP2 for same conditions.

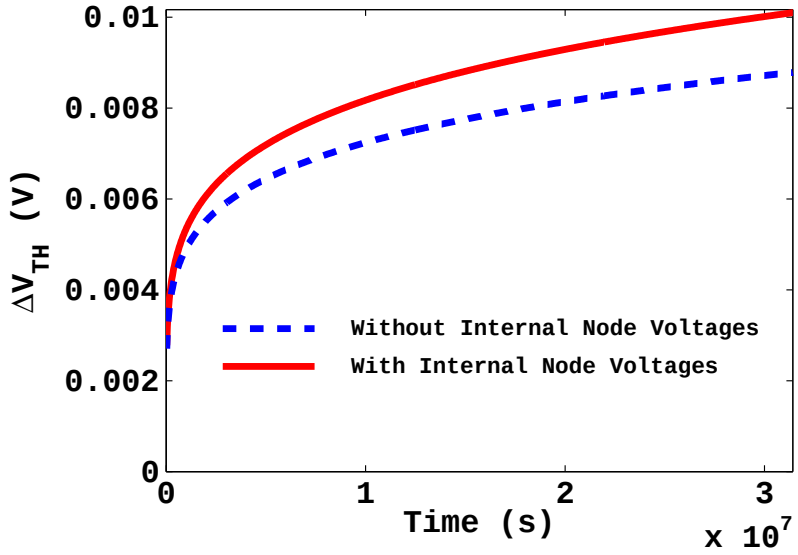
The positive feedback loop between the V_{TH} and internal node voltages results in more degradation of circuit performance parameters e.g., gain of the common source amplifier which is shown in the Figure 4.4.

Thus, it is necessary first to develop a transistor level model which can reflect the changes of BTI on key model parameters, simultaneously including real time operating conditions. Second is to develop a model from transistor level to circuit level for incorporation of changes in model parameters on performance parameters.

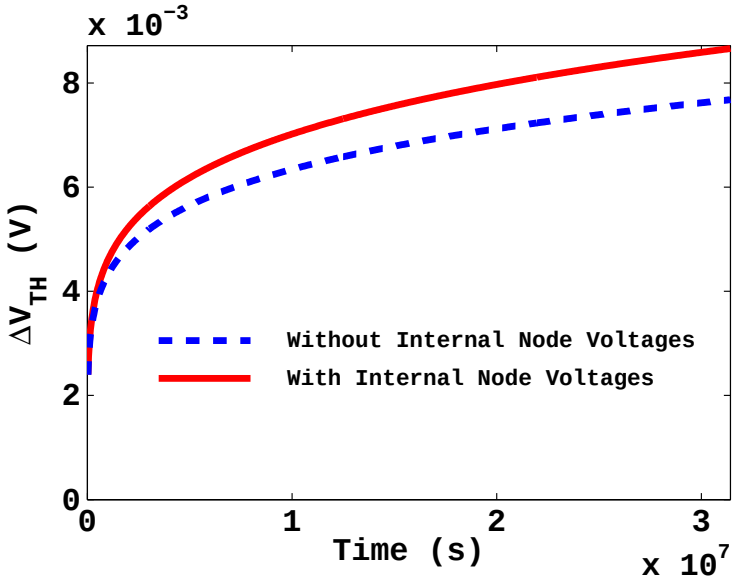
4.2 Need to develop an accurate long term model

The impact of aging on IC remain for a long term e.g., 5 years or more. Thus, the short term models have limited usage in design practice. The need of long term model arises to predict the degradation after many cycles of operation. In order to develop an accurate aging model at the circuit level, the major challenge is time dependency of operating points of the circuit, which modulate the electrical stress voltage of each transistor. Previously available models estimated aging degradation for a long term by performing measurements in a short period of time under accelerated stress conditions. Further,

extrapolation is used to predict the lifetime degradation. In this extrapolation, the stress conditions are considered constant. That is, the internal node voltages of each device are considered to be same over the whole time interval of extrapolation. However, this is not the case and stress conditions do change during the circuit lifetime. There is a strong feedback between device aging and device biasing. Thus the calculation of the long term degradation in a single step results in incorrect value of model as well as performance parameters.



(a)



(b)

Figure 4.2: Effect of real time operating conditions on $\triangle V_{TH}$ degradation (a) MP1(b) MP2

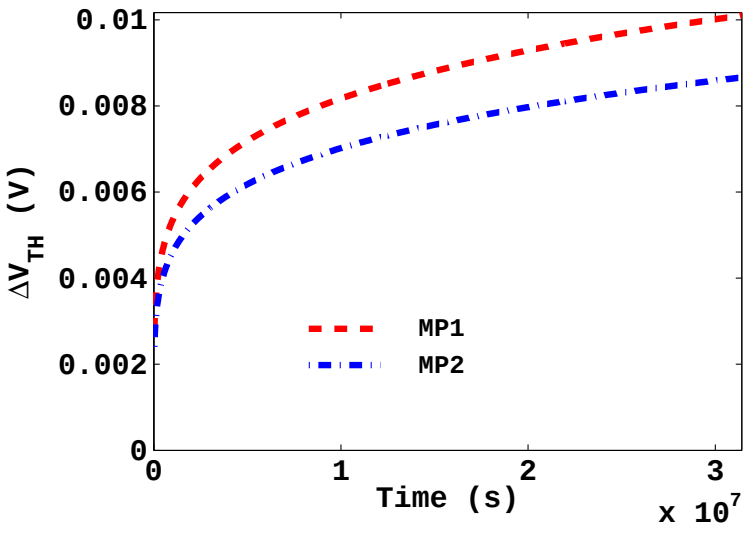


Figure 4.3: Comparison of $\triangle V_{TH}$ degradation of both PMOS transistors while including internal node voltages

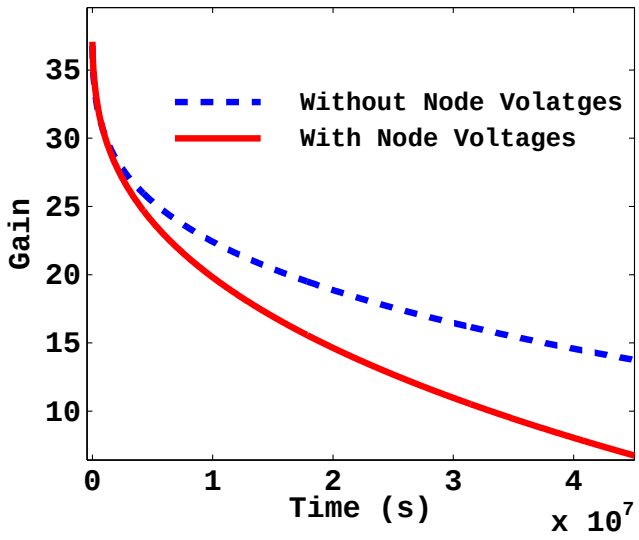


Figure 4.4: Effect of internal node voltages on performance parameter i.e. Gain

Total simulation time should be divided in the number of time steps, to update the stress conditions through new transient simulations, at the end of each step. Hence, change in electrical stress on each transistor should be taken into account periodically, to calculate the actual shift in key model parameters for the next time step. In [84] RD and TD based long term model for both analog and digital circuit have been proposed that can handle random stress. These models do not include real time operating conditions which leads to inaccurate V_{TH} extraction. Furthermore, extrapolation causes any small

amount of modeling error to be amplified, which results in significant error in the final long term model. Authors in [83] proposed a long term model for both analog and digital circuits. It uses constant time step to include the effect of real time operating conditions for a given lifespan (0 to lifetime), which may require more number of simulations to be performed by transistor level simulator (SPICE). Authors in [45, 143] used logarithmic time step to improve the simulation speed. Degradation due to aging is faster in the initial life cycle and become slower as time span increases. In logarithmic case, size of each time step (step size) remains constant across all states (worst case degradation) and circuits. The distance between two time steps is termed as step size. A step size is an important parameter to find an accurate degradation. This work proposes an algorithm to find an accurate time step, to develop a long term model. This work also presents a long term V_{TH} degradation model for analog circuits, which obviates the need of calculation of V_{TH} degradation in every cycle of given transient run, further for the lifetime. This causes the reduction in simulation time to calculate exact V_{TH} degradation in each cycle. In order to combine BTI induced degradation in circuit simulation, several reliability simulators have been proposed. These simulators used the SPICE simulations to calculate the aging effect. In [49, 144] SPICE simulation based DC operating point analysis has been performed to calculate the degradation of digital circuit only. For analog circuit, this analysis is not sufficient and hence provides very less information about aging degradation. SPICE simulations are computationally expensive with large memory requirements and only feasible for small circuit designs. Thus for large scale design in order to reduce simulation complexity the surrogate model is a good choice. In this work, NBTI aware long term surrogate model has been developed by using SVM.

4.3 Proposed Algorithm to calculate The Dynamic Time Step

4.3.1 Motivation to develop algorithm

For long term aging analysis previous simulation tools used either constant or logarithmic time steps, which led to inefficiency and more pessimist results. In case of constant step, smaller step size increases the simulation time, hence reduces efficiency while

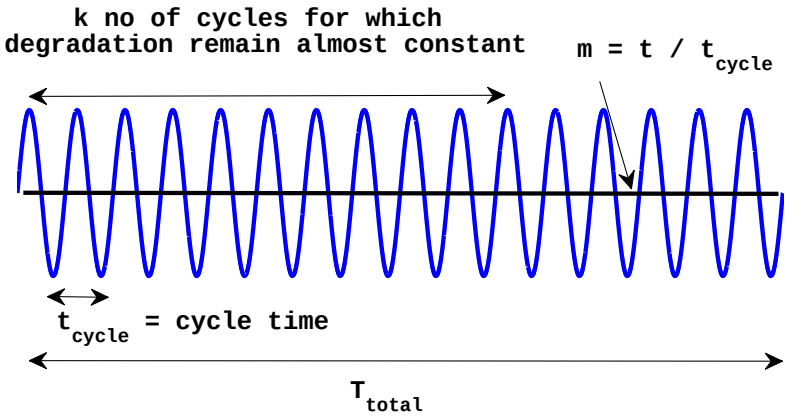


Figure 4.5: Idea used in Algorithm

larger step size enhances prediction error. In case of logarithmic steps, same step size has been used across all circuits and conditions (including worst case) which results in inaccurate results. Thus step size plays an important role, to update real time operating conditions for accurate aging analysis.

4.3.2 Idea behind algorithm

BTI causes degradation in electrical parameter V_{TH} with time. This change in threshold voltage (ΔV_{TH}) is finally converted into the degradation of performance parameter. In order to predict the long term threshold voltage degradation due to BTI at a time t, $m = t/t_{cycle}$ cycles need to be simulated. The value of m can be enormous even for $t = 1$ month, which makes impractical solution in order to predict ΔV_{TH}. It is important to note that the value of (ΔV_{TH}) almost remain constant (insignificant change) for the numerous number of cycles for e.g., k , which reduces the need to calculate $\triangle V_{TH}$ in every cycle of a transient run as shown in Figure 4.5. This insignificant change in model (device) parameter (for those k cycles) affects very less on performance (circuit) parameter. Hence produces very less information in those k cycles. To reduce the value of m and overall simulation time, this k number of cycles can be skipped during every ΔV_{TH} calculation. Moreover, updated node voltage values can also be included after every k cycles to get more accurate V_{TH} degradation.

4.3.3 Proposed Algorithm

In previous work of long term aging simulation, entire lifetime is divided into a certain number of time steps. At the end of each step, partial simulations are performed to calculate V_{TH} degradation and other electric stress. These captured values are used to calculate the parameter shift for the next step. These time steps are either constant or logarithmic. In this section, an algorithm is proposed which uses dynamic time step to calculate the electric stress on the device. The flow of the proposed algorithm is shown in Figure 4.6. This algorithm uses reverse approach to find dynamic time step. Instead of calculating V_{TH} degradation at particular time step (constant/logarithmic), it finds a time instance (in terms of k number of cycles) to obtain a particular ΔV_{TH}. Input to the algorithm is given in the form of ΔV_{TH} which is called *key*. For simulation, the entire lifetime is divided in different *keys* (ΔV_{TH}). The value of every *key* is found by the proposed algorithm in terms of k number of cycles. The value of ΔV_{TH} between two *keys* changes very less (insignificant). The value of *keys* ranges from 0.1mV to 10mV with a *key_step* which ranges from 0.1mV to 1mV. *Key_step* is used to modulate the value of *key*. Its value is kept less for initial one year as degradation mostly occurs in this period so that variation in electric stress at every node can be included more often.

Algorithm 4.1 provides a code of skipping k cycles in order to reduce overall simulation time while including node voltages effect. In this algorithm, *key* represents the value of current ΔV_{TH}. For a given *key*, the algorithm tries to find the k cycles for which this value remain almost constant. The value of maximum time limit by which each iteration of algorithm iterates is given by *max_limit_cross*, that also varies dynamically with every *key*. As V_{TH} degradation follows the power law with time, degradation is faster in initial time cycles and slower for the later time cycles. Thus we have obtained equation between time and $\triangle V_{TH}$ for *max_limit_cross* with the help of curve fitting method ($max\_limit\_cross = f(\Delta V_{TH} = current\,key)$. *Time_step* is the time added to the current time in order to search the current *key*. Value of *time_step* is also chosen adaptively. For lower *keys*, *time_step* is $1ms$ which is increased to $1000s$ for higher *keys* values. This increases the simulation speed.

$LEFT$ and $RIGHT$ show the lower and upper limit of the time, which is the search space for a particular *key*. We have calculated absolute error termed as ABS_{ERR}, which is the difference between the current *key* and ΔV_{TH} ($ABS_{ERR} = |key - \Delta V_{TH}|$). We have

used a variable *err* to track the ABS_{ERR}. The value of *err* has been varied from 10^{-7} to 10^{-3} with a multiplication factor of 10. If ABS_{ERR} is lesser than the *err*, then algorithm terminates the current iteration ($iter$) and the maximum value of k has been found which is denoted by T_F. Otherwise $LEFT$, $RIGHT$, *err* and $iter$ are updated for the current *key* value. After finding the value of dynamic time step for current *key*, the *err* is set to the initial value and *key* is updated to the next value. The algorithm terminates whenever the maximum value of *key* reaches which is denoted by *key_max*. At nominal values the DC stress is applied for 5 years on the circuit shown in Figure 4.1 and value of maximum V_{TH} degradation is obtained to get the value of *key_max*.

4.4 BTI Aware Long Term Surrogate Model

4.4.1 Analysis Flow

The aim of this work, is to develop the NBTI aware long term SVM regression model for analog circuits. Predictive Technology Model (PTM) in 32nm is used for all simulations. A simulation flow is developed to include the effect of reliability to evaluate the effected circuit performance during the transient analysis of the circuit. Further, the proposed algorithm has also incorporated in the flow to include the effect of real time operating conditions at particular time step, which finally affect the circuit performance parameter. The entire simulation uses the different number of SPICE, MATLAB and PERL Scripting Files. The complete simulation methodology requires two types of information - (a) To invoke the simulation (b) To run the simulation.

- To invoke the simulation method, two sets of parameters are required that affect internal node voltages.

1. The first set includes different width samples for PMOS transistor (10% variation in nominal width) which are generated by LHS sampling. LHS [63] covers entire design space with less number of samples.

2. The second set includes the value of *key*s (ΔV_{TH}) which are used in the proposed algorithm to find the value of dynamic time step where the effect of internal node voltages should be included.

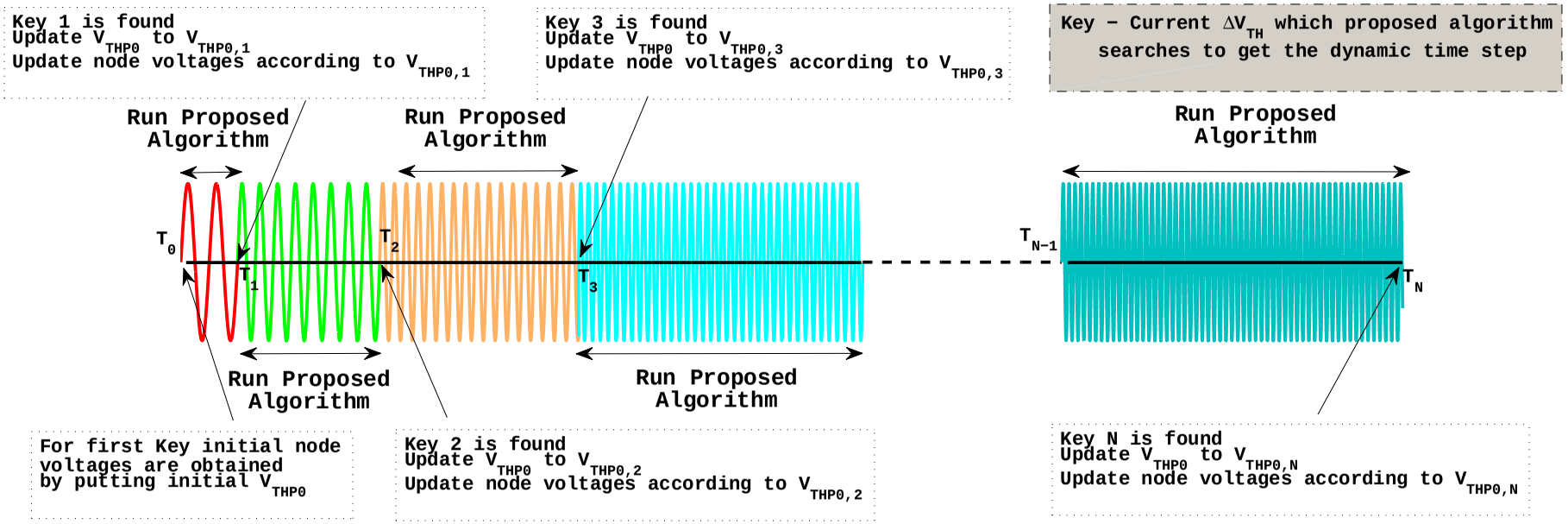


Figure 4.6: Flow of the Proposed Algorithm

Algorithm 4.1 Proposed Algorithm to find Dynamic Time Step while including change in node voltages

Input:
key_max = Last ΔV_{TH} which need to find
N_V = Node Voltages
Proposed_Algorithm(*key_step*, *key_max*, N_V)
Initialization
$iter$ = 0 (Time iteration variable)
$err = 10^{-7}$
K_F = 0 (Key found flag)
T_F= Time Found (Dynamic Time Step, Initial Value = $0.1ms$)
key = Current ΔV_{TH} (Initial Value = $0.1mV$)
T_S = *time_step* (Time added to current time)
key_step = Amount by which ΔV_{TH} need to be increased
max_limit_cross = Maximum limit of time for current *key*

1. ***while*** ($key <= key\_max$) // Termination condition for Algorithm
   (a) LEFT=T_F , $K_F = 0$, $max\_limit\_cross = f(\Delta V_{TH} = current\,key)$
   (b) ***while*** ($(err \leq 10^{-3})$ && $(K_F == 0)$)
      i. ***while*** $((K_F == 0)$ && $(iter \leq max\_limit\_cross))$
         A. $(RIGHT, T) = Updation(LEFT, RIGHT, T_S)$; // Update $RIGHT$ and T
         B. ΔV_{TH}= $CalculateThresholdVoltage(T, N_V)$; // Calculate ΔV_{TH} using T and N_V
         C. $ABS_{ERR} = (|\Delta V_{TH} - key|)$
         D. ***if*** $(ABS_{ERR} < err)$ // Termination condition for a particular *key*
            - $T_F = T$, K_F = 1; // Maximum value of k has been found, given by T_F
         E. ***else if*** $(\Delta V_{TH} < key)$ // Time not found
            - $LEFT = T + T_S$;
         F. ***else*** // Time not found
            - $RIGHT = T$;
         G. ***end***
         H. $iter = iter + T_S$; // Increment in iteration with *time_step*
      ii. ***end***
      iii. $err = err \times 10$;
   (c) end
   (d) *key*=*key*+ *key_step*
   (e) $err = 10^{-7}$
2. ***end***

Function $Updation(LEFT, RIGHT, T_S)$

$RIGHT = LEFT + T_S$

$T = \frac{LEFT+RIGHT}{2}$

Return $(RIGHT, T)$

- To run the simulation method, three types of data are required which gives the

value of circuit performance parameter including the effect of reliability in real time operating mode.

1. Definition of the circuit which is defined by the netlist, where PMOS transistors (in case of NBTI) are selected for reliability analysis.

2. Definition of test bench which performs the required transient analysis for a corresponding width and ΔV_{TH} to obtain the internal node voltages related to each transistor and the value of circuit performance parameter.

3. Definition of the proposed algorithm which is used to find that how many time cycles need to be skipped corresponds to particular ΔV_{TH} to improve the simulation time while including node voltages effect.

Methodology to develop long term model is shown in Figure 4.7. First the single width sample, initial V_{TH} and *key* (from section 4.3.3) are read from the input file and automatically replaced in SPICE and model files. Then an automatic script starts to run the file for transient analysis and two output files are created. *Nodes_Profile* file contains the information about the node voltages of each transistor which is further used in the proposed algorithm to calculate the degradation at a particular time. *Performance_Parameter* file stores the degraded value of circuit performance parameter i.e., gain for corresponding width and V_{TH} value by including the node voltages effect. Then the proposed algorithm is run that takes input from a *Nodes_Profile* file and calculate the number of time cycles which need to be skipped for a particular ΔV_{TH}.

A long term model has been developed for 5 years. For a single width sample, the entire process is repeated for every updated *key* and continues till the *key_max* reaches. This whole process is repeated for every sample of width to develop the final SVM regression model.

4.4.2 Long Term Models

The value of width (W), gain (G), ΔV_{TH} and corresponding dynamic time step are used to develop initial SVM model. To develop SVM model with less number of samples initially SVM is trained with few samples. Samples which are used to train the model are called training samples. For testing purpose, another set of samples has been used

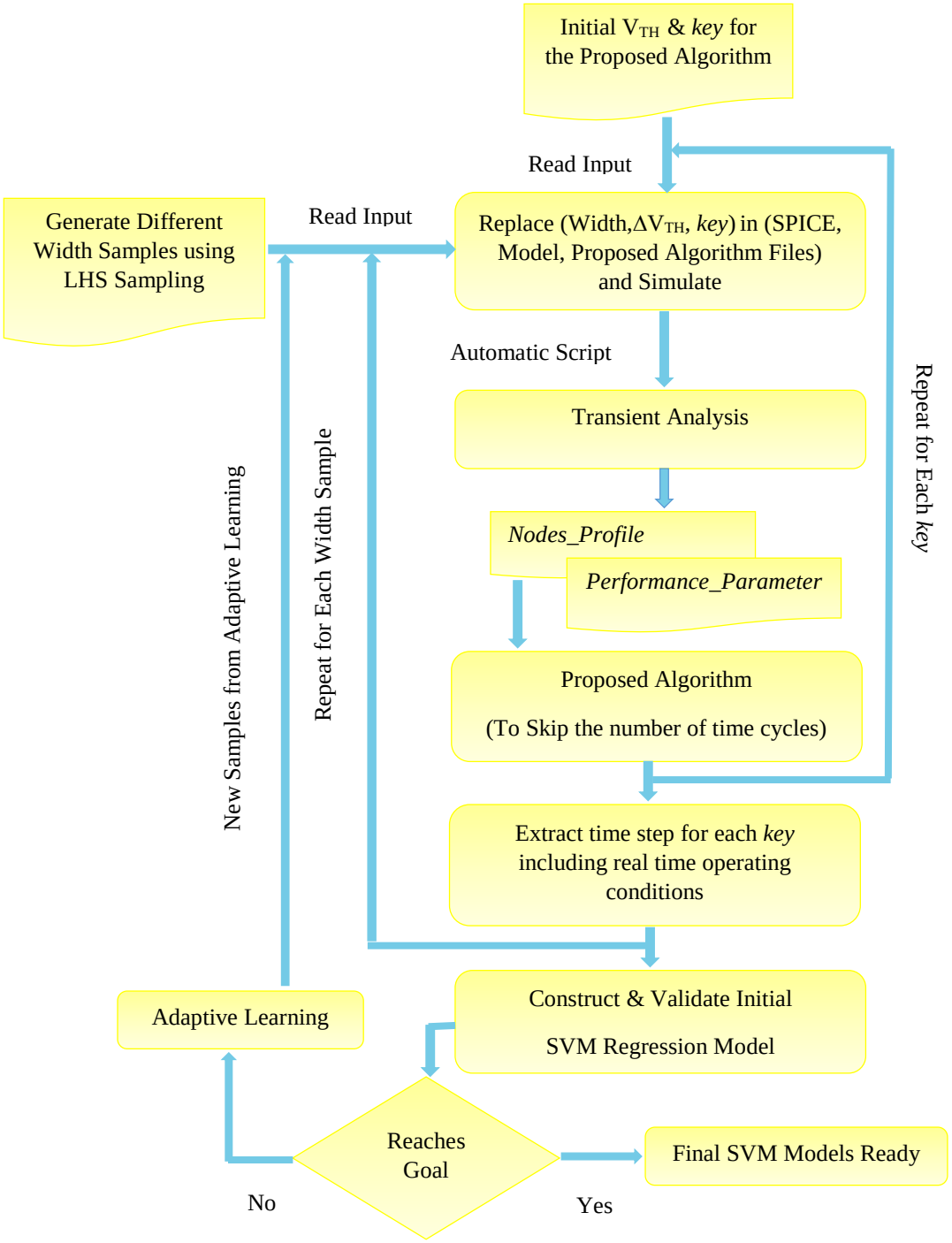


Figure 4.7: Flowchart for the Long Term Model

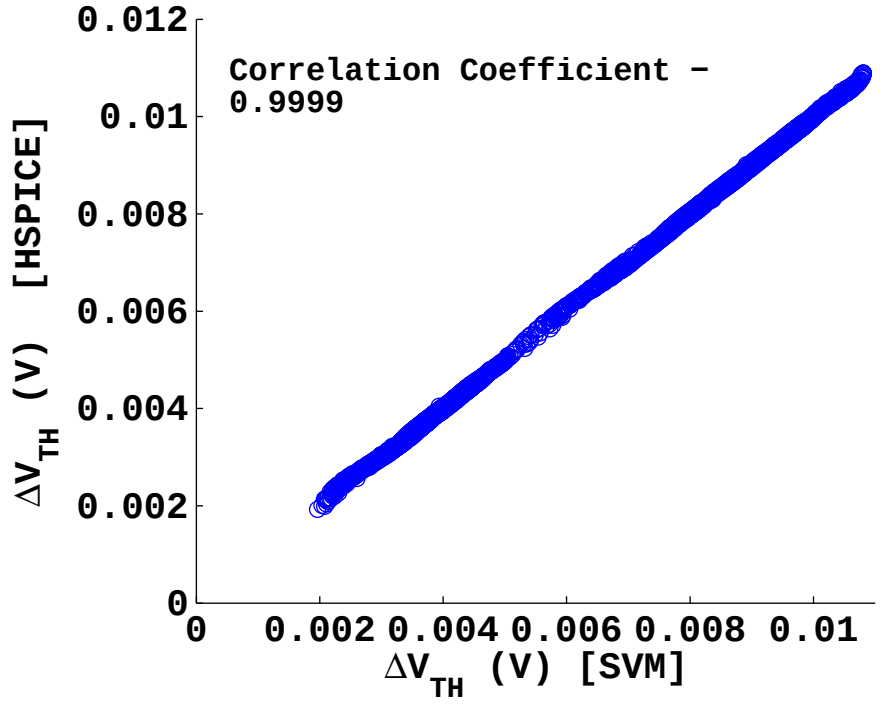
which are denoted as testing samples. The accuracy is checked by finding the correlation coefficient between SVM and SPICE. If target accuracy is achieved then the final model is prepared else adaptive learning is used, to obtain the desired accuracy. Adaptive learning iteratively checks the previous outputs and generates new input training samples in the area of maximum error. These new samples are again passed through SPICE circuit simulations to get output training samples. These new input and output samples are added to previous training samples. Now SVM model is trained again and accuracy is checked. This process is repeated until the desired accuracy has been achieved. After that final SVM model is prepared. Initially, 2200 samples of width are generated through LHS. For every width sample the proposed algorithm has been run for the given ranges of *keys* to find the time steps and gain. Two long term NBTI aware surrogate models have been proposed.

1. Transistor Level Model - This model is developed for each PMOS transistor of the circuit. This model shows the dependence of each ΔV_{TH} on W and T_F (Time Found from section 4.3.3). In this work, two PMOS transistors were chosen from Figure 4.1. The model will be represented as

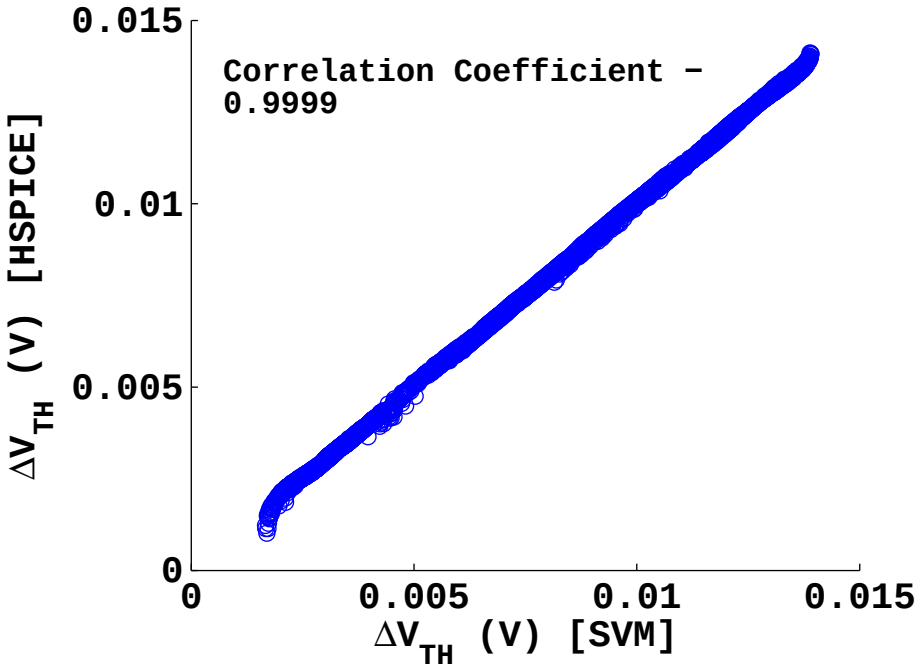
$$Model\,1 \quad (\Delta V_{TH1}, \Delta V_{TH2} = f(W, T_F)) \tag{4.4.1}$$

Initially, 120 training and 2080 testing samples are used in both transistor cases which results in low correlation coefficient. Then adaptive learning is used that provides 720 and 700 training samples for MP1 and MP2 respectively, which increases correlation coefficient to 0.9999. Run time for single sample evaluation are 0.193ms and 0.181ms for MP1 and MP2 respectively. Figure 4.8(a) and 4.8(b) represents the correlation curves between HSPICE and SVM model for both MP1 and MP2 case. These curves are linear, which show that the proposed long term transistor level SVM models are closely associated with HSPICE output. These curves also exhibit the significant variation in ΔV_{TH} with W and T_F.

2. Circuit Level Model - This is a single model for all selected PMOS transistors. This model shows the effect of NBTI in terms of change in threshold voltages $(\Delta V_{TH1}, \Delta V_{TH2})$ on circuit performance parameter at different widths. In this work, circuit differential gain is chosen as a performance parameter. The model will be represented as



(a)



(b)

Figure 4.8: Transistor Level Model (a) MP1 (b)MP2

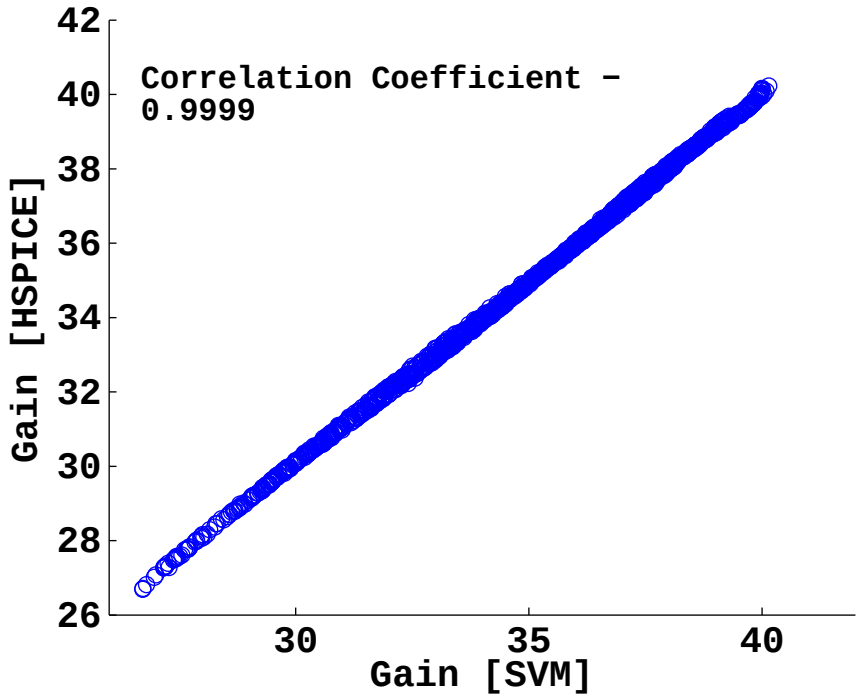


Figure 4.9: Circuit Level Model for all Transistors

$$Model\,2 \quad (G = f(\Delta V_{TH1}, \Delta V_{TH2}, W)) \tag{4.4.2}$$

Initially 220 training and 1980 testing samples are used which results in low correlation coefficient. Then adaptive learning is used that provides 503 training samples and 0.9999 correlation coefficient. Run time for evaluation of a single sample of gain requires 0.102ms. Figure 4.9 shows the correlation curve between HSPICE and SVM model for gain. The linearity of the curve exhibits that proposed SVM model for circuit level finely matches with HSPICE output. It also displays significant variation in gain with ΔV_{TH} and W.

4.4.3 Comparison of the proposed algorithm with Constant and Logarithmic Step Sizes

Step size plays an important role to get accurate V_{TH} degradation. Different step sizes effect the ΔV_{TH} and performance parameter distinctly. In this section, proposed algorithm is compared with different constant and logarithmic time steps. Figure 4.10(a) shows the affect of various step sizes along with proposed algorithm (dynamic step) on

Table 4.1: Percent error for ΔV_{TH} and Gain

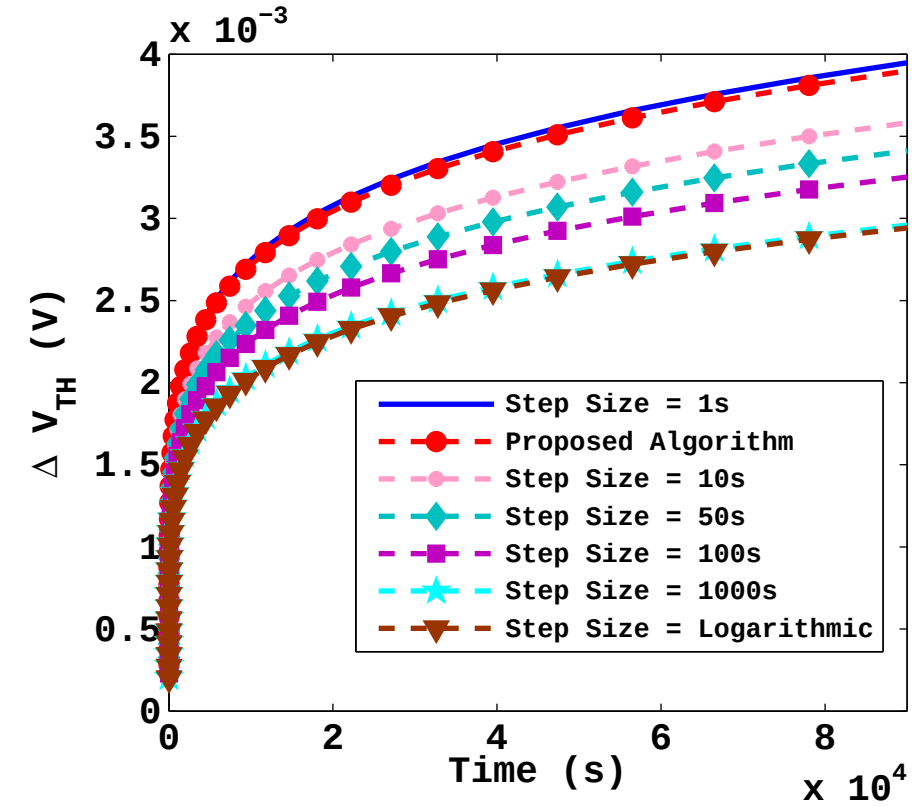
Parameter	Step	One Day	One Year	Five Year
ΔV_{TH}	Proposed Algorithm	1.22 %	1.68 %	1.81 %
	Logarithmic Step	23.60 %	24.00 %	25.47 %
Gain	Proposed Algorithm	0.16 %	0.87 %	1.40 %
	Logarithmic Step	1.10 %	4.73 %	7.17 %

Table 4.2: Simulation Time to calculate the V_{TH} degradation for one day with different step sizes

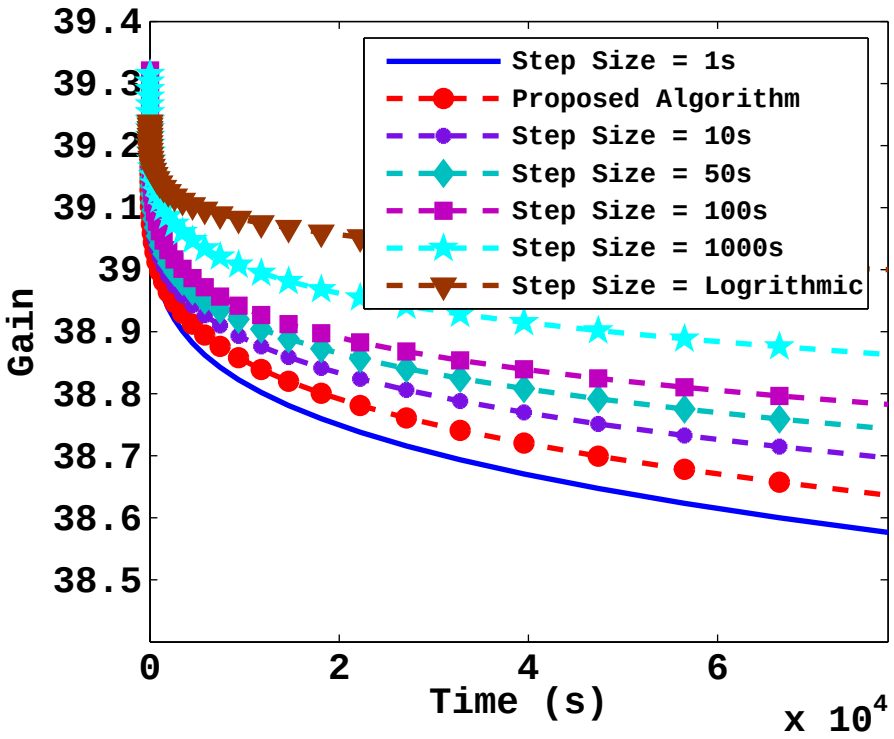
Step Size	Time (s)
1s	93165.84
10s	9636.74
50s	1818.57
100s	791.95
1000s	122.52
Dynamic Step	245.23
Logarithmic Step	16.93

ΔV_{TH}. It is visible that the proposed algorithm closely matches with the minimum step size of 1 second which shows the higher accuracy. As the step size increases, the value (magnitude) of ΔV_{TH} decreases, producing erroneous results. It is seen that logarithmic steps produce the maximum error. Figure 4.10(b) shows the affect of various step sizes along with proposed algorithm (dynamic step) on gain. The proposed dynamic step is closely associated with minimum step size of 1 second providing higher accuracy. As the step size increases change in gain decreases, providing inaccurate results.

Table 4.1 shows the percent error for ΔV_{TH} and gain in case of dynamic and logarithmic step. It is observed that error is more in case of logarithmic step in comparison of dynamic step. This error increases with time. Table 4.2 shows the simulation time to calculate the V_{TH} degradation for one day under various step sizes. It is evident that in case of minimum step size, simulation time is very large even for one day of estimation. Although logarithmic step takes minimum time but error produced is maximum. Our proposed algorithm for dynamic time step takes more time in comparison to logarithmic step but very less in comparison to minimum step size and its accuracy closely matches with the minimum step size.



(a)



(b)

Figure 4.10: Effect of Different Step Sizes on (a) ΔV_{TH} (b) Gain

4.4.4 Effect of Process Corners on V_{TH} Degradation

In nanoscale CMOS technologies there are three sources of variations at the time of manufacturing; two environmental (supply voltage and temperature) and one process variation. These temperature and process (threshold voltage) variations are the crucial reliability concern [145]. When process and environmental variations are combined, process or design corners are defined. These are the extreme of parameter variations within which circuit should work properly. The term corner refers to an imaginary box that ensures the guaranteed performance of the circuit. At the design corner of the design space circuits are most likely to fail. Thus to ensure that non saturated circuit operates correctly in every case, they should be simulated at all corners. A circuit running on devices fabricated at these process corners may run faster or slower than specified. But if the circuit does not work on any of these extremes then design have inadequate design margins. The combined effect of environmental and process variation can be lumped into their effect on transistors : Fast, Slow and Nominal (Typical).

In this section we will analyze the effect on V_{TH} degradation under three process corners; FF (Fast-Fast), NN (Nominal-Nominal), SS (Slow-Slow) where first/second letter represents NMOS/PMOS transistor. Three parameters (V_{TH} ,V_{DD}, tempreature) are chosen under each process corner. Variation in these parameters are given as [146]

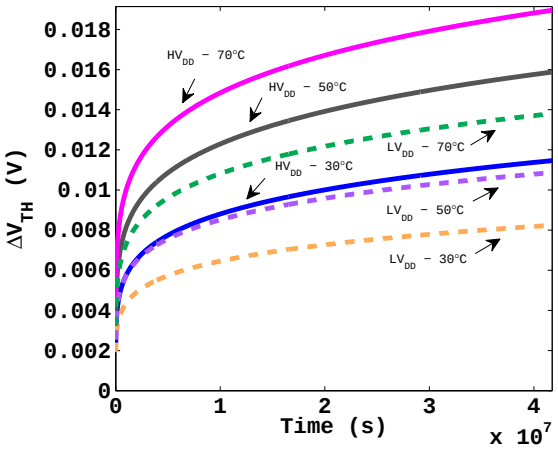
1. Three different temperatures $30°C$,$50°C$ and $70°C$ are considered.

2. 10% variation is considered in nominal V_{TH} which results in high, nominal and low values. In case of NMOS/PMOS transistor these values are 0.559/-0.495, 0.509 /-0.450 and 0.458/-0.405 for slow, nominal and fast cases respectively. These values are considered as initial V_{TH} in the proposed flow.

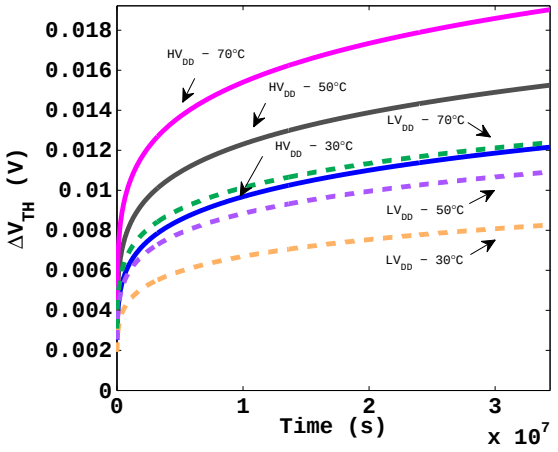
3. 10% variation in nominal V_{DD} yields Low V_{DD} (LV_{DD}- 1.08V), Nominal V_{DD} (NV_{DD}- 1.2V) and High V_{DD} (HV_{DD}- 1.32V).

Figure 4.11 shows the effect of temperature and V_{DD} on $\triangle V_{TH}$ under different process corners. It is visible that as temperature and V_{DD} increases, $\triangle V_{TH}$ also increases. This change in V_{TH} with time is obtained using proposed algorithm under different process corners which proves that proposed model is valid under different process corners.

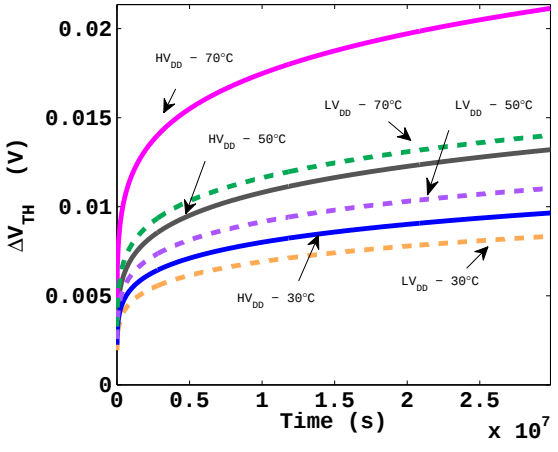
Figure 4.12(a) and 4.12(b) shows the effect of HV_{DD} and LV_{DD} on $\triangle V_{TH}$ in case of



(a)



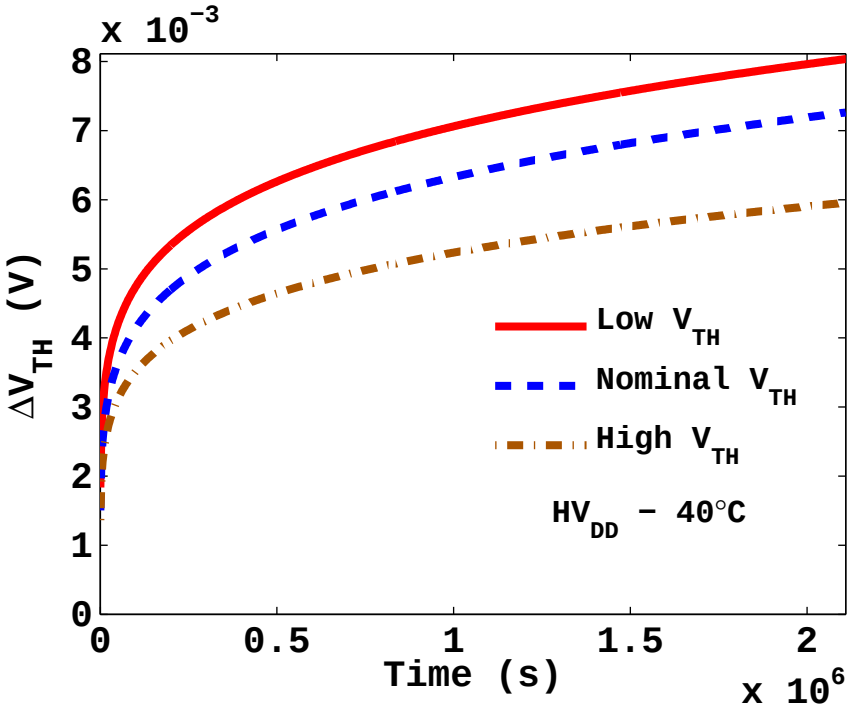
(b)



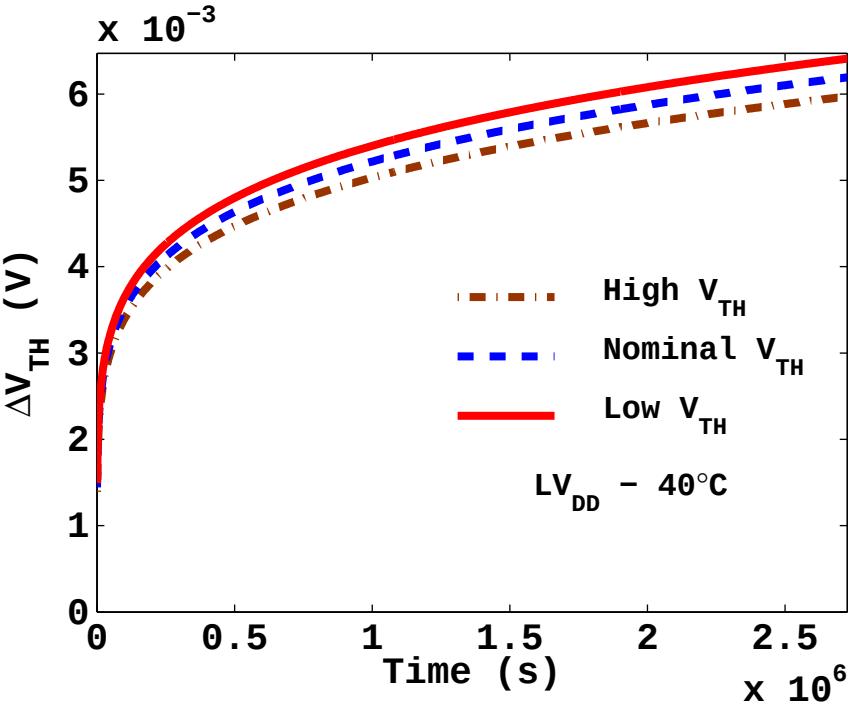
(c)

Figure 4.11: Process Corner (a) FF (b) NN (c) SS

Low, Nominal and High V_{TH}. It is evident that in case of HV_{DD} and FF corner, $\triangle V_{TH}$ degrades more which follows the MOSRA model.



(a)



(b)

Figure 4.12: Low, Nominal and High V_{TH} under (a) HV_{DD} (b) LV_{DD}

4.5 Summary

This chapter has proposed a NBTI aware long term SVM based surrogate model for 5 years for an analog circuit. The correlation between the BTI and voltages at the internal node of the circuit is studied. The affect of NBTI and internal node voltages is simulated on common source amplifier using 32nm technology. It is observed that NBTI effects each transistor in a circuit distinctly. Both model parameter (V_{TH}) and performance parameter (gain) degrades more by taking into account the indirect influence of BTI due to internal node voltages. Further, a NBTI aware long term model is developed. Step size plays an important role to develop a long term model. Minimizing step size increases accuracy but also increases model development time. As step size increases, model development time decreases but at the cost of accuracy. A new algorithm is proposed which finds the dynamic step to include the effect of real time operating conditions. This proposed algorithm is compared with different constant and logarithmic step sizes. It is found that proposed algorithm closely matches with a minimum step size of 1 second and requires less time in order to develop the final long term model which shows higher accuracy. This effect of different process corners on V_{TH} degradation have been studied. It is observed that in FF corner under high temperature and high V_{DD}, V_{TH} degradation is more. Finally a transistor and a circuit level SVM regression models have been developed. Adaptive learning has been used to improve the accuracy while reducing the simulation time. The accuracy of these models are validated by finding the correlation coefficient and correlation curves between HSPICE and SVM. These models are found highly accurate with HSPICE results.

Chapter 5

Combined V_{DD} & V_{BL} Tuning Technique for SRAM Read Stability Improvement & Degradation Aware Surrogate Model for Sense Amplifier

Part I

Combined Supply Voltage and Bit Line Tuning Technique for SRAM Read Stability Improvement

SRAM's occupies a more than 40% of on chip silicon area in state of the art design [147]. They are performance bottlenecks in high performance VLSI circuits. To increase the memory density, memory cells must be as small as possible to reduce their area by 50% in each technology node. These smaller devices make SRAM more vulnerable for time based degradations. SRAM's include many sub circuits such as 6T bit cell, logic circuits like decoders, read/write access timing control circuit, pre-charge circuit and sense amplifier. BTI not only effect SRAM cell array but its peripheral circuitry too. Nanoscale SRAM design must ensure robust operations against degradation over the usage lifetime. SRAM can be characterized through several performance parameters like read/write stability, speed, V_{MIN} (minimum supply voltage). Among all these parameters stable read/write operations are the critical one because it defines the reliability of SRAM. This chapter shows the effect of NBTI on SRAM read/write operations and suggest the compensation technique to improve the read stability.

Memory circuits pose a much greater concern to mitigate the effect of degradation. Since the area is a much greater concern in memory circuits, so area speed trade off solution does not work efficiently for SRAM array as compared to digital CMOS or analog circuit design [148].

5.1 Background of the SRAM Cell

5.1.1 SRAM Structure

SRAM is a type of semiconductor memory which is widely used in microprocessors and SoC. SRAM need not be refreshed periodically due to its static nature. There exist several SRAM memory cell designs which depends on the number of transistors used. The standard choice is the 6T (6 Transistors) SRAM cell. It provides the optimum trade-off between area and stability. Figure 5.1 shows the schematic diagram of 6T SRAM cell. It consists of two cross coupled inverters which are connected through positive feedback. Thus there are two output or memory nodes to store the data. The PMOS transistors P1 & P2 in the core cell are called pull up transistors and NMOS transistors N1 & N3 are called pull down transistors. There are two more NMOS transistors N2 & N4 called access transistors that are required to enable the SRAM cell for read/write operations. Word line WL is used to enable or disable the access transistors. Bit lines

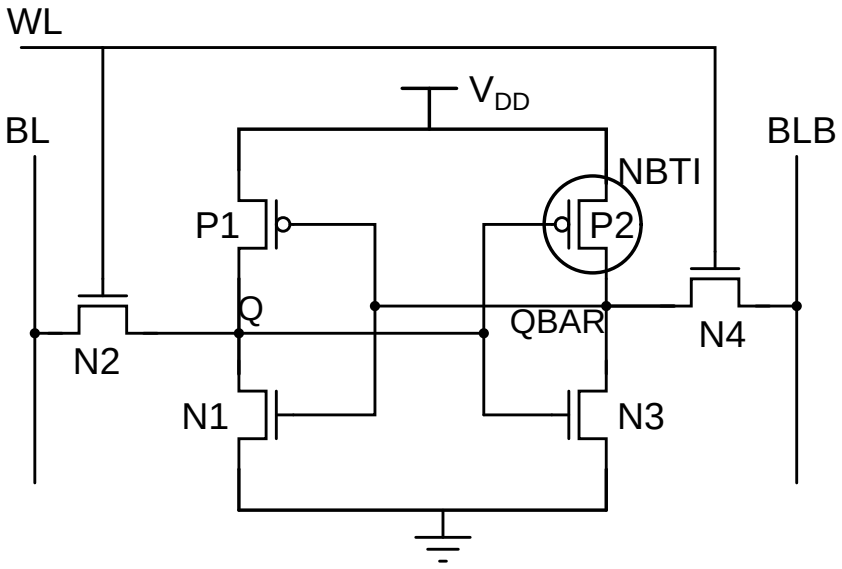


Figure 5.1: Schematic of 6T SRAM Cell

BL and BLB are used during read/write operation to transfer the data in a differential manner. The data is stored at points Q and Q', as stable states denoted by 0 and 1 respectively.

5.1.2 SRAM Operations

SRAM mainly follows three working modes -

1. **Hold Operation** - In this mode SRAM cell remains in the idle state. The access transistor remains OFF as the word line (WL=0) is not asserted. The cross coupled inverter pair "Hold" the information stored.

2. **Read Operation** - In this mode, the stored data in SRAM cell is being read. During read mode both BL & BLB are precharged to V_{DD}. Then WL is set to 1 to enable the access transistors. When the cell stores '0', the BL gets discharged through N2 and N1 to logical '0' while BLB remains precharged. Thus the value of storing nodes gets transfer to BL and BLB. When the cell stores '1', the BLB gets discharged while BL remains precharged. In both cases, a sense amplifier detects the sloping voltage on either side and concludes that side to be '0' memory node and other to be '1' memory node. The sense amplifier is used to speed up the read process as bit line discharging process is slow. For sustainable read mode, pull down transistors should be strong than the access transistors. Otherwise it

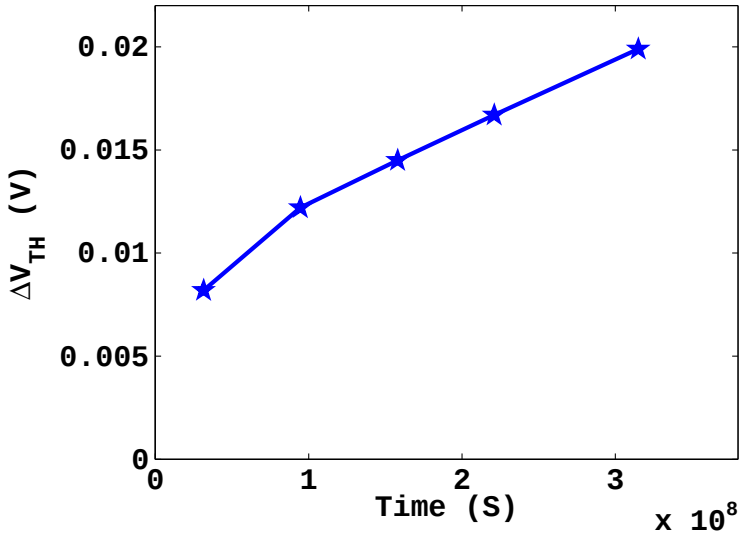
may help for data flipping during the read mode.

3. **Write Operation** - In this mode, the data is being written in the SRAM cell. The data (0 or 1) to be written is applied to BL and it's inverted value is applied to BLB. Then WL is set to 1 to enable the access transistors. In case of writing '0', BL is tied to ground and BLB is precharged. If memory node Q has '0' already then no charging/discharging takes place. In another case, if Q has '1', then it will be discharged to '0' via N2 and through the inverter action the other memory node Q' get pulled up to '1' (via pull up transistor). For sustainable write mode, the access transistor should be stronger than pull up transistor, so that they can easily overwrite the already stored data on other node.

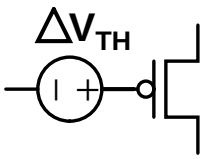
5.2 NBTI Impact on 6T SRAM Cell

SRAM transistors are more prone to BTI phenomenon due to their symmetric topologies. SRAM cells are composed of cross coupled inverters. Each memory cell either store 0 or 1 at all times, creating unbalanced stress and one of the PMOS transistor (due to NBTI) and NMOS transistor (due to PBTI) are always under stress causing a reduction in SRAM cell reliability characteristics [98]. This introduces asymmetric V_{TH} shift in both PMOS devices and skewed transfer characteristics of an inverter which results in the degraded read/write operations [149]. SRAM cells are designed to make sure that during a read operation the contents of the cell are not altered and during a write operation the content of the cell changes quickly. Reliability of the SRAM cell measured in terms of static noise margin (SNM), is significantly degraded due to the effect of BTI. The SNM during the read mode is called read SNM (RSNM) and during the write mode is called write SNM (WSNM). In Figure 5.1, V_{TH} of the 'ON' transistor P2 increases under NBTI effect.

In order to integrate the effect of NBTI in SRAM operations, a threshold voltage shift ($\triangle V_{TH}$) for a single PMOS transistor is obtained for a given technology node. MOSRA model [135] is used for this purpose. Figure 5.2 shows the effect of NBTI on single PMOS transistor. For 32nm technology, 20mV change in V_{TH} is observed for 10 years. This $\triangle V_{TH}$ is modeled as a voltage source, as shown in Figure 5.2, applied in series with both PMOS transistors [150] to integrate the effect of NBTI in SRAM cell.



(a)



(b)

Figure 5.2: (a) Effect of NBTI on PMOS Transistor (b) Simulation setup for modeling of NBTI in 6T SRAM cell

When V_{TH} of P2 is increased under NBTI effect, the trip point of the right inverter becomes lower. This results in the flipping of stored data during the read operation, hence read margin degrades with time. Figure 5.3 shows the impact of NBTI on the read operation. Read SNM degrades from 0.0349V to 0.0291V. During the write operation, slower P2 (due to increase in V_{TH}) will help in discharging of the 'Q=1' node, hence write margin improves. Figure 5.4 shows the impact of NBTI on write operation. Write SNM improves from 0.143V to 0.154V. Since NBTI improves the WSNM and degrades the RSNM, so we will only consider the time based read stability degradation. For rest of the chapter, RSNM will be written as SNM.

5.3 Read Operation related Performance Metrics

1. **Read Stability (SNM)** - The SRAM cell stability is characterized by a SNM. It is the minimum amount of noise present at the nodes Q and Q' to flip the state

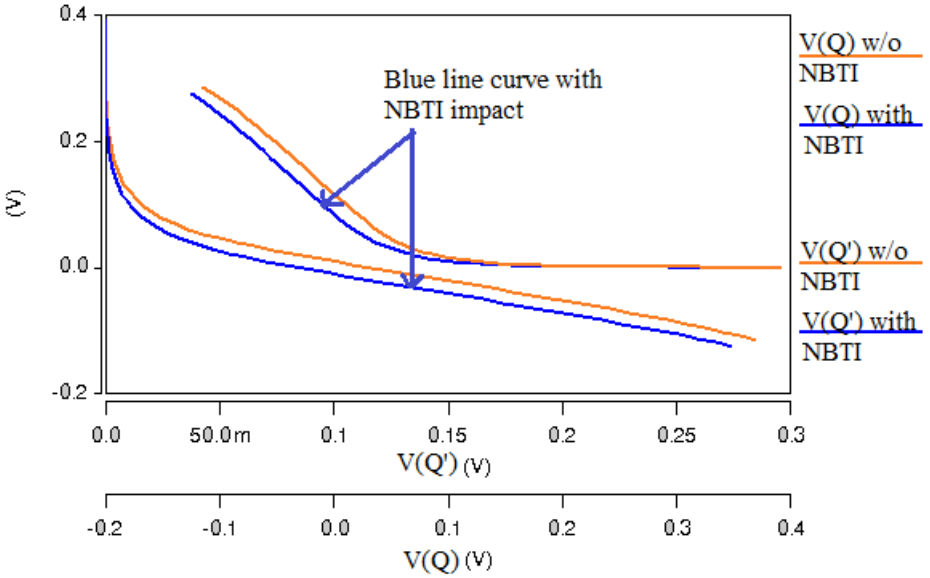


Figure 5.4: NBTI impact on write operation

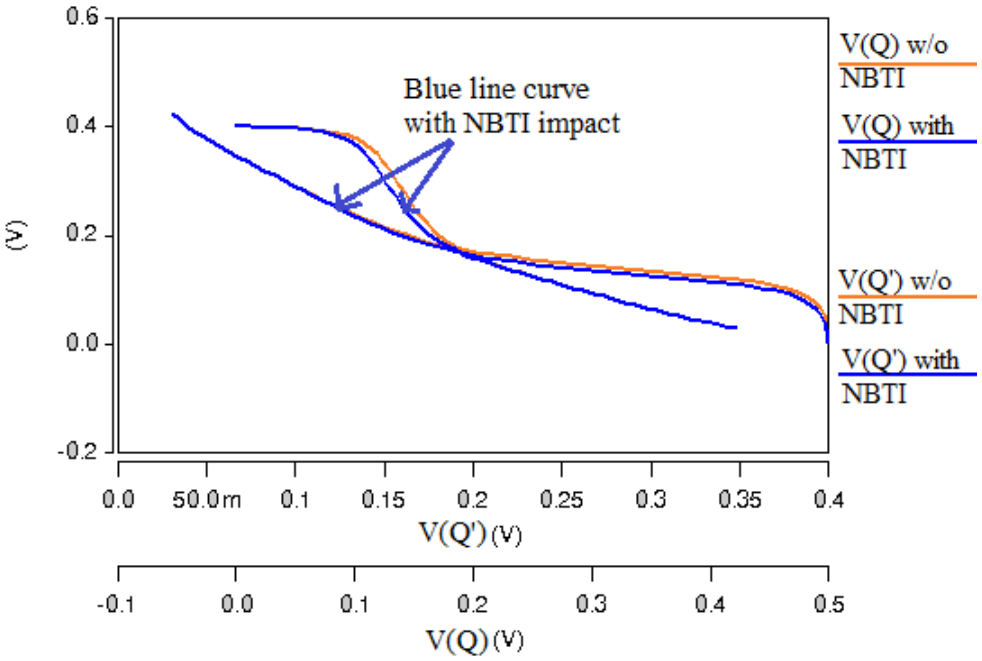


Figure 5.3: NBTI impact on read operation

(stored data) of the cell. It depends on the intensity of the noise on the node that stores '0' during the read operation. Stronger pull down and weaker access transistors are required for a proper read operation. Seevinck et al. [151] proposed a simulation and graphical based technique to calculate the SNM. Nowadays, DC circuit simulator is used to measure the SNM. In this case, it is estimated that

how much DC voltage is left until the cell will flip. Thus both cross coupled inverters are treated independently and their transfer characteristics (VTC curves) are obtained. These curves are plotted while keeping one VTC mirrored. This results in butterfly curve. The biggest square between curves is a measure that how much DC noise is needed to trigger the opposite inverter under read conditions. For this DC value, the butterfly shape of the curve shall still be retained. The higher the SNM value, the more stable the cell [152].

2. **Read Current (I_{READ})** - It is the current that flows from the bit line into SRAM node storing a 0. I_{READ} is inversely proportional to delay i.e., higher I_{READ} results in lower delay and vice verse. It defines the speed of the SRAM. In a read operation, this current is responsible for discharging the precharged bit-line capacitances. It determines the time required to discharge the BL's to a value where the sense amplifier detects the '0' node. For successful read operation, BL's should discharge to a voltage differential which can trigger the sense amplifier correctly. If I_{READ} goes below to a certain level, the read failure occurs.

3. **Minimum Operating Voltage (V_{MIN})** - Lowering V_{DD} is the simplest way to save energy in low-power systems not only in hold mode but also in read/write mode. It defines the minimum supply voltage that provides the full functionality in all working modes. For a read operation, it is defined as the minimum supply voltage for which bit line discharges to logic '0'. When SRAM operates below V_{MIN}, all 6 transistors work in the subthreshold region and are prone to degradation. For low power operations, it is required to operate SRAM cell with V_{MIN}. It is necessary to identify V_{MIN}, at which correct read operation takes place without failure. In Figure 5.5 at V_{MIN} = 0.4V, BL reads correct data Q = '0'. Data flip is observed below 0.4 V. SNM is 0.0349V at this V_{MIN} without considering NBTI.

5.4 Compensation Techniques

NBTI degrades the V_{TH} of PMOS transistor, and this degradation affects the performance and read margin of the 6T SRAM cell. Its stability decreases and data flips easily. Therefore, it is essential to compensate this effect and restore the SNM value. Over

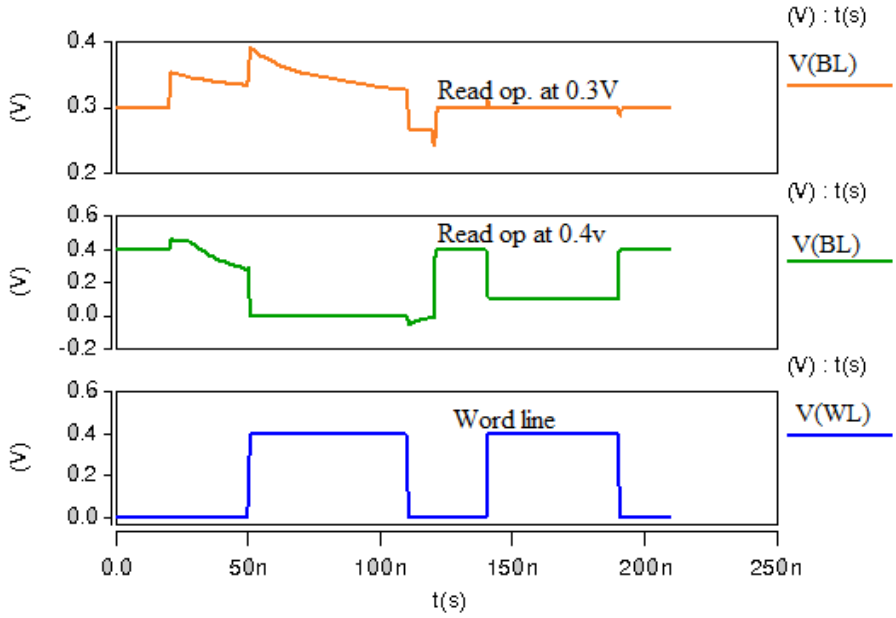


Figure 5.5: Determination of minimum operating voltage during read operation.

the years, several compensation techniques have been proposed for reliable SRAM operation. These compensation or mitigation techniques can be broadly divided into three [153] categories :

a. **Transistor Level** - At this level, the SRAM functionality can be improved by changing either the transistor sizes or the threshold voltages.

b. **Control Voltage Level** - At this level, the SRAM functionality can be improved by changing the supply voltage, word line and bit line voltages.

c. **Architecture Level** - At this level, The SRAM functionality can be improved by changing the size of the SRAM array.

The focus of this work is on control voltage level techniques because they have been proven to be effective without changing the cell design. Different voltage level techniques are proposed in the literature which are categorized into read assist and write assist techniques. Here we are discussing few techniques w.r.t. read operation.

1. **Guard Banding** - In order to save leakage power V_{DD} is reduced to V_{MIN}, but at the cost of reduced stability. To increase the stability, some "Guard Band" is introduced between V_{DD} and V_{MIN} rather than lowering the V_{DD} up to V_{MIN}. It is very simple way to improve read stability without altering the system. Unfortunately, the optimum power saving is not obtained.

2. **Dual** V_{DD} - Continues scaling demands lower supply voltage, to keep power

consumption minimum. However, reduced supply voltage decreases the SRAM cell stability. To overcome this issue, an additional power supply is employed (Dual V_{DD}) in several designs [154]. In 6T SRAM cell, higher cell power supply ($V_{DD-Cell}$) means increase in read stability but decrease in write stability. On the basis of read/write operation, the switching of SRAM $V_{DD-Cell}$ can be helpful to improve the cell stability. As $V_{DD-Cell}$ increases during read operation, the differential bit line voltage also increases. The voltage difference between the node storing '1' and corresponding bit line produces a current which passes through an access transistor, charging the node capacitance and increases the bit line voltage which finally enhances the voltage difference between both bit lines. In [154] the authors employed 100mV higher $V_{DD-Cell}$ than the normal V_{DD} and 10x reduction in cell failure was obtained. However, the area penalty was not reported.

3. **Word Line Voltage** - The SNM is improved by reducing the word line voltage (V_{WL}). Higher V_{WL} leads to more current flowing through access transistor but it also decreases the differential bit line voltage which results in less reliable read operation. In [155, 156] authors proposed the replica access transistor which self compensate V_{WL} suppression under dynamic voltage and frequency environment This gives maximum V_{WL} lowering under fast/hot corners where I_{READ} is large to start and vice verse. The cell stability is not limited by maximum V_{DD}, unlike the dual V_{DD} approach.

4. **Bit Line Control** - When bit line voltage reduces (V_{BL}), the amount of charge sharing between bit line and the cell storage node also reduces. This amount of charge sharing is not sufficient to invert the stored SRAM cell value but this is achieved at the cost of less I_{READ} which may increase the delay. Controlling BL and WL simultaneously is another effective way to increase SNM. Khellah et al. [106] employed the pulsed BL and WL scheme to improve cell stability at low voltages in single $V_{DD-Cell}$ design. Both precharged BL & BLB are pulled down upto 300 mV just before turning on WL during read operation. Lower BL causes less I_{READ} and the amount of charge sharing between the BL and storage node. Thus cell is less likely to flip during the read operation, hence more stability. This scheme preserves the speed and simplicity of conventional full V_{DD} precharge, eliminating the overhead to generate another voltage level for BL precharge.

5. **Body Bias** - Another way to suppress the V_{TH} variation effect is body biasing. In [111, 157] both forward and reverse body biasing was introduced. Hamzaoglu et al. [157] used forward body bias (FBB) to increase the strength of pull up device. Applying the positive bias V_{BS} to the bulk, shifts the threshold voltage to more positive values. It helps in compensating the increased V_{TH} variation due to aging. This degrades the write margin, but overall cell stability is increased so that V_{MIN} can be reduced. In an SRAM array, all pMOS transistors have one common n-well, which means that V_{BS} must be adjusted equally to all pMOS transistors. This could only be avoided by a triple-well process. Yamaoka et al. [111] proposed separate body bias control of PMOS and NMOS. Initially, V_{TH} variation was monitored and then body bias of NMOS and PMOS was adjusted externally, but this results in additional area consumption.

5.5 Proposed Mitigation Technique

NBTI degrades the V_{TH} of PMOS transistor, and this degradation affects the performance and read margin of the 6T SRAM cell. Its stability decreases and data flips easily. Therefore, it is essential to compensate this effect. To improve the stability or to mitigate the NBTI effect, different approaches have been reported. One of the approaches is V_{DD} tuning [97] and other is V_{BL} reduction technique [106]. We have proposed a mitigation technique which is a combination of abovesaid techniques. To implement this technique we have developed a hybrid model comprised of both V_{DD} and V_{BL}. Our aim is to select V_{BL} and V_{DD} to improve read stability while avoiding the degradation of other performance parameters i.e. P_{READ} and I_{READ} or delay. In the following section both approaches have been discussed and compared with our proposed technique. For all the simulations PTM 32nm model has been used. All the simulations are performed using HSPICE and MATLAB curve fitting toolbox.

5.5.1 V_{DD} Tuning

SNM is a linear function of V_{DD} as shown in Figure 5.6(a). In this approach, V_{DD} is increased to compensate the degraded SNM. As V_{DD} increases, the strength of the access transistors decreases which increases the time to flip the data during read oper-

ation [97]. At different values of $\triangle V_{TH}$ considering NBTI effect, degraded values of SNM are obtained using HSPICE simulation. Further, this data is used to develop the analytical model using MATLAB as in Equation (5.5.1).

$$SNM(\triangle V_{TH}, V_{DD}) = SNM(0, V_{DD}) + c * \triangle V_{TH} \tag{5.5.1}$$

where t is time, $\triangle V_{TH} = d * t^{0.2475}$, $c = -0.2893$ and $d = 1.49e^{-6}$ are constants, $SNM(0,V_{DD})$ and $SNM(\triangle V_{TH},V_{DD})$ are the noise margins with and without NBTI at fixed V_{DD}. Figure 5.6(b) shows the SNM variation as the function of both V_{DD} and NBTI, which shows that SNM degrades more in case of higher NBTI effect. This degradation is more at higher values of V_{DD} due to large V_{gs} values.

To improve SNM, V_{DD} need to be increased. The value of V_{DD} can be calculated by equating the SNM with higher $V_{DD}(V_{DDH})$ considering NBTI to SNM at nominal V_{DD} without considering NBTI as in Equation (5.5.2). It results in increased value of V_{DD} i.e. V_{DDH} as a function of $\triangle V_{TH}$ as in Equation (5.5.3).

$$SNM(\triangle V_{TH}, V_{DDH}) = SNM(0, V_{DD}) \tag{5.5.2}$$

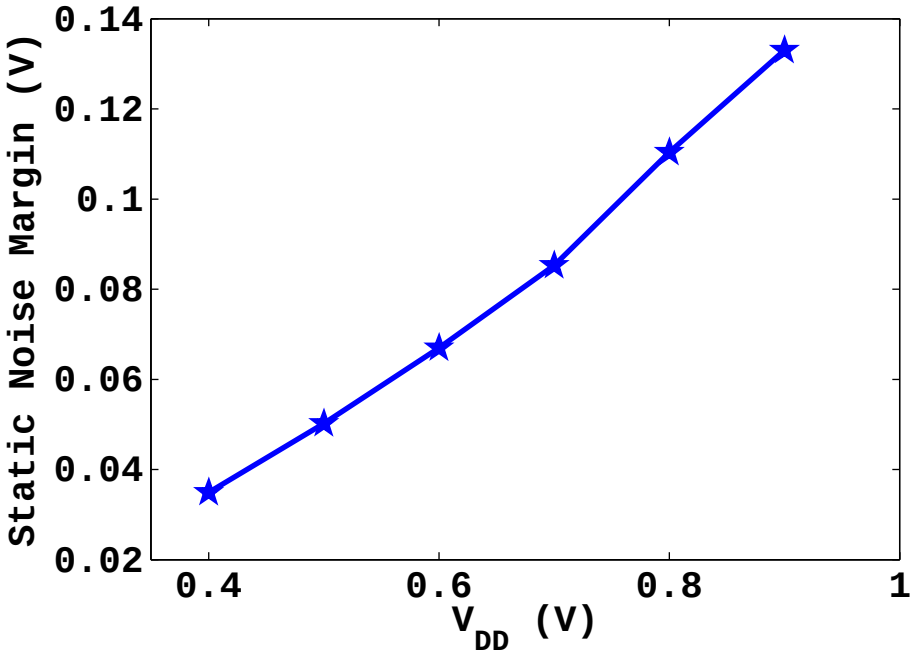
$$V_{DDH} = e * \triangle V_{TH} + f \tag{5.5.3}$$

where $e = 1.904$ and $f = 0.4009$ are constants. Table 5.1 shows increased V_{DD} values at different $\triangle V_{TH}$. Higher V_{DD} is required to compensate higher degradation which also increases P_{READ} and I_{READ}. Figure 5.7 and 5.8 shows the linear increment in P_{READ} and I_{READ} as a function of $\triangle V_{TH}$ with the corresponding increment in V_{DD}.

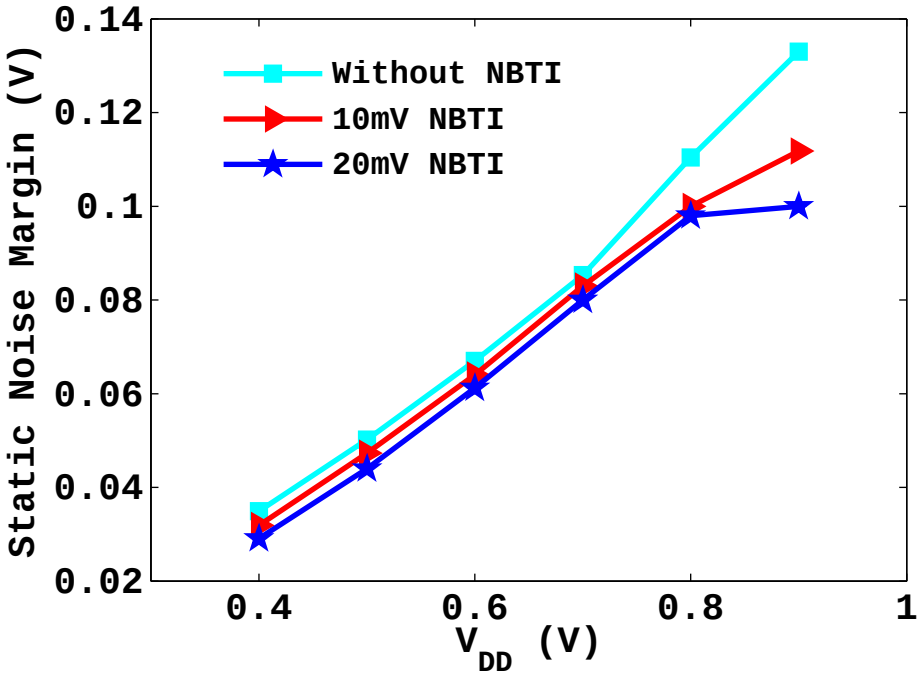
Table 5.1: Increased V_{DD} values to compensate NBTI

$\triangle V_{TH}$ **(mV)**	V_{DDH} **(V)**	P_{READ} **(nW)**	I_{READ} **(nA)**
8	0.416	15.64	19.80
10	0.42	16.19	21.03
14	0.428	17.33	23.72
18	0.435	18.22	26.41
20	0.439	18.84	28.02

To compensate $\triangle V_{TH}$ = 20mV, this approach increases the P_{READ} up to 40% and I_{READ} up to 80% from the nominal values (without NBTI). However, delay is reduced



(a)



(b)

Figure 5.6: (a) SNM as function of V_{DD} (b) SNM vs. V_{DD} as a function of NBTI

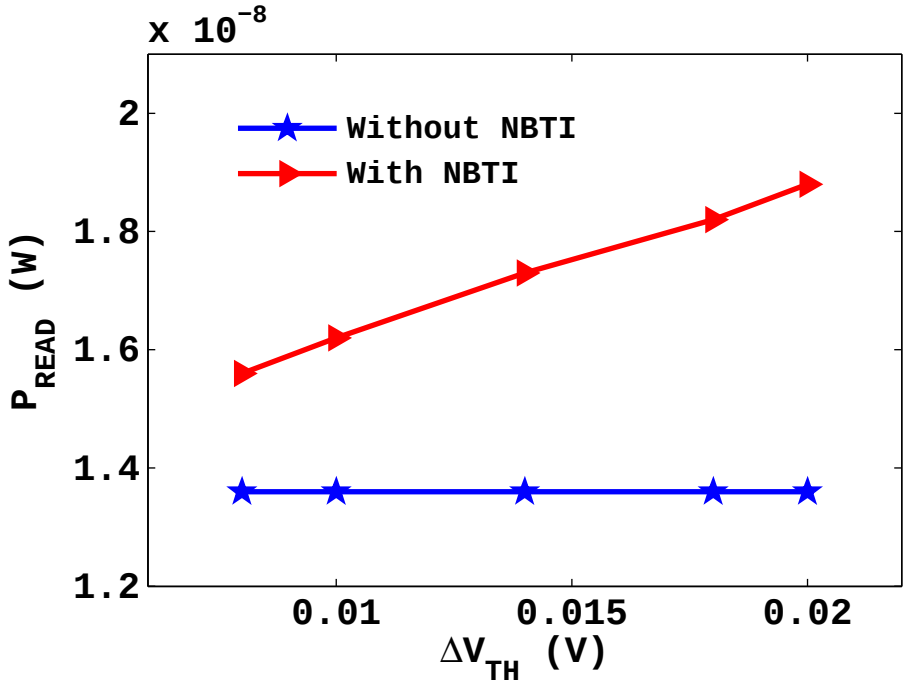


Figure 5.7: P_{READ} vs $\triangle V_{TH}$ at corresponding V_{DDH}. Blue curve shows P_{READ} at constant (V_{DD}, V_{TH}). Red curve shows P_{READ} at increased V_{DD}

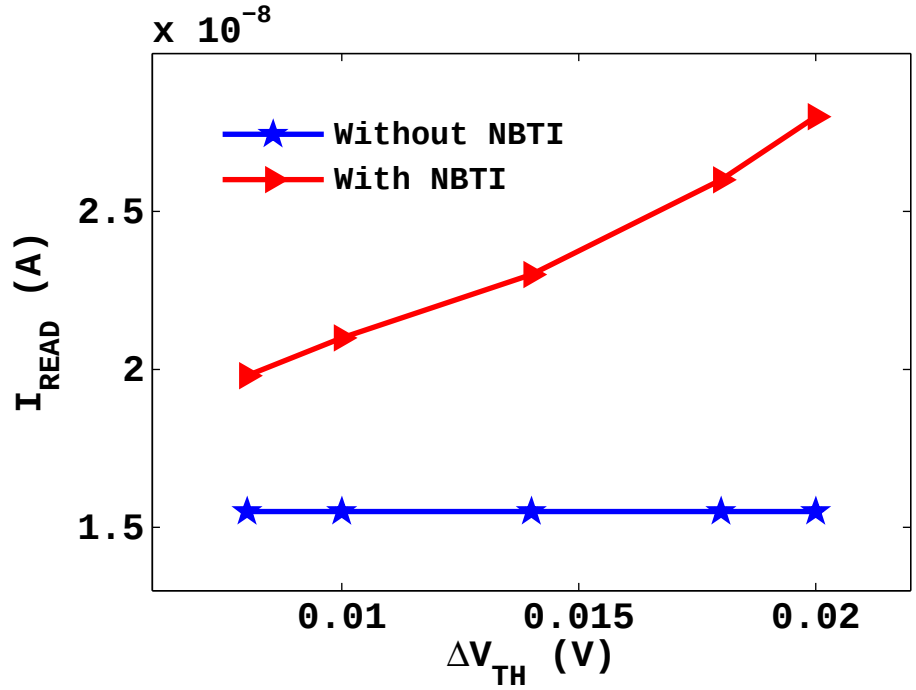


Figure 5.8: I_{READ} vs $\triangle V_{TH}$ at corresponding V_{DDH}. Blue curve shows I_{READ} at constant (V_{DD}, V_{TH}). Red curve shows I_{READ} at increased V_{DD}

Table 5.2: Reduced Bit line Voltage values to compensate NBTI

$\triangle V_{TH}$ **(mV)**	V_{BLL} **(V)**	P_{READ} **(nW)**	I_{READ} **(nA)**
8	0.3710	12.39	14.53
10	0.3654	12.10	14.31
14	0.3500	11.55	13.88
18	0.3349	11.03	13.40
20	0.3280	10.78	13.19

due to increased I_{READ} but at the cost of increased P_{READ}.

5.5.2 Bit Line Voltage Reduction Technique

When bit line voltage reduces, the amount of charge sharing between the bit line and the cell storage node also reduces [106]. This amount of charge sharing is not sufficient to invert the stored SRAM cell value. To improve SNM, V_{BL} needs to be decreased. Value of V_{BL} can be calculated by equating the SNM with lower $V_{BL}(V_{BLL})$ considering NBTI to SNM at nominal V_{BL} without considering NBTI as in Equation (5.5.4). It results in a reduced value of V_{BL} i.e. V_{BLL} as a function of $\triangle V_{TH}$ as in Equation (5.5.5).

$$SNM(\triangle V_{TH}, V_{BLL}) = SNM(0, V_{BL}) \tag{5.5.4}$$

$$V_{BLL} = g * \triangle V_{TH} + h \tag{5.5.5}$$

where $g = -3.654$ and $h = 0.401$ are constants. Table 5.2 shows the reduced bit line voltage required for NBTI compensation. Figure 5.9 and 5.10 shows the effect of reduction in V_{BL} on P_{READ} and I_{READ} as a function of $\triangle V_{TH}$.

To compensate $\triangle V_{TH}$ = 20mV using this approach, P_{READ} reduces by 20% due to lower voltage and I_{READ} reduces by 15% due to lower discharging rate of bit line capacitance from the nominal values (without NBTI). However, P_{READ} is reduced but at the cost of increased delay.

5.5.3 Proposed Methodology

We have proposed a combined mitigation technique using both boosted supply voltage and bit line voltage reduction, to avail the advantages of both approaches. We have

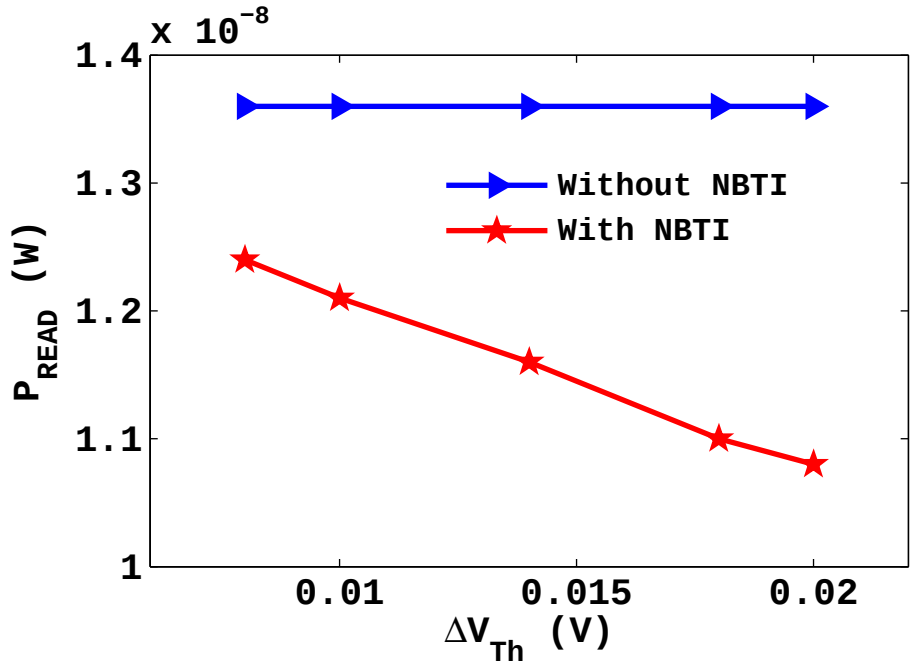


Figure 5.9: P_{READ} vs $\triangle V_{TH}$ at corresponding V_{BLL}. Blue curve shows P_{READ} at constant (V_{BL}, V_{TH}). Red curve shows P_{READ} at reduced V_{BL}

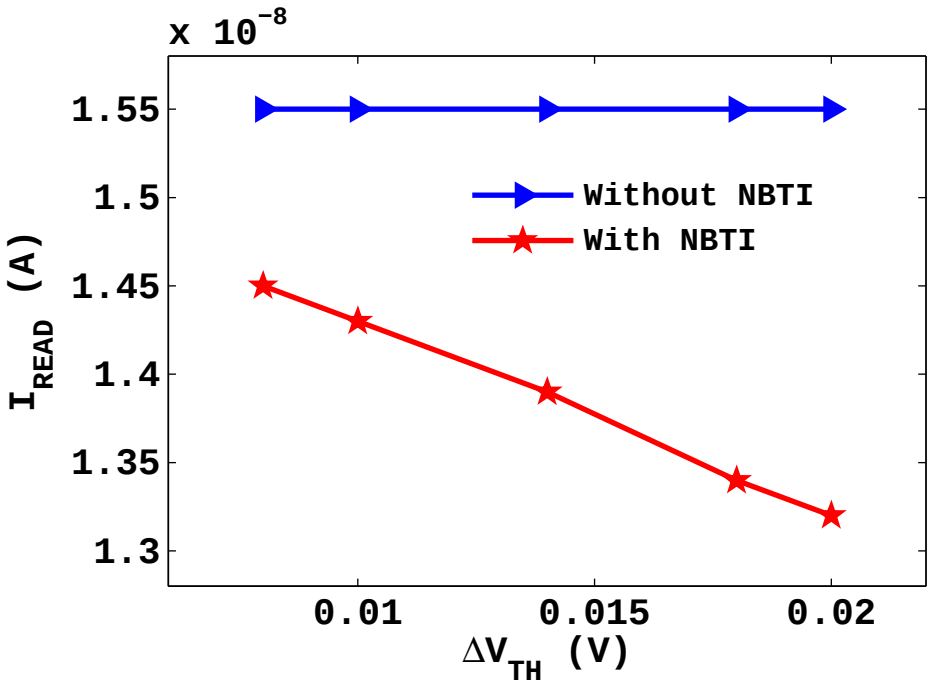


Figure 5.10: I_{READ} vs $\triangle V_{TH}$ at corresponding V_{BLL}. Blue curve shows I_{READ} at constant (V_{BL}, V_{TH}). Red curve shows I_{READ} at reduced V_{BL}

Table 5.3: Developed Hybrid Model to compensate NBTI

$\triangle V_{TH}$ **(mV)**	V_{DDH} **(V)**	V_{BLL} **(V)**	P_{READ} **(nW)**	I_{READ} **(nA)**
8	0.405	0.387	13.30	16.12
10	0.405	0.377	13.03	15.73
14	0.406	0.367	12.60	15.63
18	0.407	0.358	12.38	15.71
20	0.409	0.354	12.28	15.75

developed a hybrid model to implement this technique. Equation (5.5.3) and Equation (5.5.5) are used to obtain the hybrid model as in Equation (5.5.6).

$$V_{DDH} - V_{BLL} = i * \triangle V_{TH} + j \tag{5.5.6}$$

where $i = 5.558$ and $j = 0.001$ are constants. Table 5.3 shows the increased V_{DD} and decreased V_{BL} required to compensate NBTI effect. It is observed that V_{DDH} values are less as compared to the values given in Table 5.1, while V_{BLL} values are higher compared to the values given in Table 5.2. These set of V_{DDH} and V_{BLL} voltages result in lower P_{READ} and higher I_{READ} i.e., lower delay without SRAM failure. Figure 5.11 and Figure 5.12 indicates P_{READ} and I_{READ} as a function of $\triangle V_{TH}$ for corresponding V_{DDH} and V_{BLL} values.

Table 5.4 shows the comparison of all compensation techniques and values of SRAM metrics with and without NBTI. By using the proposed technique, P_{READ} is reduced by 10% and I_{READ} is increased by 3% compared to V_{DD} up-scaling [97] and V_{BL} reduction [106] approach respectively. It can be observed that using proposed technique, values of P_{READ} and I_{READ} closely matches with the values when no NBTI effect was present in the circuit.

5.6 Summary

In this chapter, it has been observed that NBTI is challenging reliability issue in nanoscale devices, which degrades the circuit performance. Due to NBTI, 20mV change is observed in V_{TH} of a single PMOS transistor. Further, SNM degradation is observed in SRAM cell. In order to compensate the effect of NBTI, a new mitigation technique is proposed. This technique utilizes two different approaches i.e., V_{DD} tuning and V_{BL} re-

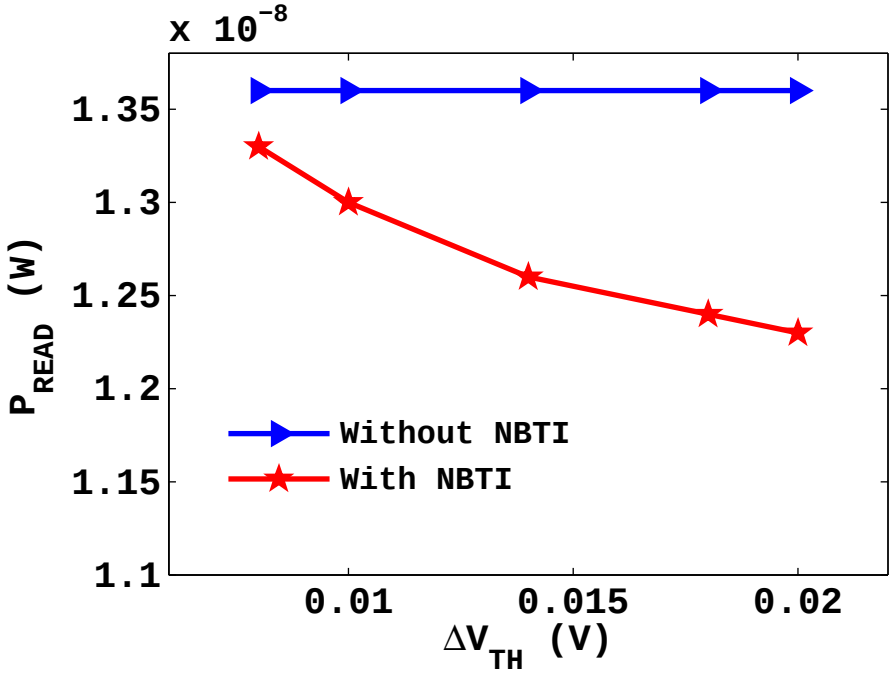


Figure 5.11: P_{READ} vs $\triangle V_{TH}$ for Proposed Hybrid Model. Blue curve shows P_{READ} at constant (V_{DD}, V_{BL}, V_{TH}). Red curve shows P_{READ} at increased V_{DD} and reduced V_{BL}

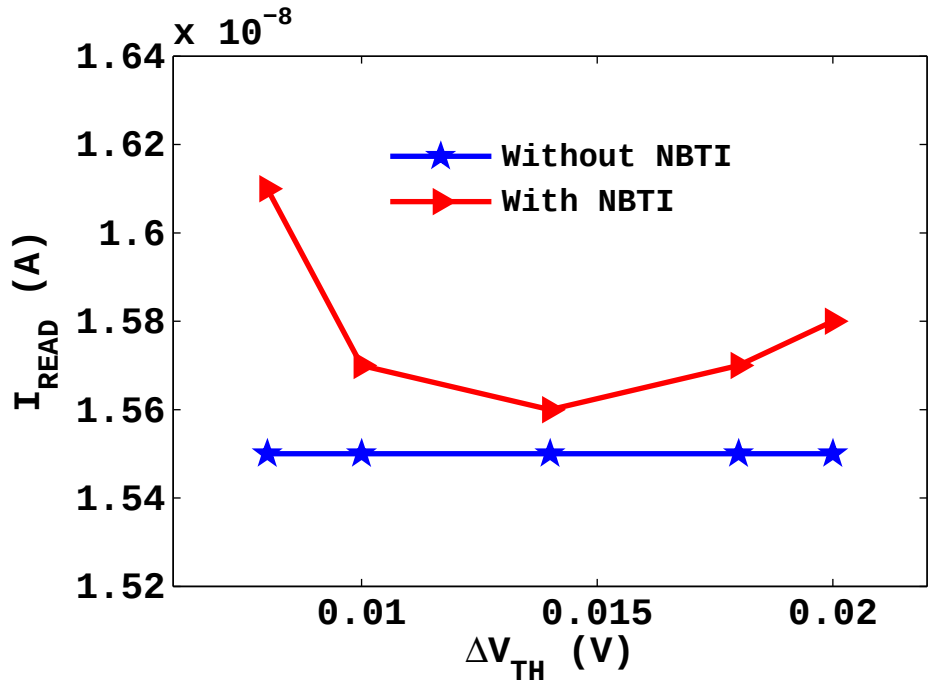


Figure 5.12: I_{READ} vs $\triangle V_{TH}$ for Proposed Hybrid Model. Blue curve shows I_{READ} at constant (V_{DD}, V_{BL}, V_{TH}). Red curve shows I_{READ} at increased V_{DD} and reduced V_{BL}

Table 5.4: Comparison between Previous approaches and Our Developed Hybrid Model

Minimum V_{DD} operating voltage without NBTI	
V_{DD} = 0.4V, $\triangle V_{TH}$ = 0 mV	SNM = 0.0349V, P_{READ}= 13.59nW I_{READ}= 15.50nA
After NBTI degradation [10 Years]	
$\triangle V_{TH}$ = 20mV	SNM = 0.0291V
Compensation Techniques	
V_{DD} Boosting [97]	SNM = 0.0349V, P_{READ} = 18.84nW I_{READ}= 28.03nA
V_{BL} Reduction [106]	SNM = 0.0349V, P_{READ} = 10.78nW I_{READ}= 13.19nA
Developed Hybrid Model (This Work)	SNM = 0.0349V, P_{READ} = 12.28nW I_{READ}= 15.75nA

duction, to avail the advantages of both methods. The values of performance parameters P_{READ} and I_{READ} have been estimated. The proposed technique shows a reduction in P_{READ} by 10% and increment in I_{READ} by 3% without degrading SNM. This results in less delay and power, considering NBTI effect. Using hybrid model SNM is improved to the point when there is no NBTI effect present in the SRAM without degrading other performance parameters. This shows that such kind of techniques can provide better controllability to mitigate the NBTI effect.

PART II

Degradation Aware Surrogate Model for Sense Amplifier

The memory cell is a basic component of a memory circuit. The signal swing on the bit lines and read access time to be minimized to get fast and power efficient memory design. One of the most critical, SRAM peripheral circuit is the sense amplifier, which is related to the read access time of the SRAM. Sense amplifier uses minimum bit line differential current or voltage to provide full rail output swing, to make fast read/write operations possible. Designing fast, robust and high performance sense amplifier is necessary for SRAM designing, but with increasing process variations and time based degradations, it is becoming a challenging task. Sense amplifier is comprised of a pair of matched transistors in a positive feedback environment. The increasing intra die variations along with BTI effect results in a mismatch between the matched transistors. This leads to sense amplifier performance degradation, like increased delay and resulting yield loss is more pronounced than before. Thus it is necessary for the designer to accurately predict the impact of transistor mismatch at the circuit level to avoid the yield loss due to reliability issues. High fidelity models like SPICE are used to find circuit performances, which are computation intensive. An accurate and fast process variability and reliability aware model would be required to estimate the performance degradation with less computation cost. A surrogate model is widely accepted to replicate the behavior of complex simulation model while being computationally effective. In this work, initially impact of process variation and aging on sense amplifier performance is evaluated and then SVM based surrogate model is developed.

5.7 Sense Amplifier Background

The sense amplifier is a most critical peripheral circuit of SRAM. Its main function is to sense the data from a read selected memory cell and translate the small differential voltage to full swing signal. The performance of the sense amplifier depends on how fast it provides the output signal which can be used by further digital logic. They are designed with symmetrical structure. Despite of careful designing, variations in V_{TH} and width due to BTI and parametric variations, results in degraded performance of sense amplifier. Sense amplifiers can broadly divided into two categories.

1. **Voltage Mode Sense Amplifier** - It is used in conventional memories, and present high input impedance to the bit lines. This allows the sense amplifier to provide

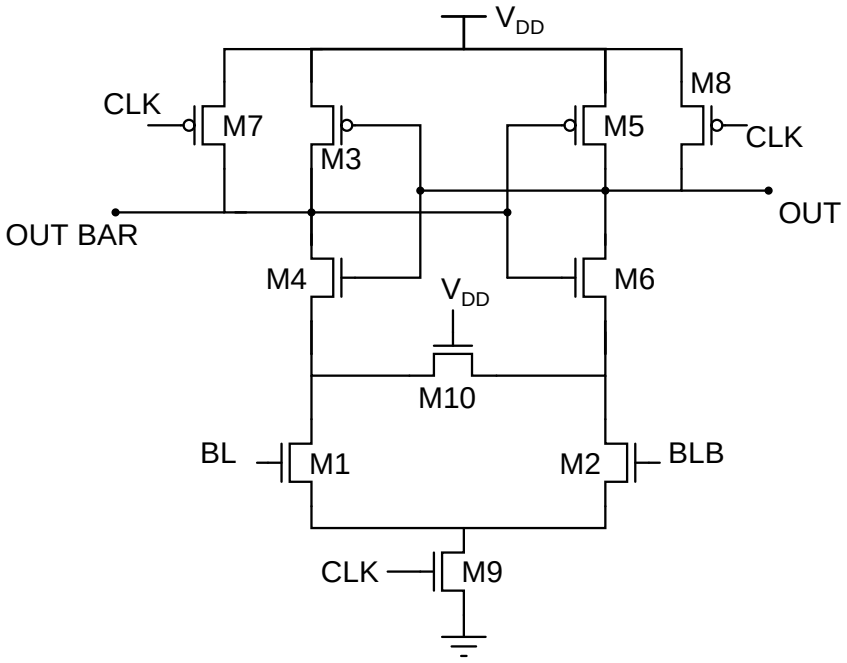


Figure 5.13: Conventional Voltage Mode Sense Amplifier

a high voltage gain with the use of simple circuits. For sensing the voltage difference, it requires differential discharging of the bit line capacitance. It detects the input after building up the certain amount of charge on the bit line capacitance.

2. **Current Mode Sense Amplifier** - It operates by sensing the bit cell current directly. It converts and amplifies a small current difference into CMOS voltage levels. It does not depend on the differential voltage across the bit lines. They provide low common input/output impedance, hence less sensing delay. The small input impedance at bit line results in less voltage swing, substrate currents and cross talk, but at the cost of large area and high power consumption.

For optimized SRAM, balancing act among delay, area and power consumption is required. Thus full CMOS latch type voltage mode sense amplifier is studied further. In this work, conventional voltage mode sense amplifier (CVSA) is addressed as shown in Figure 5.13.

CVSA consists of a differential input stage and a pair of the cross coupled inverter. Transistors $M1-M2$ form the differential input stage, which amplifies the difference of input signals. Transistors $M3-M6$ act as the cross coupled inverter that generates positive feedback to the output. Transistor $M10$ is used for equalization to reduce the aperture time of sense amplifier. The operation of the circuit is performed in two phases

by controlling the gate voltages of transistors $M7$, $M8$ and $M9$. In the first phase called precharge, the clock remains low and $M7 - M8$ keep all the internal nodes to the high level. In the second phase called evaluation, the clock is kept high which turns on $M9$ and provides current. In this phase, sense amplifier determines the polarity of the input signal. $M1 - M2$ converts the differential input voltage to the differential current which creates charge imbalance in $M4$ and $M6$. This results in one of the output nodes to discharge faster than the other. When both the outputs have significant differential voltage, then positive feedback of $M3 - M6$ pushes the lower voltage to ground and pulls the higher voltage to supply voltage (V_{DD}). Conduction of $M10$ starts just before the positive feedback action, shortens the source nodes of $M4$ and $M6$ which isolates the regenerative nodes from the input signal applied at the gates of $M1$ and $M2$. After the evaluation phase, all the internal nodes will rise to voltage of logic 1.

5.7.1 Output Metric: The Sensing Delay

The speed of the read operation depends on the delay (sensing delay) of the sense amplifier. It is the time between when the sense amplifier clock (CLK) signal reaches 50% of the V_{DD} and any of the output signal (OUT or OUTBAR) reaches 50% of the V_{DD}. Figure 5.14 shows the sensing delay between CLK and OUT (read 0) signal. For Figure 5.13 nominal values of sensing delay are 8.237ps and 8.175ps, for read 0 and read 1 respectively in 45nm technology node. This delay is affected by the variations and aging in transistor parameters, which enhances the time of read operation.

5.8 Effect of Process Variation on Sensing Delay

Process variations are the natural fluctuations that exist in transistor parameters (width, length, oxide thickness) at the time of manufacturing. It is difficult to fabricate a large number of devices on a chip that works within specified limits. Global variations affect all devices in an equal manner but local variations affect all devices differently, hence are more severe [158]. MOS transistor dimensions and V_{TH} are the key parameters that control the device drive current. Further, the device delay depends on this drive current. Thus statistical variations in transistor dimensions and V_{TH} causes significant variation in the sensing delay. In the worst case, it may amplify the input signal in the

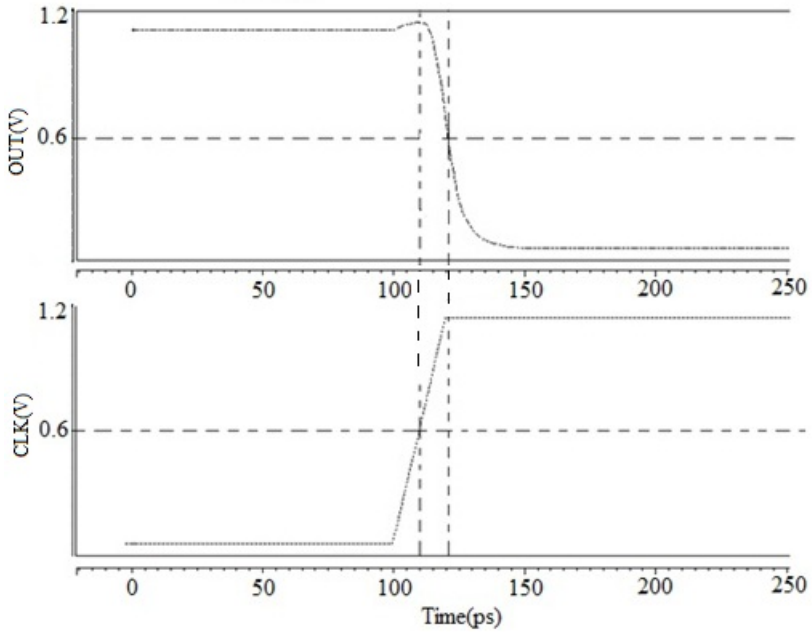


Figure 5.14: Output Metric: Sensing Delay

wrong direction due to incorrect sensing. In this work, channel width (W) is chosen to show the impact of variability on delay. Delay is inversely proportional to channel width. The effect of width variation on sensing delay is analyzed by using 1000 monte carlo simulations. Figure 5.15 shows the impact of width variation on sensing delay (read 0) of the sense amplifier. Each symbol corresponds to single monte carlo run. It is observed that 10% variation in width from the nominal value, causes 8% variation in sensing delay.

5.9 Effect of Aging on Sensing Delay

BTI attributes increment in absolute value of V_{TH}. In sense amplifier design V_{TH} variation can cause operational failure. Let we consider the Figure 5.13, if there is a V_{TH} mismatch between M1 and M2 due to BTI effect, the current in M2 could be larger even if the input voltage of M1 is higher. This generates a faster discharge of voltage at the output node (OUT) which causes the circuit to flip in the wrong direction, due to the current mismatch. V_{TH} variation also induces failure due to trip point mismatch in the cross coupled inverters (M3-M6) and lead to flipping in the wrong direction. This BTI induced V_{TH} variation also effects the sensing delay. The drain current of a transistor in the saturation region can be defined as

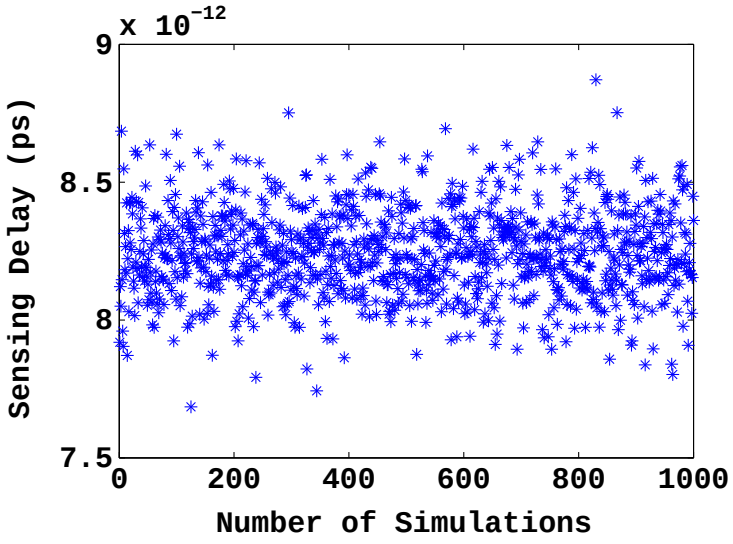


Figure 5.15: Effect of Width variation on Sensing Delay

$$I_d = \beta(V_{gs} - V_{TH})^{\alpha} \tag{5.9.1}$$

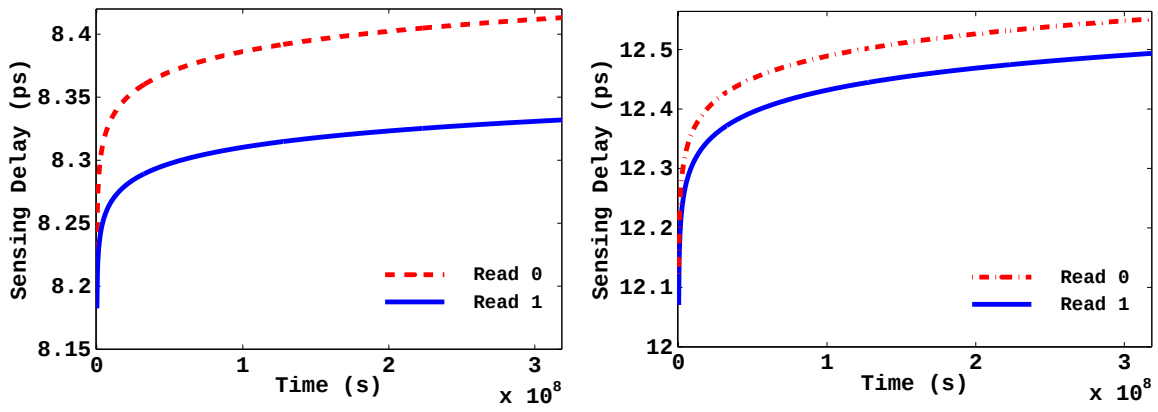
where α is majority carriers velocity saturation index [159]. The delay of a gate can be given as

$$\tau = \frac{C_L V_{DD}}{I_d} = \frac{K_1}{(V_{gs} - V_{TH})^{\alpha}} \tag{5.9.2}$$

where C_L is the load capacitance. Differentiating with respect to V_{TH} we get

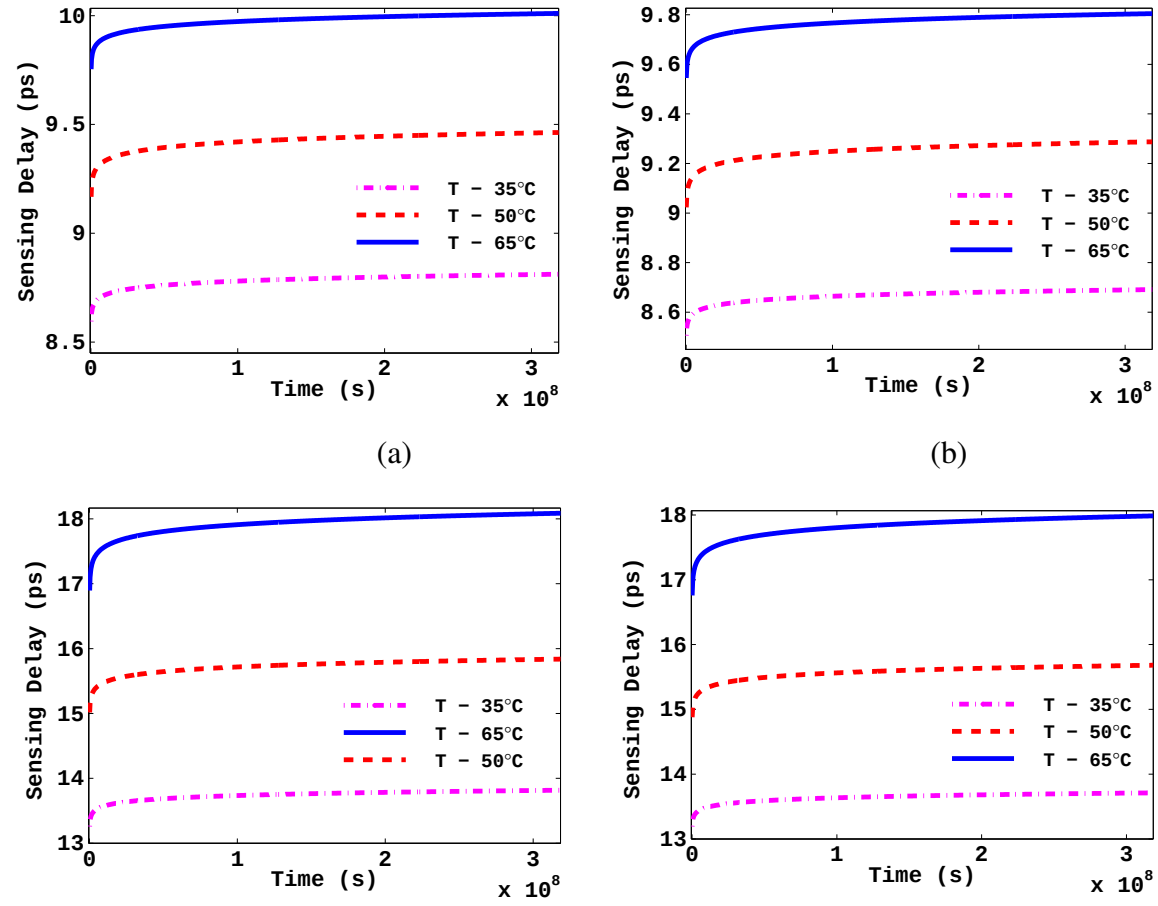
$$\frac{\triangle\tau}{\tau} = \frac{\alpha\Delta V_{TH}}{(V_{gs} - V_{TH})} \tag{5.9.3}$$

NBTI (PBTI) causes ΔV_{TH} increment of PMOS (NMOS) transistor, hence delay increases in both cases. Figure 5.16(a) and 5.16(b) shows the impact of PBTI and NBTI on sensing delay for both read 0 and read 1 respectively. At room temperature, for both read 0 and read 1, PBTI causes 2.19% and 1.96% variation and NBTI causes 52.48% and 52.90% variation in sensing delay respectively. The BTI effect enhances at high temperatures. Figure 5.17 shows the integrated effect of temperature and BTI (PBTI and NBTI) on sensing delay. It is evident from the Figure 5.17 that both PBTI and NBTI effect enhances by increasing temperature, which further increases the delay. Table 5.5 shows the values of sensing delay after one year due to BTI at different temperatures. It is seen from the Table 5.5 that NBTI gets worse at a higher temperature.



(a) (b)

Figure 5.16: Effect of BTI on Sensing Delay (a) PBTI (b) NBTI



(a) (b)

(c) (d)

Figure 5.17: Integrated effect of Temperature and BTI on Sensing Delay (a) PBTI read 0 (b) PBTI read 1 (c) NBTI read 0 (d) NBTI read 1

Table 5.5: Sensing Delay under BTI effect at different Temperatures after one year

Operation	Temperature ($^{\circ}C$)	Delay (ps)	
		PBTI	NBTI
Read 0	35	8.745	13.64
	50	9.372	15.58
	65	9.930	17.71
Read 1	35	8.634	13.55
	50	9.206	15.43
	65	9.721	17.60

5.10 Effect of Process Corners on Sensing Delay

In this section we will analyze the effect of different process corners on the sensing delay of the sense amplifier. Five process corners (PC) are considered; Nominal-Nominal (NN), Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS), and Slow-Fast (SF). Here the first letter represents NMOS transistor and second represents PMOS transistor (for e.g., in FS corner, F represent NMOS and S represent PMOS). Three parameters V_{TH}, V_{DD} and temperature are chosen to show the impact of process corners on sensing delay. Variation in all these parameters are given as [146] below :

- To account for inter die variation, 2% variation is assumed in nominal V_{TH} which yields low, nominal and high values. For NMOS transistor corresponding values are 0.456V, 0.466V and 0.475V. For PMOS transistor corresponding values are -0.403V, -0.4118V and -0.42V.
- 10% variation is considered in nominal V_{DD} (1.2V) value which results into three different values of V_{DD} i.e., 1.08V, 1.2V and 1.32V.
- The temperature of the device varies due to work environment and work load. To account for temperature change three different temperatures 35°, 50° and 65° are considered.

Table 5.6 shows the effect of different process corners on sensing delay. It is evident that for FF corner when both NMOS and PMOS have minimum V_{TH} values, delay reduces to lowest value and transistor speed increases. Similarly, for SS corner when both NMOS and PMOS have maximum V_{TH} values, delay increases to highest value and transistor speed reduces. NN corner falls between these two. Delay is inversely

Table 5.6: Effect of Process Corners on Sensing Delay

PC	V_{TH} (V) NMOS/PMOS	Temperature ($^{\circ}C$)		
		35	50	65
		Sensing Delay (ps)		
		Read 0/Read 1	Read 0/Read 1	Read 0/Read 1
V_{DD}= 1.2V				
NN	0.466/-0.4118	8.580/8.498	9.150/9.010	9.749/9.554
SF	0.475/-0.403	8.723/8.624	9.311/9.151	9.918/9.709
FS	0.456/-0.420	8.421/8.359	8.979/8.858	9.560/9.389
FF	0.456/-0.403	8.413/8.350	8.968/8.849	9.549/9.379
SS	0.475/-0.420	8.743/8.633	9.320/9.160	9.927/9.719
V_{DD}= 1.32V				
NN	0.466/-0.4118	7.809/7.705	8.274/8.176	8.802/8.681
SF	0.475/-0.403	7.909/7.807	8.388/8.289	8.943/8.809
FS	0.456/-0.420	7.701/7.593	8.152/8.052	8.646/8.541
FF	0.456/-0.403	7.694/7.584	8.145/8.042	8.635/8.532
SS	0.475/-0.420	7.916/7.816	8.399/8.299	8.954/9.719
V_{DD}= 1.08V				
NN	0.466/-0.4118	9.826/9.681	10.440/10.330	11.100/11.00
SF	0.475/-0.403	10.00/9.875	10.640/10.530	11.310/11.23
FS	0.456/-0.420	9.639/9.460	10.240/10.100	10.870/10.76
FF	0.456/-0.403	9.630/9.447	10.230/10.090	10.860/10.74
SS	0.475/-0.420	10.010/9.886	10.650/10.540	11.320/11.24

proportional to V_{DD}. It is observed that as V_{DD} decreases to 1.08V, delay increases to maximum values across all process corners at different temperatures. Similarly, for V_{DD} = 1.32V, delay decreases to minimum values. It is evident as temperature increases under different V_{DD}, delay also increases and reaches to a maximum at 65$^{\circ}C$ across all process corners.

5.11 Surrogate Model for Sensing Delay

The aim of this work, is to develop the variability and reliability aware SVM regression model for sensing delay. In this work, 45 nm PTM model is used for all the simulations performed. To illustrate the effect of process variation and aging, the sense amplifier circuit (Figure 5.13) is chosen. HSPICE is used to draw initial samples for further model development. LS-SVM toolbox is coupled in MATLAB to generate the surrogate model. This section explains the surrogate model development flow for proposed work.

In order to develop any surrogate model; input variables need to be defined first.

Channel width is crucial in an analog circuit sizing and yield improvement. Thus it is taken as one of the input parameters to show the variability effect. BTI impacts the V_{TH} of the

transistor, so taken as another input parameter. Hence (W, V_{THN}, V_{THP}) forms tuple of input sample which is represented as $X_i = f(W, V_{THP}, V_{THN})$. Here V_{THP} and V_{THN} are the threshold voltages of PMOS and NMOS transistors respectively. Figure 5.18 shows the flowchart to develop a SVM model which is explained as follows:

1. Initially, design problem and variables of input sample vector are specified.

2. Now input samples are generated for variability and reliability analysis. In variability analysis, every variable follows the gaussain distribution. Thus width samples are generated around mean value, following the gaussian random distribution. Aging is a time dependent phenomenon. Thus time samples are generated through LHS sampling within the lower and upper bound. These time samples are used to generate V_{TH} degradation of PMOS and NMOS transistor i.e., V_{THP} and V_{THN}.

3. HSPICE is used for circuit simulations to generate output performance parameter (sensing delay samples) for corresponding input samples. These input and output samples are used to develop initial SVM regression model.

4. To develop SVM model with less number of samples, initially SVM is trained with few input and output samples (obtained in step 3). Samples which are used to train the model are called training samples. For testing purpose, another set of samples has been used which are called testing samples. Accuracy is checked by finding correlation coefficient between SVM and HSPICE. If target accuracy is achieved then the final model is prepared.

5. If accuracy is not achieved then adaptive learning is used, till the desired accuracy has not been obtained.

6. These new samples are again passed through SPICE circuit simulations in order to get output training samples. These new input and output samples are added to previous training samples.

7. Now SVM model is trained again and accuracy is checked. This process is repeated until the desired accuracy has been achieved. After that final SVM model is prepared.

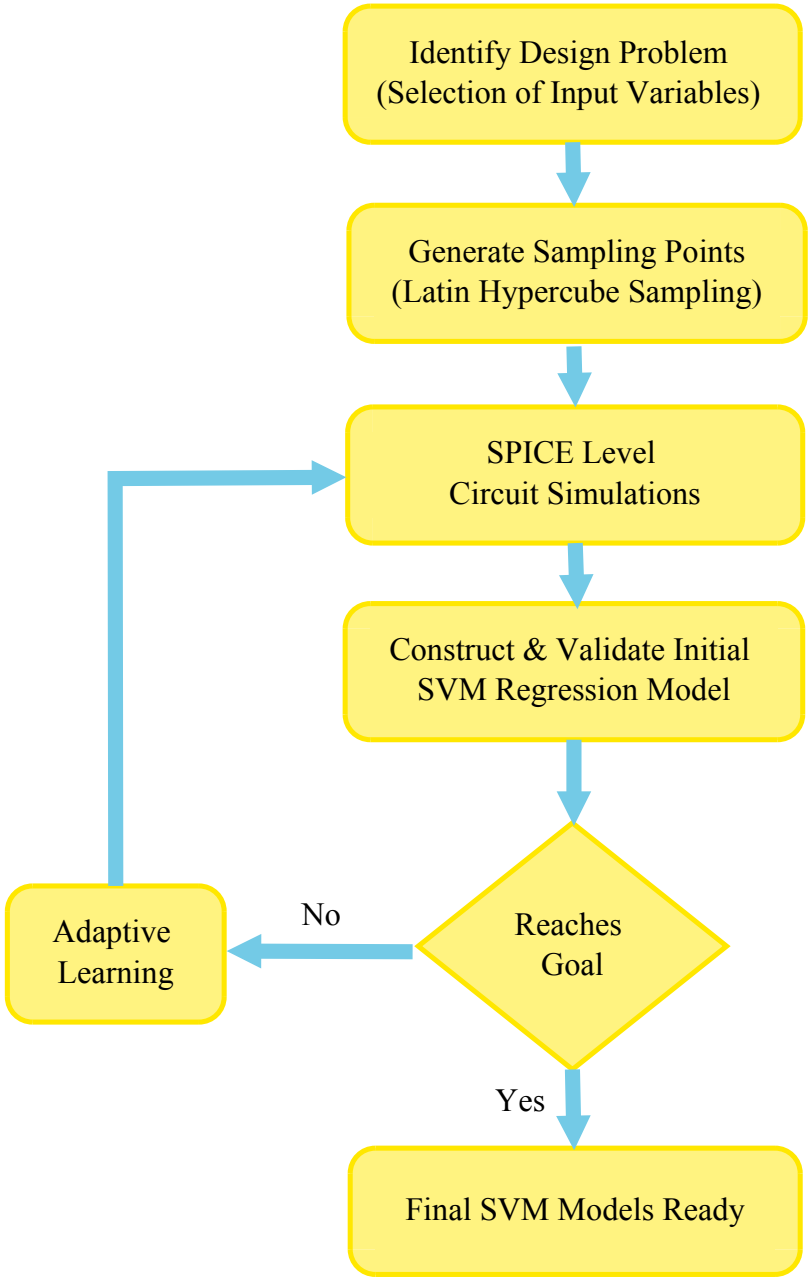


Figure 5.18: Methodology to develop the SVM Regression Model

In this work two SVM models have been developed; for read 0 and read 1.

5.12 Results

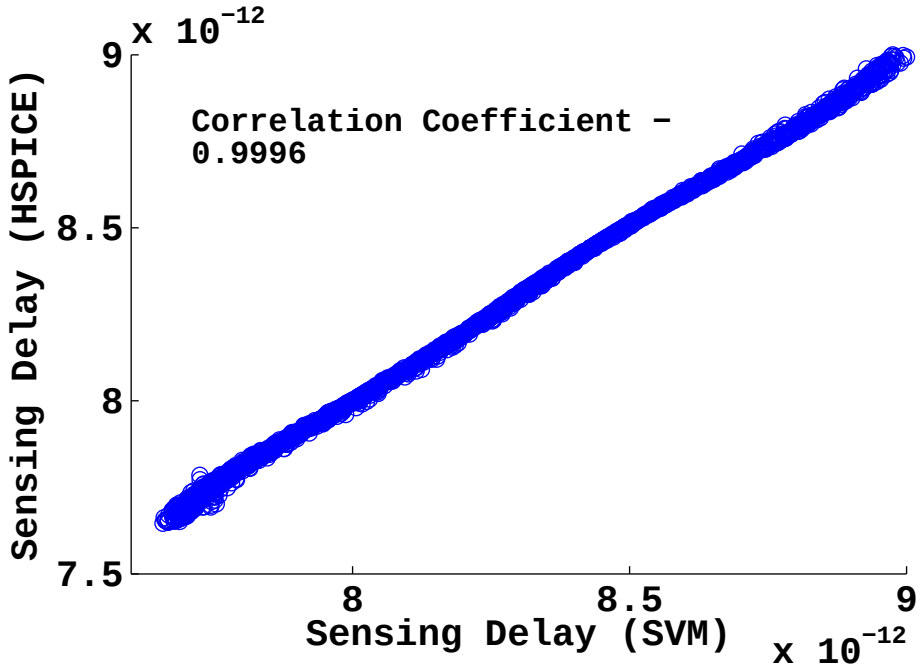
In this work SVM based variability and reliability aware surrogate model is developed for 45nm technology node. Initially, 3000 input samples of W, V_{THN} and V_{THP} are generated within given range. Then circuit simulations have been done using these input samples to produce 3000 output samples of sensing delay. Initially, 100 training and 2900 testing, samples are used to develop SVM model for both read 0 and read 1 case. These samples results in 0.9894 and 0.9889 correlation coefficient in read 0 and read 1 case respectively, which is not accurate enough. Then adaptive learning is used that results into 483 and 489 training samples for read 0 and read 1 respectively, which finally increases correlation coefficient. Correlation coefficient and run time for both models are shown in Table 5.7. Figure 5.19(a) and 5.19(b) shows the correlation curves between HSPICE and SVM model for both read 0 and read 1 case. These curves are linear which show that SVM model is closely associated with HSPICE output. These curves also shows the significant variation in sensing delay by variation in width and V_{TH} values.

Table 5.7: Correlation Coefficient and Run Time for Regression Model of Sensing Delay

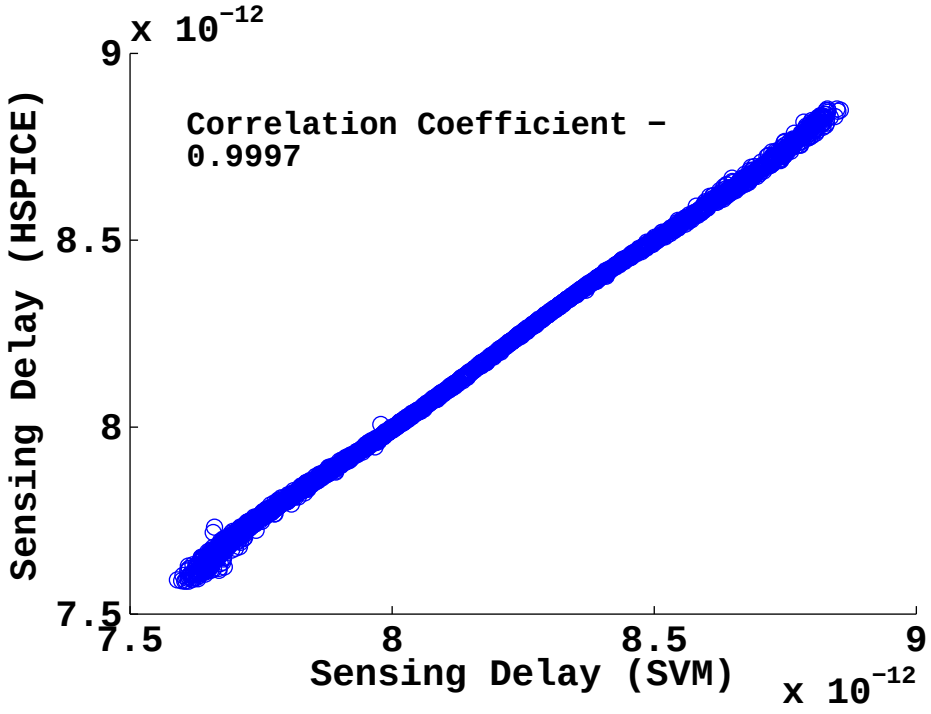
	Read 0	Read 1
Correlation Coefficient	0.9996	0.9997
Run Time	0.077ms	0.081ms

5.13 Summary

This work presents a SVM based variability and reliability aware surrogate model for sensing delay of the sense amplifier. The effects of process variation and aging are analyzed on SRAM sense amplifier. Sensing delay increases due to aging effect. Width variation due to variability also causes a shift in delay from its nominal value. It shows that both variability and aging poses a threat in nano scale regimes. It has been observed that PBTI impact is less severe in comparison to NBTI on sensing delay for both read 0 and read 1 case. It has also been observed that BTI effect increases with temperature, which enhances delay degradation. Sense amplifier has also been simulated at different process corners with various V_{DD} and temperatures. It has been observed that under



(a)



(b)

Figure 5.19: Correlation Curves between SVM and HSPICE (a) read 0 (b) read 1

FF and SS corner, sense amplifier works in fastest and slowest mode respectively. At higher V_{DD} and lower temperature, delay decreases. Further SVM regression model has been developed by using adaptive learning for sensing delay of sense amplifier for both read 0 and read 1 case. Adaptive learning helps to reduce simulation time, by using few training samples while improving the accuracy to the desired level. Correlation coefficient and correlation curve are used to check the accuracy of the model. The values of correlation coefficient are 0.9996 and 0.9997 for read 0 and read 1 respectively, which shows that our models are highly accurate.

Chapter 6

Conclusions & Future Work

Aggressive scaling introduces the reliability issue which causes the circuit performances to deviate from it's specified values. An accurate and quick prediction of performance degradation is required during design phase at the circuit level. The previous reliability simulation tools are built around the SPICE simulator which are computation intensive. In present work, the surrogate models of analog circuit performances are developed to improve the simulation efficiency. These surrogate models are as accurate as SPICE and require less simulation time.

We have developed NBTI aware surrogate model for the analog circuit which is based on machine learning technique i.e., SVM. Initially, we have developed a feasibility based surrogate model using SVM classifier to find feasibility design space. Feasibility design space identifies and exclude the insignificant training samples which speed up the simulation time for the regression model. Then the performance based surrogate models are developed using SVM regressor for the gain and the slew-rate of a differential amplifier. To generate SVM models using the minimum number of training samples, we have employed sampling method using both adaptive learning and LHS. Adaptive learning chooses samples adaptively, resulting in less simulation time. These SVM models are found not only faster than SPICE simulations and but also highly accurate. The proposed SVM surrogate models are kernel based black box models and can be used in place of SPICE simulations using proper sampling method. The RBF kernel is used in all simulations.

We have also presented NBTI aware SVM based long term aging model for the analog circuit. For long term aging simulation, we have proposed a dynamic time step

algorithm. The proposed algorithm update the stress condition adaptively to get the accurate aging degradation at the end of the lifetime. The proposed algorithm closely matches the minimum constant step size using very less simulation time. Further, we have developed a long term transistor level surrogate model which provides the NBTI degradation of all the transistors in the circuit individually. These transistor level models are also extended to circuit level surrogate model for performance parameter i.e., gain of common source amplifier.

Further we have proposed a mitigation technique to reduce the NBTI effect in SRAM cell. The proposed technique is a combination of previous two mitigation techniques i.e., V_{DD} tuning and V_{BL} reduction. The proposed method improves the read stability i.e., SNM without degrading the other read parameters i.e., read power and read current. We have also developed process and aging aware SVM surrogate model for sensing delay of the sense amplifier. The effect of different process corners on sensing delay have also been studied.

We believe that SVM based surrogate models can be used in CAD tools for future technologies to accurately model the aging effect on different performance parameters of analog circuits and to predict their reliability.

Future Work

Since proposed SVM surrogate models are based on single aging effect i.e., NBTI. These models can be extended by including the impact of other aging phenomena like HCI and TDDB. Apart from RBF kernel, other kernels based exploration to develop aging aware model can be good area of further research. Further finding out new kernels for more accurate and faster SVM models is also a good future direction. Different combination of compensation techniques can be explored to mitigate the NBTI effect. Hardware circuits can be designed to implement these compensation techniques. Not only sense amplifier but the surrogate model of other peripheral circuit of SRAM can be proposed.

List of Publications out of thesis work

Accepted / Published

- S. Khandelwal, L. Garg, and D. Boolchandani, "Reliability-aware support vector machine-based high-level surrogate model for analog circuits," IEEE Transactions on Device and Materials Reliability, vol. 15, no. 3, pp. 461–463, Sept 2015.

- S. Khandelwal, K. Singh, L. Garg, and D. Boolchandani,"NBTI-aware bit line voltage control with boosted supply voltage for improvement of 6T SRAM cell read stability," in 2015 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Sept 2015, pp. 1–4.

- S. Khandelwal, L. Garg, and D. Boolchandani, "Variability and Reliability Aware Surrogate Model for Sensing Delay Analysis of SRAM Sense Amplifier" in 20th International Symposium on VLSI Design and Test (VDAT), May 2016, pp. 1-6.

Submitted

- "NBTI Aware Machine Learning Based Long Term Model for Analog Circuit" in Microelectronics Journal.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, April 1965.

[2] L. Gerrer, J. Ding, S. Amoroso, F. Adamu-Lema, R. Hussin, D. Reid, C. Millar, and A. Asenov, "Modelling rtn and bti in nanoscale mosfets from device to circuit: A review," *Microelectronics Reliability*, vol. 54, no. 4, pp. 682 – 697, 2014.

[3] "International technology roadmap for semiconductors," 2015.

[4] J. Lienig and H. Bruemmer, *Fundamentals of Electronic Systems Design*, 1st ed. Springer Publishing Company, Incorporated, 2017.

[5] E. Maricau and G. Gielen, *Analog IC Reliability Simulation*. New York, NY: Springer New York, 2013, pp. 93–149.

[6] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *Journal of Applied Physics*, vol. 94, no. 1, pp. 1–18, 2003.

[7] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the surface state charge (qss) of thermally oxidized silicon," *Journal of The Electrochemical Society*, vol. 114, no. 3, pp. 266–274, 1967.

[8] M. A. Alam, H. Kufluoglu, D. Varghese, and S. Mahapatra, "A comprehensive model for pmos nbti degradation: Recent progress." *Microelectronics Reliability*, vol. 47, no. 6, pp. 853–862, 2007.

[9] S. Mahapatra, M. Alam, P. B. Kumar, T. Dalei, D. Varghese, and D. Saha, "Negative bias temperature instability in cmos devices," *Microelectronic Engineering*,

vol. 80, no. 0, pp. 114 – 121, 2005, 14th biennial Conference on Insulating Films on Semiconductors INFOS2005.

[10] J. Stathis and S. Zafar, "The negative bias temperature instability in mos devices: A review," *Microelectronics Reliability*, vol. 46, no. 2, pp. 270 – 286, 2006.

[11] F. Crupi, C. Pace, G. Cocorullo, G. Groeseneken, M. Aoulaiche, and M. Houssa, "Positive bias temperature instability in nmosfets with ultra-thin hf-silicate gate dielectrics," *Microelectronic Engineering*, vol. 80, pp. 130 – 133, 2005, 14th biennial Conference on Insulating Films on Semiconductors.

[12] N. Aymerich, S. Ganapathy, A. Rubio, R. Canal, and A. GonzÃ¡lez, "Impact of positive bias temperature instability (pbti) on 3t1d-dram cells," *Integration, the VLSI Journal*, vol. 45, no. 3, pp. 246 – 252, 2012, special Issue of GLSVLSI 2011: Current Trends on VLSI and Ultra Low-Power Design.

[13] F. J. Grunthaner, P. J. Grunthaner, R. P. Vasquez, B. F. Lewis, J. Maserjian, and A. Madhukar, "Local atomic and electronic structure of oxide/gaas and sio2/si interfaces using high resolution xps," *Journal of Vacuum Science and Technology*, vol. 16, no. 5, pp. 1443–1453, 1979.

[14] R. Entner, "Modeling and simulation of negative bias temperature instability," *PhD thesis, Technische Universitat Wien*, April 2007.

[15] D. K. Schroder, "Negative bias temperature instability: What do we understand?" *Microelectronics Reliability*, vol. 47, no. 6, pp. 841 – 852, 2007, modelling the Negative Bias Temperature Instability.

[16] A. H. Edwards, "Interaction of h and h2 with the silicon dangling orbital at the 111 si/sio2 interface," *Phys. Rev. B*, vol. 44, pp. 1832–1838, Jul 1991.

[17] B. Ziaie, A. Baldi, and M. Atashbar, *Introduction to Micro/Nanofabrication*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2007, pp. 197–238.

[18] J. Segura and C. F. Hawkins, *CMOS Electronics: How It Works, How It Fails*. John Wiley & Sons, 2004.

[19] T. J. J. Ho, D. S. Ang, A. A. Boo, Z. Q. Teo, and K. C. Leong, "Are interface state generation and positive oxide charge trapping under negative-bias temperature stressing correlated or coupled?" *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 1013–1022, April 2012.

[20] I. T. J. W. R. C. I. T. C. on the Physics of SiO2, its Interfaces, and S. Pantelides, *The Physics of SiO2 and Its Interfaces: Proceedings of the International Topical Conference Held at the IBM Thomas J. Watson Research Center New York, 1978*, 1978.

[21] K. O. Jeppson and C. M. Svensson, "Negative bias stress of mos devices at high electric fields and degradation of mnos devices," *Journal of Applied Physics*, vol. 48, no. 5, pp. 2004–2014, 1977.

[22] S. Mahapatra, "Fundamentals of bias temperature instability in mos transistors," *Springer Series in Advanced Microelectronics*, vol. 52, no. 1, pp. XVI, 269, 2016.

[23] W. Wang, V. Reddy, A. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact modeling and simulation of circuit reliability for 65-nm cmos technology," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 509–517, 12 2007.

[24] E. Maricau and G. Gielen, "Analog ic reliability in nanometer cmos," *Analog Circuits and Signal Processing*, no. 1, pp. XVI, 198, 2013.

[25] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Physical mechanisms of negative-bias temperature instability," *Applied Physics Letters*, vol. 86, no. 14, p. 142103, 2005.

[26] X. Pan and H. Graeb, "Degradation-aware analog design flow for lifetime yield analysis and optimization," in *16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009, Yasmine Hammamet, Tunesia, 13-19 December, 2009*, 2009, pp. 667–670.

[27] F. R. Chouard, S. More, M. Fulde, and D. Schmitt-Landsiedel, "An analog perspective on device reliability in 32nm high-3ba; metal gate technology."

[28] S. Rauch, "The statistics of nbti-induced vt and beta; mismatch shifts in pmosfets," *Device and Materials Reliability, IEEE Transactions on*, vol. 2, no. 4, pp. 89–93, Dec 2002.

[29] S. V. Bussche, P. D. Wit, E. Maricau, and G. G. E. Gielen, "Impact analysis of stochastic transistor aging on current-steering dacs in 32nm cmos," in *ICECS*, 2011.

[30] E. Maricau and G. G. E. Gielen, "Efficient variability-aware nbti and hot carrier circuit reliability analysis," *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol. 29, no. 12, pp. 1884–1893, 2010.

[31] S. Zafar, "Statistical mechanics based model for negative bias temperature instability induced degradation," *Journal of Applied Physics*, vol. 97, no. 10, p. 103709, 2005.

[32] M. A. Alam, "A critical examination of the mechanics of dynamic nbti for pmosfets," in *IEEE International Electron Devices Meeting 2003*, Dec 2003, pp. 14.4.1–14.4.4.

[33] J. Yang, J. Yang, X. Y. Liu, R. Q. Han, J. F. Kang, Z. H. Gan, C. C. Liao, and H. M. Wu, "A new model for two-dimensional electrical-field-dependent v_{th} instability of pmosfets with ultrathin dpn gate dielectrics," *IEEE Electron Device Letters*, vol. 32, no. 5, pp. 605–607, May 2011.

[34] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "An analytical model for negative bias temperature instability," in *2006 IEEE/ACM International Conference on Computer Aided Design*, Nov 2006, pp. 493–496.

[35] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and minimization of pmos nbti effect for robust nanometer design," in *2006 43rd ACM/IEEE Design Automation Conference*, July 2006, pp. 1047–1052.

[36] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive modeling of the nbti effect for reliable design," in *IEEE Custom Integrated Circuits Conference 2006*, Sept 2006, pp. 189–192.

[37] J. B. Velamala, K. Sutaria, T. Sato, and Y. Cao, "Physics matters: Statistical aging prediction under trapping/detrapping," in *DAC Design Automation Conference 2012*, June 2012, pp. 139–144.

[38] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 33–44.

[39] H. Kufluoglu, V. Reddy, A. Marshall, J. Krick, T. Ragheb, C. Cirba, A. Krishnan, and C. Chancellor, "An extensive and improved circuit simulation methodology for nbti recovery," in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 670–675.

[40] K. Joshi, S. Mukhopadhyay, N. Goel, and S. Mahapatra, "A consistent physical framework for n and p bti in hkmg mosfets," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, April 2012, pp. 5A.3.1–5A.3.10.

[41] S. Gupta, B. Jose, K. Joshi, A. Jain, M. A. Alam, and S. Mahapatra, "A comprehensive and critical re-assessment of 2-stage energy level nbti model," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, April 2012, pp. XT.3.1–XT.3.6.

[42] B. Yan, J. Qin, J. Dai, Q. Fan, and J. B. Bernstein, "Reliability simulation and circuit-failure analysis in analog and mixed-signal applications," *IEEE Transactions on Device and Materials Reliability*, vol. 9, no. 3, pp. 339–347, Sept 2009.

[43] E. Maricau and G. Gielen, "Efficient variability-aware nbti and hot carrier circuit reliability analysis," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 29, no. 12, pp. 1884–1893, Dec 2010.

[44] ——, "Variability-aware reliability simulation of mixed-signal ics with quasi-linear complexity," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2010*, March 2010, pp. 1094–1099.

[45] N. K. Jha, P. S. Reddy, D. K. Sharma, and V. R. Rao, "Nbti degradation and its impact for analog circuit reliability," *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2609–2615, Dec 2005.

[46] M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H. Muthali, and S. Jacobs, "Pmos nbti-induced circuit mismatch in advanced technologies," in *2004 IEEE International Reliability Physics Symposium. Proceedings*, April 2004, pp. 171–175.

[47] X. Li, B. Huang, J. Qin, X. Zhang, M. Talmor, Z. Gur, and J. Bernstein, "Deep submicron cmos integrated circuit reliability simulation with spice," in *Quality of Electronic Design, 2005. ISQED 2005. Sixth International Symposium on*, March 2005, pp. 382–389.

[48] X. Li, J. Qin, and J. Bernstein, "Compact modeling of mosfet wearout mechanisms for circuit-reliability simulation," *Device and Materials Reliability, IEEE Transactions on*, vol. 8, no. 1, pp. 98–121, March 2008.

[49] X. Li, J. Qin, B. Huang, X. Zhang, and J. Bernstein, "A new spice reliability simulation method for deep submicrometer cmos vlsi circuits," *Device and Materials Reliability, IEEE Transactions on*, vol. 6, no. 2, pp. 247–257, June 2006.

[50] F. Marc, B. Mongellaz, C. Bestory, H. Levi, and Y. Danto, "Improvement of aging simulation of electronic circuits using behavioral modeling," *Device and Materials Reliability, IEEE Transactions on*, vol. 6, no. 2, pp. 228–234, June 2006.

[51] J. Martin-Martinez, R. Rodriguez, M. Nafria, and X. Aymerich, "Time-dependent variability related to bti effects in mosfets: Impact on cmos differential amplifiers," *Device and Materials Reliability, IEEE Transactions on*, vol. 9, no. 2, pp. 305–310, June 2009.

[52] J. L. Wong, A. Davoodi, V. Khandelwal, A. Srivastava, and M. Potkonjak, "A statistical methodology for wire-length prediction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 7, pp. 1327–1336, July 2006.

[53] A. Lamecki, L. Balewski, and M. Mrozowski, "Towards automated full-wave design of microwave circuits," in *MIKON 2008 - 17th International Conference on Microwaves, Radar and Wireless Communications*, May 2008, pp. 1–2.

[54] B. Liu, N. Deferm, D. Zhao, P. Reynaert, and G. G. E. Gielen, "An efficient high-frequency linear rf amplifier synthesis method based on evolutionary computation and machine learning techniques," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 981–993, July 2012.

[55] S. Wen, Z. Zeng, and T. Huang, "Associative learning of integrate-and-fire neurons with memristor-based synapses," *Neural Process. Lett.*, vol. 38, no. 1, pp. 69–80, Aug. 2013.

[56] S. Wen, Z. Zeng, T. Huang, and G. Bao, "Robust passivity and passification for a class of singularly perturbed nonlinear systems with time-varying delays and polytopic uncertainties via neural networks," *Circuits, Systems, and Signal Processing*, vol. 32, no. 3, pp. 1113–1127, Jun 2013.

[57] L. Xia, I. M. Bell, and A. J. Wilkinson, "A robust approach for automated model generation," in *2009 4th International Conference on Design Technology of Integrated Systems in Nanoscal Era*, April 2009, pp. 281–286.

[58] J. Xu, M. C. E. Yagoub, R. Ding, and Q. J. Zhang, "Feedforward dynamic neural network technique for modeling and design of nonlinear telecommunication circuits and systems," in *Proceedings of the International Joint Conference on Neural Networks, 2003.*, vol. 2, July 2003, pp. 930–935 vol.2.

[59] G. Wolfe and R. Vemuri, "Extraction and use of neural network models in automated synthesis of operational amplifiers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 2, pp. 198–212, Feb 2003.

[60] S. Mohanty, E. Kougianos, and G. Zheng, "Intelligent metamodel integrated verilog-ams for fast and accurate analog block design exploration," May 2015, uS Patent 9,026,964.

[61] D. Gorissen, L. De Tommasi, W. Hendrickx, J. Croon, and T. Dhaene, "Rf circuit block modeling via kriging surrogates," in *Microwaves, Radar and Wireless Communications, 2008. MIKON 2008. 17th International Conference on*, May 2008, pp. 1–4.

[62] J. A. K. Suykens, "Nonlinear modelling and support vector machines," in *IMTC 2001. Proceedings of the 18th IEEE Instrumentation and Measurement Technology Conference. Rediscovering Measurement in the Age of Informatics (Cat. No.01CH 37188)*, vol. 1, May 2001, pp. 287–294 vol.1.

[63] M. Yelten, P. Franzon, and M. Steer, "Surrogate-model-based analysis of analog circuits; part i: Variability analysis," *Device and Materials Reliability, IEEE Transactions on*, vol. 11, no. 3, pp. 458–465, Sept 2011.

[64] ——, "Surrogate-model-based analysis of analog circuits; part ii: Reliability analysis," *Device and Materials Reliability, IEEE Transactions on*, vol. 11, no. 3, pp. 466–473, Sept 2011.

[65] D. Gorissen, L. De Tommasi, K. Crombecq, and T. Dhaene, "Sequential modeling of a low noise amplifier with neural networks and active learning," *Neural Computing and Applications*, vol. 18, no. 5, pp. 485–494, Jun 2009.

[66] L. Garg, "On efficient and accurate surrogate models of leakage in cmos gated circuits," *PhD thesis, Malaviya National Institute of Technology*, May 2016.

[67] D. Boolchandani, L. Garg, S. Khandelwal, and V. Sahula, "Variability aware yield optimal sizing of analog circuits using svm-genetic approach," in *Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), 2010 XIth International Workshop on*, Oct 2010, pp. 1–6.

[68] A. Ciccazzo, G. D. Pillo, and V. Latorre, "A svm surrogate model-based method for parametric yield optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 7, pp. 1224–1228, July 2016.

[69] B. Settles, "Active learning literature survey," University of Wisconsin–Madison, Computer Sciences Technical Report 1648, 2009.

[70] S. Tong and D. Koller, "Support vector machine active learning with applications to text classification," *J. Mach. Learn. Res.*, vol. 2, pp. 45–66, Mar. 2002.

[71] N. Roy and A. McCallum, "Toward optimal active learning through sampling estimation of error reduction," in *Proceedings of the Eighteenth International*

Conference on Machine Learning, ser. ICML '01. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., 2001, pp. 441–448.

[72] V. Ceperic, G. Gielen, and A. Baric, "Recurrent sparse support vector regression machines trained by active learning in the time-domain," *Expert Systems with Applications*, vol. 39, no. 12, pp. 10 933 – 10 942, 2012.

[73] B. Liu, D. Zhao, P. Reynaert, and G. Gielen, "Synthesis of integrated passive components for high-frequency rf ics based on evolutionary computation and machine learning techniques," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, no. 10, pp. 1458–1468, Oct 2011.

[74] E. Maricau, D. D. Jonghe, and G. Gielen, "Hierarchical analog circuit reliability analysis using multivariate nonlinear regression and active learning sample selection," in *2012 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2012, pp. 745–750.

[75] T. Zhu, M. B. Steer, and P. D. Franzon, "Surrogate model-based self-calibrated design for process and temperature compensation in analog/rf circuits," *IEEE Design Test of Computers*, vol. 29, no. 6, pp. 74–83, Dec 2012.

[76] F. D. Bernardinis, M. I. Jordan, and A. SangiovanniVincentelli, "Support vector machines for analog circuit performance representation," in *Proceedings 2003. Design Automation Conference (IEEE Cat. No.03CH37451)*, June 2003, pp. 964–969.

[77] T. Kiely and G. Gielen, "Performance modeling of analog integrated circuits using least-squares support vector machines," in *Proceedings Design, Automation and Test in Europe Conference and Exhibition*, vol. 1, Feb 2004, pp. 448–453 Vol.1.

[78] A. Toro-Frias, P. Martin-Lloret, J. Martin-Martinez, R. Castro-Lopez, E. Roca, R. Rodriguez, M. Nafria, and F. Fernandez, "Reliability simulation for analog ics: Goals, solutions, and challenges," *Integration, the VLSI Journal*, vol. 55, no. Supplement C, pp. 341 – 348, 2016.

[79] E. Afacan, G. Berkol, G. Dundar, A. E. Pusane, and F. Baskaya, "A deterministic aging simulator and an analog circuit sizing tool robust to aging phenomena," in *2015 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Sept 2015, pp. 1–4.

[80] B. Eghbalkhah, M. Kamal, H. Afzali-Kusha, A. Afzali-Kusha, M. B. Ghaznavi-Ghoushchi, and M. Pedram, "Workload and temperature dependent evaluation of bti-induced lifetime degradation in digital circuits," *Microelectronics Reliability*, vol. 55, no. 8, pp. 1152 – 1162, 2015.

[81] F. Salfelder and L. Hedrich, "Ageing simulation of analogue circuits and systems using adaptive transient evaluation," in *2015 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2015, pp. 1261–1264.

[82] K. B. Sutaria, A. Mohanty, R. Wang, R. Huang, and Y. Cao, "Accelerated aging in analog and digital circuits with feedback," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 3, pp. 384–393, Sept 2015.

[83] Y. Cao, J. Velamala, K. Sutaria, M. S. W. Chen, J. Ahlbin, I. S. Esqueda, M. Bajura, and M. Fritze, "Cross-layer modeling and simulation of circuit reliability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 1, pp. 8–23, Jan 2014.

[84] K. Sutaria, A. Ramkumar, R. Zhu, R. Rajveev, Y. Ma, and Y. Cao, "Bti-induced aging under random stress waveforms: Modeling, simulation and silicon validation," in *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, June 2014, pp. 1–6.

[85] X. Li, J. Qin, B. Huang, X. Zhang, and J. B. Bernstein, "Sram circuit-failure modeling and reliability simulation with spice," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2, pp. 235–246, June 2006.

[86] K. Kang, M. A. Alam, and K. Roy, "Characterization of nbti induced temporal performance degradation in nano-scale sram array using iddq," in *2007 IEEE International Test Conference*, Oct 2007, pp. 1–10.

[87] X. Li, J. Qin, B. Huang, X. Zhang, and J. Bernstein, "Sram circuit-failure modeling and reliability simulation with spice," *Device and Materials Reliability, IEEE Transactions on*, vol. 6, no. 2, pp. 235–246, June 2006.

[88] K. Kang, H. Kufluoglu, K. Roy, and M. A. Alam, "Impact of negative-bias temperature instability in nanoscale sram array: Modeling and analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 10, pp. 1770–1781, Oct 2007.

[89] A. Carlson, "Mechanism of increase in sram vmin due to negative-bias temperature instability," *Device and Materials Reliability, IEEE Transactions on*, vol. 7, no. 3, pp. 473–478, Sept 2007.

[90] T.-H. Kim, W. Zhang, and C. Kim, "An sram reliability test macro for fully-automated statistical measurements of vmin degradation," in *Custom Integrated Circuits Conference, 2009. CICC '09. IEEE*, Sept 2009, pp. 231–234.

[91] W. Abadeer and W. Ellis, "Behavior of nbti under ac dynamic circuit conditions," in *2003 IEEE International Reliability Physics Symposium Proceedings, 2003. 41st Annual.*, March 2003, pp. 17–22.

[92] M. Basoglu, M. Orshansky, and M. Erez, "Nbti-aware dvfs: A new approach to saving energy and increasing processor lifetime," in *2010 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, Aug 2010, pp. 253–258.

[93] E. Mintarno, J. Skaf, R. Zheng, J. B. Velamala, Y. Cao, S. Boyd, R. W. Dutton, and S. Mitra, "Self-tuning for maximized lifetime energy-efficiency in the presence of circuit aging," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 5, pp. 760–773, May 2011.

[94] L. Zhang and R. P. Dick, "Scheduled voltage scaling for increasing lifetime in the presence of nbti," in *2009 Asia and South Pacific Design Automation Conference*, Jan 2009, pp. 492–497.

[95] A. Calimera, E. Macii, and M. Poncino, "Nbti-aware power gating for concurrent leakage and aging optimization," in *Proceedings of the 2009 ACM/IEEE Interna-*

tional Symposium on Low Power Electronics and Design, ser. ISLPED '09. New York, NY, USA: ACM, 2009, pp. 127–132.

[96] ——, "Energy-optimal sram supply voltage scheduling under lifetime and error constraints," in *2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC)*, May 2013, pp. 1–6.

[97] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and minimization of pmos nbti effect for robust nanometer design," in *Design Automation Conference, 2006 43rd ACM/IEEE*, 2006, pp. 1047–1052.

[98] J. Singh and N. Vijaykrishnan, "A highly reliable nbti resilient 6t sram cell," *Microelectronics Reliability*, vol. 53, no. 4, pp. 565 – 572, 2013.

[99] J. C. Lin, A. S. Oates, and C. H. Yu, "Time dependent vccmin degradation of sram fabricated with high-k gate dielectrics," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, April 2007, pp. 439–444.

[100] A. T. Krishnan, V. Reddy, D. Aldrich, J. Raval, K. Christensen, J. Rosal, C. O'Brien, R. Khamankar, A. Marshall, W. K. Loh, R. McKee, and S. Krishnan, "Sram cell static noise margin and vmin sensitivity to transistor degradation," in *2006 International Electron Devices Meeting*, Dec 2006, pp. 1–4.

[101] T. Kim and Z. Kong, "Impacts of NBTI/PBTI on SRAM VMIN and design techniques for SRAM VMIN improvement," in *Journal of Semiconductor Technology and Science*, 2013, pp. 87–97.

[102] M. M. Khellah, A. Keshavarzi, D. Somasekhar, T. Karnik, and V. De, "Read and write circuit assist techniques for improving vccmin of dense 6t sram cell," in *2008 IEEE International Conference on Integrated Circuit Design and Technology and Tutorial*, June 2008, pp. 185–188.

[103] Y. Kunitake, T. Sato, and H. Yasuura, "A case study of short term cell-flipping technique for mitigating nbti degradation on cache," in *2nd Asia Symposium on Quality Electronic Design (ASQED)*, Aug 2010, pp. 301–307.

[104] S. V. Kumar, K. H. Kim, and S. S. Sapatnekar, "Impact of nbti on sram read stability and design for reliability," in *7th International Symposium on Quality Electronic Design (ISQED'06)*, March 2006, pp. 6 pp.–218.

[105] D. R. Bild, R. P. Dick, and G. E. Bok, "Static nbti reduction using internal node control," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 17, no. 4, pp. 45:1–45:30, Oct. 2012.

[106] M. Khellah, Y. Ye, N. Kim, D. Somasekhar, G. Pandya, A. Farhang, K. Zhang, C. Webb, and V. De, "Wordline bitline pulsing schemes for improving sram cell stability in low-vcc 65nm cmos designs," in *2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers.*, June 2006, pp. 9–10.

[107] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "A 3-ghz 70mb sram in 65nm cmos technology with integrated column-based dynamic power supply," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, Feb 2005, pp. 474–611 Vol. 1.

[108] S. Mukhopadhyay, K. Kim, H. Mahmoodi, A. Datta, D. Park, and K. Roy, "Self-repairing sram for reducing parametric failures in nanoscaled memory," in *2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers.*, June 2006, pp. 132–133.

[109] M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, S. Imaoka, H. Makino, Y. Yamagami, S. Ishikura, T. Terano, T. Oashi, K. Hashimoto, A. Sebe, G. Okazaki, K. Satomi, H. Akamatsu, and H. Shinohara, *A 45nm low-standby-power embedded SRAM with improved immunity against process and temperature variations*, 2007.

[110] H. Mostafa, M. Anis, and M. Elmasry, "Nbti and process variations compensation circuits using adaptive body bias," *Semiconductor Manufacturing, IEEE Trans. on*, vol. 25, no. 3, pp. 460–467, Aug 2012.

[111] M. Yamaoka, N. Maeda, Y. Shimazaki, and K. Osada, "65nm low-power high-density sram operable at 1.0v under 3 sigma systematic variation using separate

vth monitoring and body bias for nmos and pmos," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2008, pp. 384–622.

[112] K. Jung and S. Kang, "Design techniques for improving SRAM cell stablity in advanced technology," Technical report, University of California, Berkeley, Tech. Rep.

[113] S. Hamdioui and A. J. V. D. Goor, "An experimental analysis of spot defects in srams: realistic fault models and tests," in *Proceedings of the Ninth Asian Test Symposium*, 2000, pp. 131–138.

[114] S. Khan, M. Taouil, S. Hamdioui, H. Kukner, P. Raghavan, and F. Catthoor, "Impact of partial resistive defects and bias temperature instability on sram decoder reliablity," in *2013 8th IEEE Design and Test Symposium*, Dec 2013, pp. 1–6.

[115] I. Agbo, M. Taouil, S. Hamdioui, P. Weckx, S. Cosemans, P. Raghavan, F. Catthoor, and W. Dehaene, "Quantification of sense amplifier offset voltage degradation due to zero-and run-time variability," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2016, pp. 725–730.

[116] M. H. Abu-Rahma, Y. Chen, W. Sy, W. L. Ong, L. Y. Ting, S. S. Yoon, M. Han, and E. Terzioglu, "Characterization of sram sense amplifier input offset for yield prediction in 28nm cmos," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, Sept 2011, pp. 1–4.

[117] R. Menchaca and H. Mahmoodi, "Impact of transistor aging effects on sense amplifier reliability in nano-scale cmos," in *Thirteenth International Symposium on Quality Electronic Design (ISQED)*, March 2012, pp. 342–346.

[118] I. Agbo, M. Taouil, S. Hamdioui, P. Weckx, S. Cosemans, P. Raghavan, and F. Catthoor, "Comparative bti analysis for various sense amplifier designs," in *2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, April 2016, pp. 1–6.

[119] I. Agbo, M. Taouil, D. Kraak, S. Hamdioui, H. Kukner, P. Weckx, P. Raghavan, and F. Catthoor, "Integral impact of bti, pvt variation, and workload on sram

sense amplifier," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 25, no. 4, pp. 1444–1454, Apr. 2017.

[120] O. Garitselov, S. P. Mohanty, and E. Kougianos, "A comparative study of metamodels for fast and accurate simulation of nano-cmos circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 1, pp. 26–36, Feb 2012.

[121] M. B. Yelten, T. Zhu, S. Koziel, P. D. Franzon, and M. B. Steer, "Demystifying surrogate modeling for circuits and systems," *IEEE Circuits and Systems Magazine*, vol. 12, no. 1, pp. 45–63, Firstquarter 2012.

[122] A. I. J. Forrester, A. Sobester, and A. J. Keane, *Engineering Design via Surrogate Modelling - A Practical Guide.* Wiley, 2008.

[123] M. Y. M. Ahmed and N. Qin, "Surrogate- based aerodynamic design optimization : Use of surrogates in aerodynamic design optimization," *13th International Conference on Aerospace Sciences and Aviation Technology*, pp. 1–26, 2009.

[124] T. Zhu, M. B. Yelten, M. B. Steer, and P. D. Franzon, *Model-Based Variation-Aware Integrated Circuit Design*. New York, NY: Springer New York, 2013, pp. 171–188.

[125] C. Cortes and V. Vapnik, "Support-vector networks," *Machine Learning*, vol. 20, no. 3, pp. 273–297, Sep 1995.

[126] T. Kiely and G. Gielen, "Performance modeling of analog integrated circuits using least-squares support vector machines," in *Proceedings of the Conference on Design, Automation and Test in Europe - Volume 1*, ser. DATE '04. Washington, DC, USA: IEEE Computer Society, 2004, pp. 10 448–.

[127] D. Boolchandani, C. Gupta, and V. Sahula, "Analog circuit feasibility modeling using support vector machine with efficient kernel functions," 2009.

[128] D. Boolchandani, A. Ahmed, and V. Sahula, "Efficient kernel functions for support vector machine regression model for analog circuits' performance evaluation," *Analog Integrated Circuits and Signal Processing*, vol. 66, no. 1, pp. 117–128, Jan 2011.

[129] J. Suykens and J. Vandewalle, "Least squares support vector machine classifiers," *Neural Processing Letters*, vol. 9, no. 3, pp. 293–300, Jun 1999.

[130] H. Wang and D. Hu, "Comparison of svm and ls-svm for regression," in *2005 International Conference on Neural Networks and Brain*, vol. 1, Oct 2005, pp. 279–283.

[131] J. Suykens, T. Van Gestel, and J. De Brabanter, *Least Squares Support Vector Machines*. World Scientific, 2002.

[132] R. H. Tu, E. Rosenbaum, W. Y. Chan, C. C. Li, E. Minami, K. Quader, P. K. Ko, and C. Hu, "Berkeley reliability tools-bert," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 10, pp. 1524–1534, Oct 1993.

[133] C. Parthasarathy, M. Denais, V. Huard, G. Ribes, D. Roy, C. Guerin, F. Perrier, E. Vincent, and A. Bravaix, "Designing in reliability in advanced cmos technologies," *Microelectronics Reliability*, vol. 46, no. 9, pp. 1464 – 1471, 2006, proceedings of the 17th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. Wuppertal, Germany October 2006.

[134] Z. Xian-Jun, Y. Yin-Tang, D. Bao-Xing, C. Chang-Chun, S. Kun, and C. Bin, "Modeling of the drain-induced barrier lowering effect and optimization for a dual-channel 4h silicon carbide metal semiconductor field effect transistor," *Chinese Physics B*, vol. 21, no. 3, 2012.

[135] B. Tudor, J. Wang, Z. Chen, R. Tan, W. Liu, and F. Lee, "An accurate mosfet aging model for 28nm integrated circuit simulation," *Microelectronics Reliability*, vol. 52, no. 8, pp. 1565 – 1570, 2012, {ICMAT} 2011 - Reliability and variability of semiconductor devices and {ICs}.

[136] A. B. Kahng, B. Lin, and S. Nath, "Enhanced metamodeling techniques for high-dimensional ic design estimation problems," in *2013 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2013, pp. 1861–1866.

[137] M. D. McKay, R. J. Beckman, and W. J. Conover, "A comparison of three methods for selecting values of input variables in the analysis of output from a computer code," *Technometrics*, vol. 42, no. 1, pp. 55–61, Feb. 2000.

[138] N. V. Queipo, R. T. Haftka, W. Shyy, T. Goel, R. Vaidyanathan, and P. K. Tucker, "Surrogate-based analysis and optimization," *Progress in Aerospace Sciences*, vol. 41, no. 1, pp. 1 – 28, 2005.

[139] B. J. Lipson H, "An exploration-estimation algorithm for synthesis and analysis of engineering systems using minimal physical testing," *ASME. International Design Engineering Technical Conferences and Computers and Information in Engineering Conference*, vol. 1, 30th Design Automation Conference.

[140] C. Wang, *Hot Carrier Design Considerations for MOS Devices and Circuits*. Springer US, 2012.

[141] J. Huijsing, R. van de Plassche, and W. Sansen, *Analog Circuit Design: Operational Amplifiers, Analog to Digital Convertors, Analog Computer Aided Design*, ser. Analog circuit design. Springer, 1992.

[142] B. Liu, G. Gielen, and F. Fernández, *Automated Design of Analog and High-frequency Circuits: A Computational Intelligence Approach*, ser. Studies in Computational Intelligence. Springer Berlin Heidelberg, 2013.

[143] E. Maricau and G. Gielen, "Computer-aided analog circuit design for reliability in nanometer cmos," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 1, pp. 50–58, March 2011.

[144] X. Xuan, A. Chatterjee, A. D. Singh, N. P. Kim, and M. T. Chisa, "Ic reliability simulator aret and its application in design-for-reliability," in *Test Symposium, 2003. ATS 2003. 12th Asian*, Nov 2003, pp. 18–21.

[145] S. K. Krishnappa, H. Singh, and H. Mahmoodi, "Incorporating effects of process, voltage, and temperature variation in bti model for circuit design," 2010.

[146] S. Kumar, C. Kim, and S. Sapatnekar, "Body bias voltage computations for process and temperature compensation," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 16, no. 3, pp. 249–262, March 2008.

[147] A. Bansal, R. Rao, J. J. Kim, S. Zafar, J. H. Stathis, and C.-T. Chuang, "Impact of nbti and pbti in sram bit-cells: Relative sensitivities and guidelines for application-specific target stability/performance," in *2009 IEEE International Reliability Physics Symposium*, April 2009, pp. 745–749.

[148] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Impact of nbti on sram read stability and design for reliability," in *Proceedingsofthe7thInternationalSymposiumonQualityElectronicDesign*, ser. ISQED '06. Washington, DC, USA: IEEE Computer Society, 2006, pp. 210–218.

[149] S.-C. Yang, H.-I. Yang, C.-T. Chuang, and W. Hwang, "Timing control degradation and nbti/pbti tolerant design for write-replica circuit in nanoscale cmos sram," in *2009 International Symposium on VLSI Design, Automation and Test*, April 2009, pp. 162–165.

[150] J. Singh and N. Vijaykrishnan, "A highly reliable NBTI resilient 6T SRAM cell," *Microelec. Reliability*, vol. 53, no. 4, pp. 565 – 572, 2013.

[151] J. Lohstroh, E. Seevinck, and J. de Groot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 803–807, Dec 1983.

[152] A. Pavlov and M. Sachdev, *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test*, 1st ed. Springer Publishing Company, Incorporated, 2008.

[153] E. I. Vatajelu and J. Figueras, "Efficiency evaluation of parametric failure mitigation techniques for reliable sram operation," in *2012 Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2012, pp. 1343–1348.

[154] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "A 3-ghz 70-mb sram in 65-nm cmos technology with integrated column-based dynamic power supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 146–151, Jan 2006.

[155] K. Nii, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, S. Imaoka, H. Makino, Y. Yamagami, S. Ishikura, T. Terano, T. Oashi, K. Hashimoto, A. Sebe, G. Okazaki, K. Satomi, H. Akamatsu, and H. Shinohara, "A 45-nm bulk cmos embedded sram with improved immunity against process and temperature variations," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 180–191, Jan 2008.

[156] K. Nii, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, Y. Oda, K. Usui, T. Kawamura, N. Tsuboi, T. Iwasaki, K. Hashimoto, H. Makino, and H. Shinohara, "A 45-nm single-port and dual-port sram family with robust read/write stabilizing circuitry under dvfs environment," in *2008 IEEE Symposium on VLSI Circuits*, June 2008, pp. 212–213.

[157] F. Hamzaoglu, K. Zhang, Y. Wang, H. J. Ahn, U. Bhattacharya, Z. Chen, Y. G. Ng, A. Pavlov, K. Smits, and M. Bohr, "A 3.8 ghz 153 mb sram design with dynamic stability enhancement and leakage reduction in 45 nm high-k metal gate cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 148–154, Jan 2009.

[158] T. Fischer, E. Amirante, K. Hofmann, M. Ostermayr, P. Huber, and D. Schmitt-Landsiedel, "A 65nm test structure for the analysis of nbti induced statistical variation in sram transistors," in *Solid-State Device Research Conference, 2008. ESSDERC 2008. 38th European*, Sept 2008, pp. 51–54.

[159] B. Paul, K. Kang, H. Kufluoglu, M. Alam, and K. Roy, "Impact of nbti on the temporal performance degradation of digital circuits," *Electron Device Letters, IEEE*, vol. 26, no. 8, pp. 560–562, Aug 2005.

Brief Curriculum-Vitae

Sapna Khandelwal obtained her Bachelor of Engineering degree in Electronics & Communication from Rajasthan University, Jaipur in 2004. She obtained her Master of Technology degree in VLSI Design from the Malaviya National Institute of Technology, Jaipur in 2010. She is currently pursuing her Ph.D. in the field of VLSI at Electronics and Communication Engineering Department in Malaviya National Institute of Technology Jaipur, India. Her current research interests are in the area of modeling of analog and digital circuits.