A

DISSERTATION REPORT

On

Parameter evaluation and Simulation of Junctionless Double Gate MOSFET using Si, Ge and $In_{0.53}Ga_{0.47}As$ Substrate with different Dielectric materials at 65nm, 45nm, 22nm and 16nm Technology Using Silvaco Atlas

Submitted in
partial fulfilment for the degree of
Master of Technology in VLSI Design

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Certificate

This is to certify that this Dissertation report entitled "**Parameter Evaluation and Simulation of Double Gate Junctionless MOSFET using Si, Ge and $In_{0.53}Ga_{0.47}As$ Substrate with different Dielectric materials at 65nm, 45nm, 22nm, 16nm Technology Using Silvaco Atlas"** by **Kinnal Mehta (2015PEV5279)**, is the work completed under my supervision and guidance, hence approved for submission in partial fulfilment for the award of degree of Master Of Technology in **VLSI DESIGN** to the Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur for part time post graduation program of 2015-2018. The work is free from plagiarism, and does not reproduce contents substantially from other written resources.

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Date:

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Declaration

I, hereby declare that the work which is being presented in this project entitled "Parameter Evaluation and Simulation of Double Gate Junctionless MOSFET using Si, Ge and $In_{0.53}Ga_{0.47}As$ Substrate with different Dielectric materials at 65nm, 45nm, 22nm, 16nm Technology Using Silvaco Atlas" in partial fulfilment of degree of Master of Technology in VLSI DESIGN is an authentic record of my own work carried out under the supervision and guidance of Dr. Tarun Varma, associate professor in Department of Electronics and Communication, Malaviya National Institute of Technology, Jaipur. I am fully responsible for the matter embodied in this project in case of any discrepancy found in the project and the project has not been submitted for the award of any other degree. I also confirm that I have consulted the published work of others, the source is clearly attributed and I have acknowledged all main sources of help.

Date:

Kinnal Mehta
(2015PEV5279)

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(KINNAL MEHTA)

Abstract

The proposed work is simulation of symmetric Double Gate Junctionless MOSFET using Silvaco Atlas software version 5.10.0.R. I use three substrate Si, Ge, $In_{0.53}Ga_{0.47}As$ and for each substrate, I used three dielectric layers SiO_2, Si_3N_4, HfO_2, one by one. Goal of this system is to extract the Subthreshold Slope, DIBL, I_{on}/I_{off} ratio at different Gate length 65 nm, 45 nm, 22 nm and 16 nm for symmetric Double Gate Junctionless MOSFET. Simulation is done by Silvaco Atlas software and extracted data is compared to know which dielectric layer is give best results in terms of low Subthreshold slope, low Drain Induced Barrier Lowering and high I_{on}/I_{off} ratio and which substrate gives low DIBL.

Key terms- Double Gate Junctionless MOSFET, Comparison, SILVACO Atlas, 65nm, 45nm, 22nm, 16nm Gate Length.

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ABBREVIATIONS

DIBL	Drain Induced Barrier Lowering
SOI	Silicon on Insulator
DGJLM	Double Gate Junction Less MOSFET
SCE	Short Channel Effect
Si	Silicon
Ge	Germanium
InGaAs	Indium Gallium Arsenide
BOX	Buried Oxide Layer

1. INTRODUCTION

Silicon technologies have advanced faster year to year. The main point about silicon technologies is how many times the silicon devices can be scaled down according to Moore's law and what is the effect of shortening the dimensions of devices. There is many problem arise in metal-oxide semiconductor field-effect transistor (MOSFET) that has gate dimension in the below submicron region. Due to decrease in the channel length, the short channel effects and leakage current become crucial issues that downgrade the device performance. To overcome the problem, new technologies such as Silicon On Insulator (SOI), Double Gate, Multi Gate MOSFET structure is developed. SOI means to putting a thin layer of silicon on top of an insulator, commonly silicon dioxide (SiO_2) known as buried oxide layer.

1.1 SOI MOSFET:

The structures of SOI devices are similar to bulk CMOS but an insulation layer is inserted below the device on the silicon substrate. This dielectric layer offers lower coupling capacitance from the conducting channel to the substrate in comparison to a bulk CMOS, and the fabrication process used is identical with the bulk CMOS process. A buried oxide dielectric layer reduce current leakage from the drain/source junction to substrate.

SOI MOSFET are two types: Partially and fully depleted SOI MOSFETs. Each have their different characteristics in terms of process, performance and uses. A fully depleted SOI MOSFET has a narrow top silicon layer, so the channel is totally depleted of the majority carriers under strong inversion. Due to less width of Si layer, gate control is increased. The benefit of FD SOI MOSFET is reduce the leakage current. For Partially Depleted SOI device, Si thickness is greater than the depletion width of source/drain, so the depletion layer can't cover full Si width. There is a rapid progress in integrated circuit technology, due to this, scaling (reduce the dimensions) is prime issue. A new structure Double Gate MOSFET has developed, by which it is possible to more scaling of MOSFET,

Present CMOS technology, conventional MOSFET will be crucial to scale down, even if we use high-k gate insulators. The new structure such as Multi Gate MOSFET, FinFET is developed from past few years.

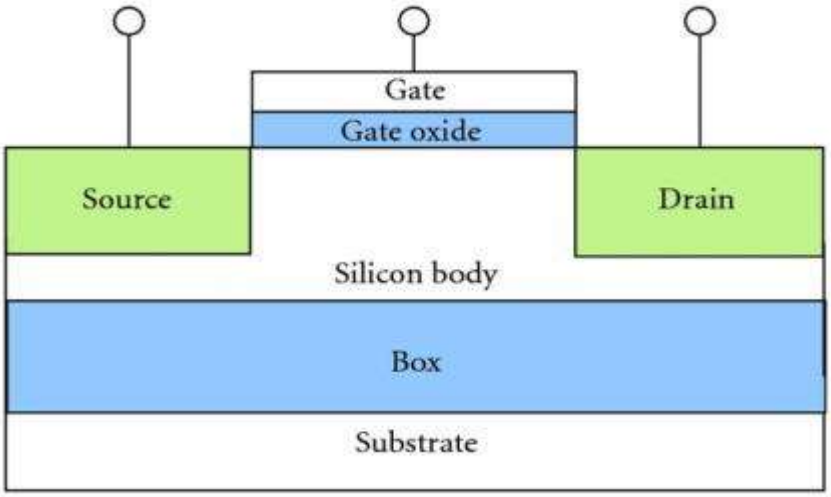

Fig. 1.1 SOI MOSFET Structure

1.2 Scaling:

Manufacturing of MOSFET in submicron range is very difficult, and it is limiting factor of IC industry in terms of technology. Scaling of MOSFET in sub micron region has following problems:

- Subthreshold leakage current
- Interconnect capacitance
- Gate oxide leakage
- DIBL and Process variations

1.2.1 Subthreshold Leakage:

Due to switching capability, MOSFET is widely used. When gate voltage is applied to certain voltage, current is flow from drain to source and transistor become ON. When gate voltage is less from certain voltage, no current is flow and transistor becomes OFF. The minimum gate voltage, which is required to turn on the MOSFET is called threshold voltage $V_{th.}$ Commonly used equations for deriving the drain current were based on the well-known quadratic transfer curve of a MOS transistor.

The above statement was true, until channel length is long in micrometer range. But due to scaling of MOSFET, this is not true. As channel length becomes in sub micrometer range, some current is flow below the threshold voltage, this current is known as Subthreshold Leakage current.

Subthreshold leakage current gives limits for scaling of MOSFET, because this current is flow even if transistor is off. So it consumes static power. New structure must be developed to reduce this current. This region, when subthreshold leakage current is flow is known as weak inversion region. There is three regions defined for operation of MOS transistor: 1. Weak Inversion Region, 2. Moderate Inversion Region, 3. Strong Inversion Region. Two mechanisms is responsible to current flow in MOS transistor: drift and diffusion.

Subthreshold leakage current is flow in weak inversion region. In weak inversion region, current is flow due to diffusion of minority carrier due to variation in concentration gradient. In strong inversion region, current is flow due to drift mechanism.

In the weak-inversion, the drain current is proportional to exponential of gate to source voltage.

1.2.2 Gate Leakage Current:

Due to advancement of IC technology, scaling of dimensions of MOSFET is used. These scaling not only reduce the channel length, it also reduce the oxide thickness under the Gate. The limit of reducing oxide thickness is 2 nm without degrade the performance. But, due to advancement in VLSI, oxide thickness is further reduced to 2 nm. In this situation, a new problem known as Gate tunnelling current is arise. It is flow even MOSFET is off. So it is necessary to reduce this static current in VLSI application. With the help of high gate dielectric oxide layer (high K) material such as Si_3N_4, Al_2O_3 and HfO_2, gate leakage current become reduced.

1.3 Double Gate MOSFET

To overcome the problem of short channel effects in single gate mosfet in nano scale, various multi gate structures like Double Gate, Trigate & Gate All Around structure has developed. The double gate (DG) MOSFETs are electro-statically better than the single gate (SG) MOSFET and permits for further gate length scaling. The double gate MOSFET has two gates, one is top of oxide layer (Front Gate) and one is bottom of Oxide layer (Back Gate). Due to two gates, gates are better control over the channel. This ensures that no part of the channel is far away from a gate electrode. The Double Gate MOSFET structure has reduce short-channel effects that allows more scaling upto 10 nm.

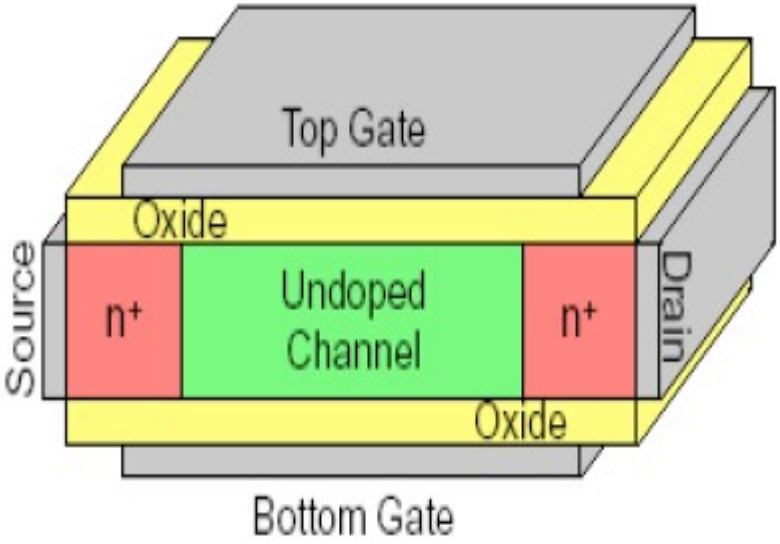

Fig. 1.2 Double Gate MOSFET

1.3.1 Advantages of DG MOSFET over Single Gate MOSFET:

There are following advantages of Double Gate MOSFET: more scalability, increase current drive, lower short channel effects, superior transconductance over single gate MOSFET. Double Gate MOSFETs have replaced bulk MOSFETs, which suffer from severe second-order problems, i.e. short channel effects (SCE) that result in degrade performance. The short channel effects consists of Drain Induced Barrier Lowering (DIBL), reduction in Threshold Voltage and leakage current.

2. Literature Survey

2.1 DOUBLE GATE JUNCIONLESS MOSFET using Si, Ge and $In_{0.53}Ga_{0.47}As$

Energy Band gap of Si is 1.1 eV, Ge is 0.67 eV and $In_{0.53}Ga_{0.47}As$ is 0.74 eV.

Mobility of electron in Ge material is higher compared to Si material.

Mobility of electron in Si is 1500 $cm^2/V/s$, Ge is 3900 $cm^2/V/s$ and $In_{0.53}Ga_{0.47}As$ is 12000 $cm^2/V/s$.

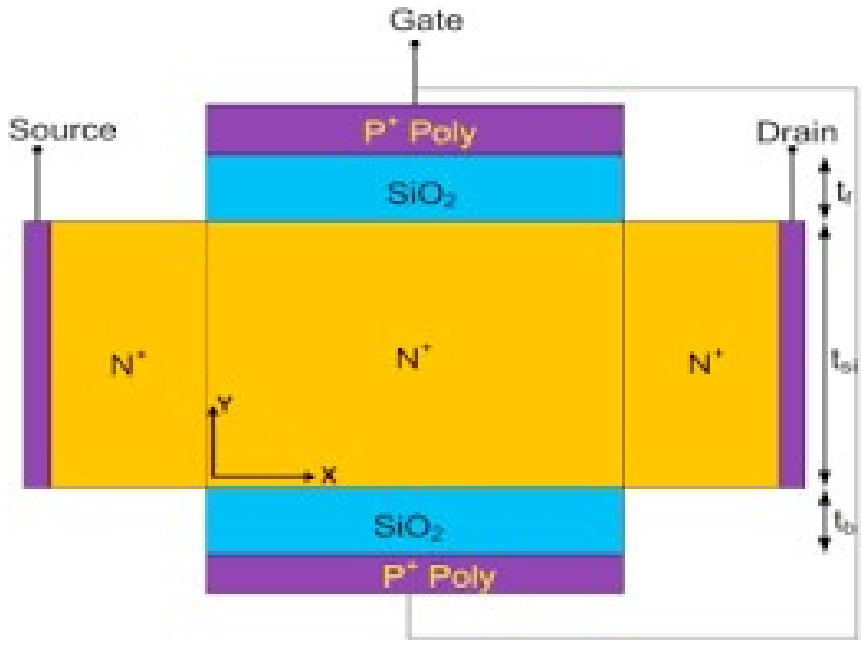

Fig. 2.1 Double Gate Junctionless MOSFET

In increasing CMOS technology, it is very difficult for manufacturer to reduce short channel effects. In Double Gate MOSFET, doping fluctuation is occur at junction. To remove these problem steep doping is required at the junction in Double Gate MOSFET, which is very difficult.

A new structure is developed, which is known as Double Gate Junctionless MOSFET. In these, there is same doping is used between source, channel and drain, so there is no need to steep doping at source/drain junction.

For this reason, Double Gate Junctionless MOSFET is more advantages compared to inversion mode MOSFET. It has low DIBL, low subthreshold slope, high I_{on}/I_{off} ratio, easy to fabricate and less sensitive to doping fluctuations. These makes the JLDGM has good structure for CMOS technology.

2.2 Literature Survey of Double Gate Junctionless MOSFET:

1) Sumathi Jyothi Medisetty, Pradipta Dutta[1]: In this paper, author describe double gate Junctionless MOSFET with Si and InGaAs(compound material). When Si is used as subtrate than SiO_2 dielctric layer is used and when InGaAs is used as a substrate than Al_2O_3 is used. By the comparison between these two DGJLM, it is observed that the $In_{0.53}Ga_{0.47}As$ with Al_2O_3 dielectric gives best results in terms of low subthreshold slope, high I_{on}/I_{off} ratio compared to Si DGJLM.

2.) Kumar P. Londhe, Y. V. Chavan[2]: In this paper, author describe that Ge substrate gives better than Si substrate. Because it give better SS, DIBL and high I_{on}/I_{off} ratio due to high mobility of Ge material. It has been also found that HfO_2 is better gate oxide layer compared to SiO_2 and Si_3N_4.

3.)Dipankar Ghosh et al.[5]: In this paper, author shows that junctionless transistor exhibit enhanced performance matrics in comparison to abrupt source/drain devices.

4.)Prerna[6]: In this paper, author describe that N-channel MOSFET structure with 80 nm gate length was designed and simulated to study the effect of high-k dielectric (TiO_2), drain voltage and oxide thickness on the device performance. Performance of the two structures- NMOS using TiO_2 with Polysilicon gate & NMOS using SiO_2 with Polysilicon gate were compared. By introduce high dielectric layer (TiO_2) subthreshold slope, DIBL is reduced and drain current is increased.

5.)Ratul Kumar Baruah, Roy P. Paily[13]: In this paper, author observed that Double gate junctionless MOSFET is superior performance compared to inversion mode Double Gate MOSFET. DGJLT gives better Subthreshold slope, DIBL, I_{on}/I_{off} ratio.

6.) Chitrakant Sahu, Jawar Singh[10]: In this paper, author comparison between double gate junctionless transistor and double gate inversion mode transistor at gate length 18 nm. Comparison is done by keeping constant threshold voltage for both devices. Junctionless device gives lower DIBL, steep subthreshold slope and lower leakage current.

3. Proposed Objectives and Methodology

3.1 Simulation Using Silvaco Atlas Software

Inputs and Outputs in Silvaco ATLAS-

Two types of input file:

i. A text file that contains Atlas commands.

ii. A structure file that defines the structure to be simulated.

It produces three types of output files:

i. The runtime output that gives error and warning messages as the simulation proceeds, after the input is loaded.

ii. The log file that stores voltage and currents.

iii. The structure file that stores 2D and 3D data relating to the values of solution variables.

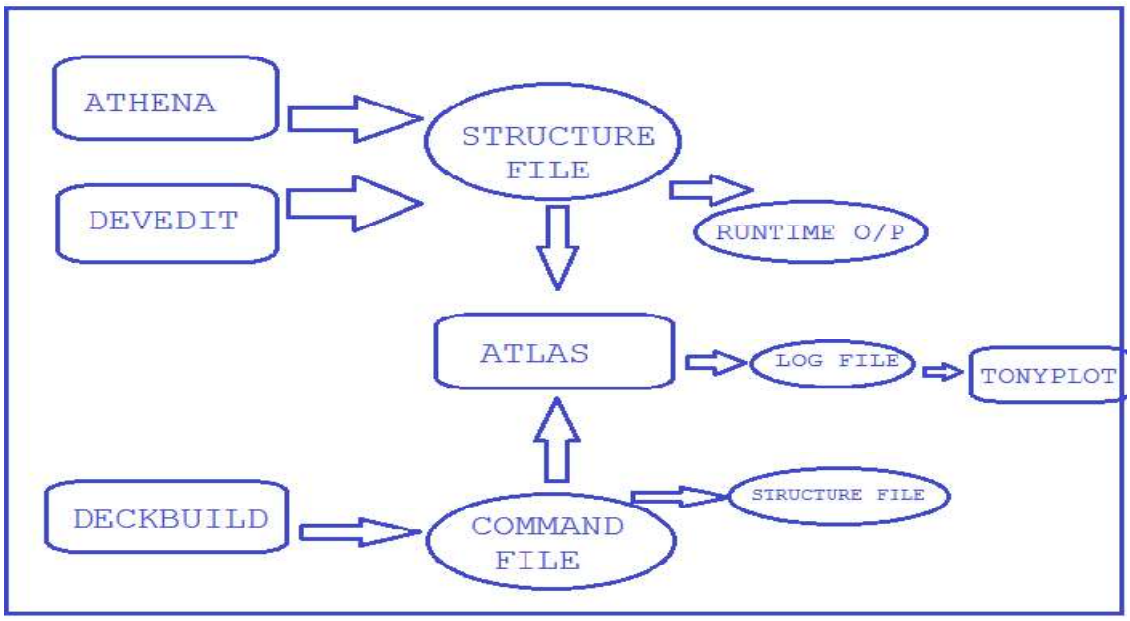

Fig. 3.1 Flow graph of Silvaco

The above flow chart shows the flow of data during the entire simulation. The Deckbuild in ATLAS has two windows. Program is written is upper window and run time output is generated in lower window. The output plot of V-I graph from log file and output plot of structure from structure file is generated by TONYPLOT tool.

3.2 Common methodology used in Simulation of Double Gate Junctionless MOSFET:

Silvaco ATLAS version 5.10.0.R is used for simulation.

Performance Comparison and Simulation of symmetric Double Gate Junctionless MOSFET using Si, Ge and $In_{0.53}Ga_{0.47}As$ with different Gate Dielectric Layers

Gate Length= 65 nm, 45nm, 22 nm, 16 nm

Oxide Thickness= 1nm

Substrate Thickness=10nm

Threshold voltage is kept constant (0.5 Volt) by adjust Gate work function

Doping =2e19 for source, channel and drain

Drain Voltage: 0.05 Volt, 1 Volt

Gate Voltage: 0 Volt to 1 Volt

Contact Resistance of Source and Drain=80E-6

For all measurements:

Threshold voltage is measured at Vds=0.05 Volt.

Subthreshold slope is measured at Vds=0.05 Volt

Ion is measured at Vds=1 Volt and Vgs=1 Volt.

Ioff is measured at Vds=1 Volt and Vgs= 0 Volt.

I have used SRH recombination model, CVT model, concentration and temperature dependent model (Analytic), Parallel electric field dependence model (FLDMOB), Reduced carrier concentration in heavily doped region model (FERMI) in simulation.

Newton method is included in simulation with maximum iteration limit is equal to 25.

3.3 Simulation of 65 nm Gate Length Double Gate Junctionless MOSFET

Si substrate and SiO_2 dielectric layer

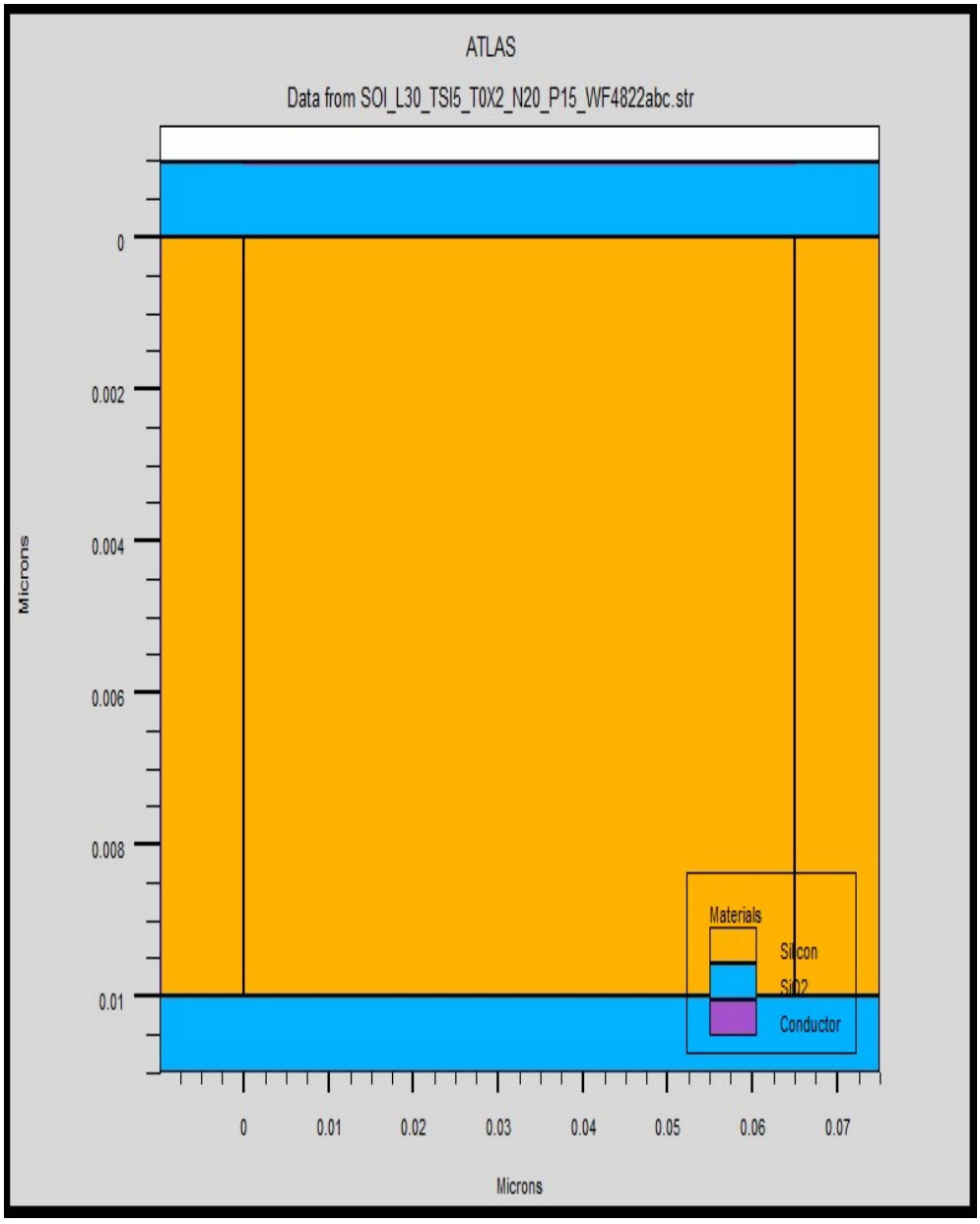

Fig. 3.2 Si and SiO_2 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Si is used as substrate and SiO_2 as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

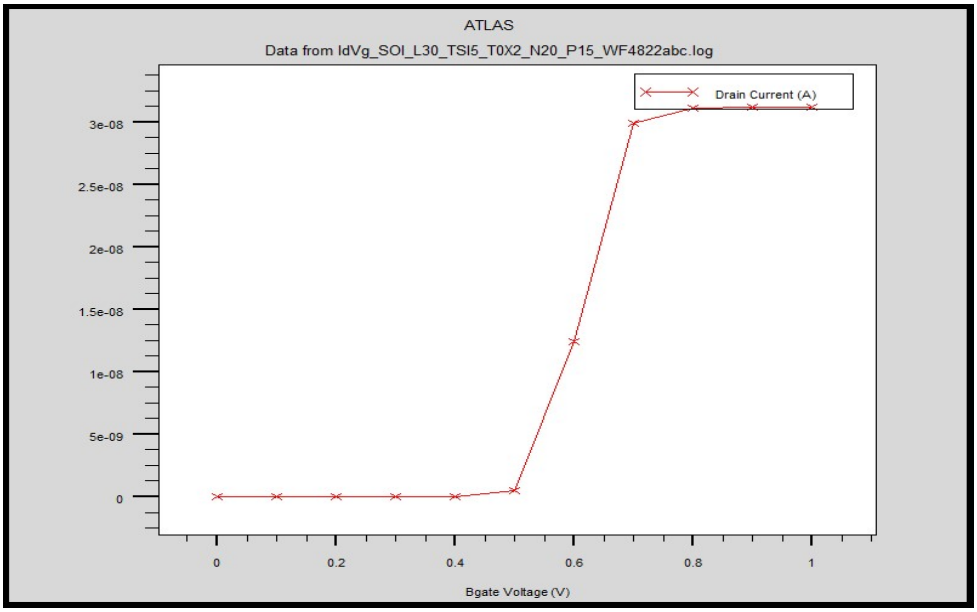

Fig. 3.3 Gate Voltage and drain Current in Linear Scale when Vds=0.05 Volt

This curve shows that at threshold voltage is set to 0.5 Volt by change the gate work function at V_{ds}=50mV. Below gate voltage=0.5 volt, MOSFET is off, after it MOSFET is ON.

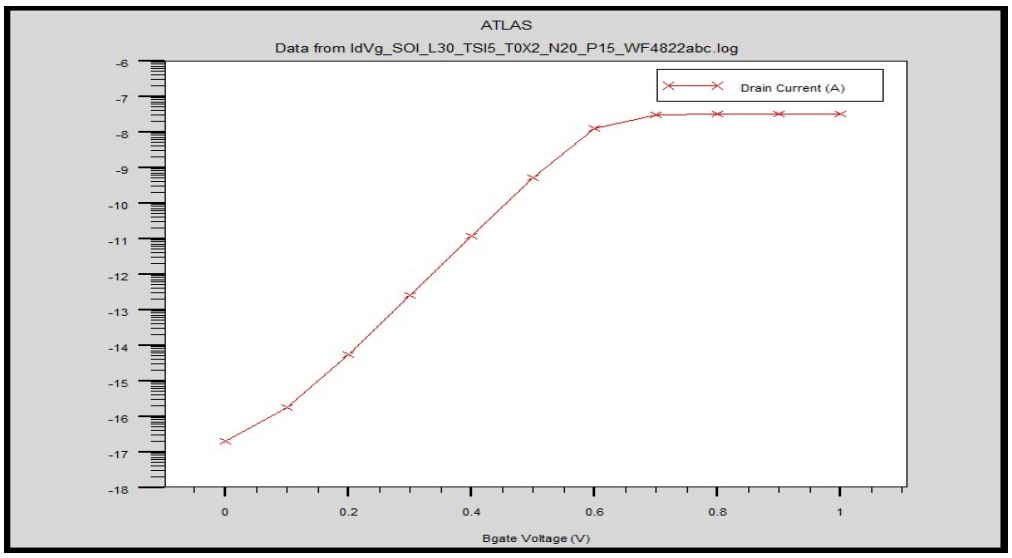

Fig. 3.4 Gate Voltage and drain Current in Log Scale when Vds=0.05 Volt

This curve shows that below Threshold voltage = 0.5 Volt, some current is flow. This current is known as Subthreshold leakage current. Subthreshold Slope is obtained by simulation is 60.12 mV/dec.

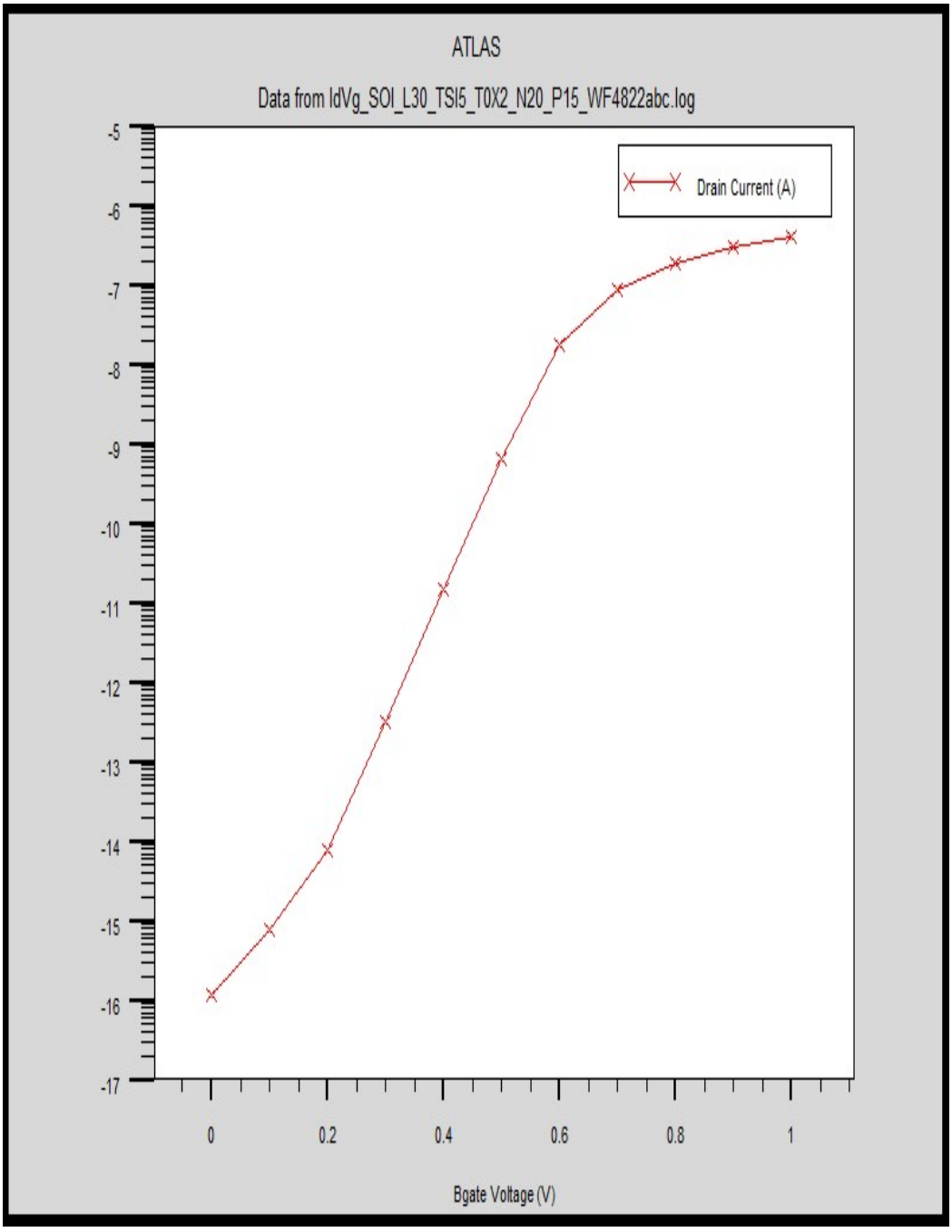

Fig. 3.5 Gate Voltage and drain Current in Log Scale when Vds=1 Volt

To obtain I_{on}/I_{off} ratio, V_{ds} is keep equal to 1 volt and V_{gs} is varied from 0 to 1 Volt. From the curve, it is measured as 10^{10}.

Si substrate and Si_3N_4 dielectric layer

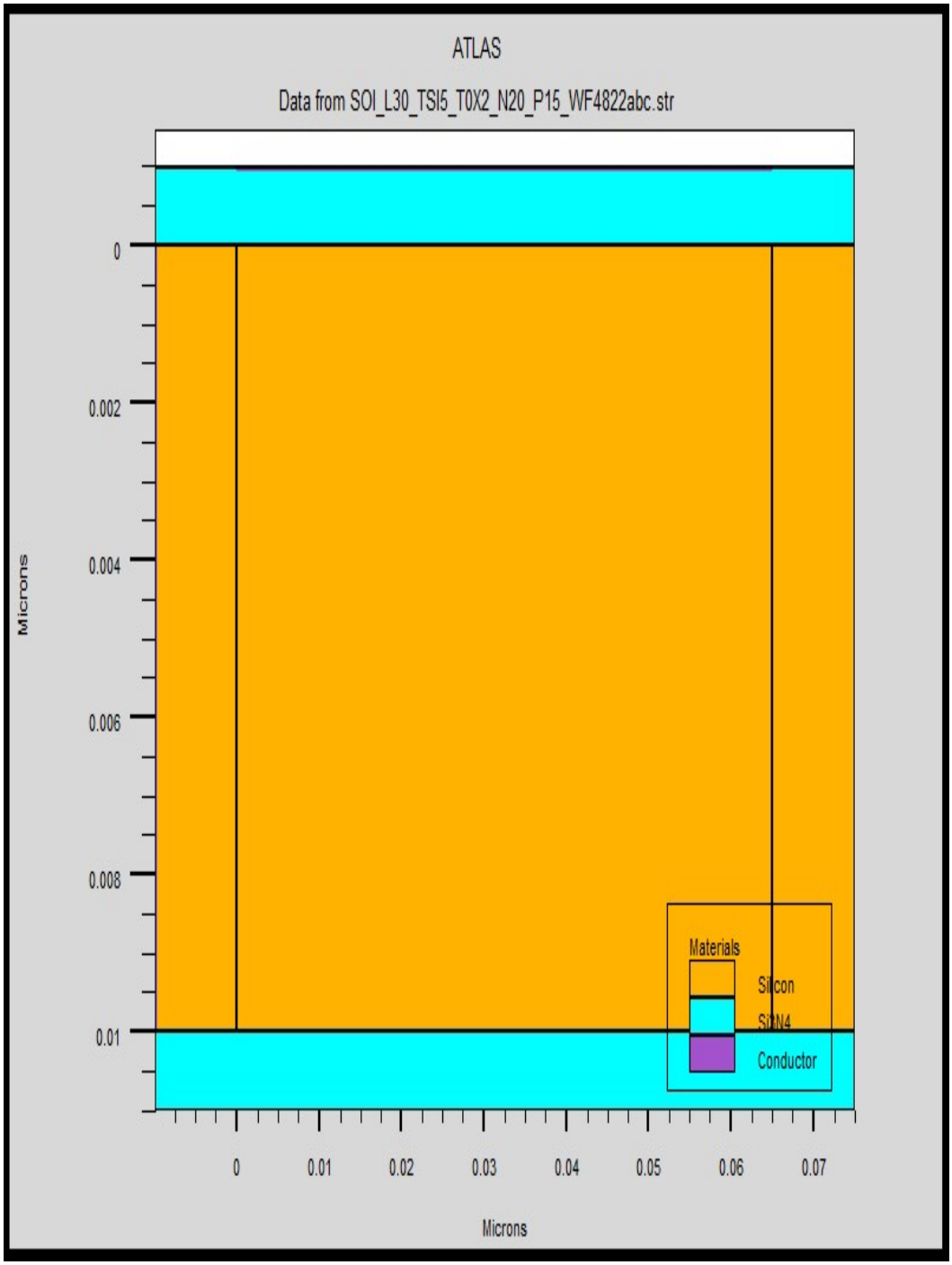

Fig. 3.6 Si and Si_3N_4 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

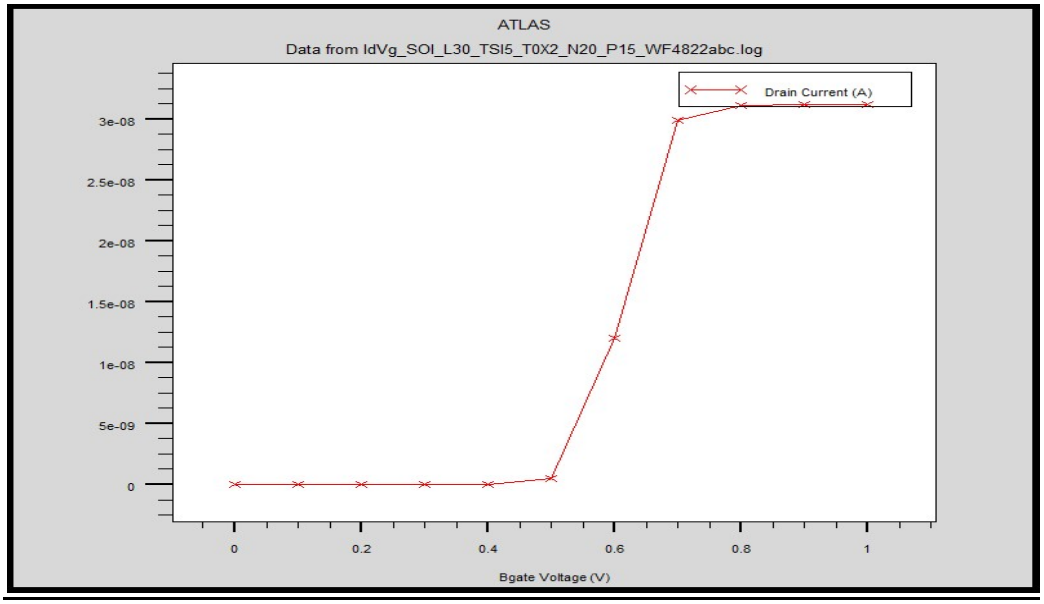

Fig. 3.7 Gate Voltage and drain Current in Linear Scale when Vds=0.05 Volt

This curve shows that at threshold voltage is set to 0.5 Volt by change the gate work function at V_{ds}=50mV. Below gate voltage=0.5 volt, MOSFET is off, after it MOSFET is ON.

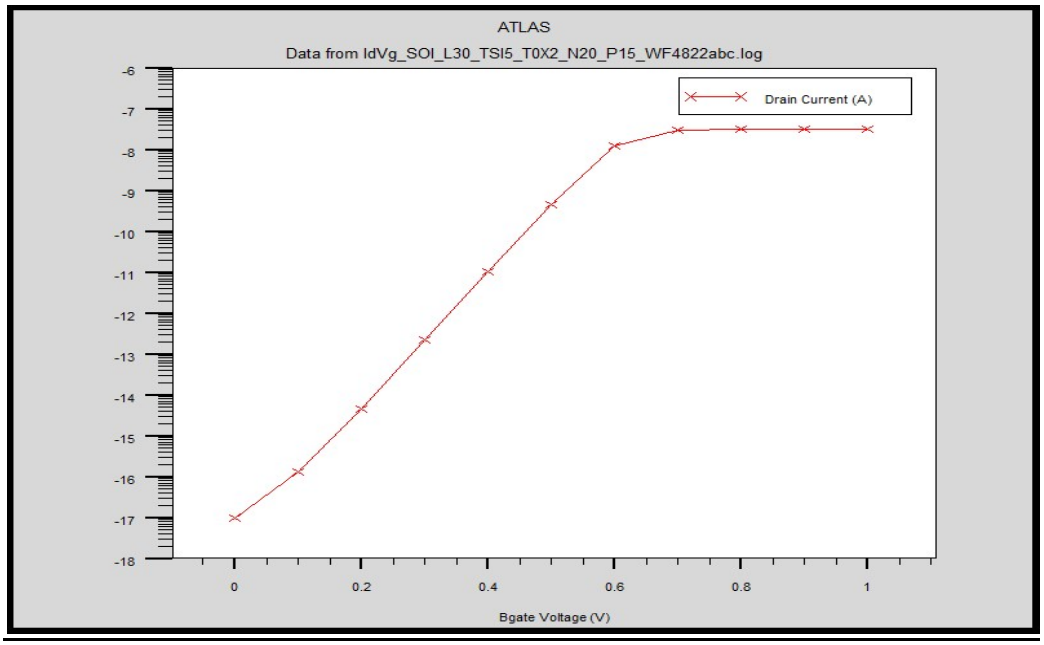

Fig. 3.8 Gate Voltage and drain Current in Log Scale when Vds=0.05 Volt

This curve shows that below Threshold voltage 0.5 Volt, some current is flow. This current is known as Subthreshold leakage current. Subthreshold Slope is obtained by simulation is 59.80 mV/dec.

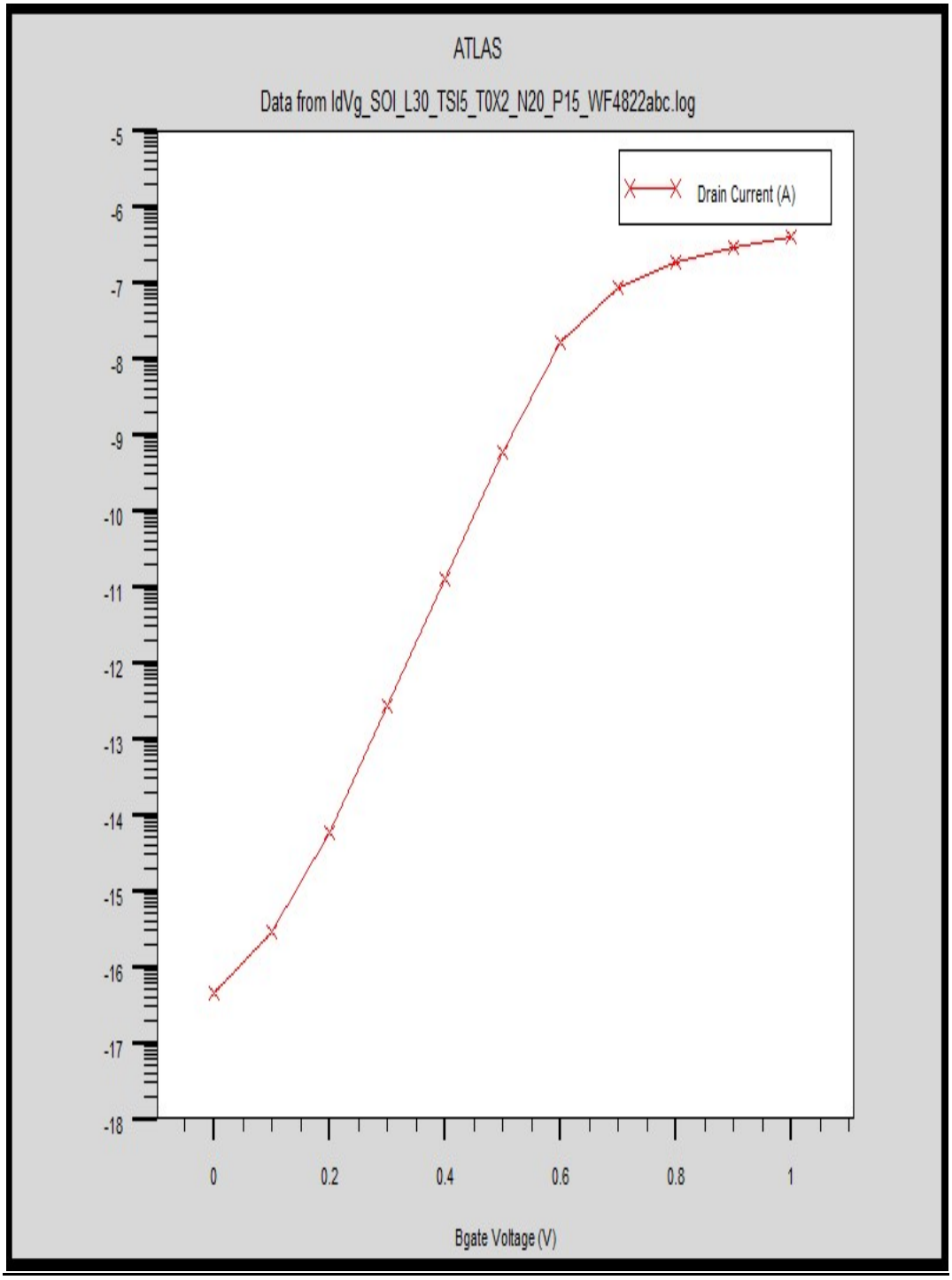

Fig. 3.9 Gate Voltage and drain Current in Log Scale when Vds=1 Volt

To obtain I_{on}/I_{off} ratio, V_{ds} is keep equal to 1 volt and gate voltage V_{gs} is varied from 0 to 1 Volt. From the curve, it is measured as 10^{11}.

Si substrate and HfO_2 dielectric layer

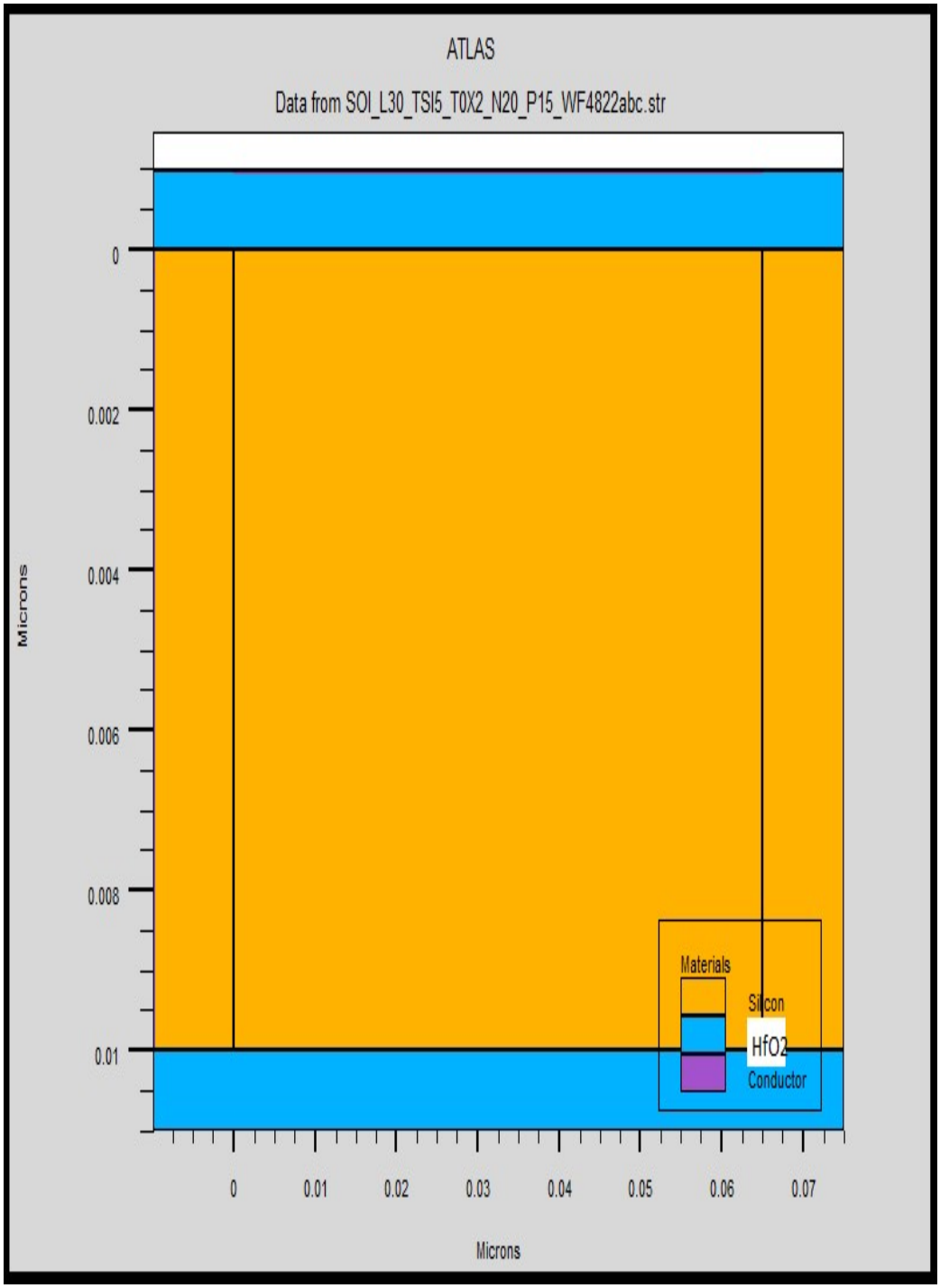

Fig. 3.10 Si and HfO_2 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

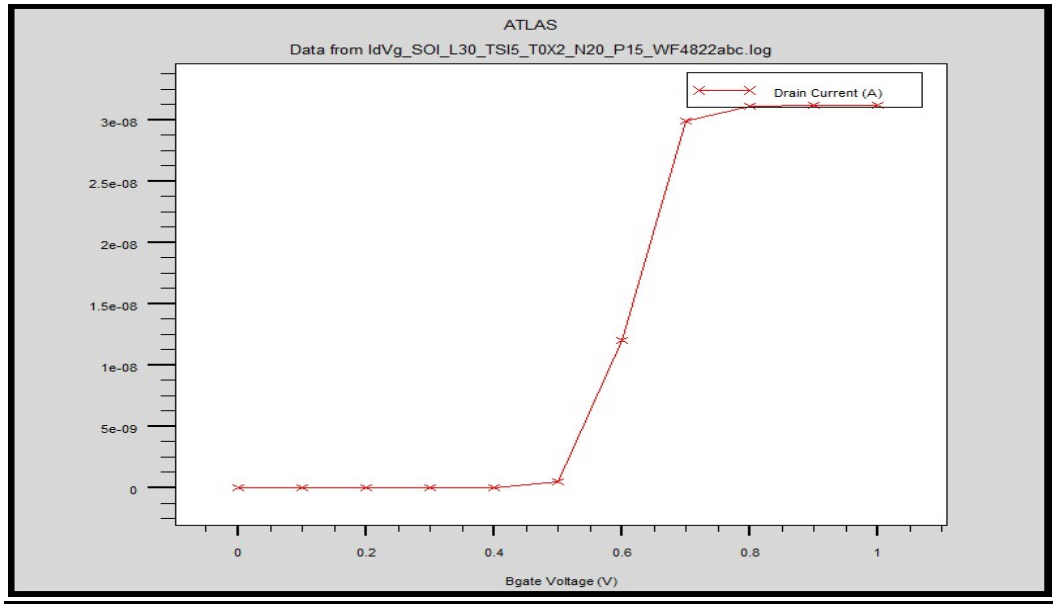

Fig. 3.11 Gate Voltage and drain Current in Linear Scale when Vds=0.05 Volt

This curve shows that at threshold voltage is set to 0.5 Volt by change the gate work function at V_{ds}=50mV. Below gate voltage=0.5 volt, MOSFET is off, after it MOSFET is ON.

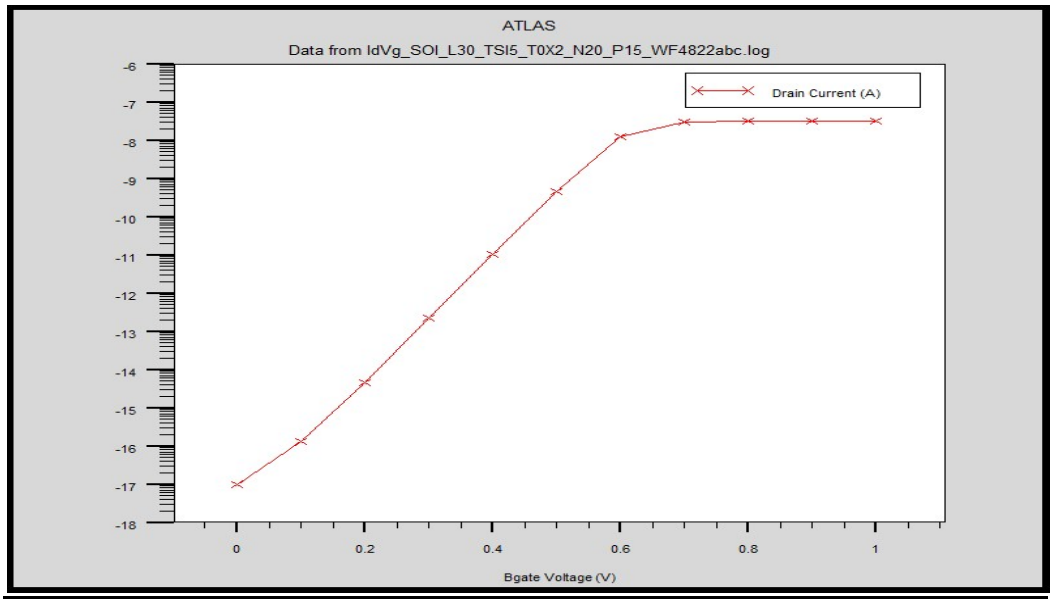

Fig. 3.12 Gate Voltage and drain Current in Log Scale when Vds=0.05 Volt

This curve shows that below Threshold voltage 0.5 Volt, some current is flow. This current is known as Subthreshold leakage current. Subthreshold Slope is obtained by simulation is 59.91 mV/dec.

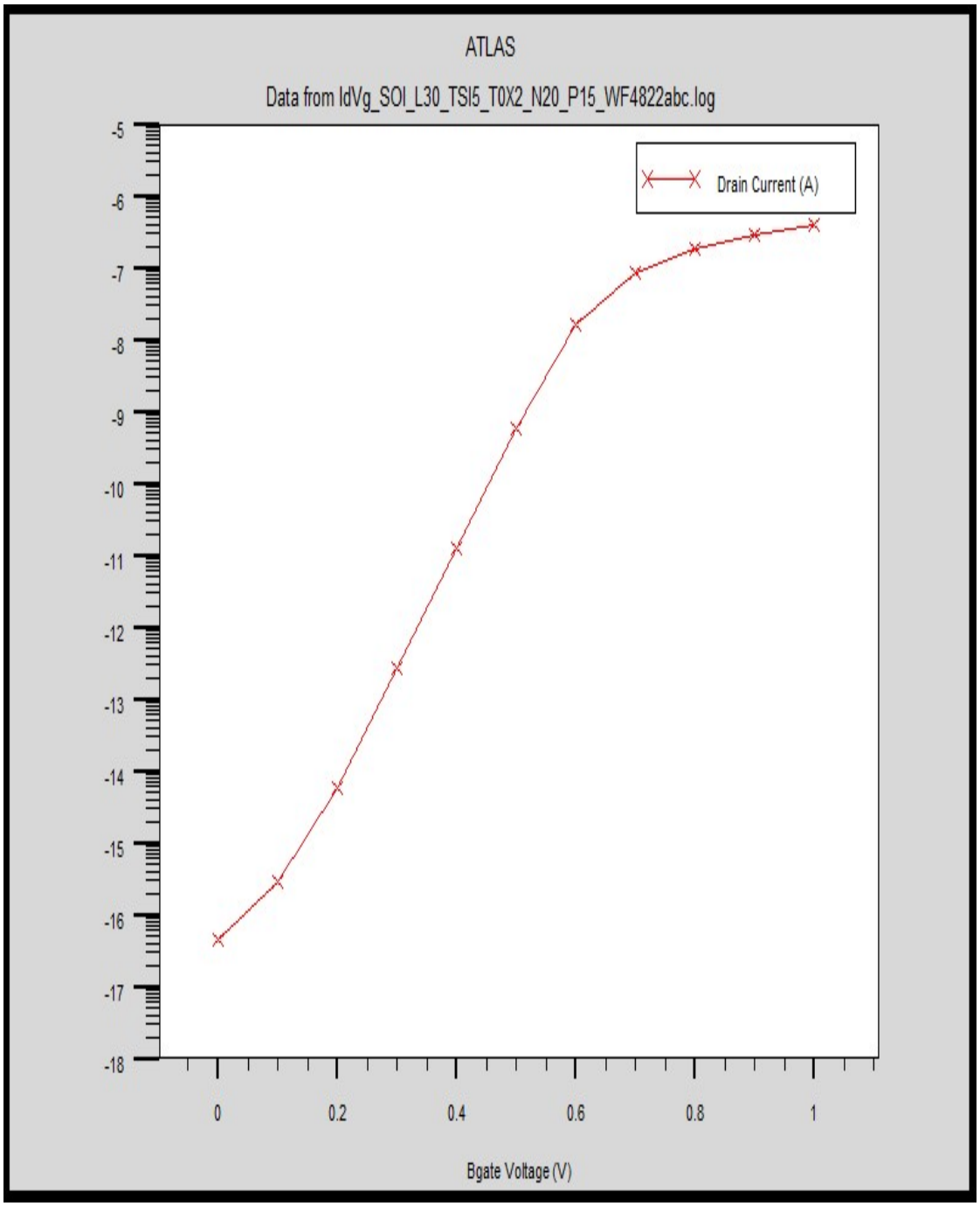

Fig. 3.13 Gate Voltage and drain Current in Log Scale when Vds=1 Volt

To obtain I_{on}/I_{off} ratio, V_{ds} is keep equal to 1 volt and gate voltage V_{gs} is varied from 0 to 1 Volt. From the curve, it is measured as 10^{11}.

Table 3.1: Comparison of **Si Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 65 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt) - V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	60.12	384.21	10^{10}
Si_3N_4(K=7.4)	0.5	59.80	382.10	10^{11}
HfO_2(K=22)	0.5	59.91	383.15	10^{11}

Ge substrate and SiO_2 dielectric layer

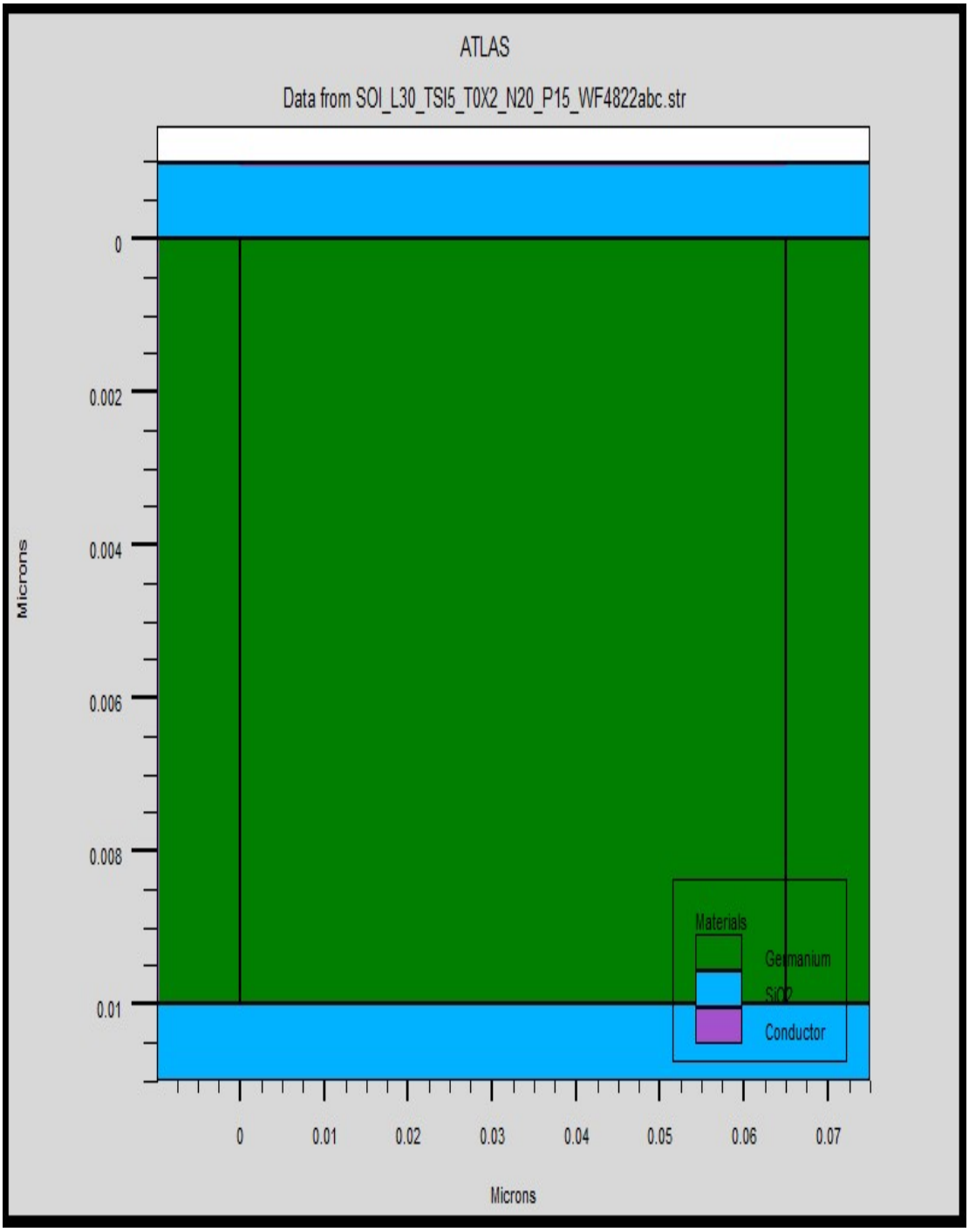

Fig. 3.14 Ge and SiO_2 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Silicon Dioxide (SiO_2) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Ge substrate and Si_3N_4 dielectric layer

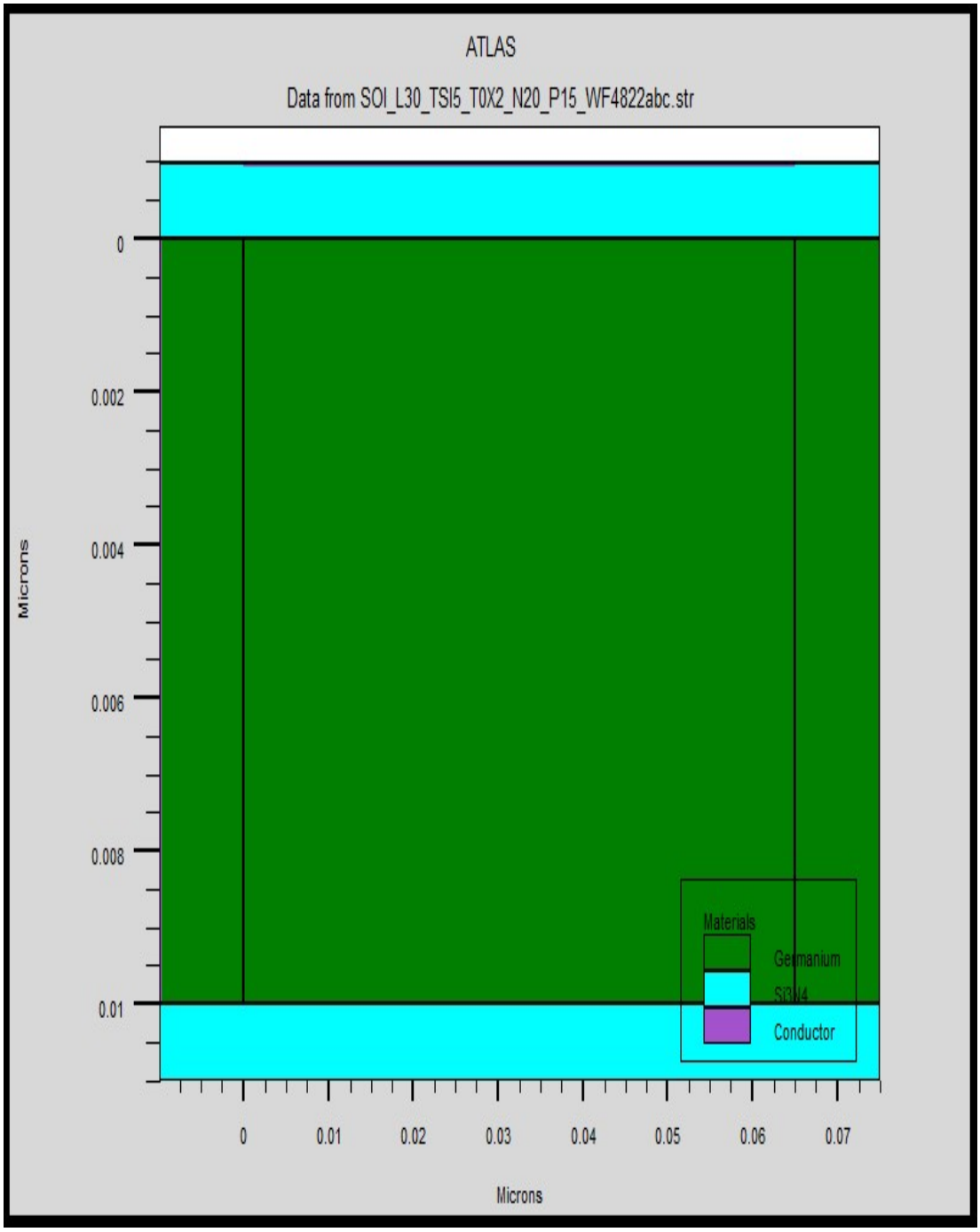

Fig. 3.15 Ge and Si_3N_4 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Silicon Nitride (Si_3N_4) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Ge substrate and HfO_2 dielectric layer

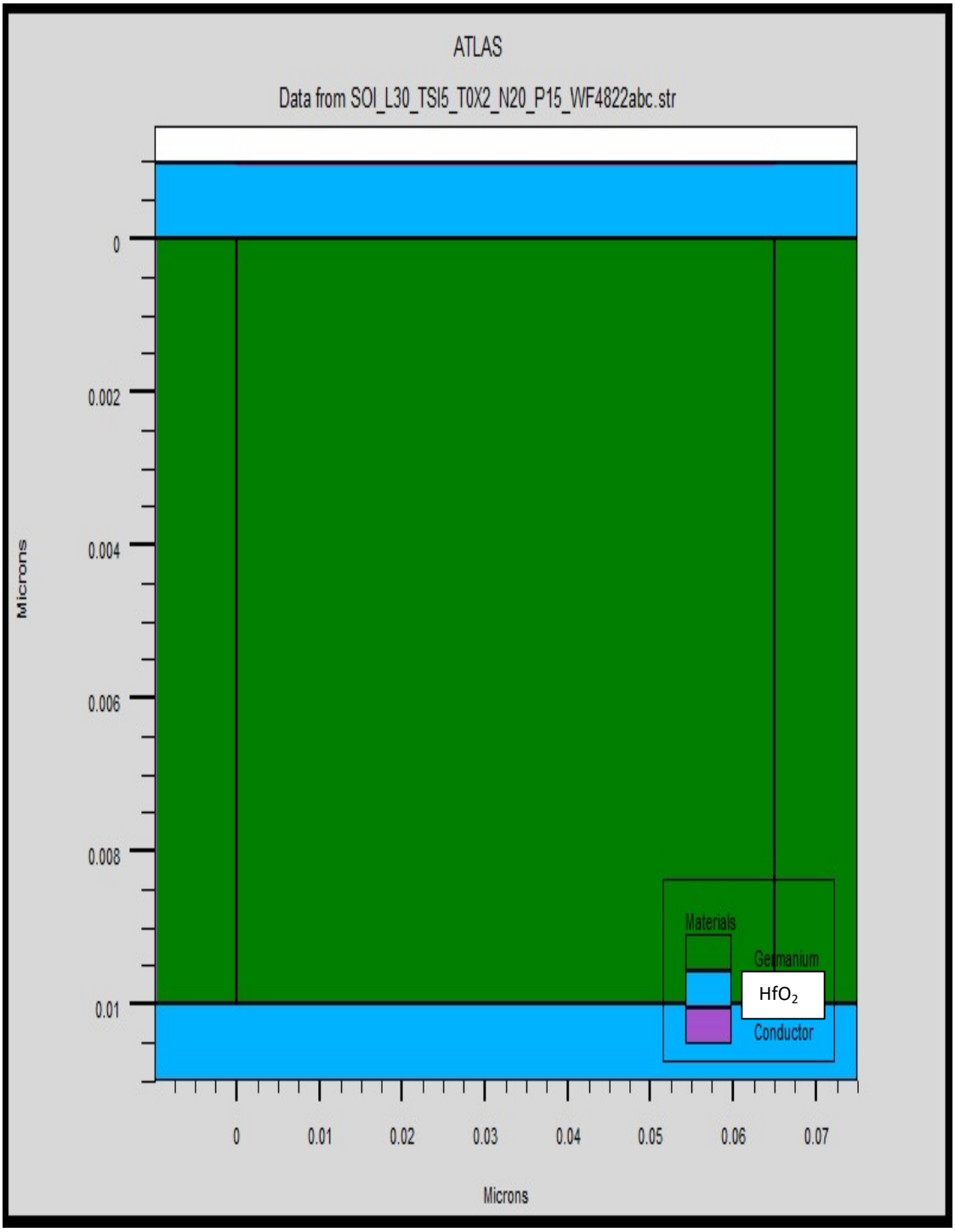

Fig. 3.16 Ge and HfO_2 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Table 3.2: Comparison of **Ge Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 65 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/ 0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	75.28	381.05	10^7
Si_3N_4(K=7.4)	0.5	73.49	383.15	10^7
HfO_2(K=22)	0.5	66.26	383.15	10^8

$In_{0.53}Ga_{0.47}As$ substrate and SiO_2 dielectric layer

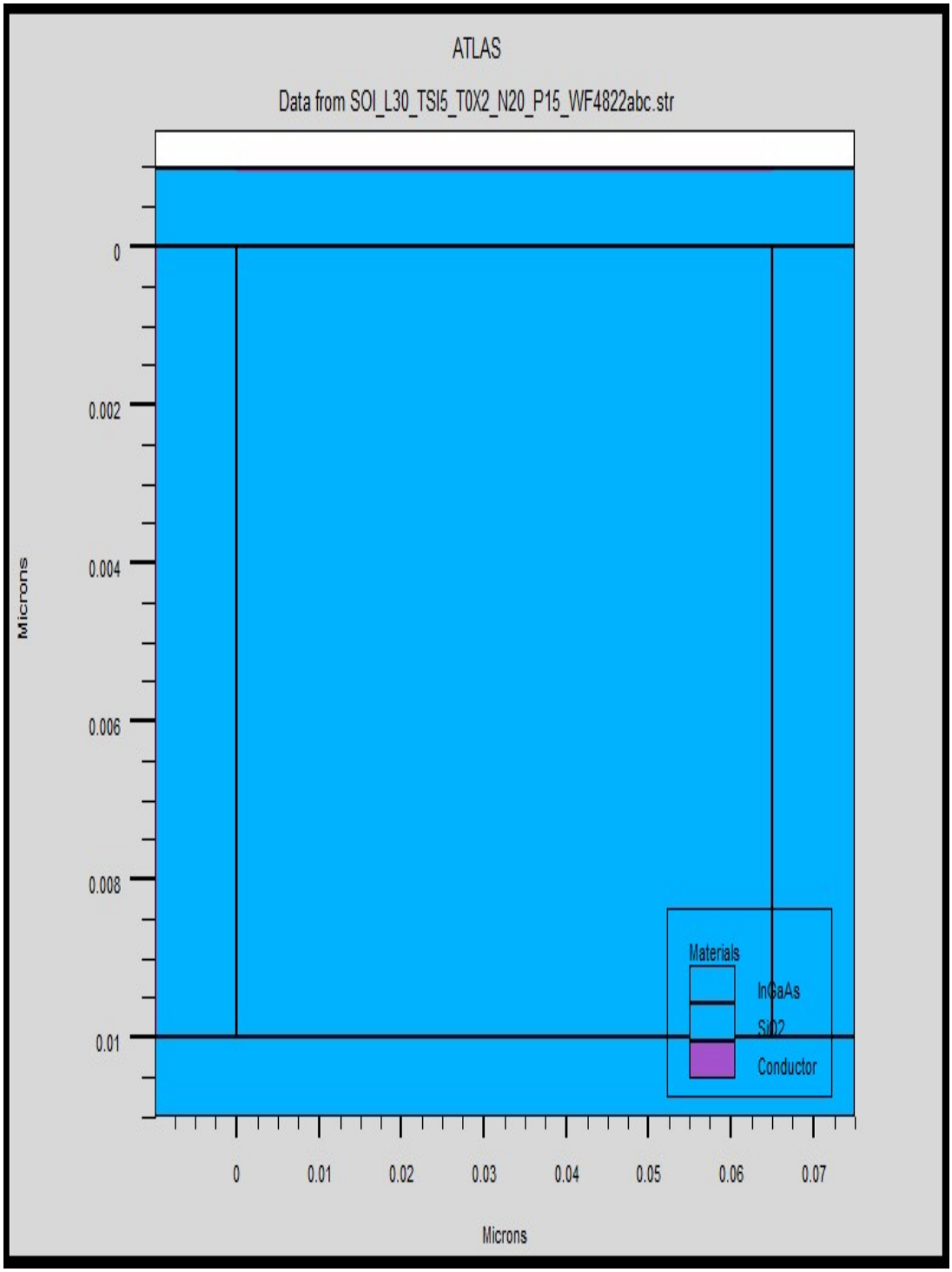

Fig. 3.17 $In_{0.53}Ga_{0.47}As$ and SiO_2 at 65 nm Gate Length

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Dioxide (SiO_2) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

$In_{0.53}Ga_{0.47}As$ substrate and Si_3N_4 dielectric layer

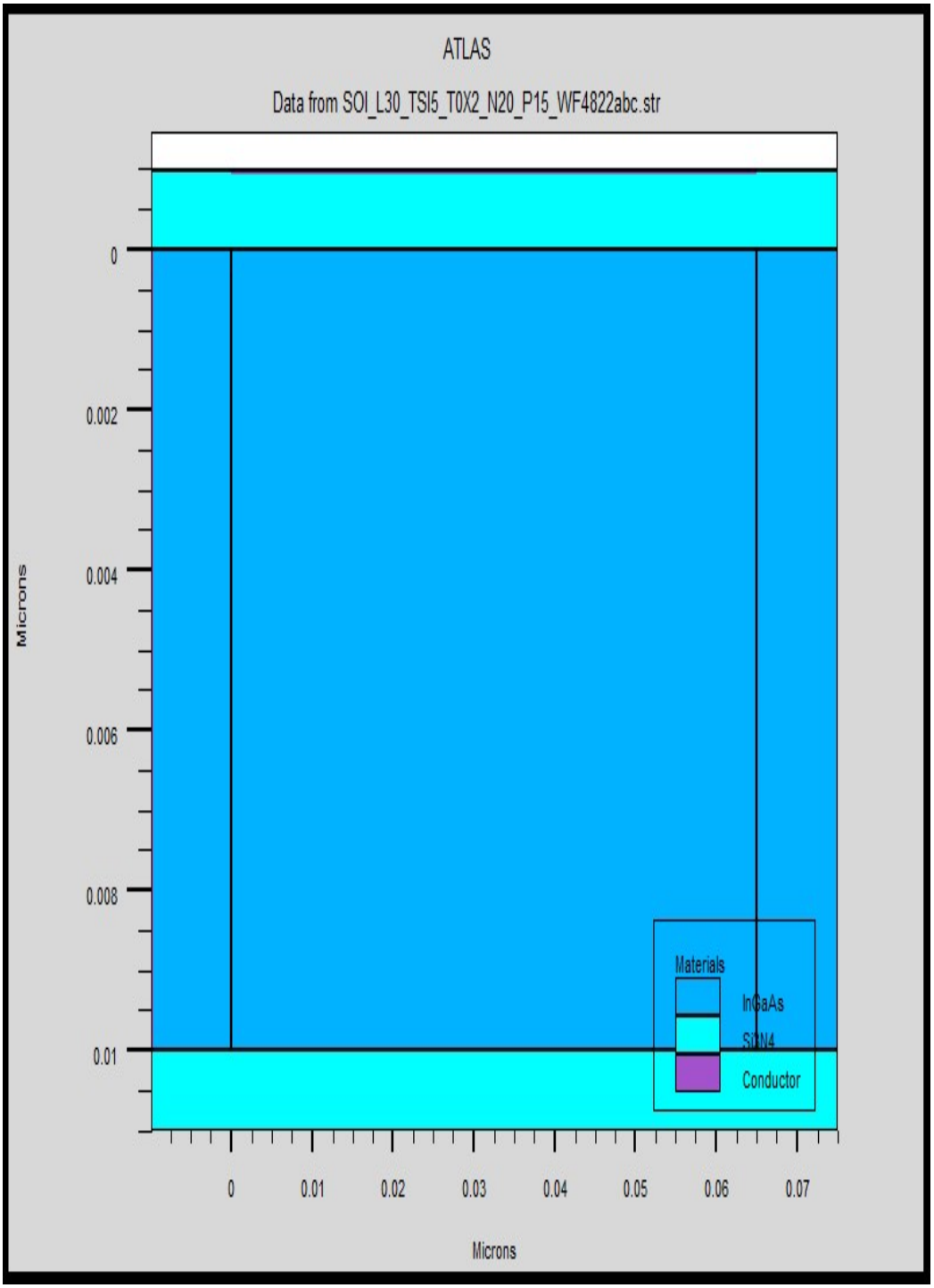

Fig. 3.18 $In_{0.53}Ga_{0.47}As$ substrate and Si_3N_4 at 65 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Nitride (Si_3N_4) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

$In_{0.53}Ga_{0.47}As$ substrate and HfO_2 dielectric layer

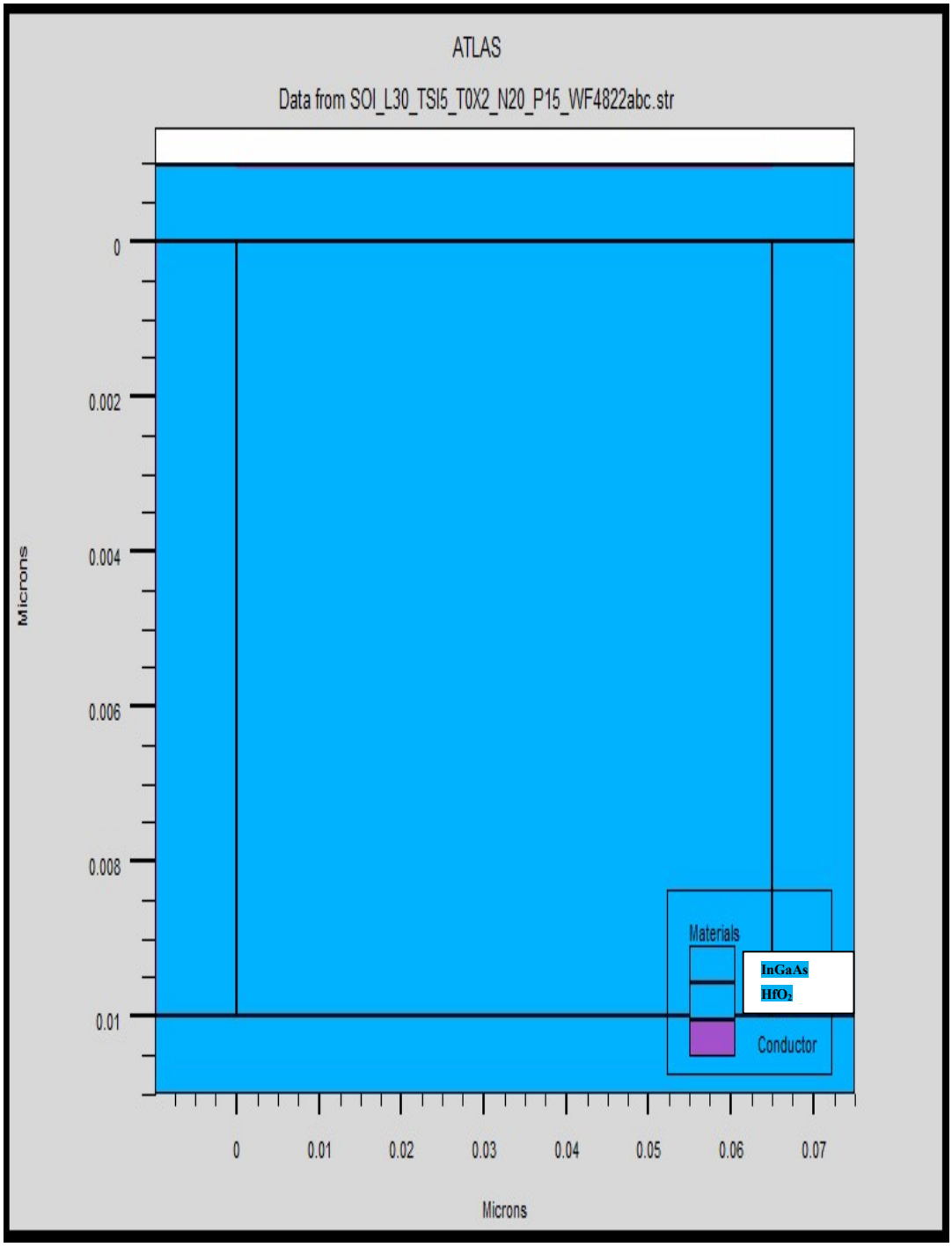

Fig. 3.19 $In_{0.53}Ga_{0.47}As$ substrate and HfO_2 at 65 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 65 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

Table 3.3: Comparison of $In_{0.53}Ga_{0.47}As$ Material and SiO_2, Si_3N_4 and HfO_2 Dielectric at 65 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	60.71	386.31	10^8
Si_3N_4(K=7.4)	0.5	60.34	382.10	10^9
HfO_2(K=22)	0.5	60.10	383.15	10^9

3.4 Simulation of 45 nm Gate Length Double Gate Junctionless MOSFET

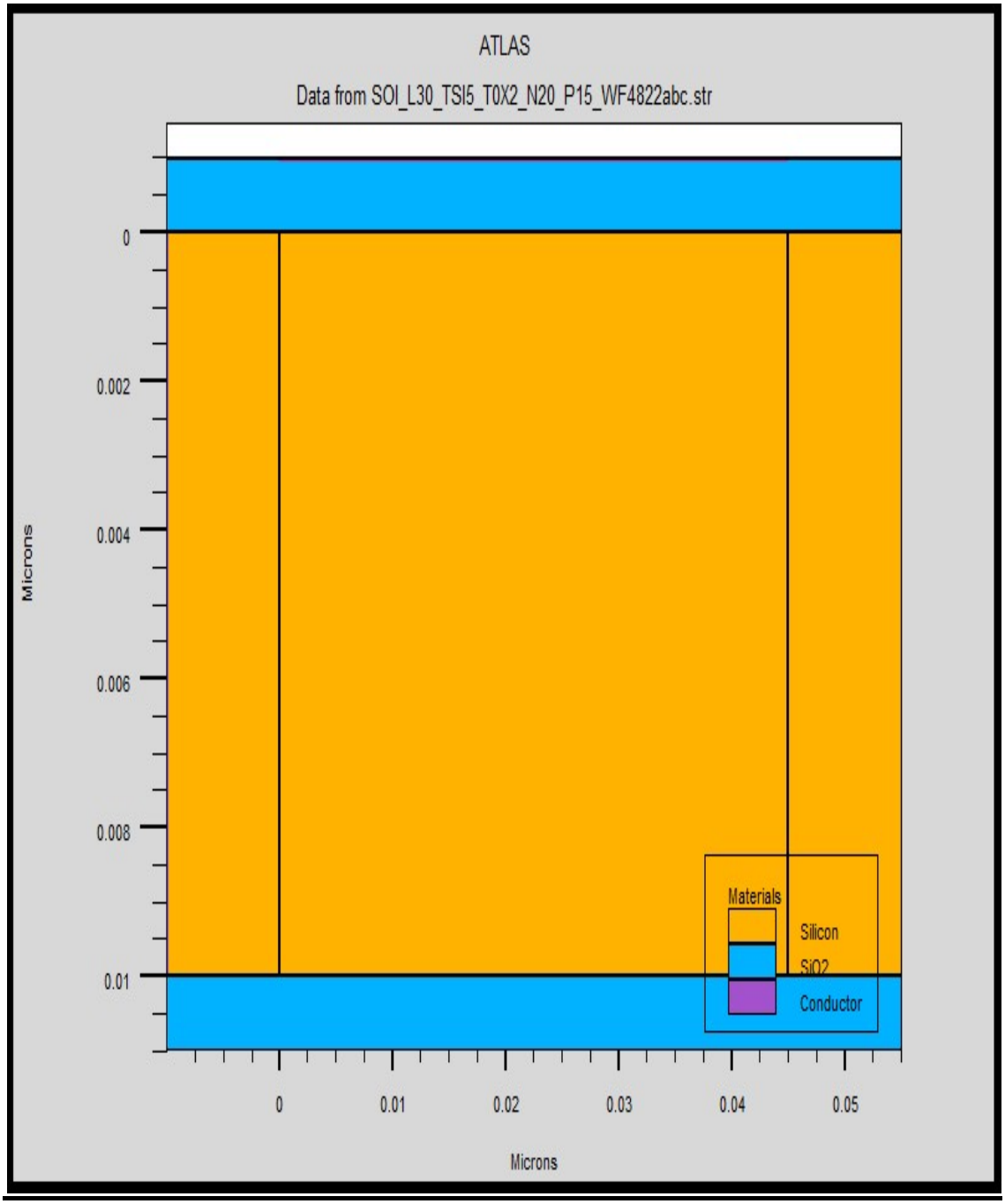

Fig.3.20 Si and SiO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and SiO_2 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

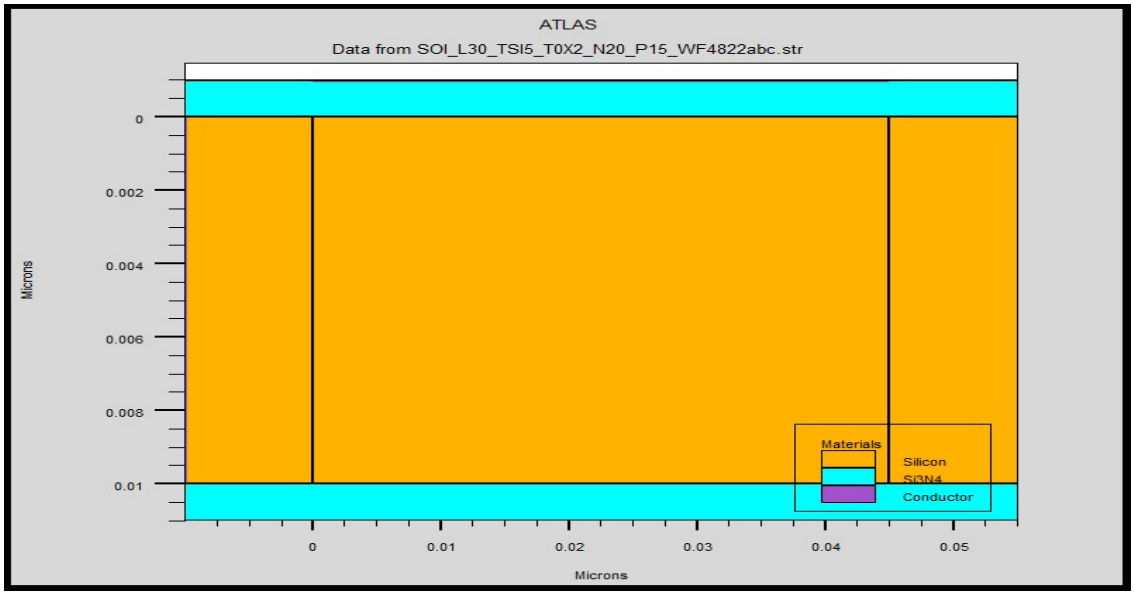

Fig.3.21 Si and Si_3N_4 at 45 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

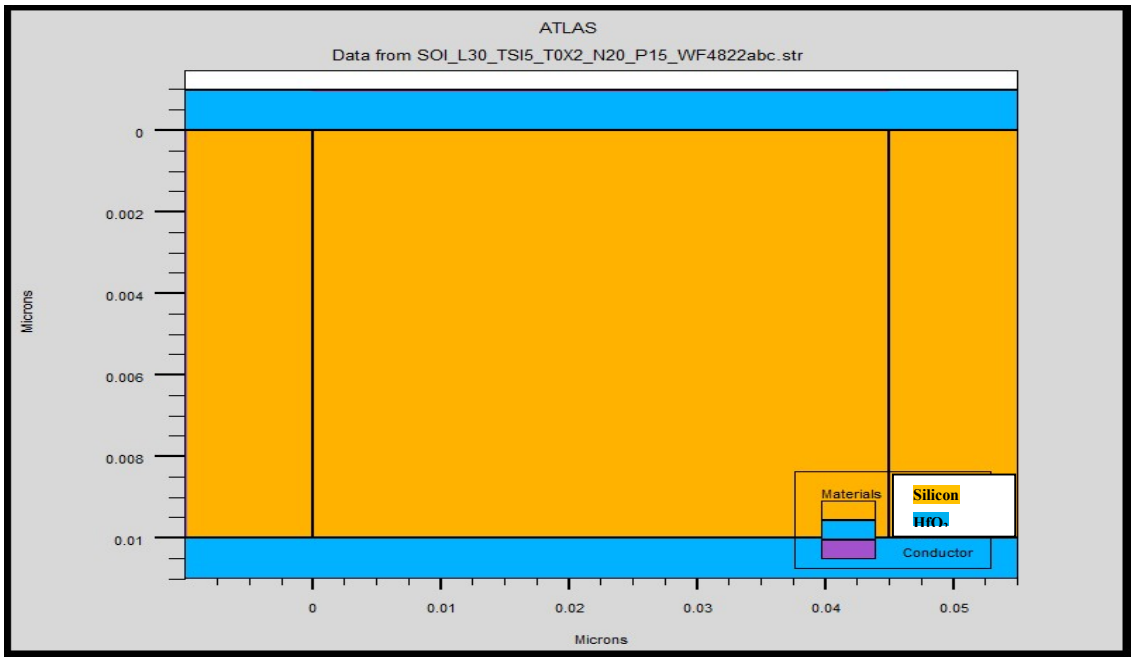

Fig. 3.22 Si and HfO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and HfO_2 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

Table 3.4: Comparison **Si Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 45 nm

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt) /0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	61.01	391.57	10^{10}
Si_3N_4(K=7.4)	0.5	60.23	390.52	10^{11}
HfO_2(K=22)	0.5	60.12	387.36	10^{11}

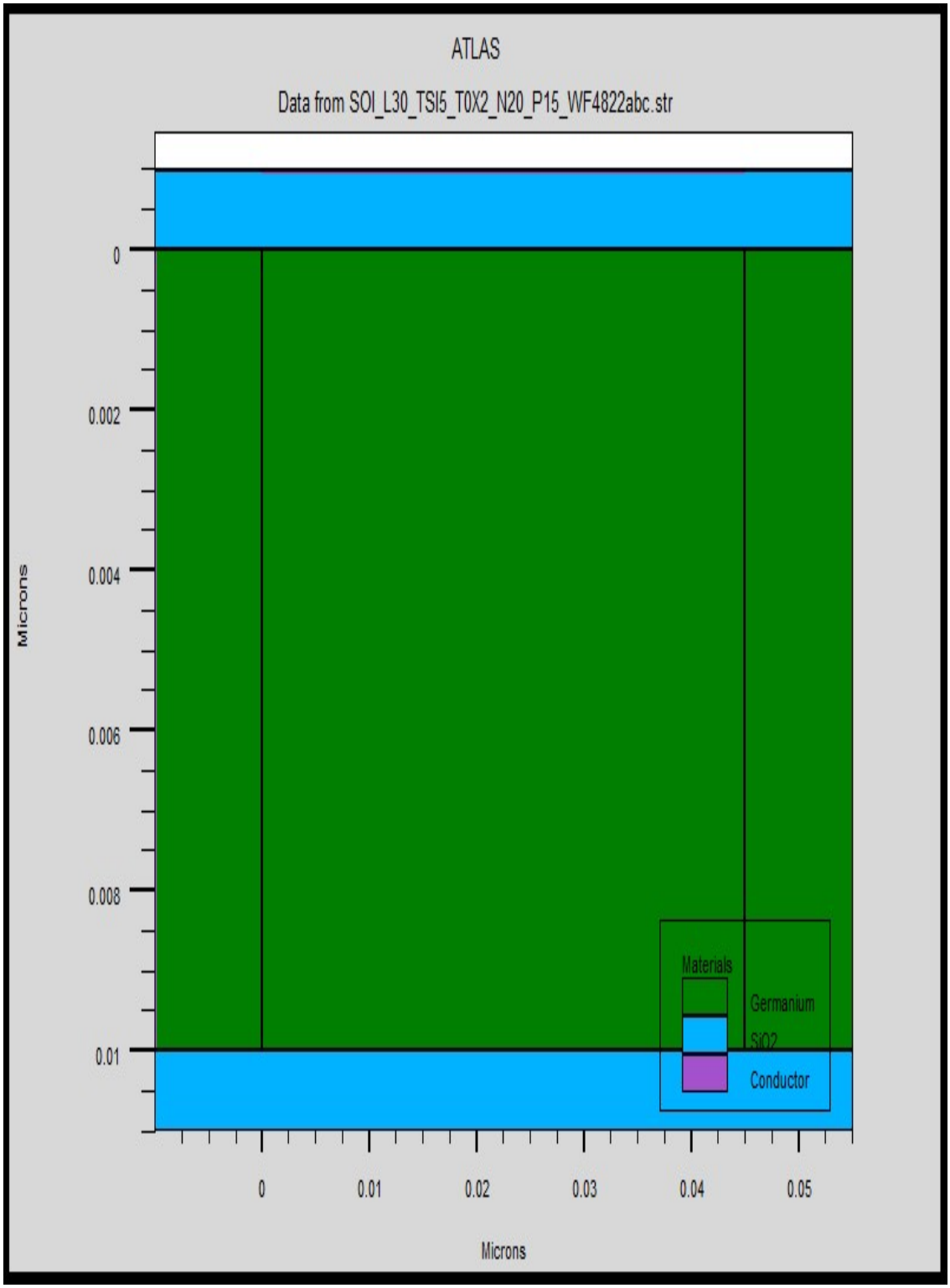

Fig. 3.23 Ge with SiO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and SiO_2 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

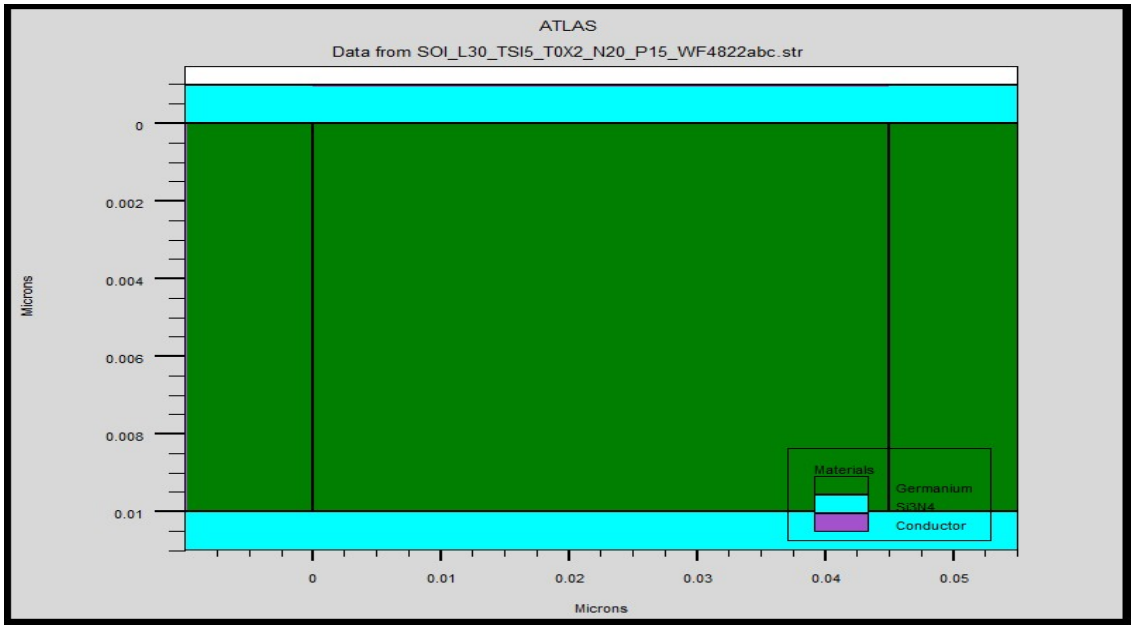

Fig. 3.24 Ge with Si_3N_4 at 45 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

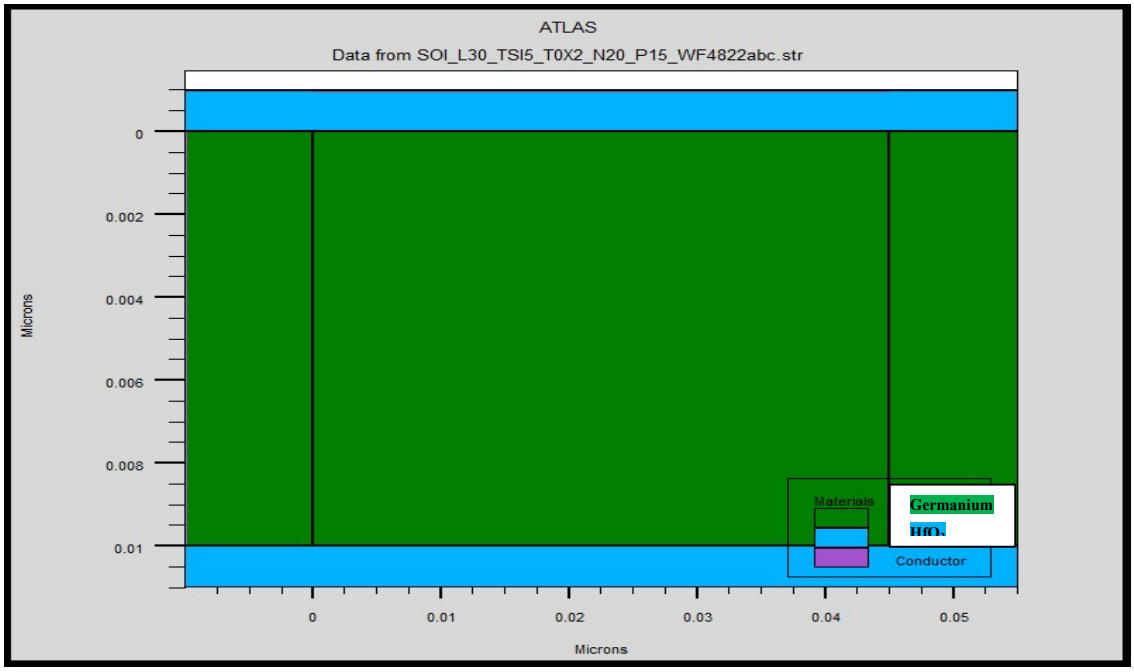

Fig. 3.25 Ge with HfO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Table 3.5: Comparison of **Ge Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 45 nm

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt) /0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	74.95	388.42	10^7
Si_3N_4(K=7.4)	0.5	73.48	385.26	10^7
HfO_2(K=22)	0.5	68.03	395.78	10^8

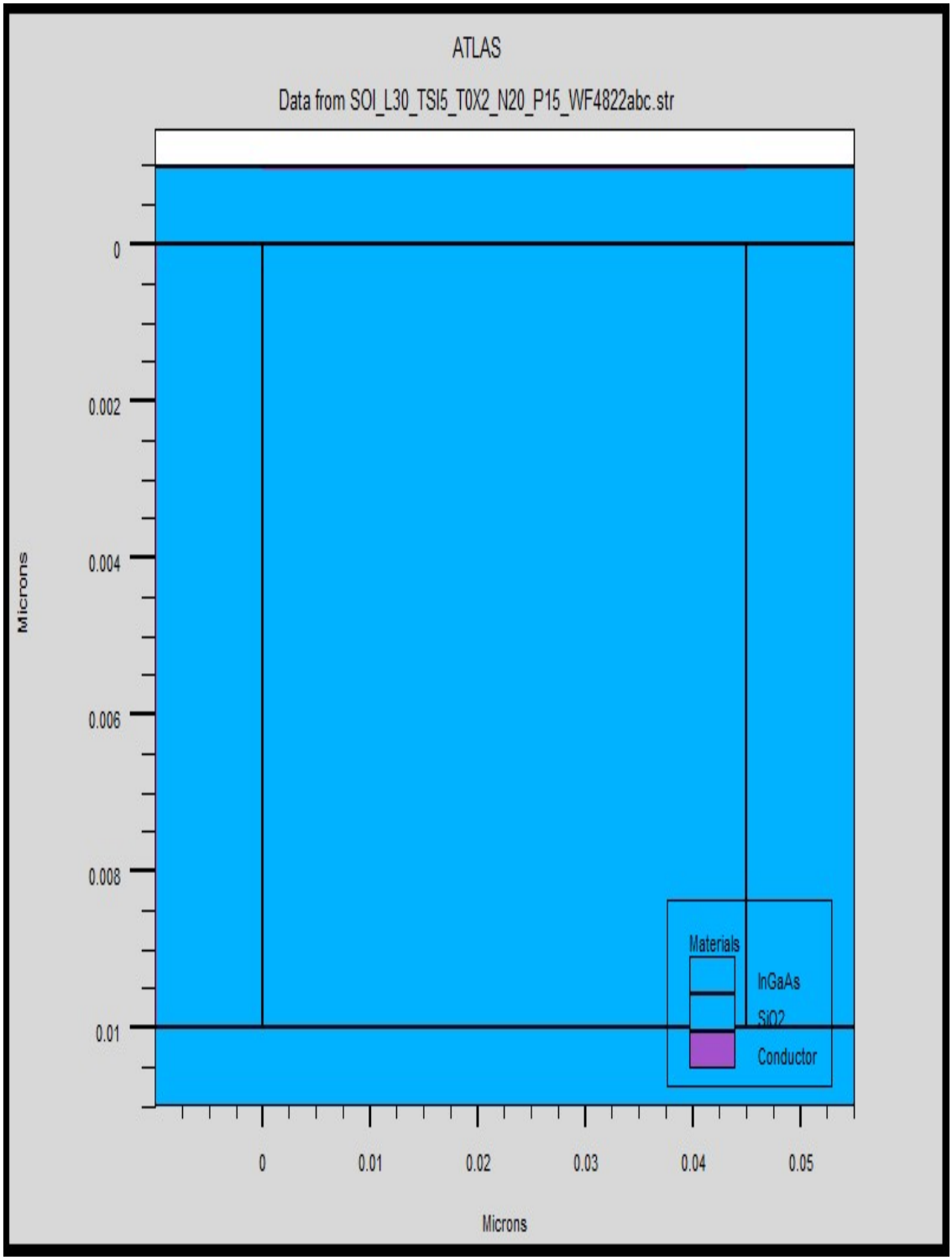

Fig. 3.26 $In_{0.53}Ga_{0.47}As$ with SiO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Dioxide (SiO_2) used as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

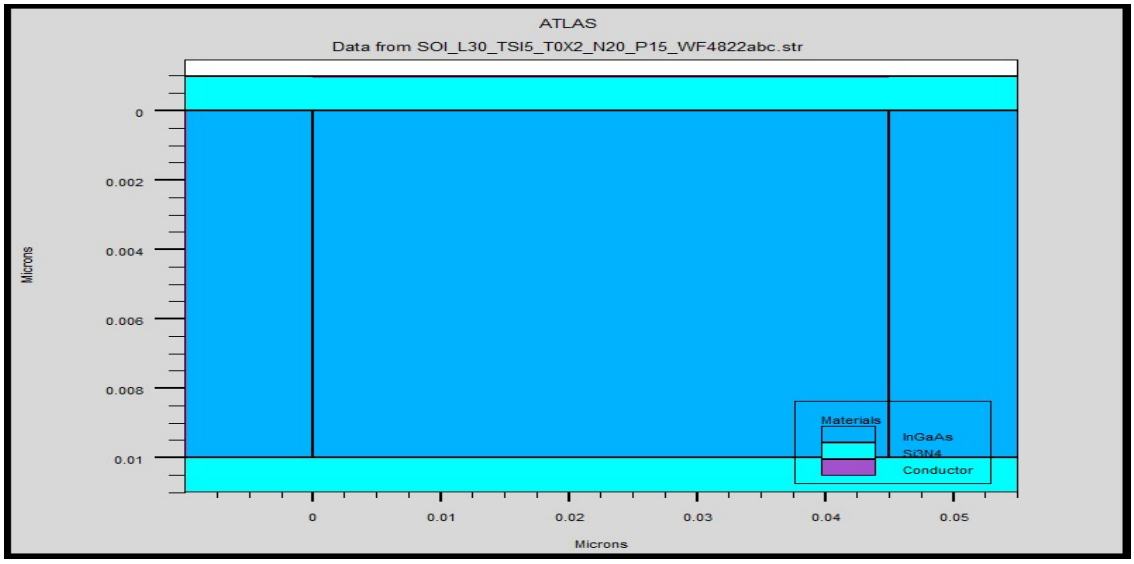

Fig. 3.27 $In_{0.53}Ga_{0.47}As$ with Si_3N_4 at 45 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Nitride (Si_3N_4) used as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

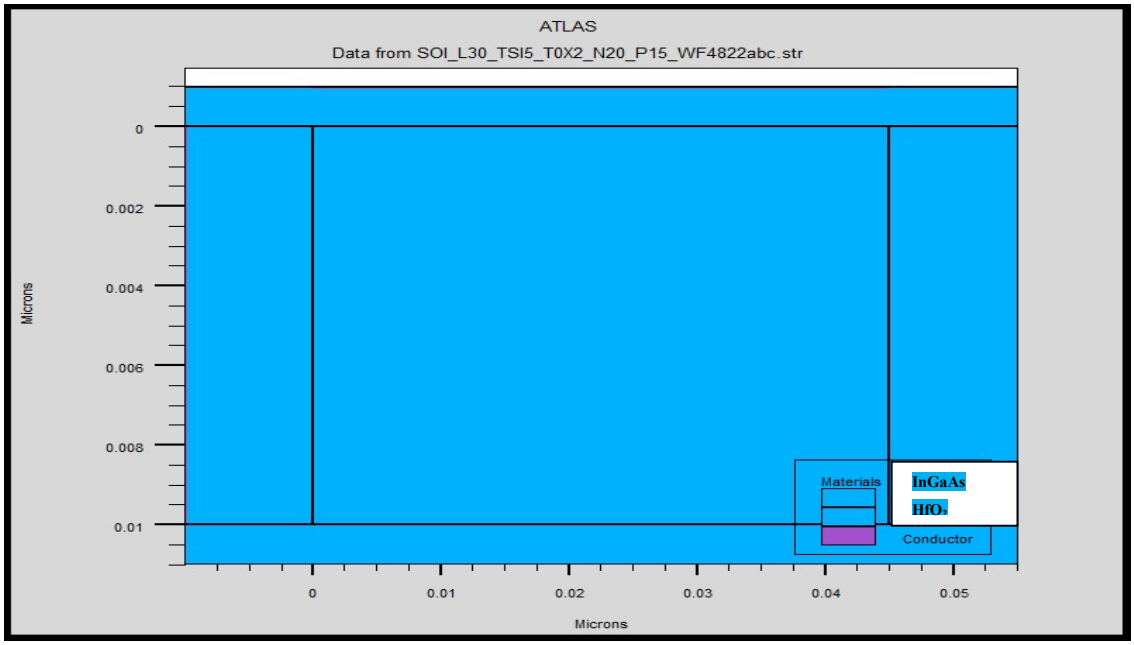

Fig. 3.28 $In_{0.53}Ga_{0.47}As$ with HfO_2 at 45 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 45 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

Table 3.6: Comparison **$In_{0.53}Ga_{0.47}As$ Material** and SiO_2, $Si_3N_4$and HfO_2 Dielectric at 45 nm

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	61.76	392.63	10^8
Si_3N_4(K=7.4)	0.5	60.74	386.31	10^9
HfO_2(K=22)	0.5	60.28	386.31	10^9

3.5 Similar work for Simulation of 22 nm Gate Length Double Gate Junctionless MOSFET:

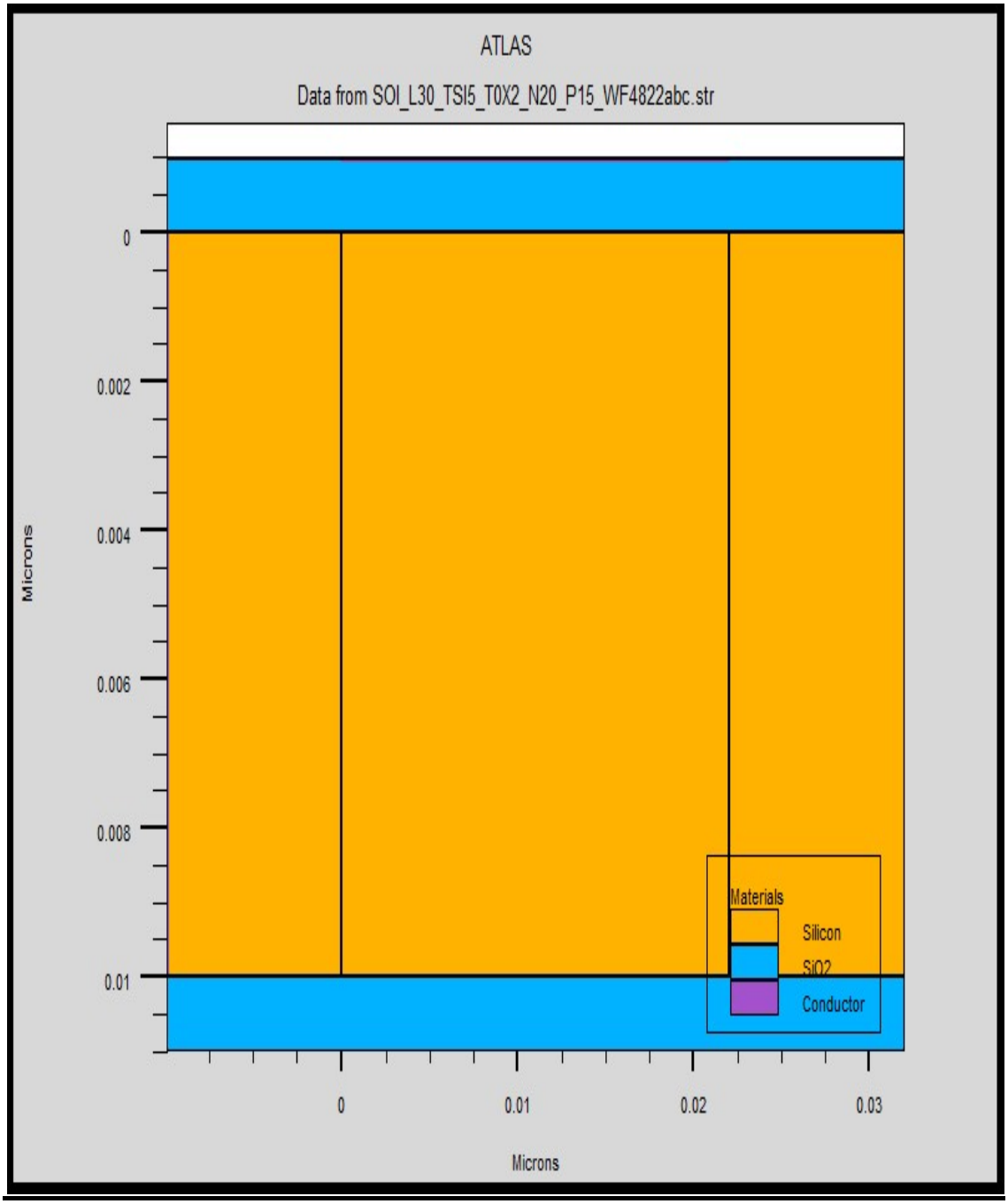

Fig. 3.29 Si and SiO_2 at 22 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and SiO_2 as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

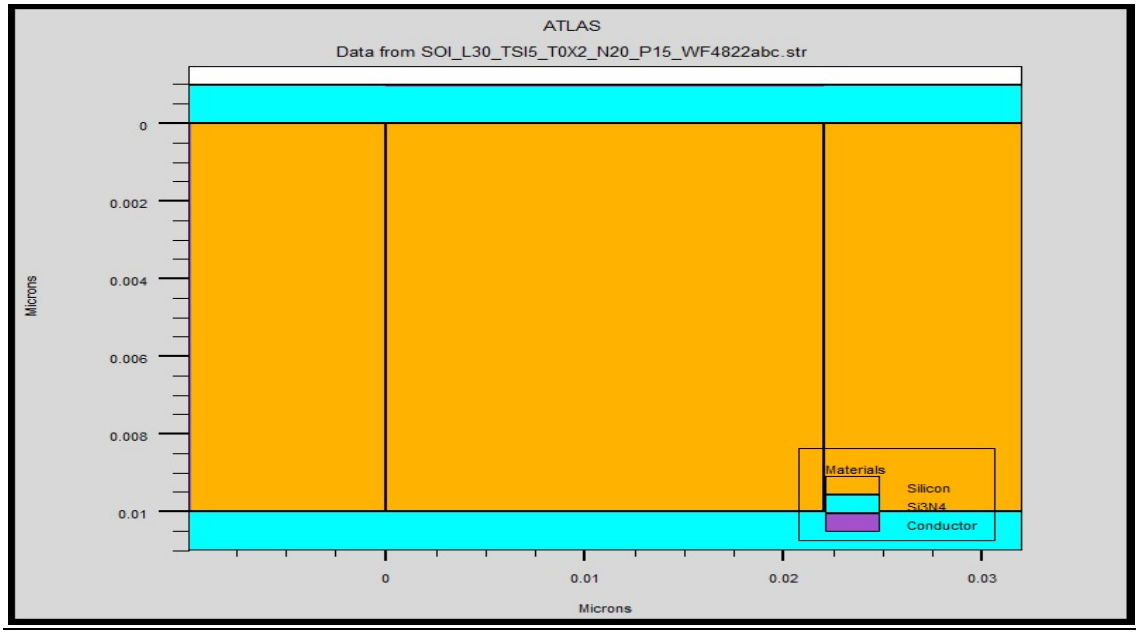

Fig. 3.30 Si and Si_3N_4 at 22 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

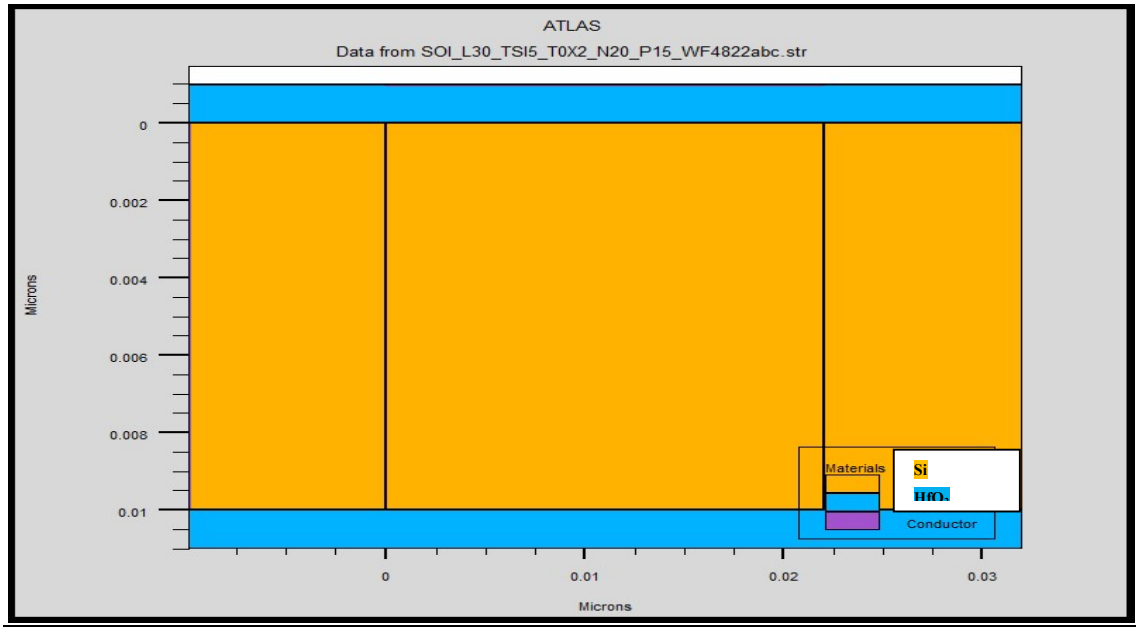

Fig. 3.31 Si and HfO_2 at 22 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

Table 3.7: Comparison **Si Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 22 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	65.23	423.15	10^9
Si_3N_4(K=7.4)	0.5	62.52	407.36	10^{10}
HfO_2(K=22)	0.5	61.28	394.73	10^{11}

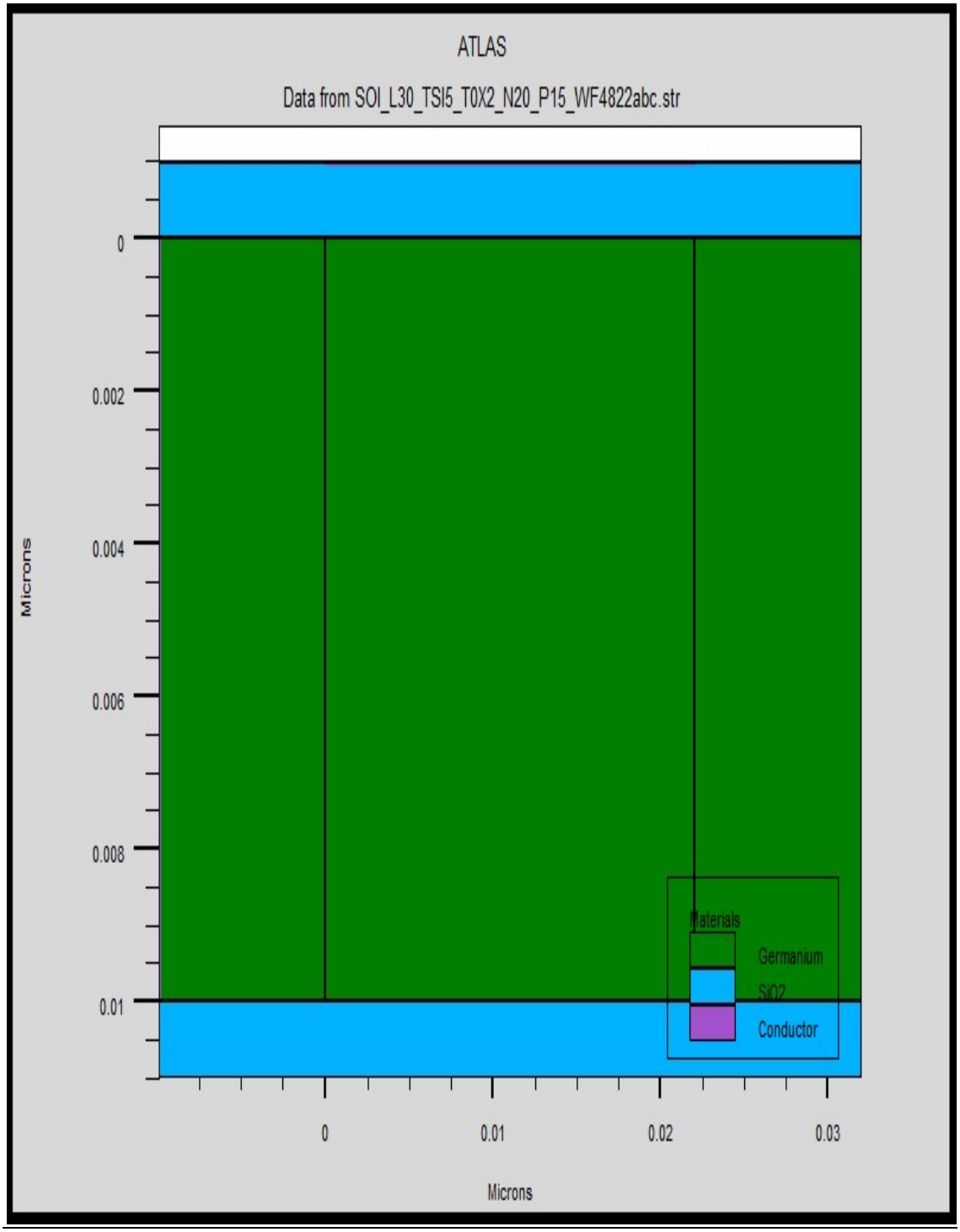

Fig. 3.32 Ge with SiO_2 structure at 22 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and SiO_2 as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

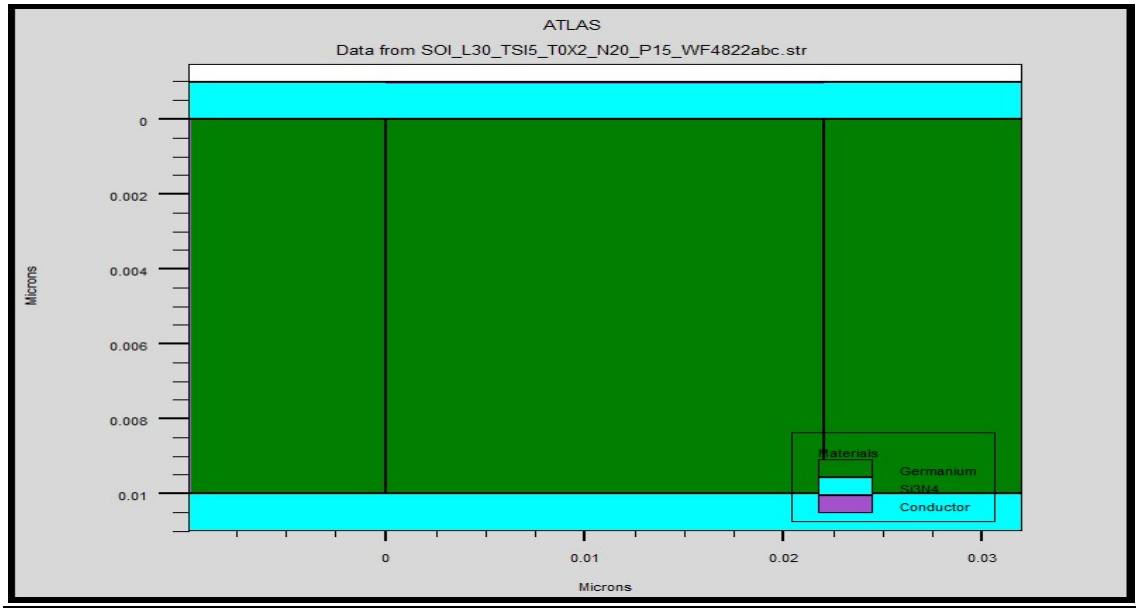

Fig. 3.33 Ge with Si_3N_4 structure at 22 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

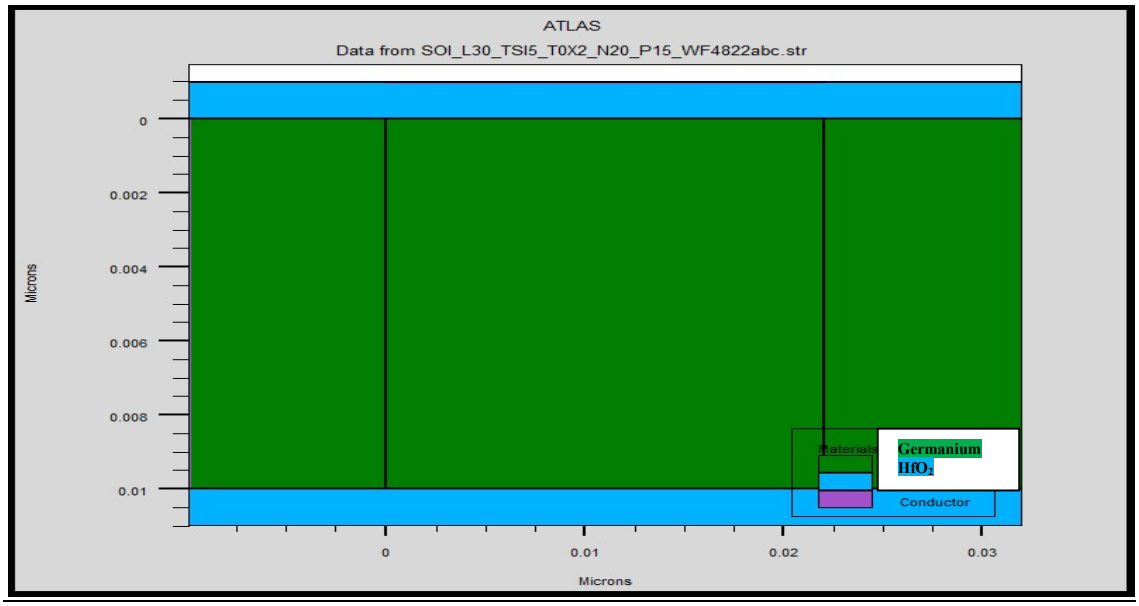

Fig. 3.34 Ge with HfO_2 structure at 22 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and HfO_2 as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Table 3.8: Comparison **Ge Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 22 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	83.64	412.63	10^6
Si_3N_4(K=7.4)	0.5	76.92	400	10^7
HfO_2(K=22)	0.5	67.52	386.31	10^8

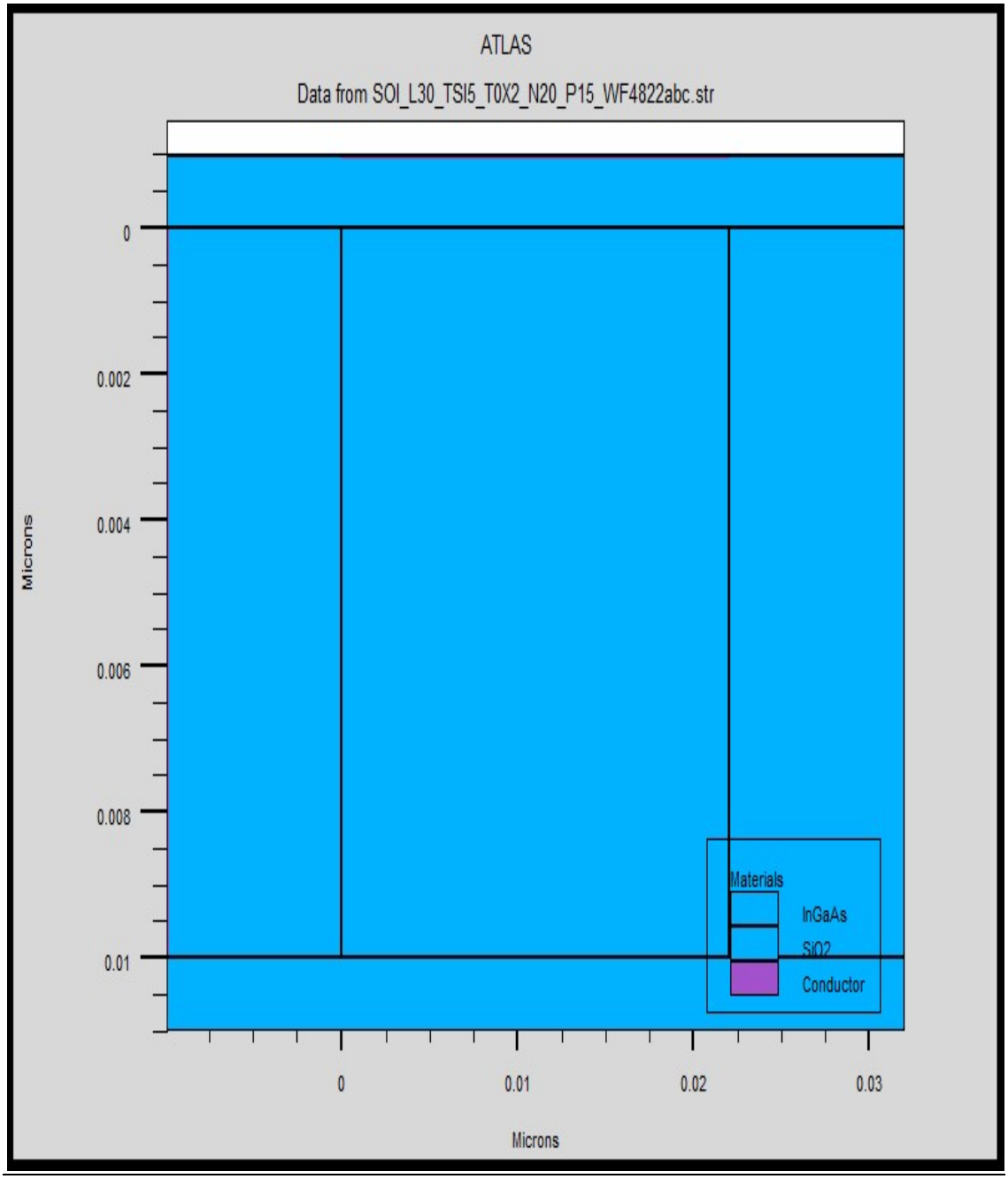

Fig. 3.35 $In_{0.53}Ga_{0.47}As$ with SiO_2 structure at 22 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and SiO_2 used as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

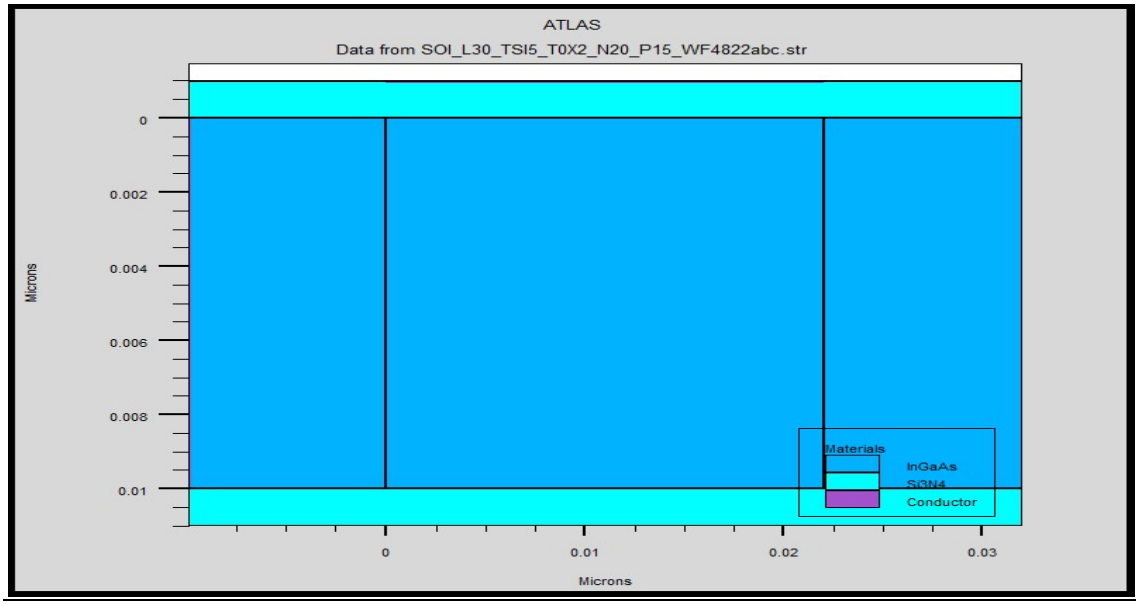

Fig. 3.36 $In_{0.53}Ga_{0.47}As$ with Si_3N_4 structure at 22 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Nitride (Si_3N_4) used as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

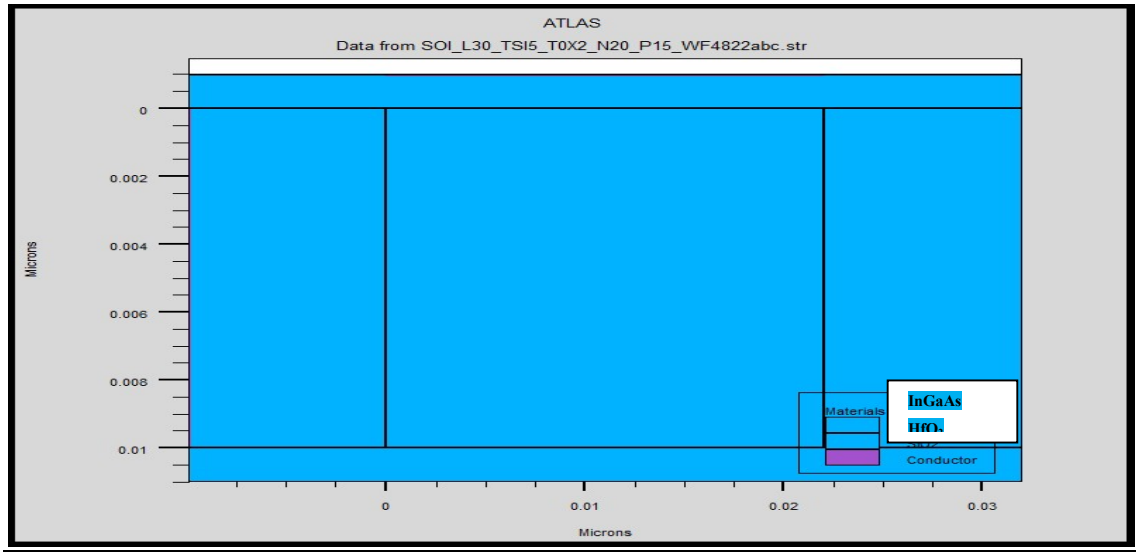

Fig. 3.37 $In_{0.53}Ga_{0.47}As$ with HfO_2 structure at 22 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 22 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

Table 3.9: Comparison **$In_{0.53}Ga_{0.47}As$ Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 22 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	67.04	418.94	10^8
Si_3N_4(K=7.4)	0.5	63.73	403.15	10^8
HfO_2(K=22)	0.5	61.68	394.73	10^9

3.6 Simulation of 16 nm Gate Length Double Gate Junctionless MOSFET

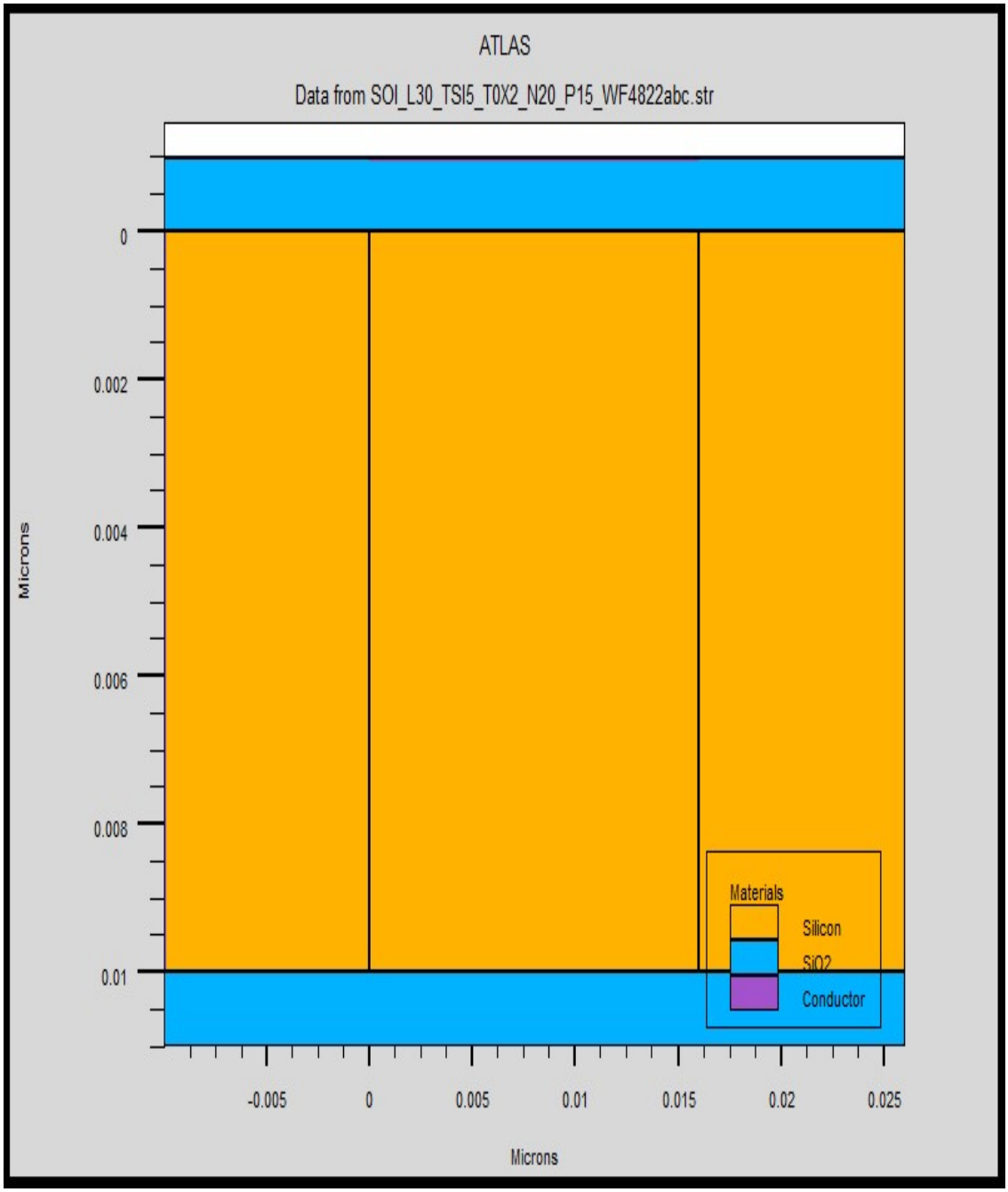

Fig.3.38 Si and SiO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and SiO_2 as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

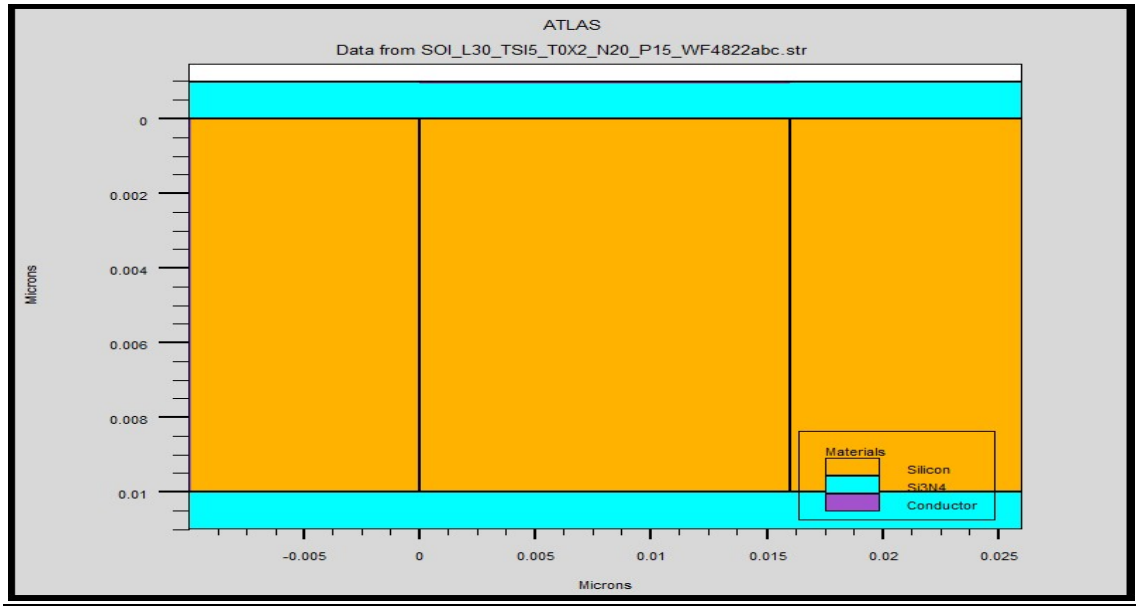

Fig.3.39 Si and Si_3N_4 at 16 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

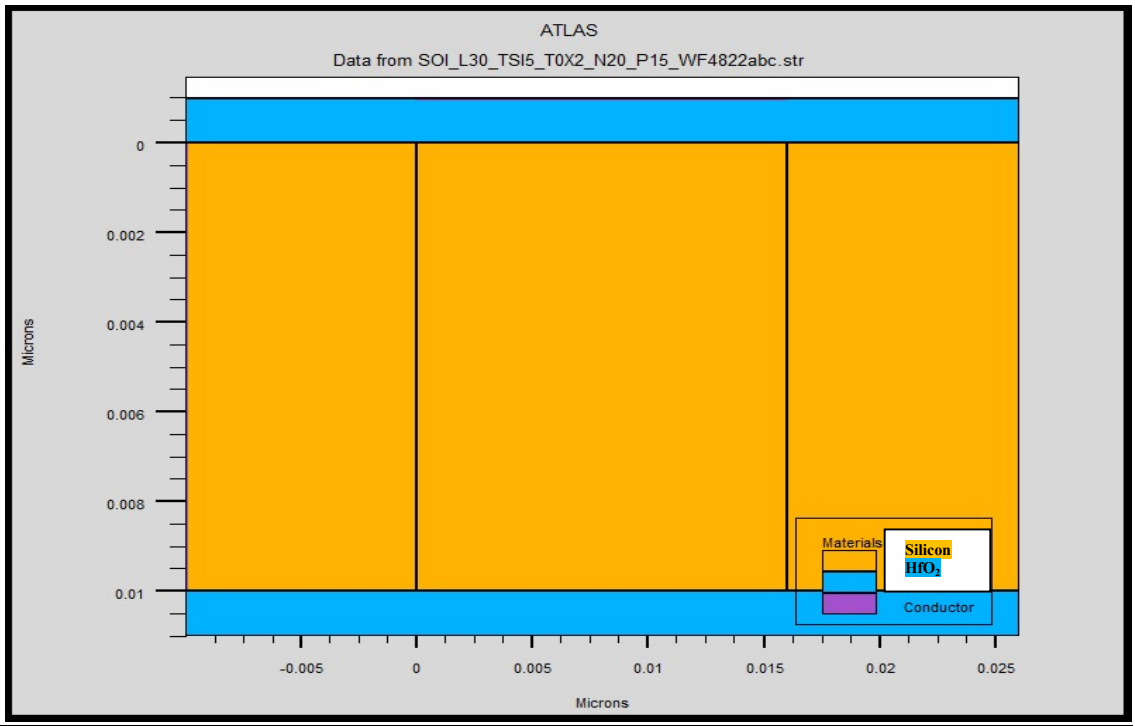

Fig. 3.40 Si and HfO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which Si is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Si thickness is 10 nm is used.

Table 3.10 Comparison **Si Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 16 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/ 0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	69.03	440.52	10^8
Si_3N_4(K=7.4)	0.5	65.22	414.73	10^9
HfO_2 (K=22)	0.5	62.96	402.10	10^{10}

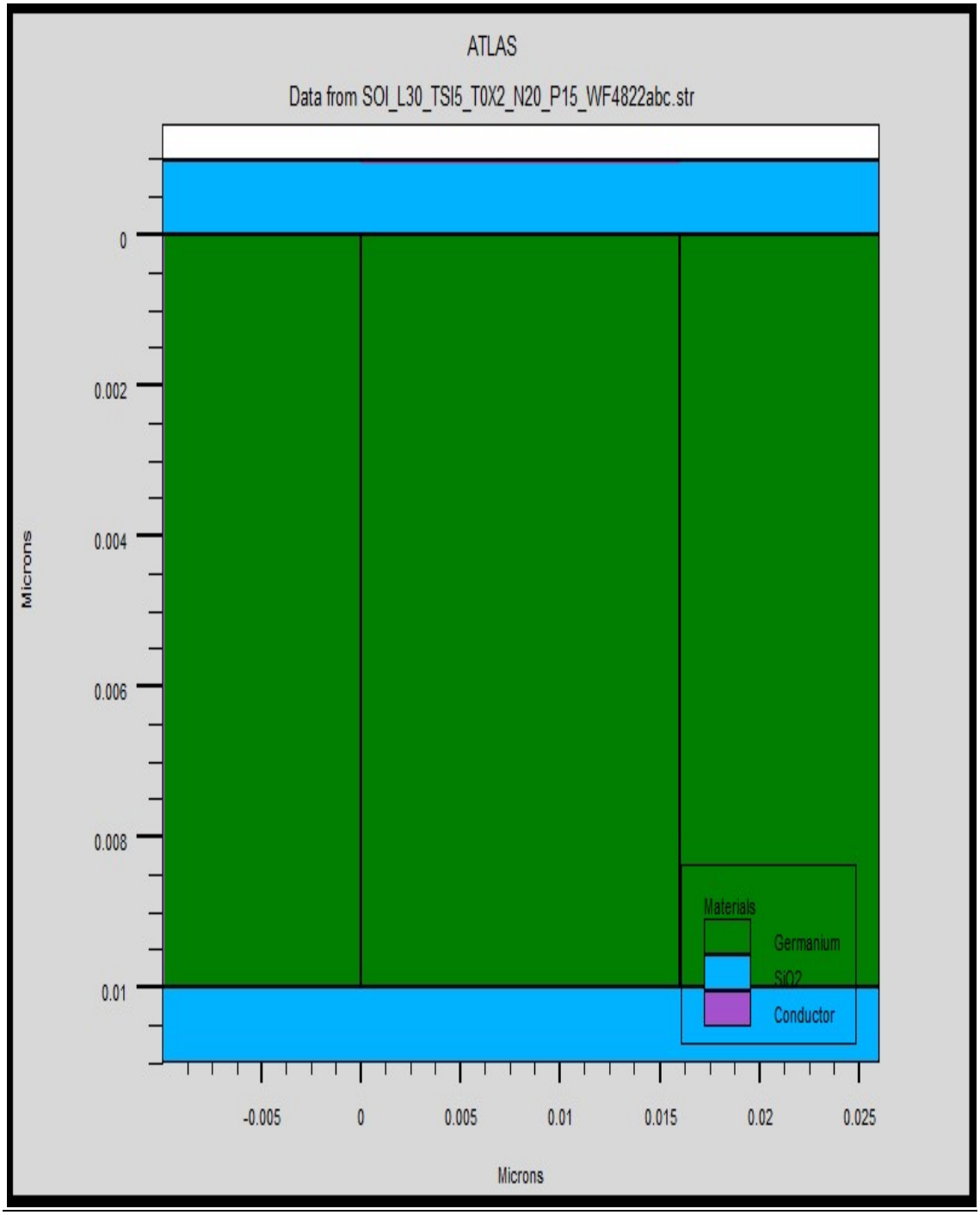

Fig. 3.41 Ge with SiO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and SiO_2 as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

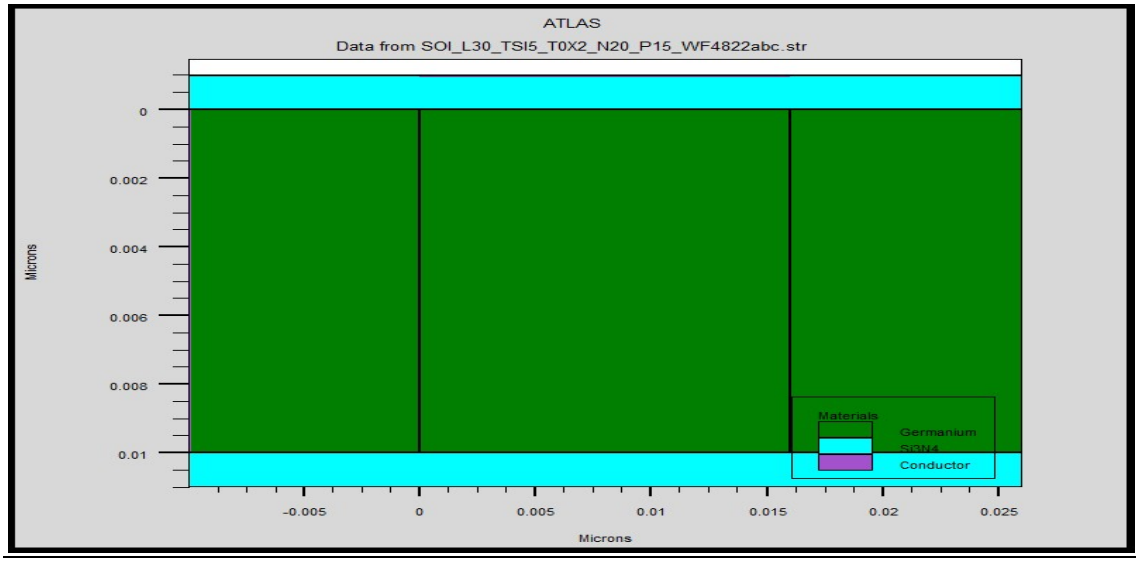

Fig. 3.42 Ge with Si_3N_4 at 16 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and Si_3N_4 as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

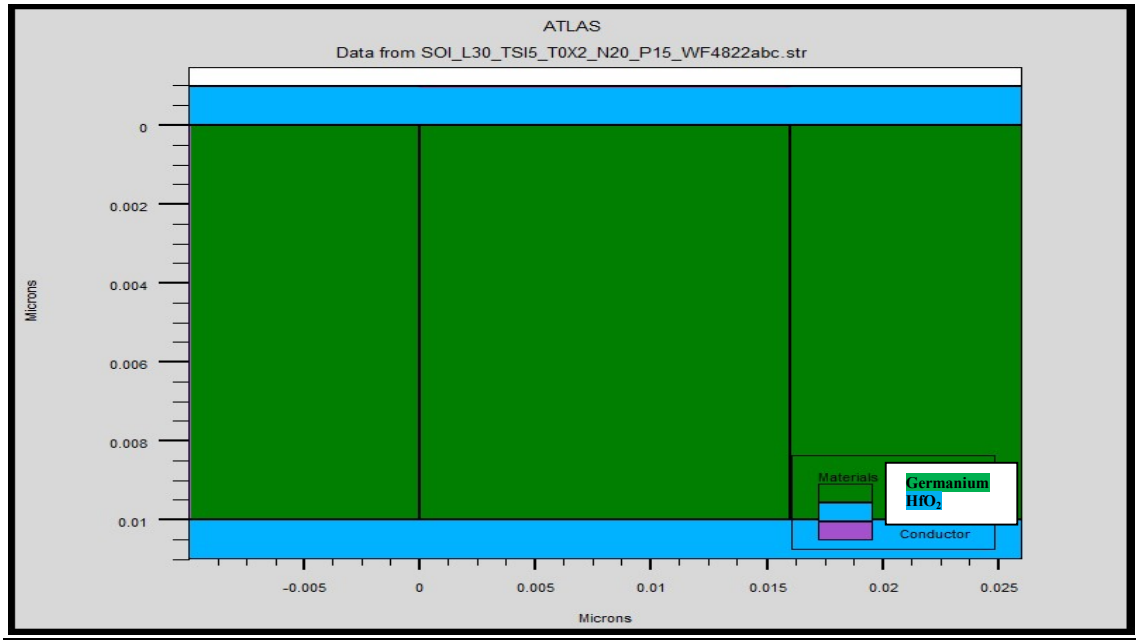

Fig. 3.43 Ge with HfO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which Ge is used as substrate and HfO_2 as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and Ge thickness is 10 nm is used.

Table 3.11: Comparison **Ge Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 16 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/ 0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	114.82	436.84	10^6
Si_3N_4(K=7.4)	0.5	89.41	411.57	10^7
HfO_2(K=22)	0.5	68.60	396.84	10^8

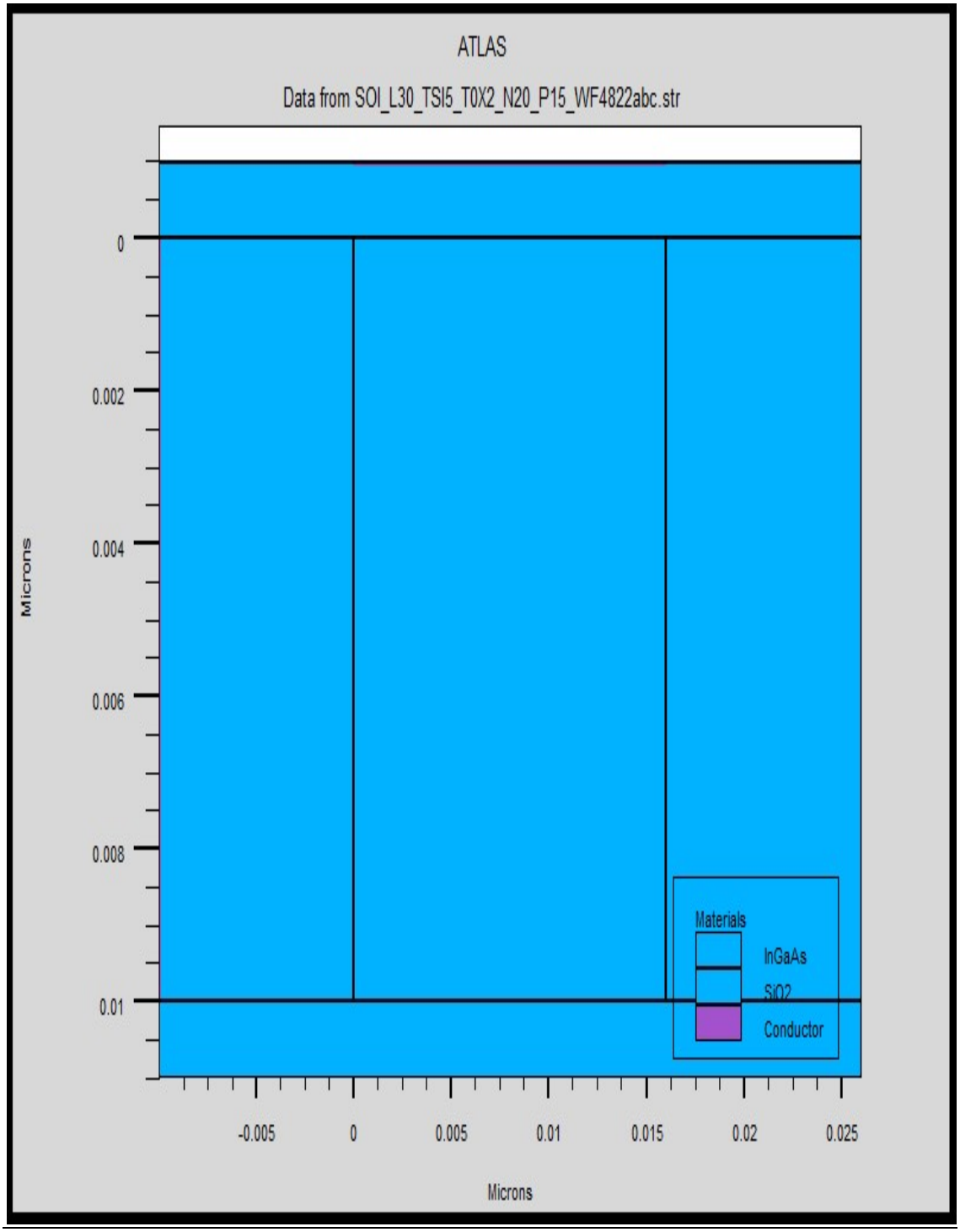

Fig. 3.44 $In_{0.53}Ga_{0.47}As$ with SiO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$is used as substrate and Silicon dioxide (SiO_2) used as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

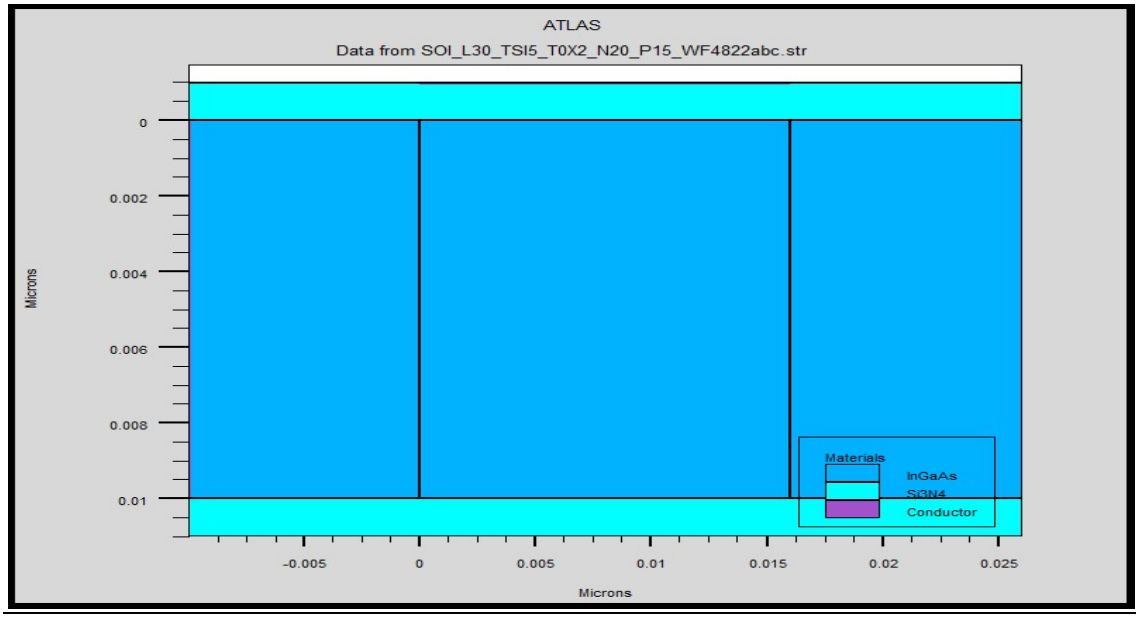

Fig. 3.45 $In_{0.53}Ga_{0.47}As$ with Si_3N_4 at 16 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Silicon Nitride (Si_3N_4) used as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

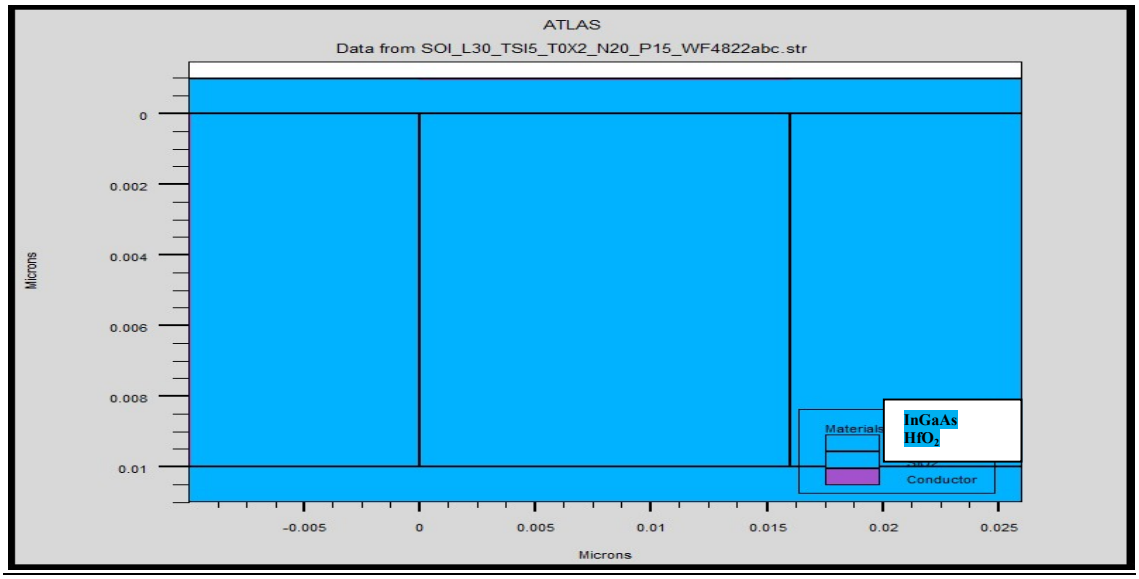

Fig. 3.45 $In_{0.53}Ga_{0.47}As$ with HfO_2 at 16 nm

This structure shows double gate junction less MOSFET, in which $In_{0.53}Ga_{0.47}As$ is used as substrate and Hafnium Oxide (HfO_2) used as gate oxide layer. Gate length is 16 nm. Oxide thickness is 1 nm and $In_{0.53}Ga_{0.47}As$ thickness is 10 nm is used.

Table 3.12: Comparison **$In_{0.53}Ga_{0.47}As$ Material** and SiO_2, Si_3N_4 and HfO_2 Dielectric at 16 nm:

Dielectric material	**Threshold Voltage V_{th} in Volt**	**Subthreshold Swing Sub V_{th} in mV/dec**	**DIBL mV/V = V_{th}(when V_{ds}=0.05 Volt)- V_{th}(when V_{ds}=1Volt)/0.95**	**Ion/Ioff ratio**
SiO_2(K=3.9)	0.5	83.35	450.52	10^6
Si_3N_4(K=7.4)	0.5	71.49	427.36	10^7
HfO_2(K=22)	0.5	64.19	403.15	10^9

4. CONCLUSION AND RESULTS

4.1 Comparison Graph of SILICON (Si) DOUBLE GATE JUNCTIONLESS MOSFET

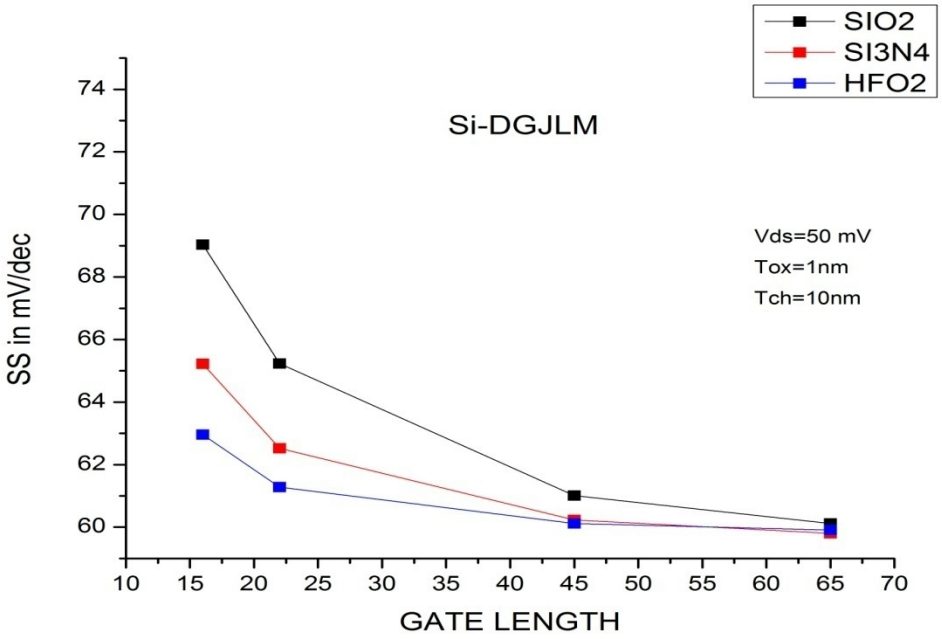

Fig. 4.1 Gate Length versus Subthreshold Slope when Substrate is Si

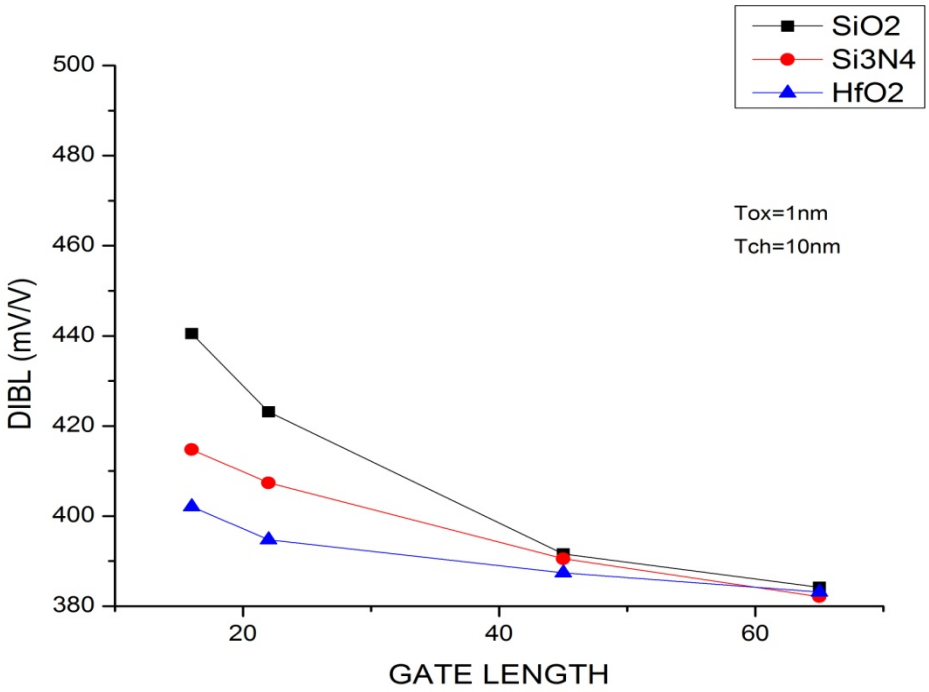

Fig 4.2 Gate Length Versus DIBL when Substrate is Si

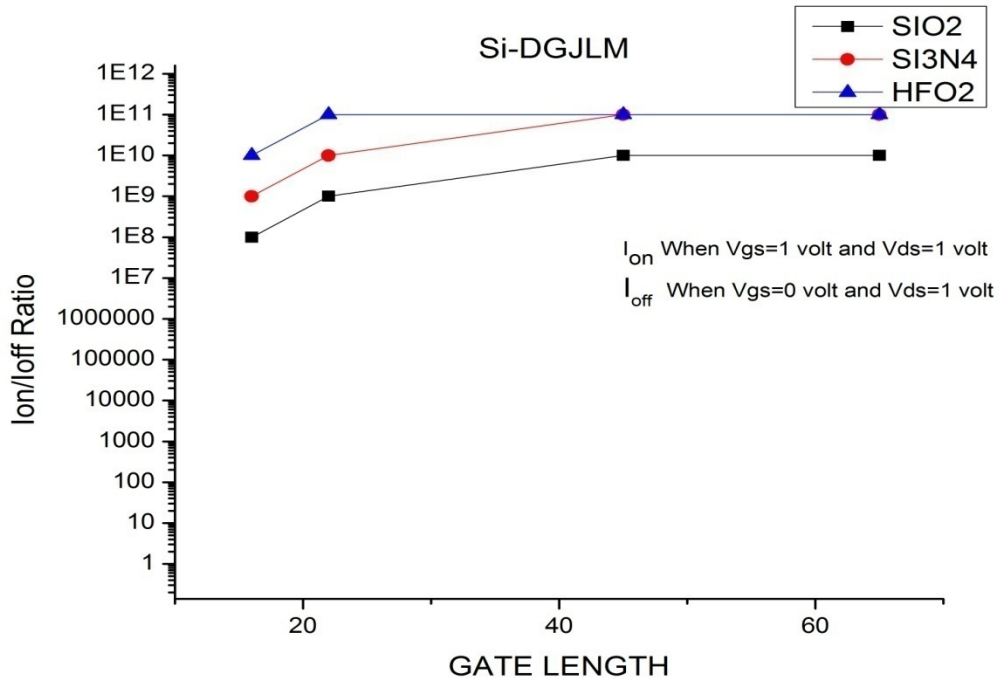

Fig 4.3 Gate Length Versus I_{on}/I_{off} when Substrate is Si

From the comparison graph of SILICON(Si) Double Gate Junctionless MOSFET with different dielectric layers, it show that hafnium oxide (HfO_2) dielectric layer gives low subthreshold slope, low DIBL and high I_{on}/I_{off} ratio.

4.2 Comparison Graph of GERMANIUM (Ge) DOUBLE GATE JUNCTIONLESS MOSFET

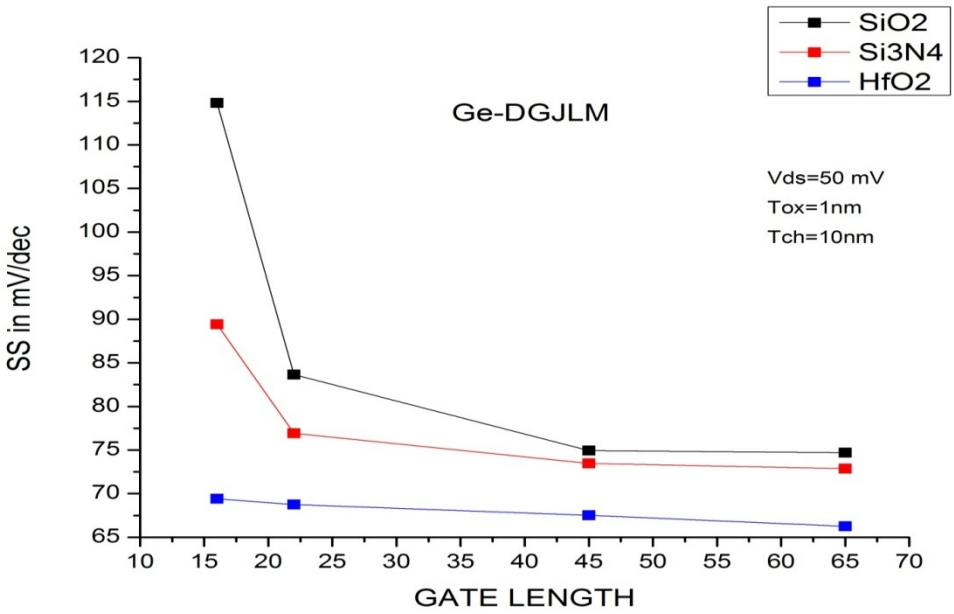

Fig. 4.4 Gate Length versus Subthreshold Slope when Substrate is Ge

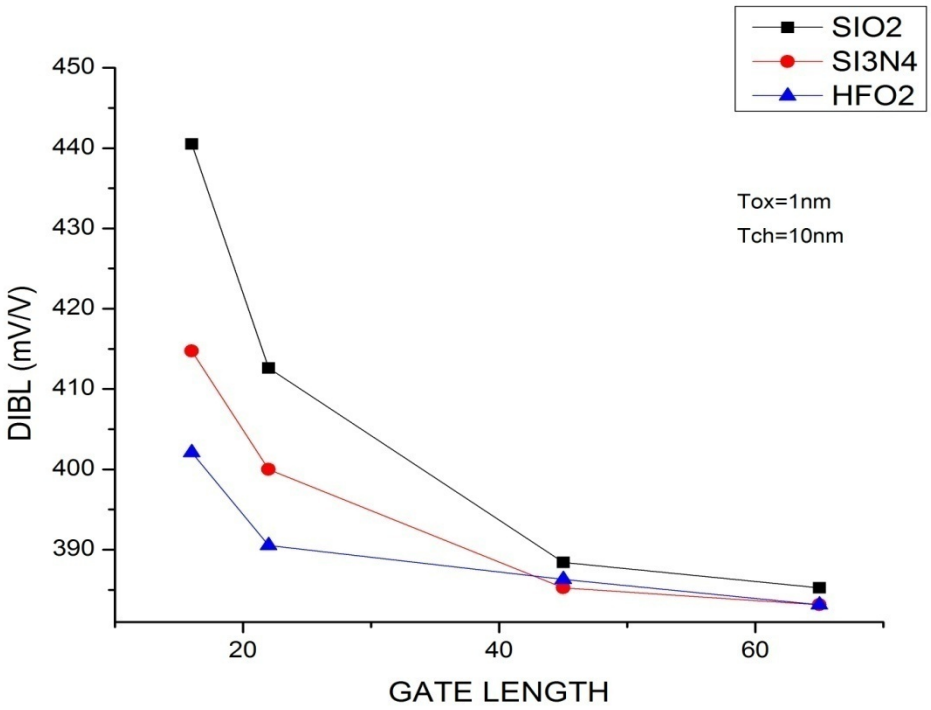

Fig. 4.5 Gate Length Versus DIBL when Substrate is Ge

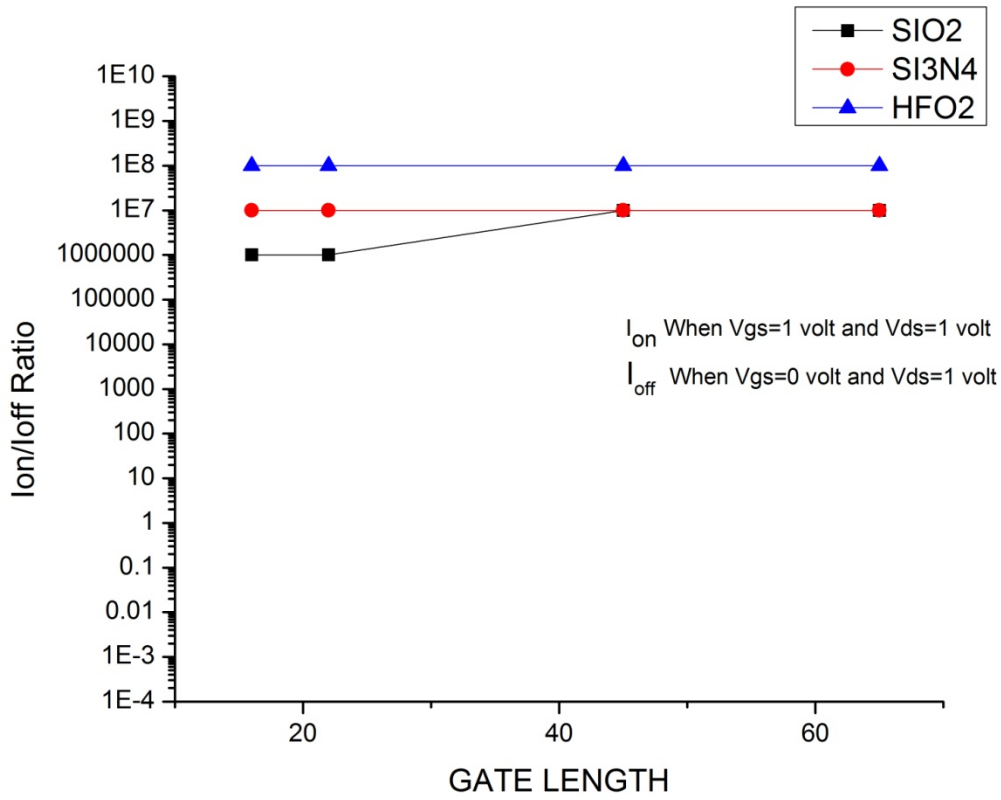

Fig. 4.6 Gate Length Versus I_{on}/I_{off} when Substrate is Ge

From the comparison graph of GERMANIUM (Ge) Double Gate Junctionless MOSFET with different dielectric layers, it show that hafnium oxide (HfO_2) dielectric layer gives low subthreshold slope, low DIBL and high I_{on}/I_{off} ratio.

4.3 Comparison Graph of $In_{0.53}Ga_{.43}As$ DOUBLE GATE JUNCTIONLESS MOSFET

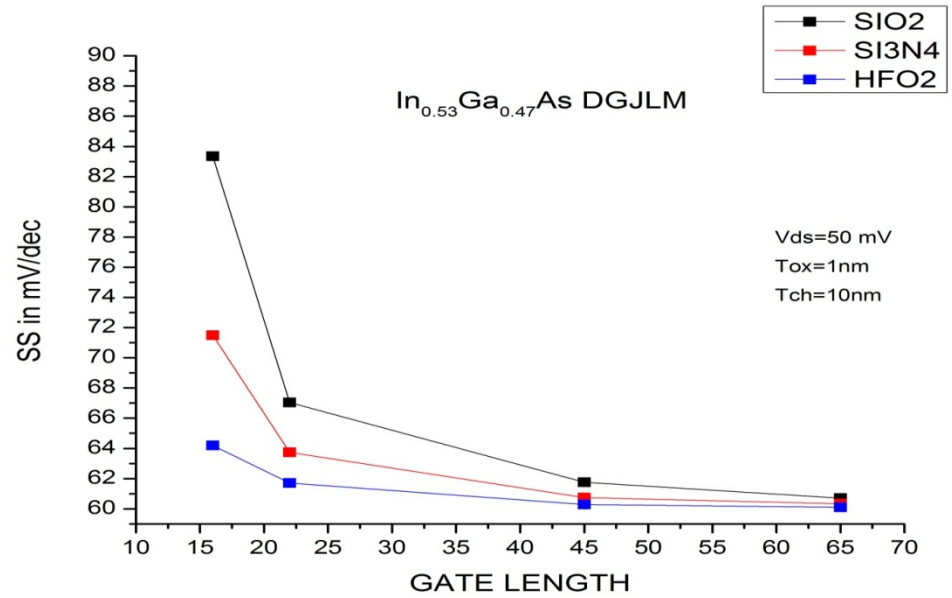

Fig. 4.7 Gate Length versus Subthreshold Slope when Substrate is $In_{0.53}Ga_{0.47}As$

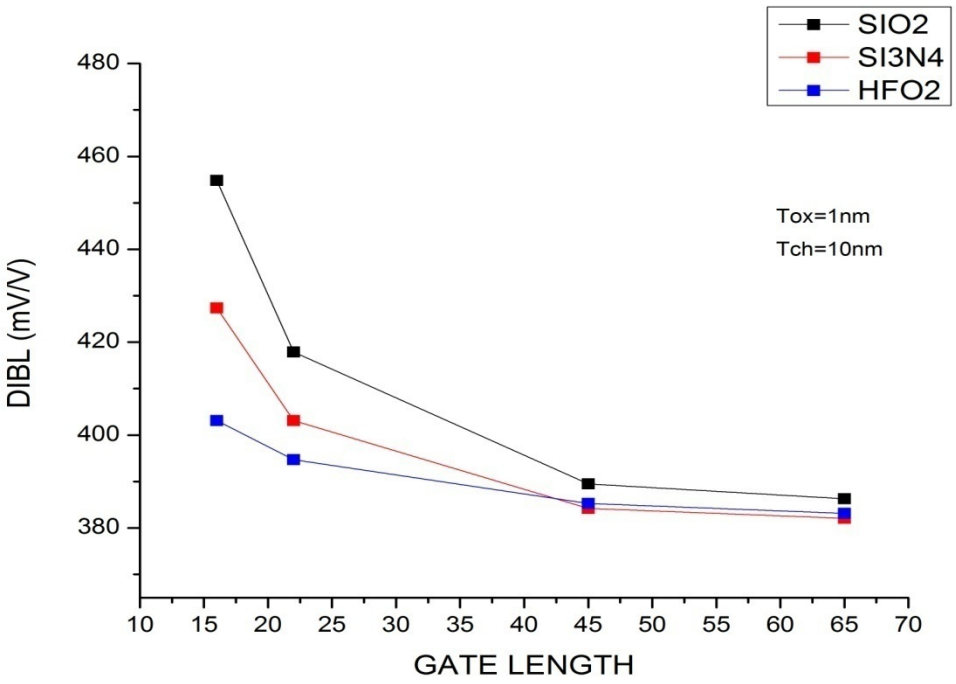

Fig. 4.8 Gate Length versus DIBL when Substrate is $In_{0.53}Ga_{0.47}As$

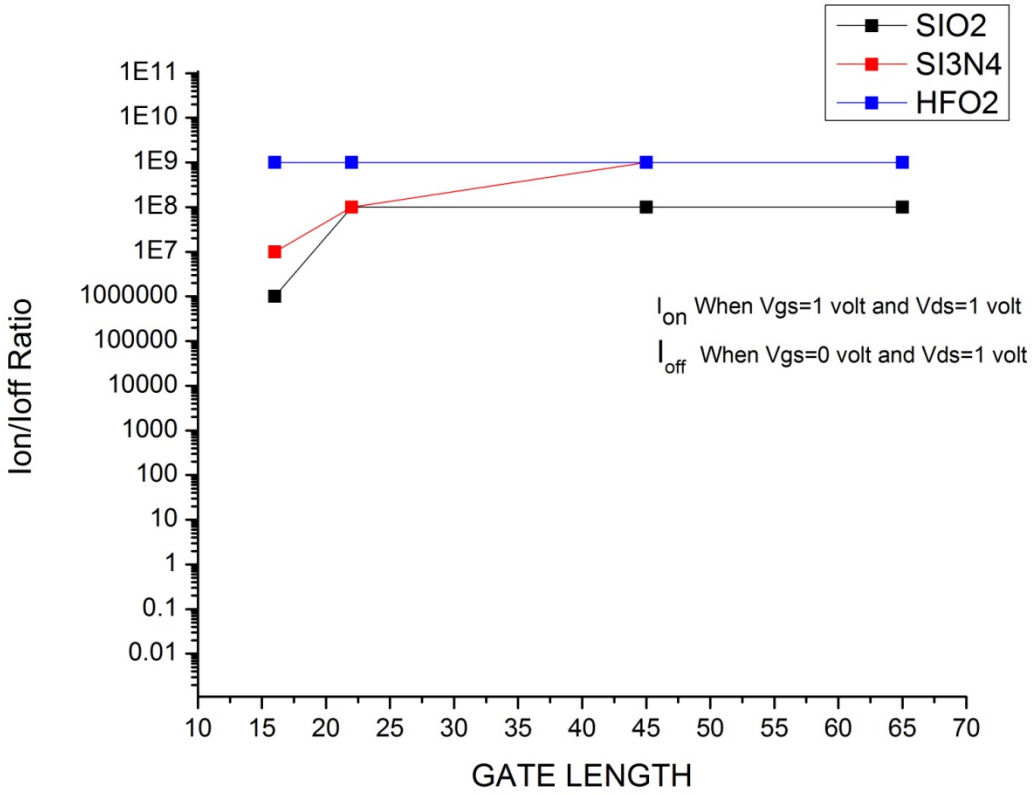

Fig. 4.9 Gate Length versus I_{ON}/I_{OFF} Ratio when Substrate is $In_{0.53}Ga_{0.47}As$

From the comparison graph of $In_{0.53}Ga_{0.47}As$ Double Gate Junctionless MOSFET with different dielectric layers, it show that hafnium oxide (HfO_2) dielectric layer gives low subthreshold slope, low DIBL and high I_{on}/I_{off} ratio.

4.4 DIBL versus Gate Length curve for different substrates with SiO_2, Si_3N_4, HfO_2 dielectric material

DIBL versus Gate Length curve for different substrates with SiO_2 dielectric material

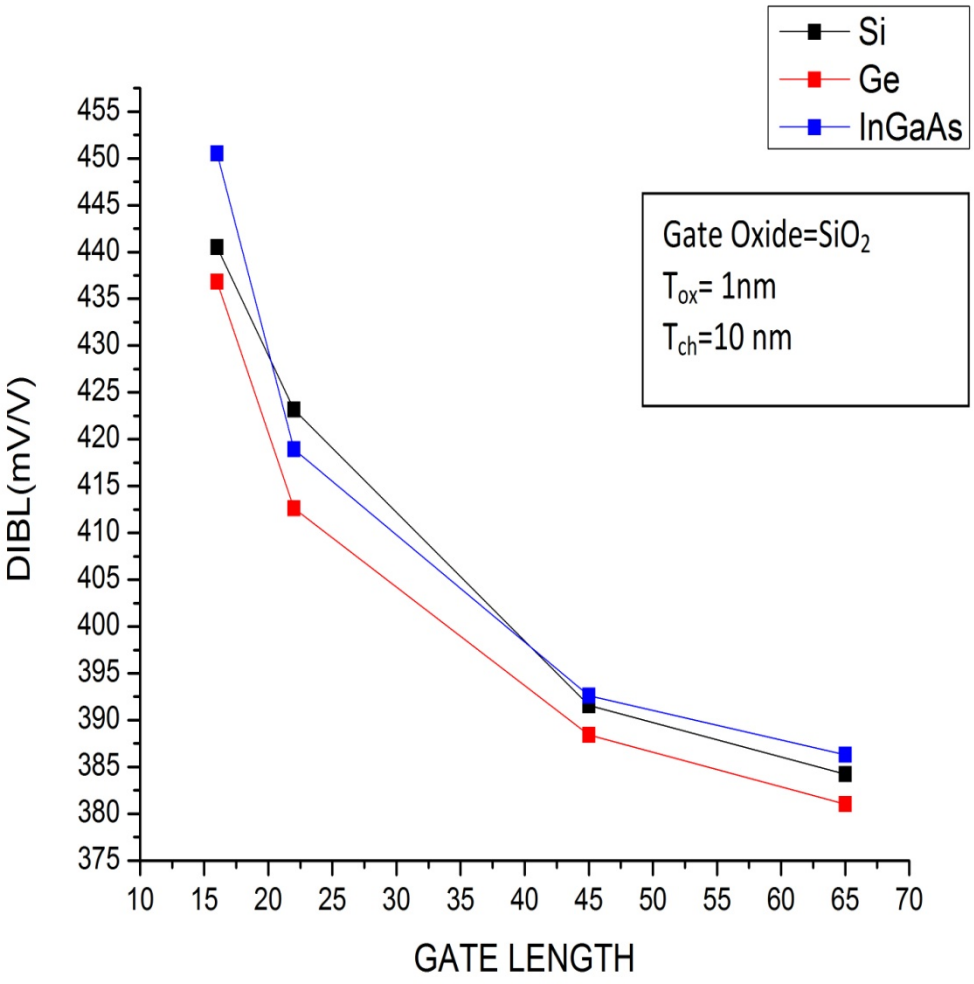

Fig. 4.10 Gate Length versus DIBL when dielectric layer is SiO_2

DIBL versus Gate Length curve for different substrates with Si_3N_4 dielectric material

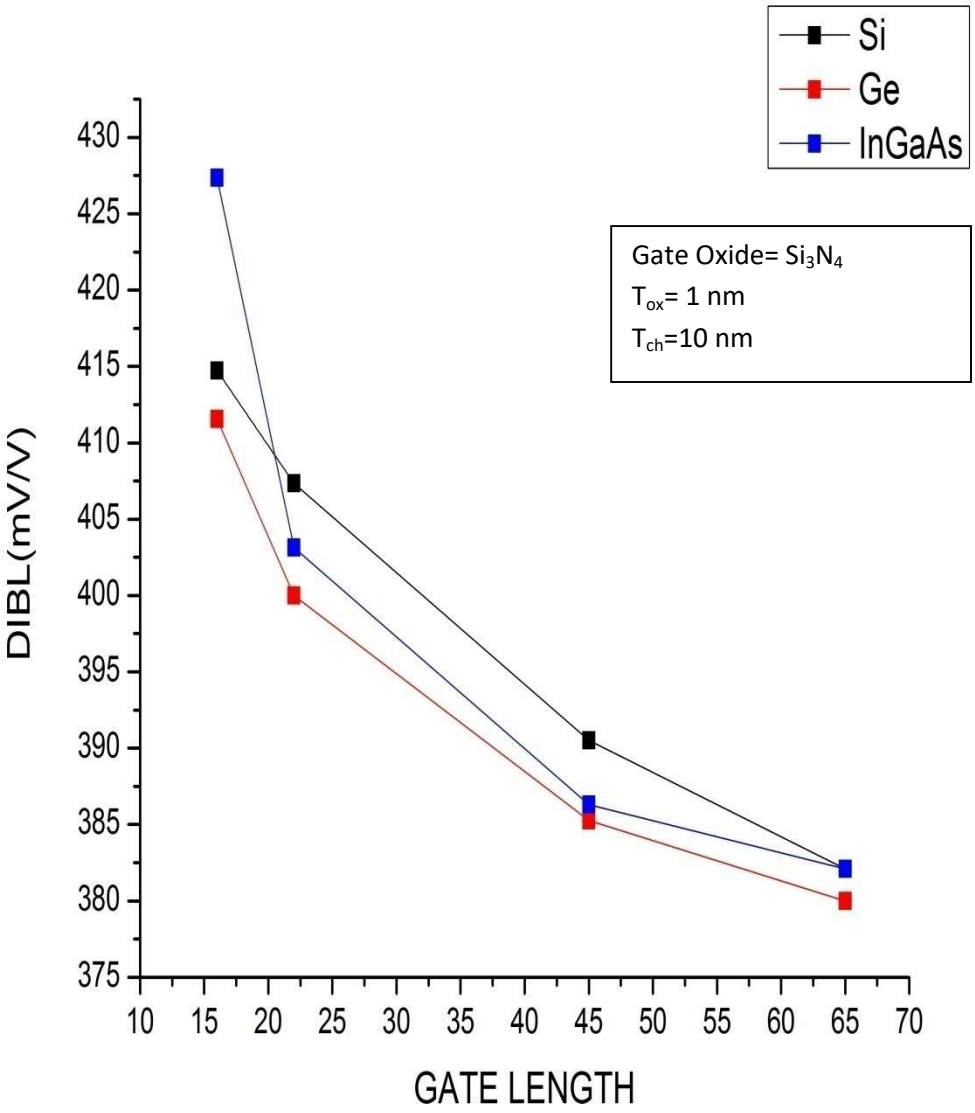

Fig. 4.11 Gate Length and DIBL when dielectric layer is Si_3N_4

DIBL versus Gate Length curve for different substrates with HfO_2 dielectric material

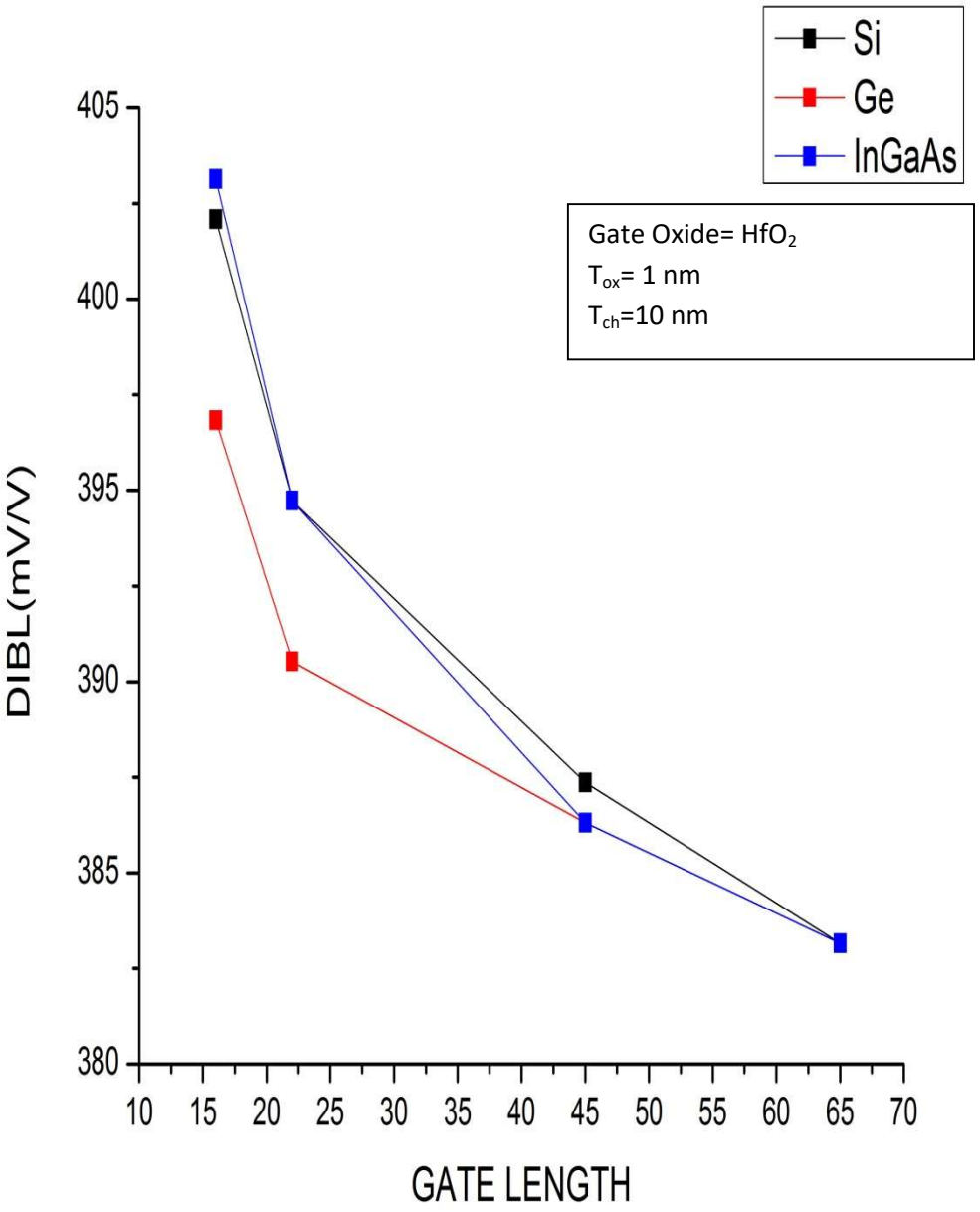

Fig. 4.12 Gate Length and DIBL when dielectric layer is HfO_2

The comparison curves between different dielectric layers with Si, Ge, $In_{0.53}Ga_{0.47}As$ shows that HfO_2 dielectric layer gives low SS(subthreshold slope), low DIBL(Drain Induced Barrier Lowering) and high I_{on}/I_{off} ratio compared to SiO_2 and Si_3N_4 dielectric layer.

When Si, Ge, $In_{0.53}Ga_{0.47}As$ material is used as substrate with different dielectric layers, then results shows that Ge gives low DIBL with all dielectric layers (SiO_2, Si_3N_4, HfO_2) in compared to Si and $In_{0.53}Ga_{0.47}As$ substrate. DIBL is reduced by using high K dielectric layer.

InGaAs substrate is combination of III-V group material such as InAs and GaAs. Results shows that $In_{0.53}Ga_{0.47}As$ has nearby DIBL values as Si. So, it can be proposed for further research and development on this material so it would used as alternative of future CMOS Si device.

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